# IBIS-AMI
# Concern for PAM4 Simulation

Asian IBIS Summit
Tokyo, Japan
November 16, 2015

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# Outline

- 56 Gbps coming soon
- How to realize 56 Gbps
- What is PAM4
- How to simulate PAM4
- IBIS-AMI
- Concern for IBIS-AMI

# 56 Gbps Coming Soon

- 400G Ethernet
- Release Schedule: 2017
- 50 Gbps x 8 Line

| Name | Speed | Date Initial Standard Ratified |
|---|---|---|
| 10Mb/s Ethernet | 10 Mb/s | 1983 |
| 100Mb/s Ethernet | 100Mb/s | 1995 |
| Gigabit Ethernet | 1 Gb/s | 1998 |
| 10 Gigabit Ethernet | 10 Gb/s | 2002 |
| 25 Gigabit Ethernet | 25Gb/s | 2016 (est)* |
| 40 Gigabit Ethernet | 40 Gb/s | 2010 |
| 100 Gigabit Ethernet | 100 Gb/s | 2010 |
| 400 Gigabit Ethernet | 400 Gb/s | 2017 (est.)** |

(http://www.ethernetalliance.org/subcommittees/roadmap-subcommittee/)

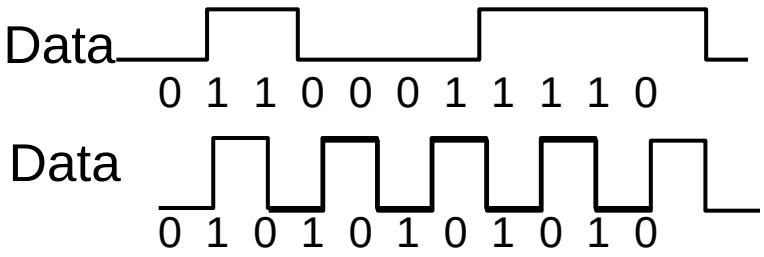
# OFI (Optical Internetworking Forum)

- CEI-56G
  - CIE-56G-USR: 2.5D/3D Chip-Chip > 1 cm
  - CIE-56G-XSR: Chip-Near Optics > 5 cm
  - CIE-56G-VSR: Chip-Module > 10 cm
  - CIE-56G-MR: Chip-Chip, Chip-Module > 50 cm/1 connector
  - CIE-56G-LR: Chip-Backplane-Chip >100 cm/2 connectors

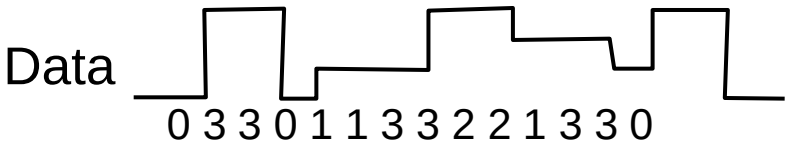
- 400G/200G: 56G x 8/4

# How to Reach 56 Gbps

- NRZ (Embedded Clock) 28 GHz/56Gbps

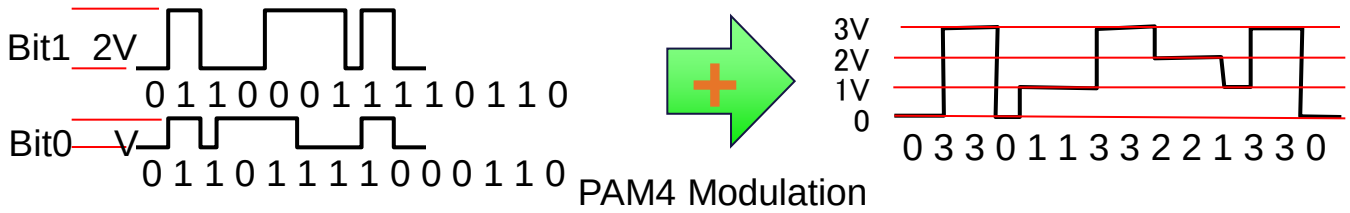



- PAM4 (4 Values Transmission) 14GHz/56Gbps

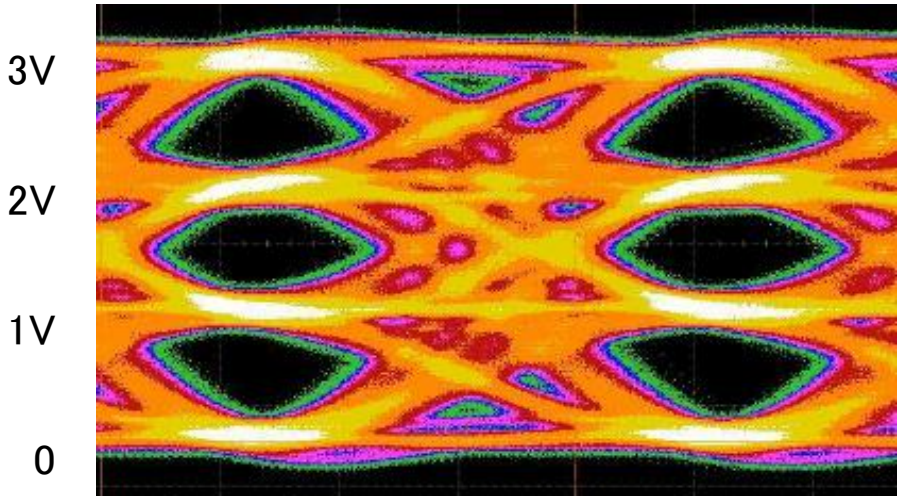


# What is PAM4

- 4 Level Transmission




PAM4 Modulation




PAM4 Eye Pattern

(E.Frlan, C.YeLiu, M.PengLi "Signal Integrity Challenges & Solutions for Next-Generation CEI-56G "Chip-to-Module" & "Chip-to-Chip" Interface, DesignCon 2015 )

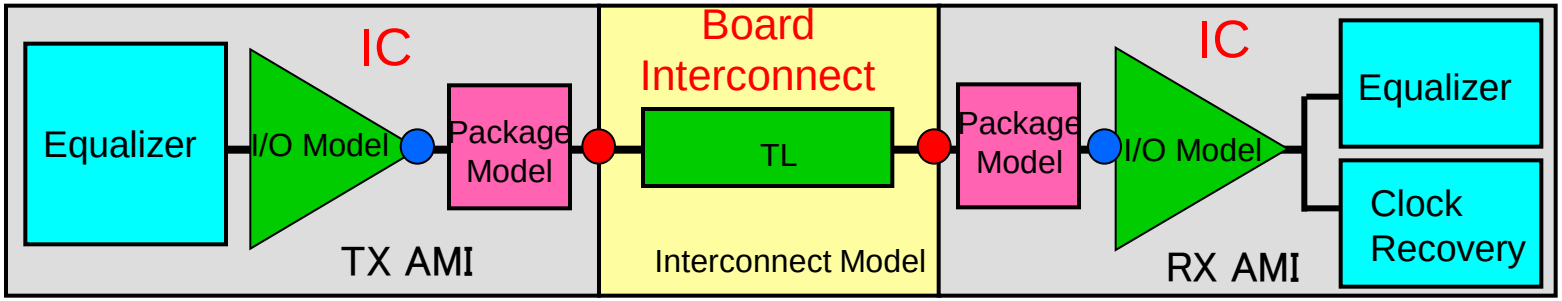
# How to Simulate PAM4

- S-parameter:  Interconnect/Connector
  - Insertion loss
- Input: Ideal input

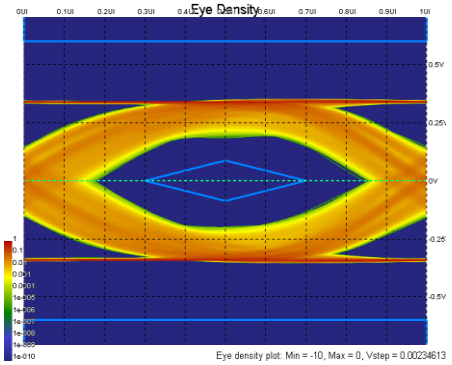
- Want to use actual driver model for simulation!
  - IBIS-AMI
- BER
  - $10^{-18}$ BER have 1 error/hr.

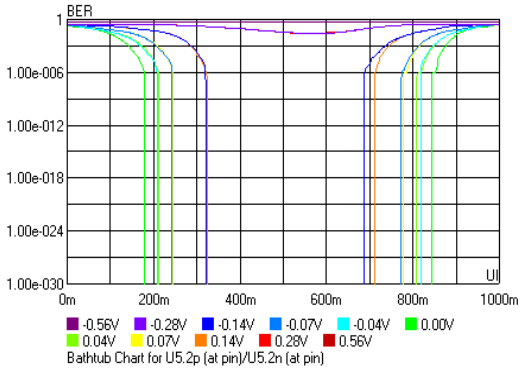
# IBIS-AMI

- Only One Solution of High-Speed Serial Link Simulation
- Analog Circuit (Active/Passive Equalizer)
- Fastest Simulation (BER Analysis)
- Random Jitter Effect Analysis




Eye
BER
(Transient)



# IBIS-AMI is Based on Linear Model

- Model Description
  - IO Model
    - AMI Model

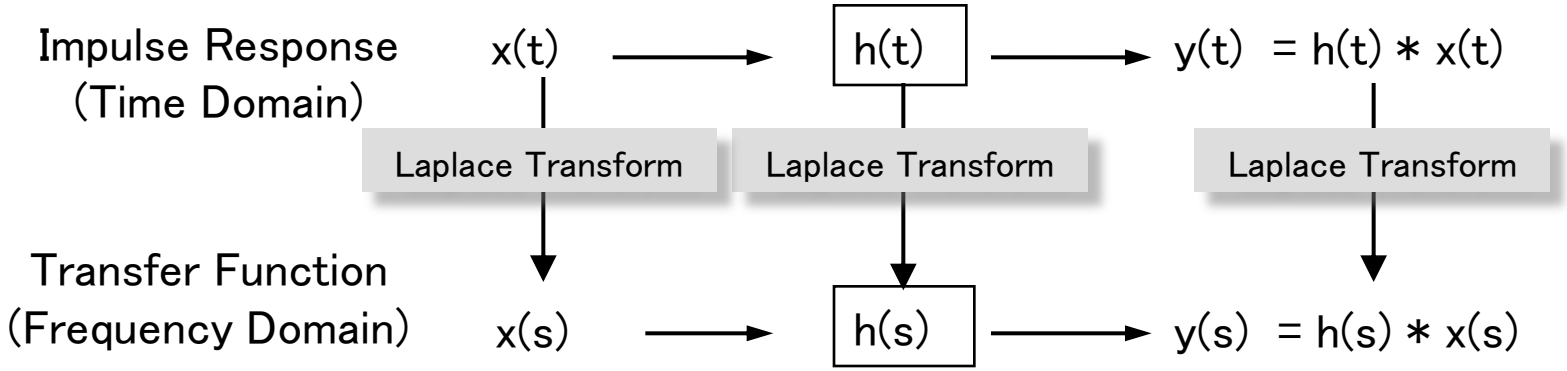
[Model] Model
[**Range]
[Algorithmic Model]
Executable
[End Algorithmic Model]
[I-V]
[Slew Rate]

```
[Model] xxxx
Model_type Output
C_comp 800f 750f 850f
Cref = 0
[Model Spec]
Vmeas .157 .15 .165
Vref .157 .15 .165
[Temperature Range]  25 100 0
[Voltage Range] .314 .299 .329
[Algorithmic Model]
Executable Windows_VisualStudio7.1.3088_32 xx_gtp_ami_tx.dll xx_gtp_ami_tx_1.ami
Executable Linux_gcc3.2.3_32 xx_gtp_ami_tx.linux.so xx_gtp_ami_tx_1.ami
[End Algorithmic Model]
[Pulldown]
-2.500 -4.95638E-02 -5.02816E-02 -4.88759E-02
0.000 +0.00000E+00 +0.00000E+00 +0.00000E+00
2.500 +4.95638E-02 +5.02816E-02 +4.88759E-02
[Pullup]
-2.500 +4.95638E-02 +5.02816E-02 +4.88759E-02
0.000 +0.00000E+00 +0.00000E+00 +0.00000E+00
2.500 -4.95638E-02 -5.02816E-02 -4.88759E-02
[Ramp]
dV/dt_r .094/60f .09/60f .098/60f
dV/dt_f .094/60f .09/60f .098/60f
|
```

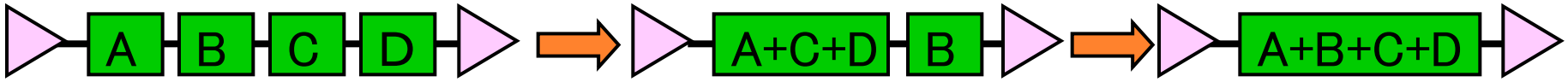
# IBIS-AMI is based on Impulse Response

- Impulse Response
  - Output when Input the Impulse (Function)


- "Impulse Response" is Laplace Transformed "Transfer Function"

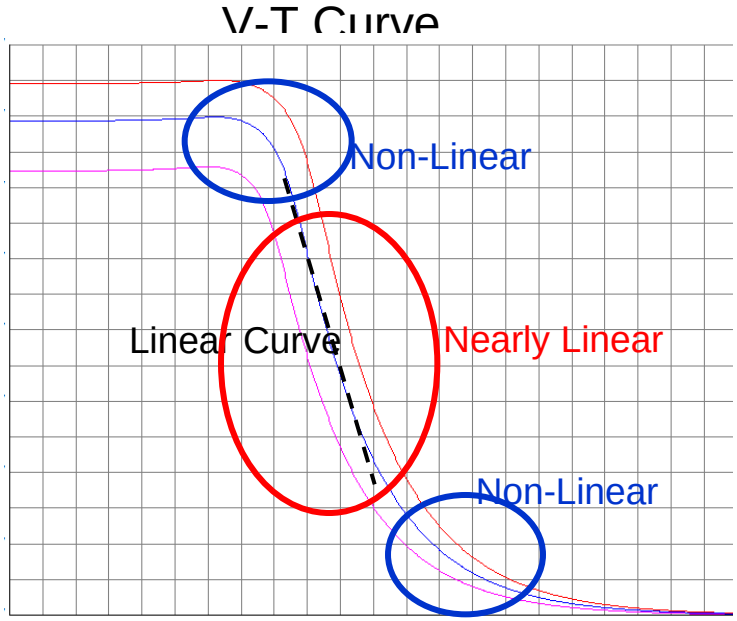



- Precondition: LTI (Linear and Time Invariant)



# Real Driver is Not Linear

- Approximation to Linear
- Can Apply LTI Condition?

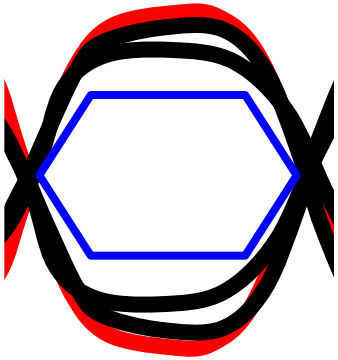



Simulation Accuracy using AMI Model?

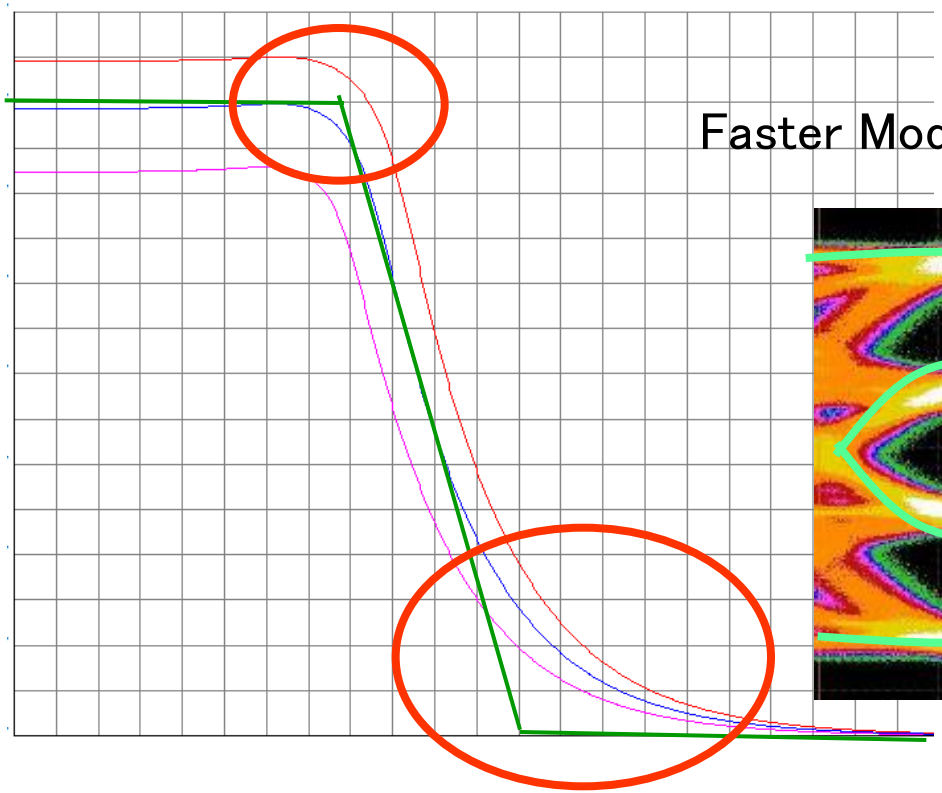
➡ Checking Simulation Accuracy by IBIS Open Forum, Vendors and Users

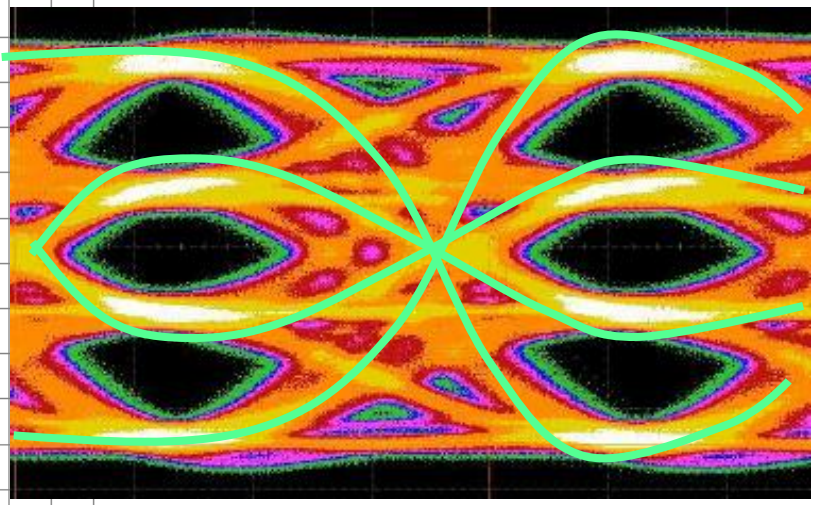
# Linear Model Makes V-Level Higher

- Linear Model is faster than actual
- Faster Model makes ringing bigger



Faster Model is not critical case for NRZ



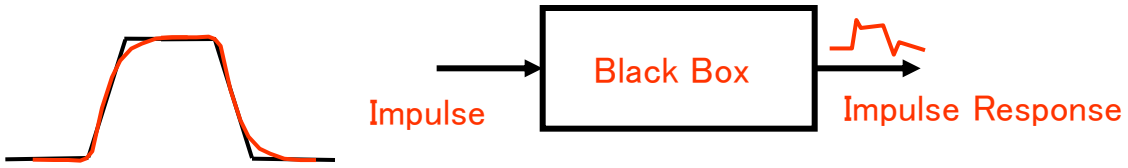


for PAM4?

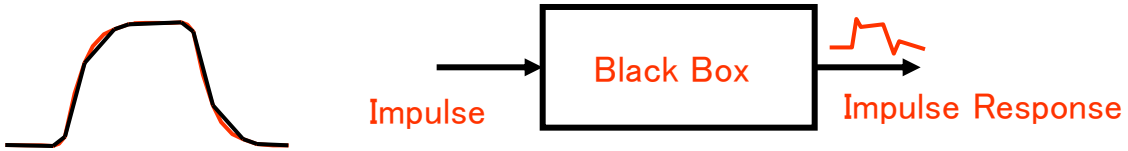
# Use More Accurate Impulse Response

- Use Stepped Linear Model

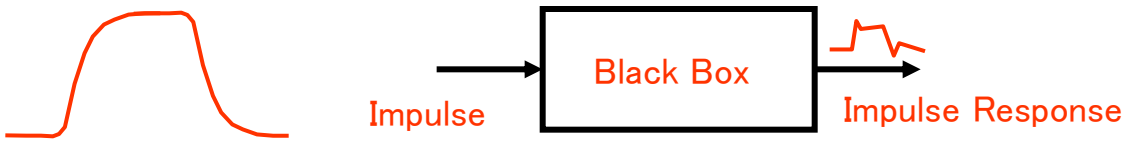
Linear Model




Divided Linear Model




Non-Linear Model



# Corner Analysis

- IBIS-AMI model: Only one case
- Critical NRZ Eye Analysis: Slow Model ?
- Critical PAM4 Eye Analysis ?
  - Which is Critical, Fast/Typ/Slow Model ?

# Conclusion

- PAM4 will be important
- How to Simulate PAM4/PAMn ?
- IBIS-AMI is best choice for now.
- There are some worries for IBIS-AMI to simulate PAM4
  - Linear Model
  - Corner Simulation

# Reference


- E.Frlan, C.YeLiu, M.PengLi “Signal Integrity Challenges & Solutions for Next-Generation CEI-56G “Chip-to-Module” & “Chip-to-Chip” Interface”, DesignCon 2015
- Shinichi Maeda, KEI Systems “IBIS-AMI Model (Algorithmic Model Interface) ~Theory & Structure~” , Asian IBIS Summit, Japan 2013
- Motoaki Mtsumura, FUJITSU Semiconductor Ltd., “The Application of Simulation Kit Using USB 3.0 IBIS-AMI Model” ” , Asian IBIS Summit, Japan 2012
- Ryan Cotts, Netlogic and others “AMI Modeling Methodology and Measurment Correlation of a 6.25Gb/s Link” IBIS Summit DAC, 2011