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IBIS Simulation for High-Speed Memory Interface Board

Suggestions : How to use IBIS model correctly

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Asian IBIS Summit
Tokyo, JAPAN
November 16, 2015

Agenda

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- IBIS Model Quality the past, the present
- Example of incorrect simulation
- Suggestion to EBD specifications for DIMM simulation
- Summary

IBIS Model Quality the past, the present

IBIS Model Quality the past, the present

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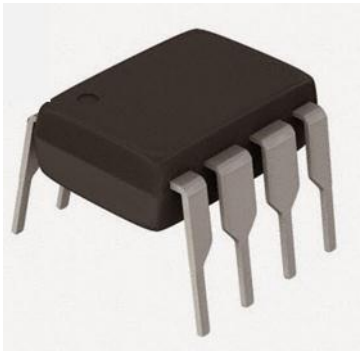
Started board simulation using the IBIS model in 1999.
At that time IBIS model was Ver3.1.
The IBIS Model quality was poor in those days.

Ex.1) There was no PKG parameter.



DIP
(Dual Inline Package)

```
[Component]      XXXXXXXX
[Manufacturer] ABC  Company
[Package]
| variable      typ            min            max
R_pkg           0.000          NA             NA
L_pkg           0.000nH        NA             NA
C_pkg           0.000pF        NA             NA
```

IBIS Model Quality the past, the present

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Ex.2) A value of C_comp was incorrect .

```
[Model]  LVTTL_12mA
Model_type I/O
Polarity       Non-Inverting
Enable         Active-Low
Vinl = 0.8
Vinh = 2.0
Vmeas =  1.65V
Cref =   0.0F
Rref =   50.000
Vref =   0.0V
C_comp   0.0pF   0.0pF   0.0pF
```

IBIS Model Quality the past, the present

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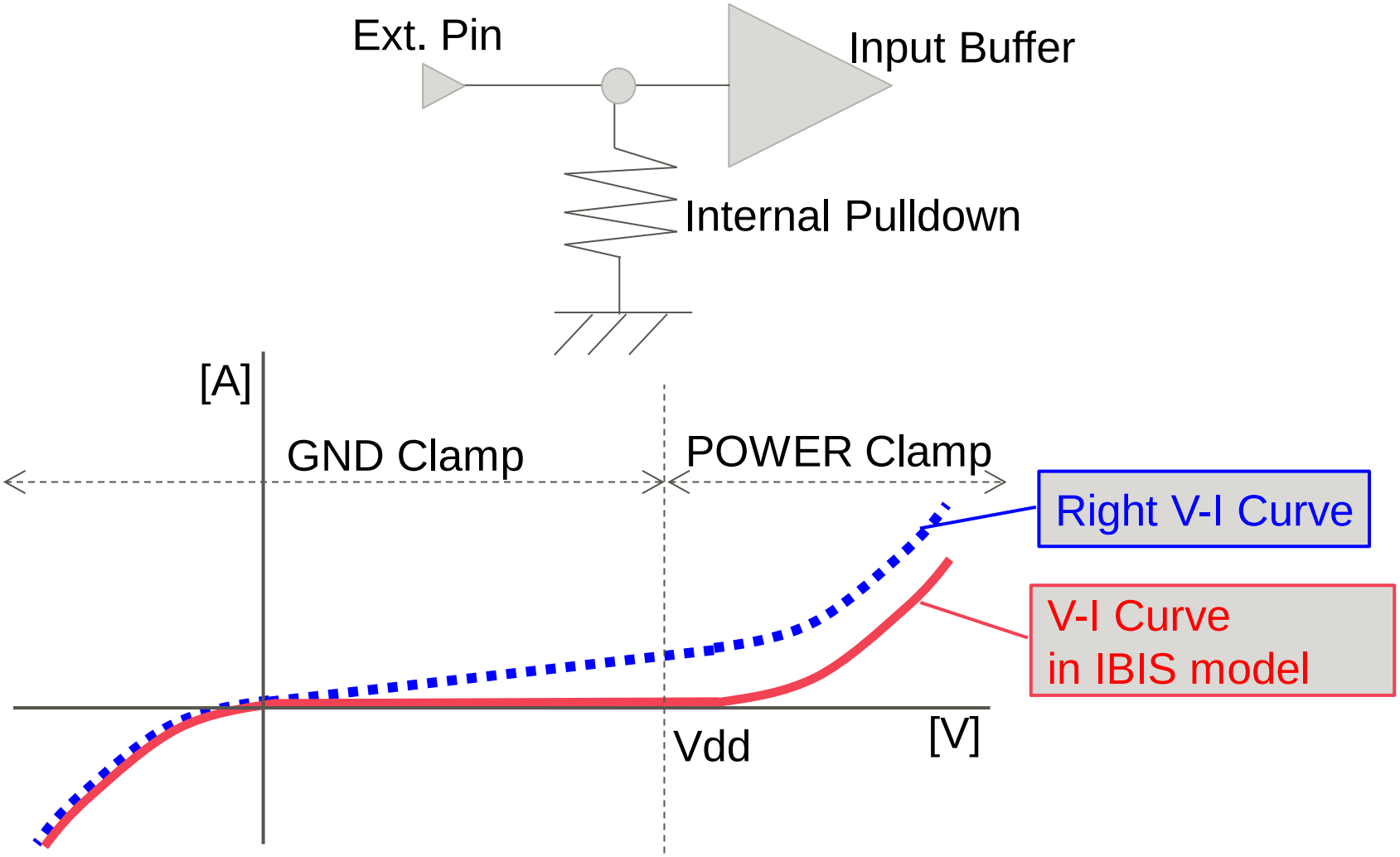
Ex.3) V-I Curve of Input Buffer with Internal Pulldown was incorrect.



IBIS Model Quality the past, the present

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Checked the IBIS model carefully.

```
[Model]  LVTTL_12mA
Model_type Input
Vinl = 0.8
Vinh = 2.0
C_comp   0.0pF   0.0pF   0.0pF
```

Corrected the incorrect part of IBIS Model.

```
[Model]  LVTTL_12mA
Model_type Input
Vinl = 0.8
Vinh = 2.0
C_comp   1.0pF   0.8pF   1.2pF
```

IBIS Model Quality the past, the present

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- The quality of the recent IBIS Model has been improved.
- Few incorrect values are seen.
- Therefore IBIS Model could be used without careful inspection.
- With adding [Model Spec]'s subparameters (S_overshoot_high, S_overshoot_low, D_overshoot_high, D_overshoot_low, D_overshoot_time) to IBIS Model, simulation can be started immediately.
- Correct result is provided in most of the cases.
- Reason to get incorrect simulation result in such situation.
  - Missed instructions provided in [Notes] .
  - The IBIS keyword that a simulator supports is not known.

Example of incorrect simulation

- Ex.1) Attention to model usage in [Notes]
- Ex.2) The IBIS keyword that a simulator supports
- Ex.3) Modeling method of Output buffer

Ex.1) Attention to model usage in [Notes]

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Demand of the circuit designer

Mode Register

Bit 2	Bit 1	Bit 0	ODT [Ohm]
0	0	0	OFF
0	0	1	XX
0	1	0	YY

Choice of the simulation engineer

IBIS Model

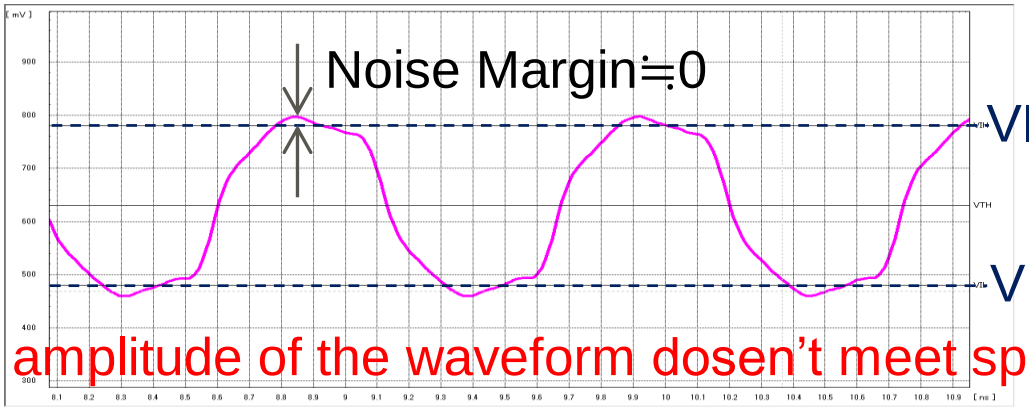
[Model Selector] INPUT

|

IN_ODT_OFF “No ODT”

IN_ODT_xx “xx Ohm ODT”

IN_ODT_yy “yy Ohm ODT”



The amplitude of the waveform dosen’t meet spec.

Simulation engineer : Need to check contents of IBIS to find the reason.

Ex.1) Attention to model usage in [Notes]

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Demand of the circuit designer

Choice of the simulation engineer

Mode Register

Bit 2	Bit 1	Bit 0	ODT [Ohm]
0	0	0	OFF
0	0	1	XX
0	1	0	YY

Right Choice

IBIS Model

[Model Selector] INPUT

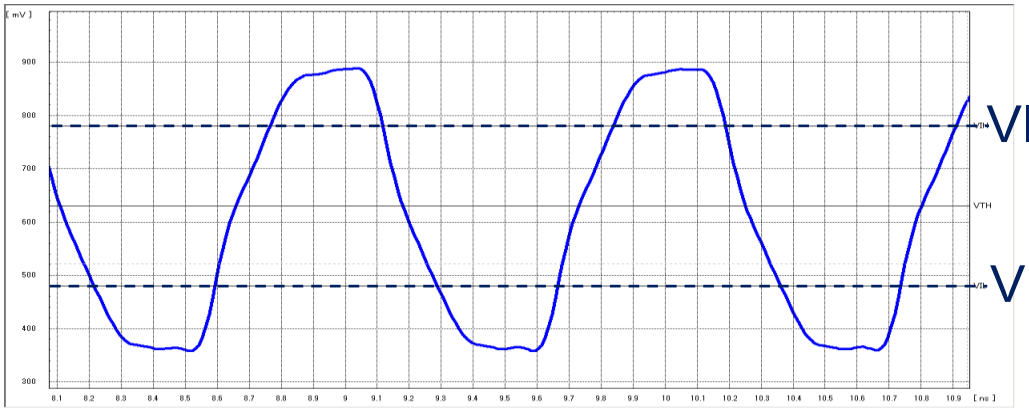
|

IN_ODT_OFF “No ODT”

IN_ODT_xx “xx Ohm ODT”

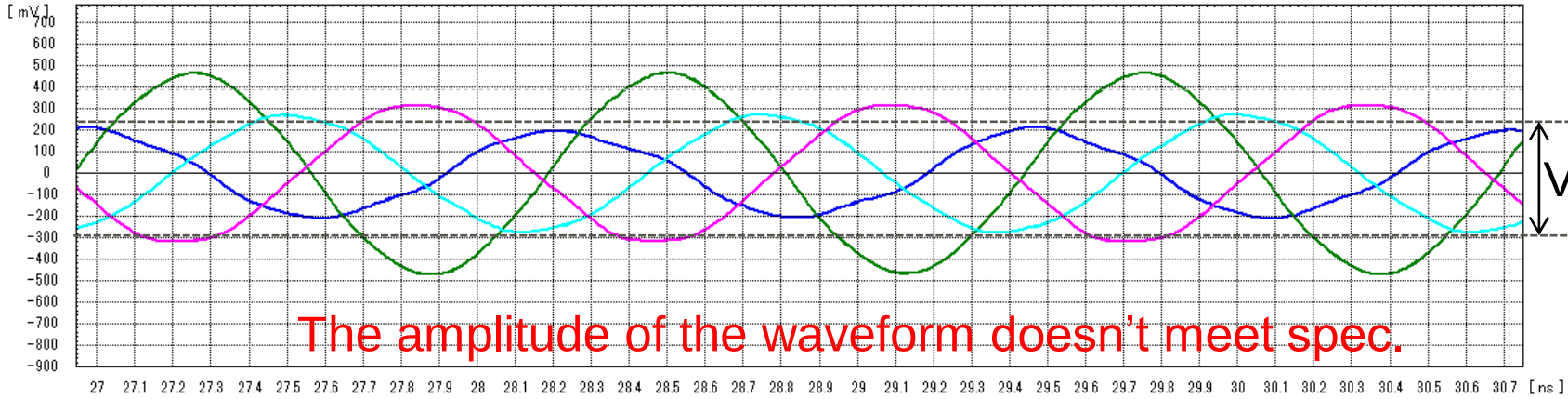
IN_ODT_yy “yy Ohm ODT”

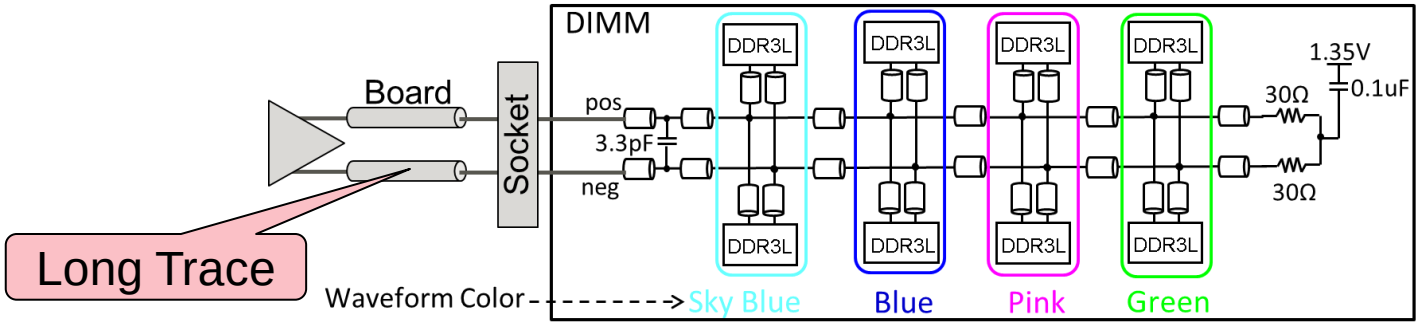
There is the explanation of the model choice corresponding to the register setting in [Notes] and “Readme.txt”



Ex.2）The IBIS keyword that a simulator supports

DDR3L SODIMM Clock Waveform (The first simulation)





Long trace is causing the problem?

Ex.2）The IBIS keyword that a simulator supports

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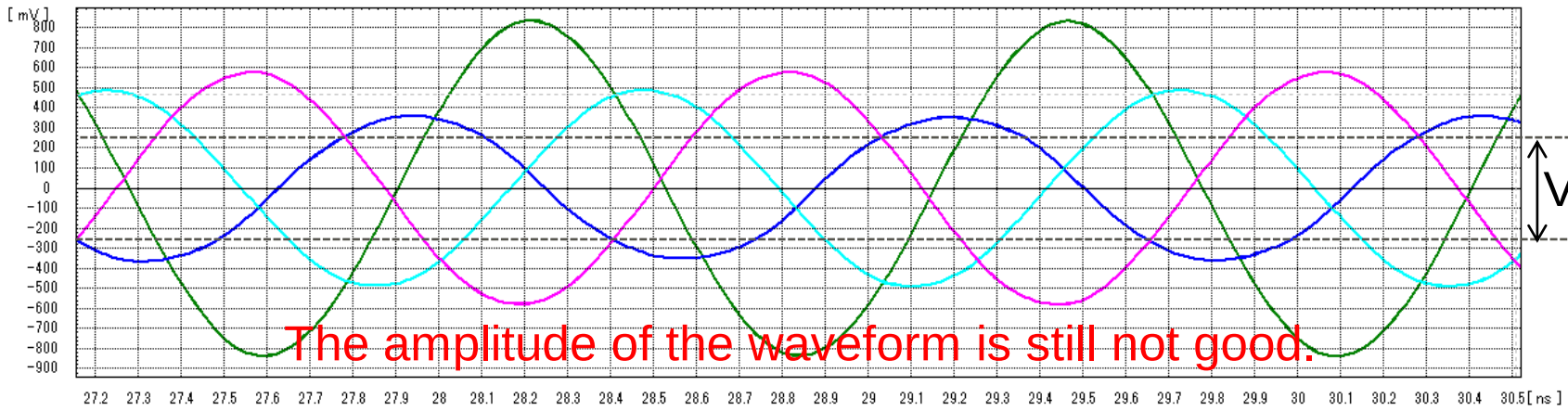
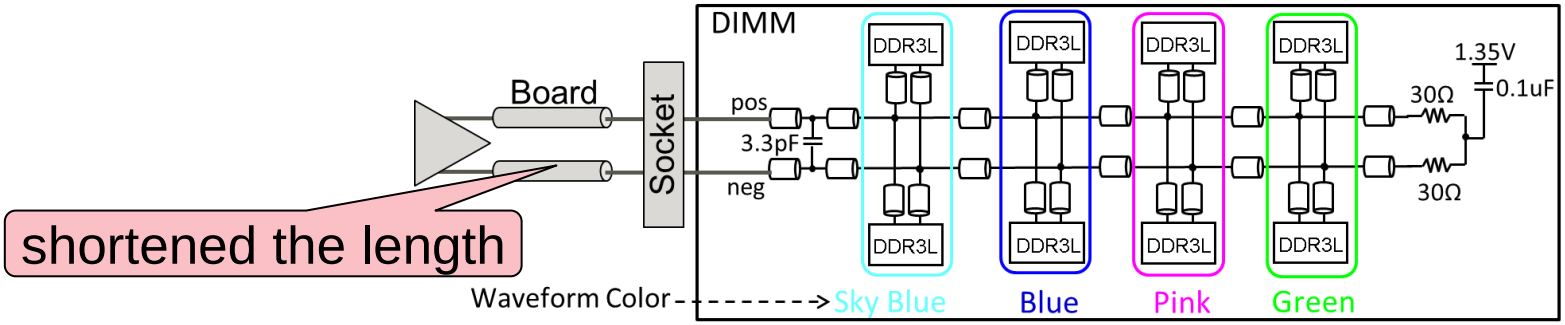
DDR3L SODIMM Clock Waveform（After a trace length change）





Reason?

Check the Buffer model and IBIS to find other causes.

Ex.2）The IBIS keyword that a simulator supports

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Cause:

- Die capacitance subparameter of the memory's IBIS :
  C_comp_power_clamp, C_comp_gnd_clamp
- The simulator does not support those subparameters.
  Therefore the simulator judged that there was no C_comp.
  And simulator's default C_comp was added to IBIS
  by an automatic correction mechanism.
- Added C_comp > C_comp_power_clamp + C_comp_gnd_clamp
  So a waveform was destroyed by a reflection noise by the big input capacitance.
- The simulator gave a message as follows, but continued processing.
  - Warning that there is no C_comp.
  - Warning that simulator will use default C_comp.

Ex.2）The IBIS keyword that a simulator supports

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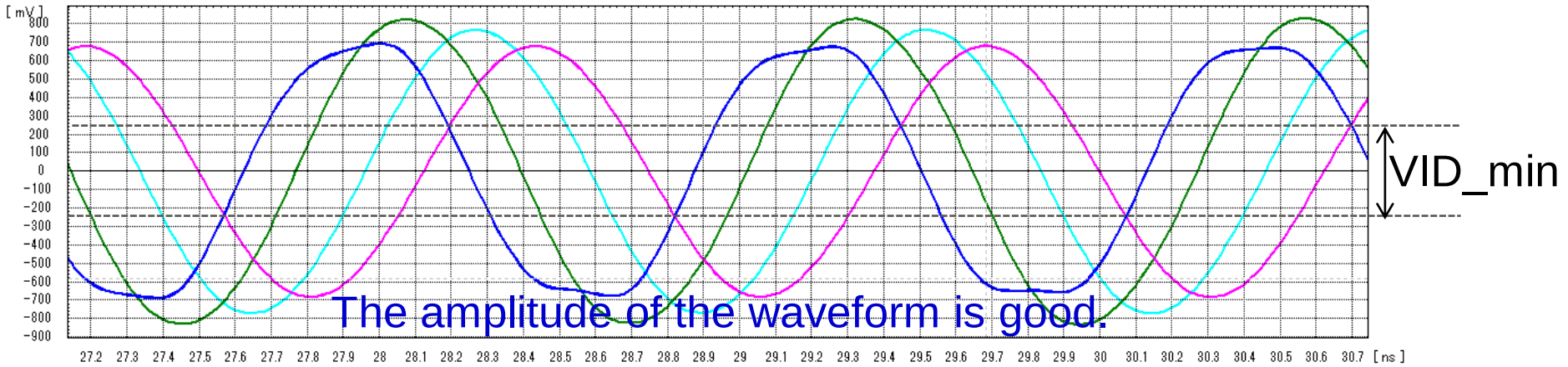
DDR3L SODIMM Clock Waveform（After C_comp correction）



Ex.3) Modeling method of Output buffer

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- For the accurate modeling of the output buffer, it is necessary to use two [Rising Waveform] and two [Falling Waveform].
  (Accuracy of the modeling：two[Rising Waveform] & two[Falling Waveform] > [Ramp])
- [Ramp] may be used for modeling by the following causes.
  - Setting of the simulator
  - Start times of four Waveforms are different.(See below.）

[Rising Waveform]
V_fixture= 0.6750
R_fixture= 25.0000

time	V(typ)	V(min)	V(max)
0.01pS	0.21V	0.26V	0.18V
30.00pS	0.21V	0.26V	0.18V

[Falling Waveform]
V_fixture= 0.6750
R_fixture= 25.0000

time	V(typ)	V(min)	V(max)
0.03pS	1.12V	0.99V	1.21V
30.00pS	1.12V	0.99V	1.21V

[Rising Waveform]
V_fixture= 0.0
R_fixture= 25.0000

time	V(typ)	V(min)	V(max)
0.00pS	0.0V	0.0V	0.0V
30.00pS	0.0V	0.0V	0.0V

[Falling Waveform]
V_fixture= 0.0
R_fixture= 25.0000

time	V(typ)	V(min)	V(max)
0.02pS	0.82V	0.63V	0.97V
30.00pS	0.82V	0.63V	0.97V

Ex.3) Modeling method of Output buffer

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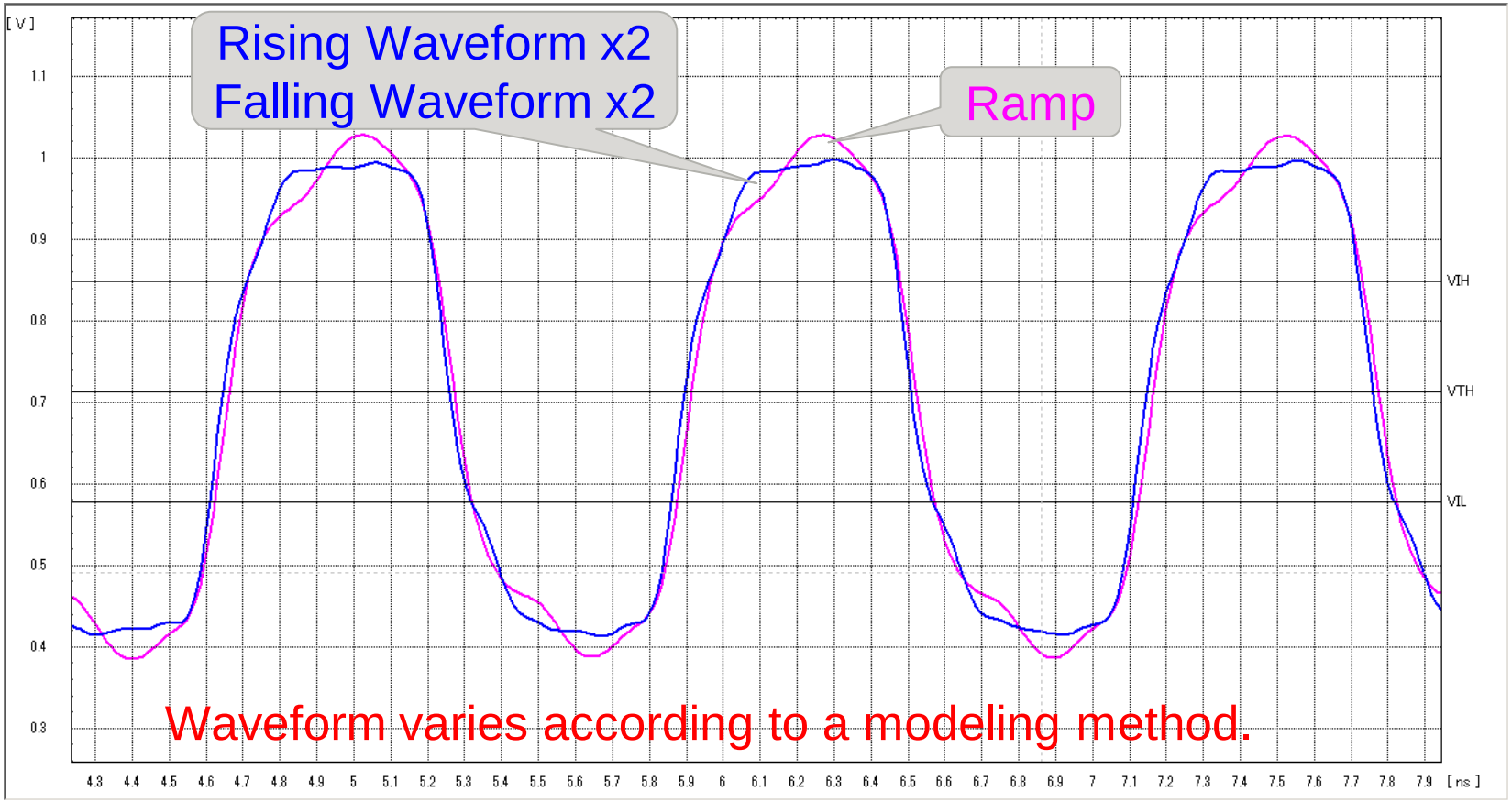
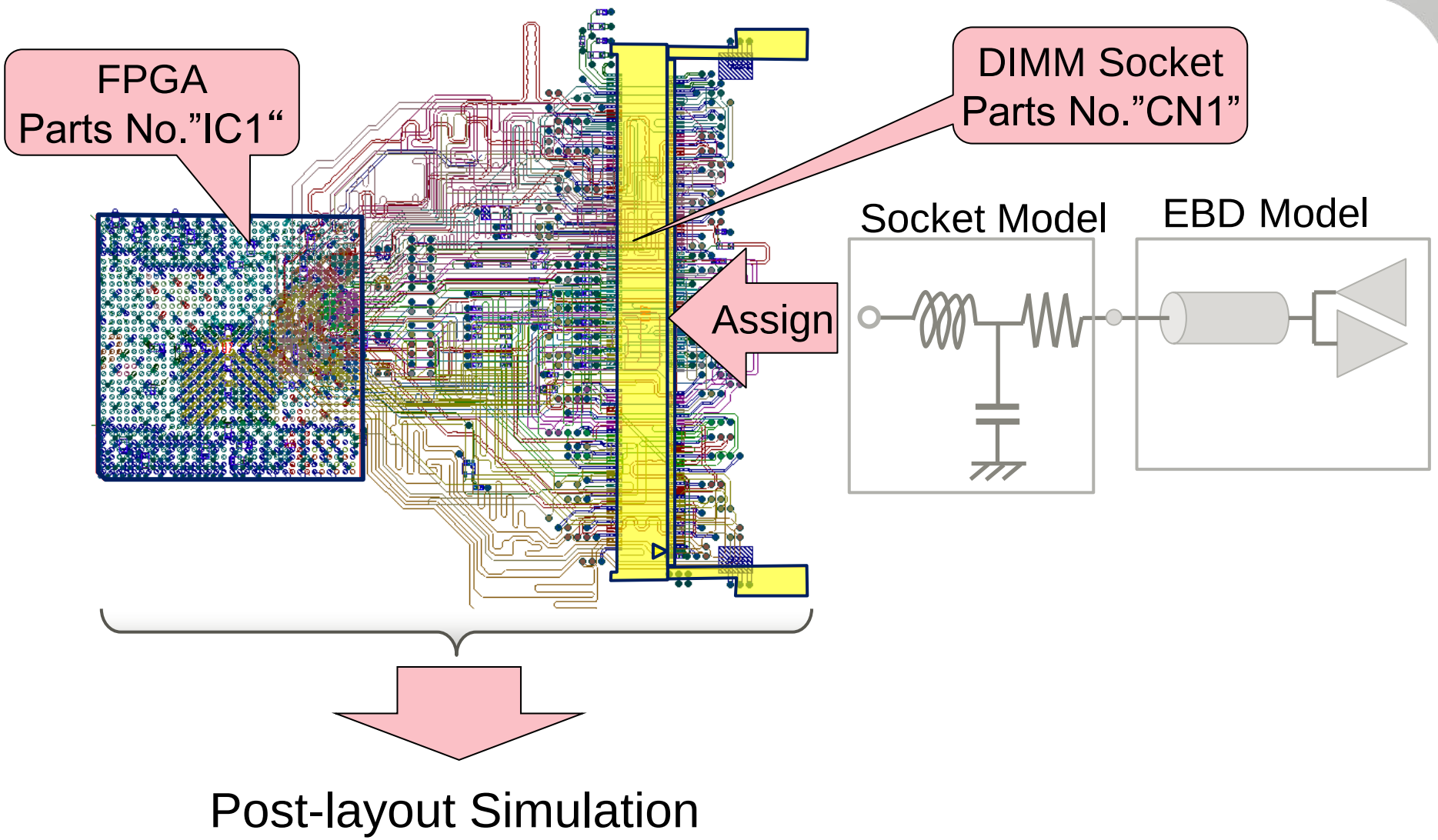
DDR3L DQ Waveform Comparison: [Waveform]x4 vs. [Ramp]



Suggestion to EBD specifications for DIMM simulation

- Addition of a socket model element to EBD
- Support the Skin effect and the Dielectric loss for EBD line model

Addition of a socket model element to EBD



Addition of a socket model element to EBD

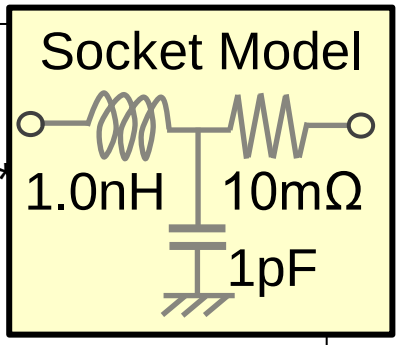
Make a model to assign for DIMM socket "CN1"

Original EBD Model

```
[Path Description] 7
Pin 7
Len=0.2 L=3.5e-9 C=1.0e-12 R=0.1 /
Len=0 R=15 /
Len=0.1 L=3.5e-9 C=1.0e-12 R=0.1 /
Len=1.3 L=4.0e-9 C=1.2e-12 R=0.1 /
Len=0.1 L=3.5e-9 C=1.0e-12 R=0.1 /
Node Mem1.C7
```

EBD model after the socket model addition

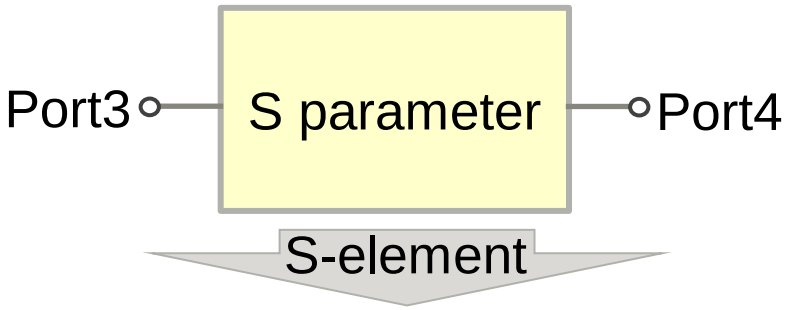
```
[Path Description] 7
Pin 7
|***** DIMM SOCKET *******
Len=0 L=1.0e-009 /
Len=0 C=1.0e-012  /
Len=0 R=1.0e-002 /
|***** DIMM SOCKET *******
Len=0.2 L=3.5e-9 C=1.0e-12 R=0.1 /
Len=0 R=15 /
Len=0.1 L=3.5e-9 C=1.0e-12 R=0.1 /
Len=1.3 L=4.0e-9 C=1.2e-12 R=0.1 /
Len=0.1 L=3.5e-9 C=1.0e-12 R=0.1 /
Node Mem1.C7
```

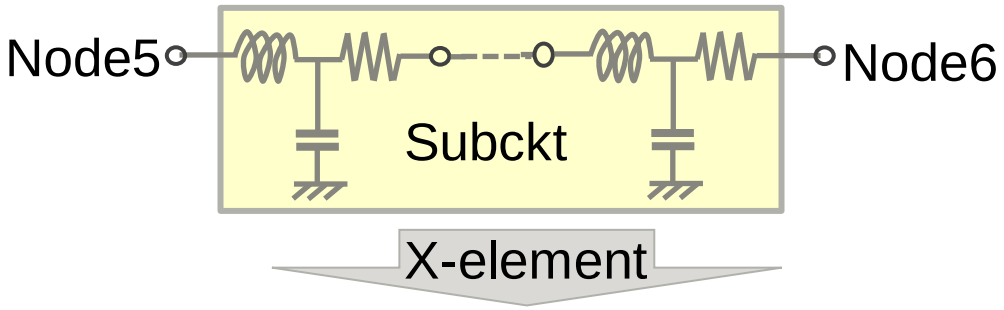


This can be done for simple models.
Need a better way for complicated models.
(S parameter, Complicated Spice Subcircuit)

Addition of a socket model element to EBD

Therefore suggestion is to be able to use S-element and X-element in EBD.
(The S-element and the X-element are available in IBIS-ISS.)





Description example

```
[Path Description] 7
Pin 7
|***** DIMM SOCKET  *******
|    Port1_No.  Port2_No.  mname
S      3              4          socket_spara  /
|***** DIMM SOCKET  *******
Len=0.2 L=3.5e-9 C=1.0e-12 R=0.1 /
          ¦
Node Mem1.C7
```

Description example

```
[Path Description] 7
Pin 7
|***** DIMM SOCKET  *******
|  node_1  node_2   subckt_name
X    5             6        socket_spice  /
|***** DIMM SOCKET  *******
Len=0.2 L=3.5e-9 C=1.0e-12 R=0.1 /
          ¦
Node Mem1.C7
```

Addition of a socket model element to EBD

Description example（Continue from the previous page）

```
[Reference Designator Map]
| Ref Des  File name   Component name
R1          rtt_clk.ibs      rtt_clk_30ohm
R2          rtt_addr.ibs     rtt_addr_36ohm
Mem1        DDR3L.ibs        DDR3L_1600_MEMORY
Mem2        DDR3L.ibs        DDR3L_1600_MEMORY

| mname              TSTONEFILE
socket_spara         dimm_soc.s4p

| subckt_name        SUBCKTFILE
socket_spice         socket_mdl.sp

[End Board Description]
```

Support the Skin effect and the Dielectric loss for EBD line model

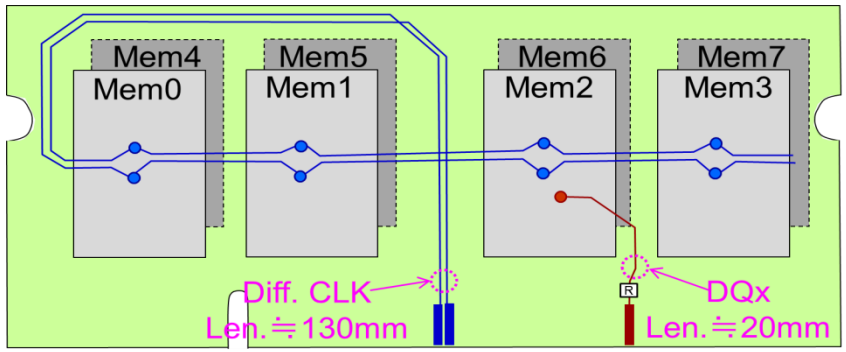
Example #1

【DDR3L SODIMM】Waveform comparison:

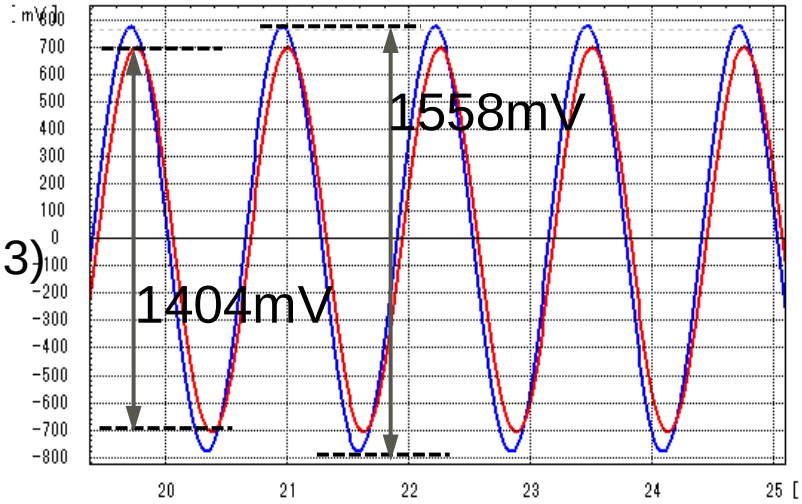
Line Model with LCR only(=EBD) vs. Line Model with Skin-Effect and Dielectric Loss

DDR3 Unbuffered SO-DIMM
Raw Card B

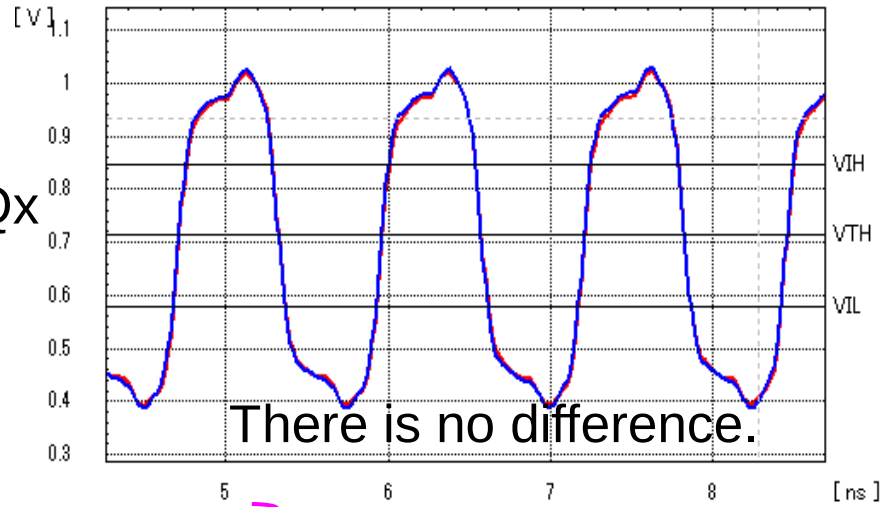
PC3-12800(DDR3-1600)



CLK
(Mem3)



DQx



Line Model with LCR only(equal to EBD)

Line Model with Skin-Effect and Dielectric Loss

11% Difference!!(CLK)

Support the Skin effect and the Dielectric loss for EBD line model

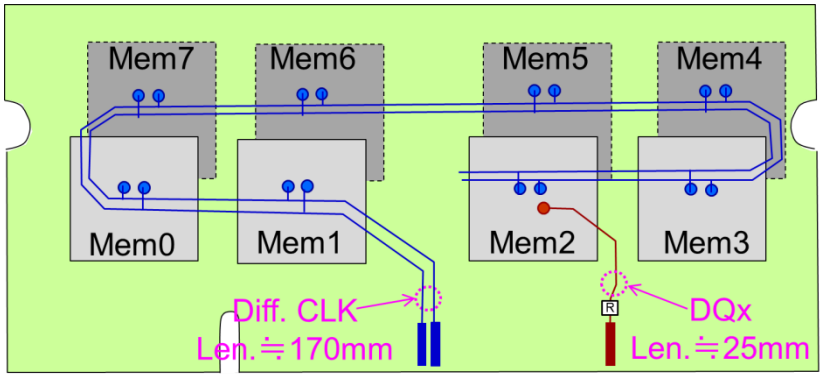
Example #2

【DDR4 SODIMM】Waveform comparison:

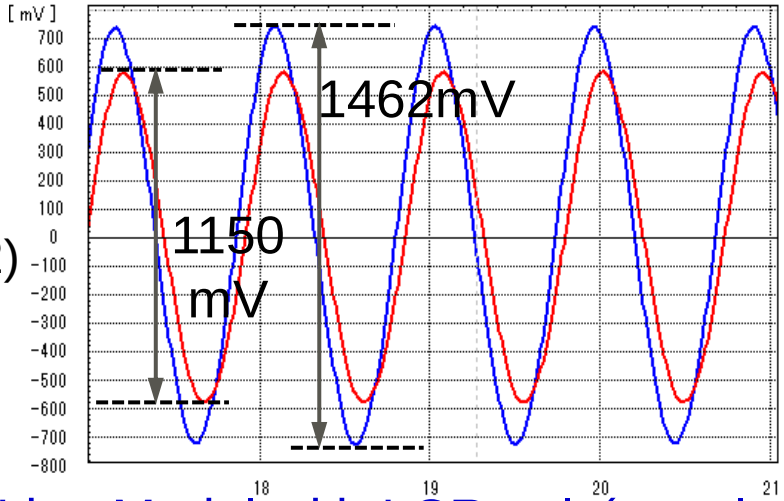
Line Model with LCR only(=EBD) vs. Line Model with Skin-Effect and Dielectric Loss

DDR4 Unbuffered SO-DIMM
Raw Card A

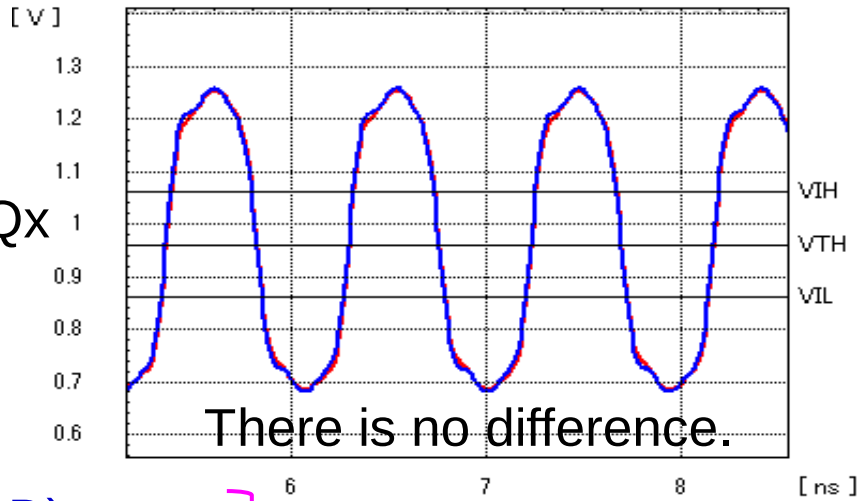
PC4-17000(DDR4-2133)



CLK
(Mem2)



DQx



Line Model with LCR only(equal to EBD)

Line Model with Skin-Effect and Dielectric Loss

27% Difference!!(CLK)

Support the Skin effect and the Dielectric loss for EBD line model

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Therefore suggestion is to be able to use W-element in EBD.
(The W-element are available in IBIS-ISS.)

Conventional EBD

```
[Path Description] 7
Pin 7
Len=0.2 L=3.5e-9 C=1.0e-12 R=0.1 /
Len=0 R=15 /
Len=0.1 L=3.5e-9 C=1.0e-12 R=0.1 /
      |
Node Mem1.C7
```

Add “Rs” and “Gd” to use the W-element for line model.

EBD example with skin-effect and dielectric loss

```
[Path Description] 7
Pin 7
Len=0.2 L=3.5e-9 C=1.0e-12 R=0.1 Rs=2.0e-5 Gd=7.6e-14 /
Len=0 R=15 /
Len=0.1 L=3.5e-9 C=1.0e-12 R=0.1  Rs=2.0e-5 Gd=7.6e-14 /
      |
Node Mem1.C7
```

Summary

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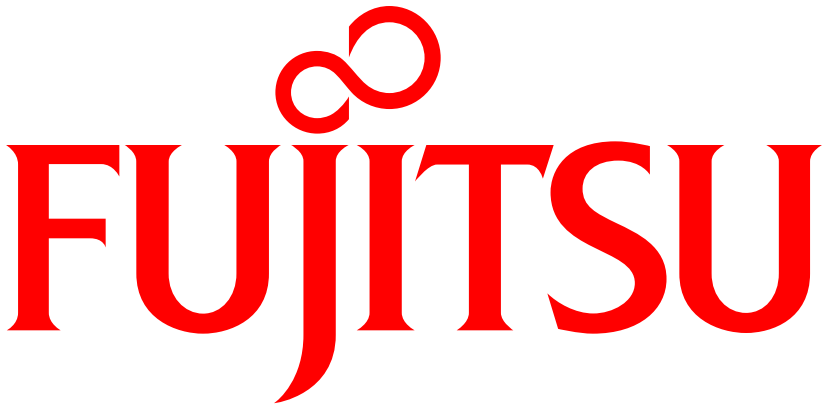
- The quality of the recent IBIS Model has been improved.
- Few models have incorrect values.
- In most cases, correct result is provided by simulation.
- Difference in Simulation Engineer's skill(about IBIS, Simulator and Device) may make incorrect simulation result.
- Suggested additions to the IBIS specification for EBD.
  - Adopt X-element and S-element for inserting socket model to DIMM model.
  - Adopt W-element "Rs", "Gd" for Skin-Effect and Dielectric Loss.

Reference

- “IBIS(I/O Buffer Information Specification)Version 6.1”, IBIS Open Forum 2015
- “IBIS Interconnect SPICE Subcircuit (IBIS-ISS) Specification Version 1.0”, IBIS Open Forum 2011
- “4.20.18 - 204-Pin DDR3 SDRAM Unbuffered SO-DIMM Design Specification“,2015 JEDEC
- “Annex A, R/C A, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM SODIMM Design Specification”,2015 JEDEC



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