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A PRACTICAL DOE APPLICATION IN STATISTICAL SI ANALYSIS USING IBIS & HOW CAN WE MAKE IBIS WORK BEYOND BEST CASE/WORST CASE?

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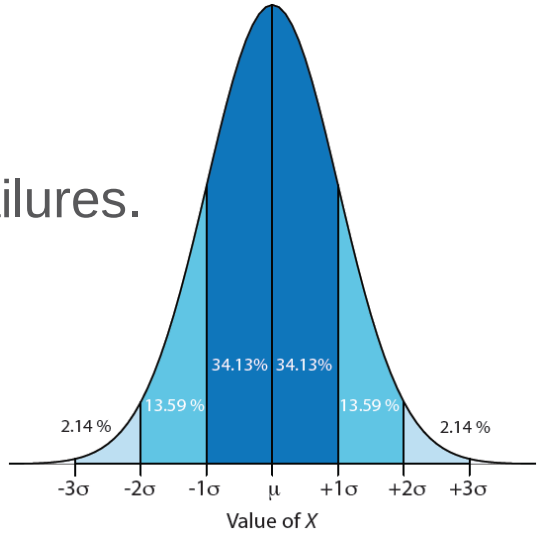
Authors:
Feng Shi, Anders Ekholm, Zilwan Mahmod & David Zhang.

AGENDA

- IBIS & Statistical analysis
- DOE as a statistical methodology
- Practical DDR3/DDR4 Topology problem solved by DOE
- How can we extend IBIS to support confidence interval analysis.
- Suggestion to enhance IBIS typ, min, max corners with distribution data.
- Conclusion

IBIS & STATISTICAL ANALYSIS

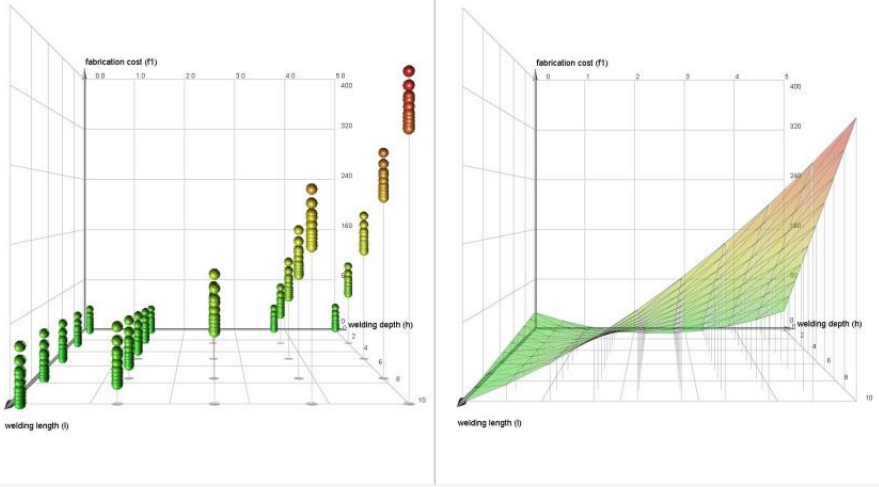
- IBIS based SI analysis uses:
  - Behavioral buffer models. typ, min, max (BC/WC)
  - Trace modeling of topology BC/WC
  - Via modeling BC/WC
- Best Case / Worst case analysis assumes:
  - 100% confidence interval. Every produced individual works.
- Statistical SI analysis predicts:
  - Defects at a given confidence interval.
  - Help manage overdesign and possible BC/WC failures.



DOE AS A STATISTICAL METHODOLOGY

- DOE Design Of Experiments will fit a model to our solutions space (often used is a RSM Response Surface Model)
- Uses much fewer simulation than sweep analysis or Monte Carlo analysis.
- Catches cross term interaction missed by OFAT analysis.
  - (OFAT, One Factor At a Time)

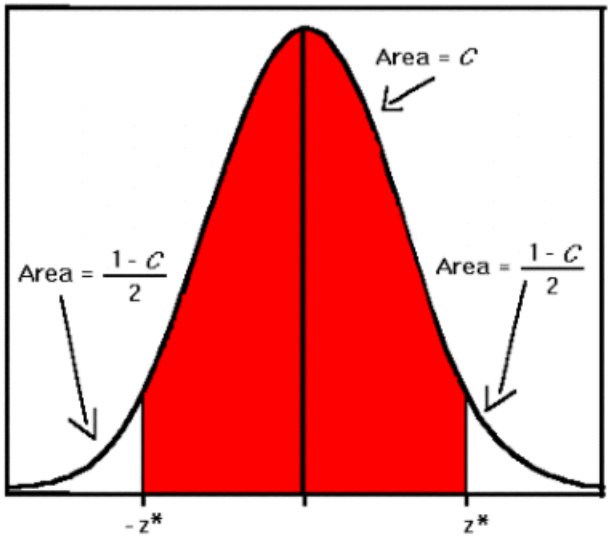
- RSM used to predict the fitted part of the solutions space and to give Confidence Intervals for the predicted respons.



PRACTICAL DDR TOPOLOGY PROBLEM SOLVED BY DOE

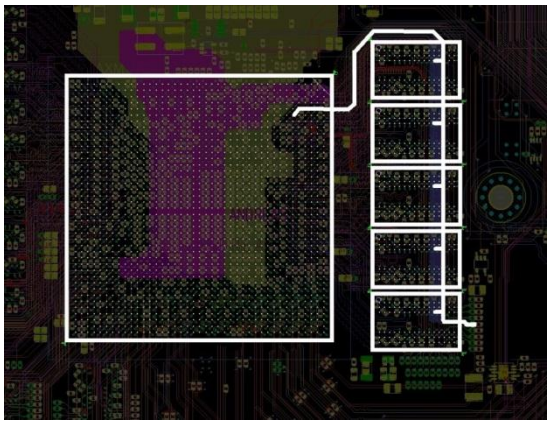
- Problem of ringing in a high speed DDR3/DDR4 address/command/control bus in memory down solutions with thick PCB's >1mm.

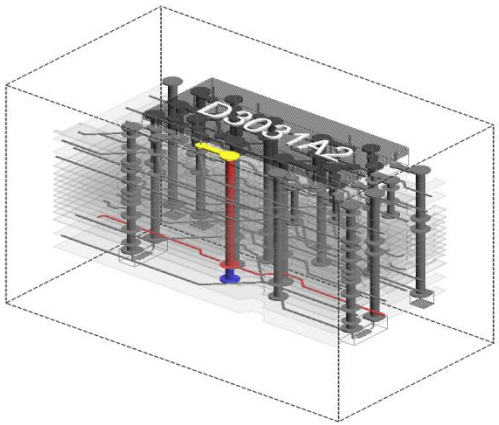
- Find an optimal topology that solves the problem with a given confidence e.g. 95%

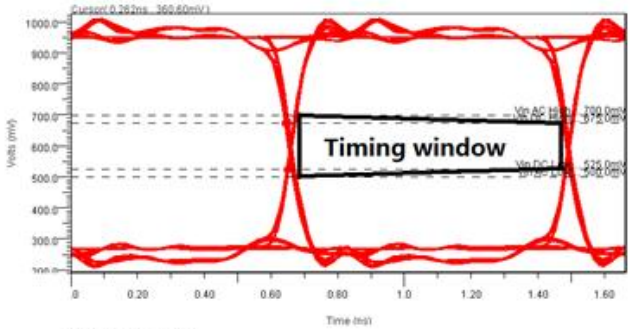


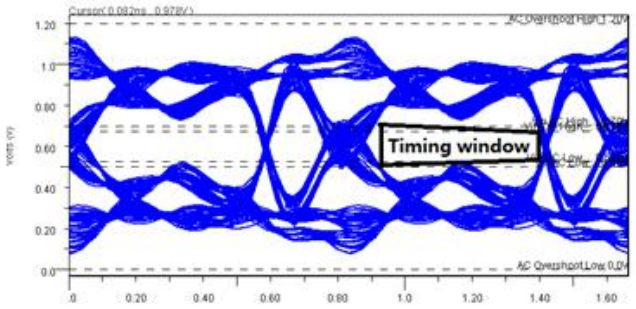
PRACTICAL DDR TOPOLOGY PROBLEM SOLVED BY DOE

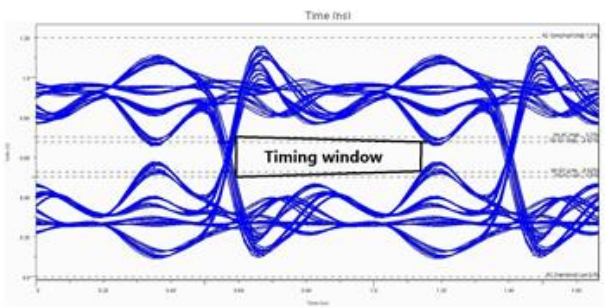
- DDR3/DDR4 address/command/control bus topology
  - Flyby? Daisy-chain. →Reflection
  - Thick PCB's >1mm. →Ringback









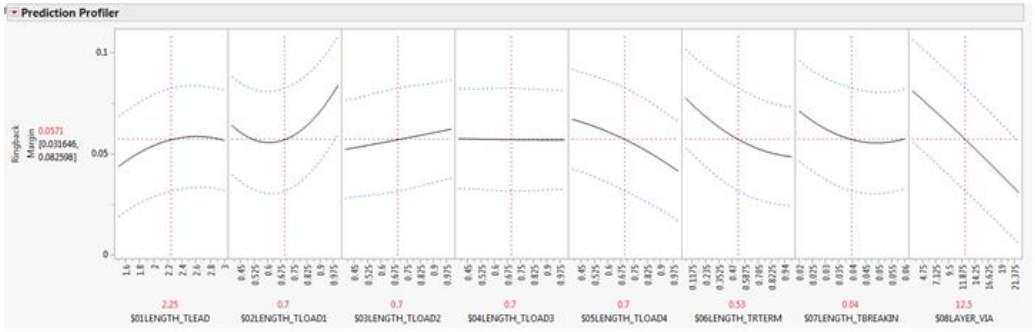


PRACTICAL DDR TOPOLOGY PROBLEM SOLVED BY DOE

Design Parameter	Factor	Factor Type	Min	Typ	Max	Analysis Type
Length of lead Tline	01Length_TLead	Continuous	1.5inch	2.25inch	3 inch	Design
Length of first load Tline	02Length_TLoad1	Continuous	0.4inch	0.7inch	1 inch	Design
Length of second load Tline	03Length_TLoad2	Continuous	0.4 inch	0.7inch	1 inch	Design
Length of third load Tline	04Length_TLoad3	Continuous	0.4 inch	0.7inch	1 inch	Design
Length of forth load Tline	05Length_TLoad4	Continuous	0.4 inch	0.7inch	1 inch	Design
Length of Tline to the termination resistor	06Length_TRterm	Continuous	0.06 inch	0.53inch	1 inch	Design
Length of memory fanout Tline	07Length_TBreakin	Continuous	0.02 inch	0.04inch	0.06 inch	Design
Routing layer/ Via barrel length	08Layer_Via	Categorical	3, 5, 7, 18, 20, 22 layer			Design
Driver impedance of controller	09Z_Controller	Categorical	34ohm	40 ohm	48 ohm	Design
Via anti-pad size	10C_Via	Categorical	1=hiC	2=typC	3=lowC	Design
Impedance of lead Tline	11Z_TLead	Categorical	40 ohm	50 ohm	60 ohm	Design& Manufacturing
Impedance of load Tline	12Z_TLoad	Categorical	40 ohm	50 ohm	60 ohm	Design& Manufacturing
Impedance of Tline to the termination resistor	13Z_TRterm	Categorical	40 ohm	50 ohm	60 ohm	Design& Manufacturing
Impedance of memory fanout Tline	14Z_TBreakin	Categorical	40 ohm	50 ohm	60 ohm	Design& Manufacturing
Input capacitance of memory IO buffer	15C_MemoryIO	Categorical	2=0.2	4=0.4	6=0.6	Manufacturing
Termination resistor	16R_Rterm	Continuous	36 ohm	39 ohm	43 ohm	Design
Packaging resistance of memory	17R_Pkg	Continuous	0.05 ohm	0.525 ohm	1 ohm	Manufacturing
Packaging inductance of memory	18L_Pkg	Continuous	0.5nH	1.75nH	3nH	Manufacturing
Packaging capacitance of memory	19C_Pkg	Continuous	0.2pF	0.5pF	0.8pF	Manufacturing

PRACTICAL DDR TOPOLOGY PROBLEM SOLVED BY DOE

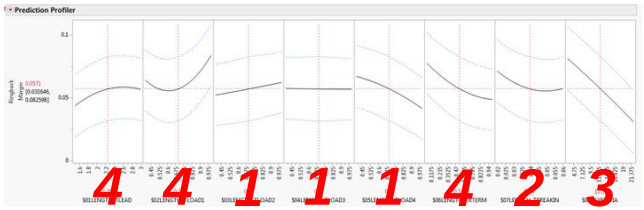
› Prediction Profiler

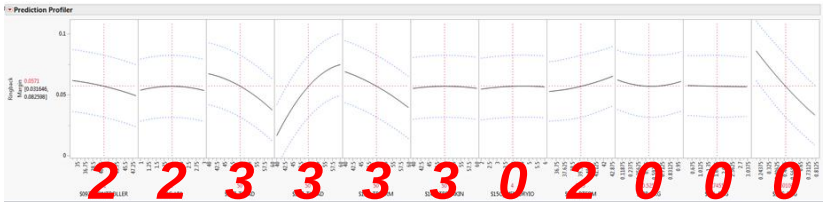


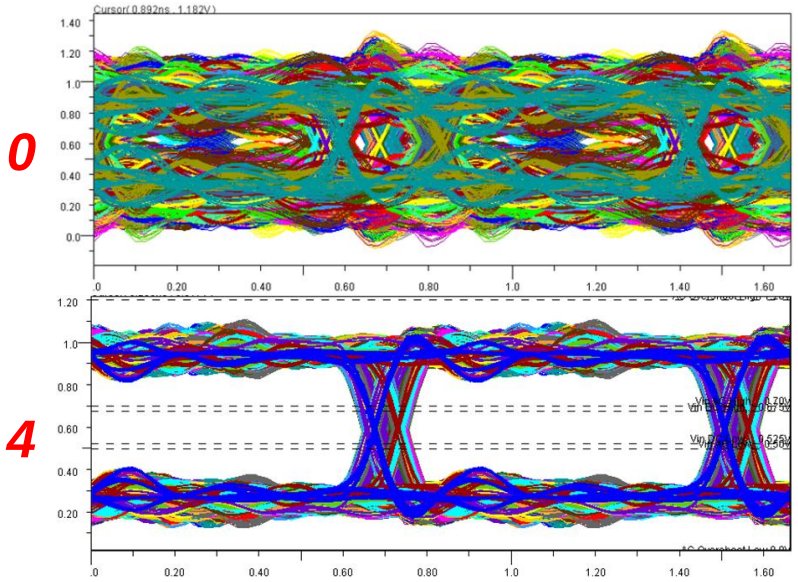
- Confidence interval ------> Quality
- Slope ------> Influence /Importance
- Vertical red line ------> “What if ” analysis & Interactions
- Desirability function ------> Optimization

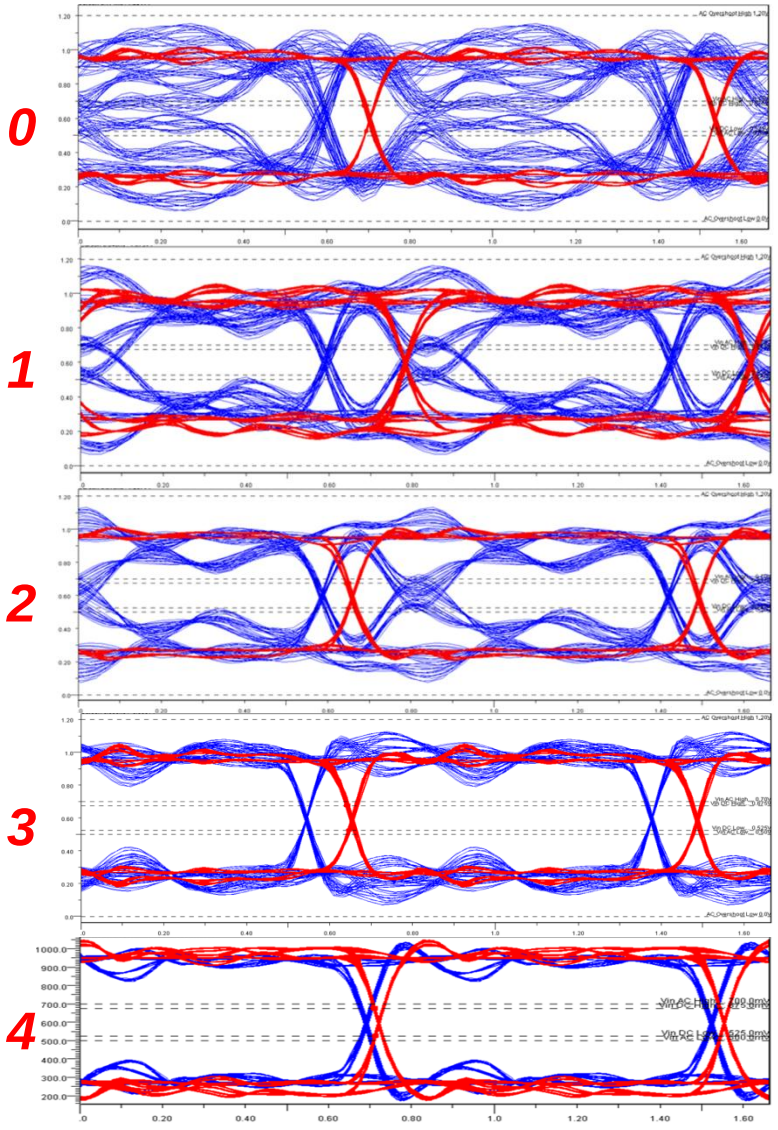
PRACTICAL DDR TOPOLOGY PROBLEM SOLVED BY DOE

› DOE Optimization



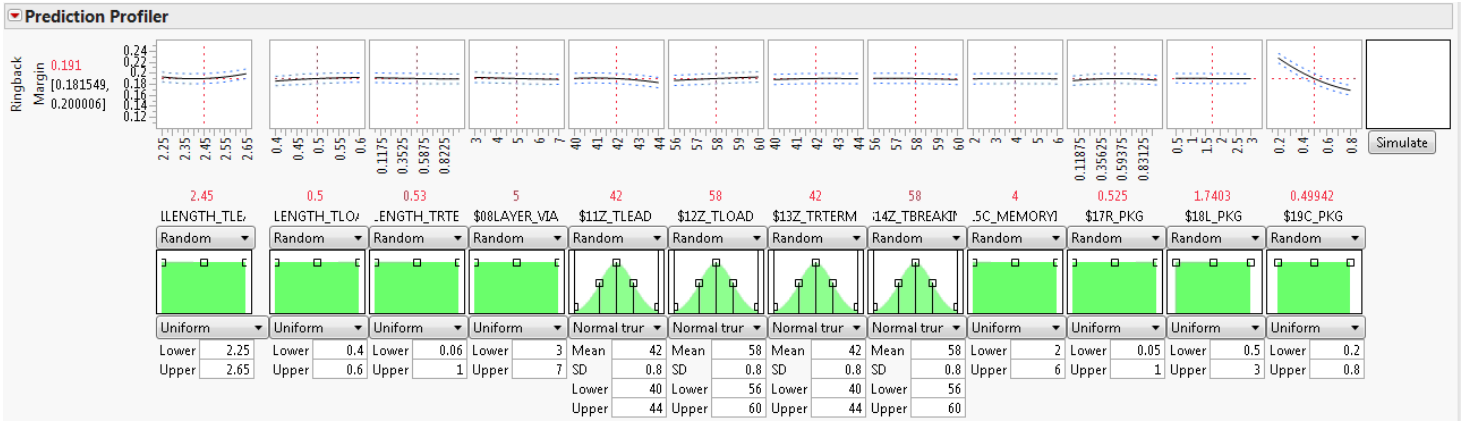




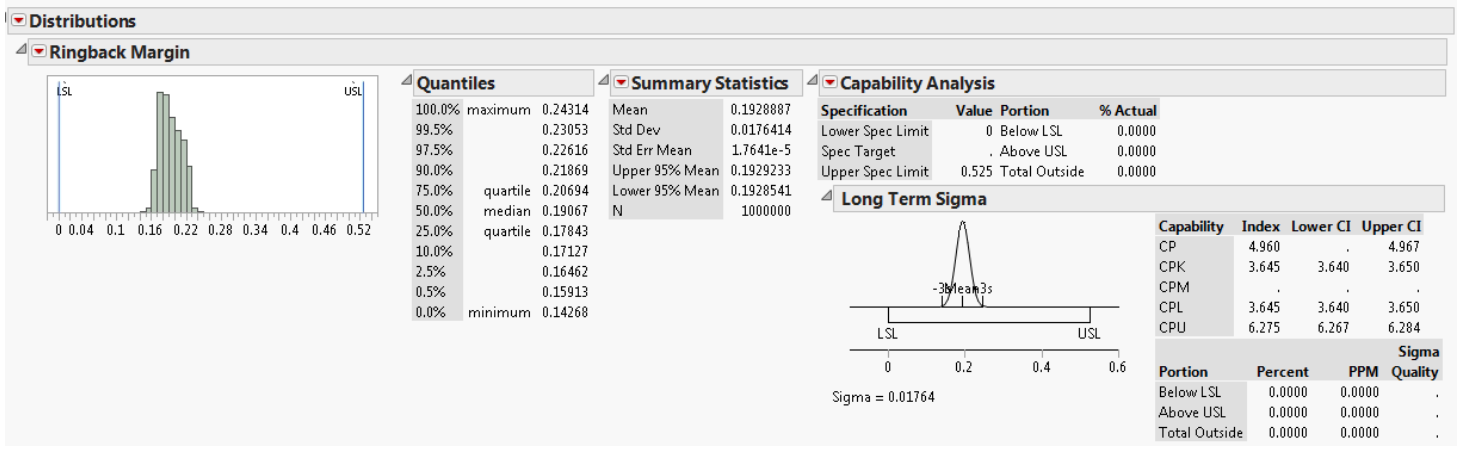


PRACTICAL DDR TOPOLOGY PROBLEM SOLVED BY DOE

- DPM (Defects per Million)
  - Equation Simulator to evaluate the response equation at millions of conditions.

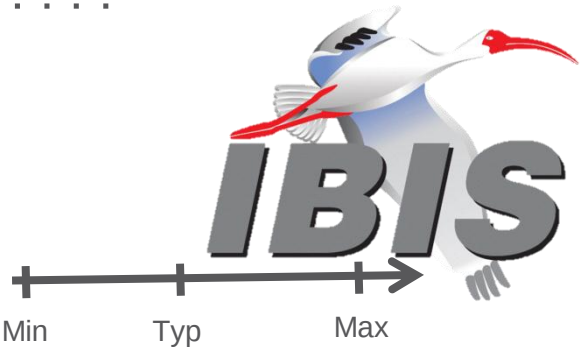


  - Realistic predicted yield plots obtained in seconds .



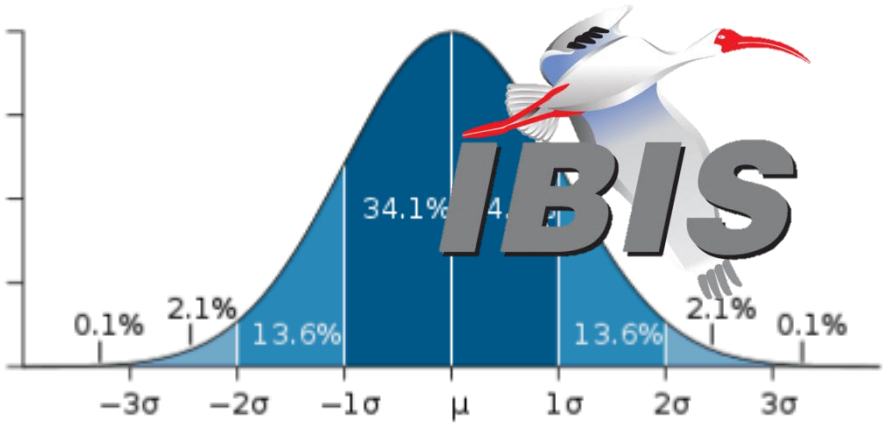
HOW CAN WE EXTEND IBIS TO SUPPORT CONFIDENCE INTERVAL ANALYSIS.

- IBIS currently and traditionally uses a typ, min, max parameter definition.
- This is based on a Best/Worst case scenario analysis. E.g. 100% confidence.
- Best/Worst case analysis has served us well during the years and still does in some cases, however more and more cases will not reach design closure using Best/Worst case analysis.
- When it does not reach design closure how will we know how many of our produced units will fail ????



ADD AN OPTION TO IBIS TYP, MIN, MAX CORNERS TO USE DISTRIBUTION DATA AS A PARAMETER DEFINITION.

- If we add an option to IBIS to support distribution data for parameters as an average/mean and a variation/sigma.
- If we feel we can not assume a standard distribution we could even add support for other distributions.
- These parameters could be used in DOE analysis scenarios and could help us predict confidence intervals for our products as well as DPM (Defect Per million) predictions.



CONCLUSIONS.

- Our design work is moving beyond Best case, Worst case analysis.
- We need to start working on an infrastructure both in modeling and tool support for statistical analysis.
- Many of us EE’s need to go back to our statistics books and review statistical analysis.
- We need to secure that we can get the correct information from IC and PCB vendors on parameter distributions.
- SI/PI statistical analysis is the next step to secure our product quality.

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