Enabling Full Power-aware Bus Simulation with Non-IBIS Device Model - A Kit using IBIS [External Model]

Skipper Liang
Cadence Design Systems
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Agenda

- Introduction
- Approach 1: Using IBIS [External Model]
- Approach 2: Using an IBIS model to drive the SPICE netlist
- Solution: A dummy IBIS model using [External Model] and additional circuit
- Summary

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Introduction

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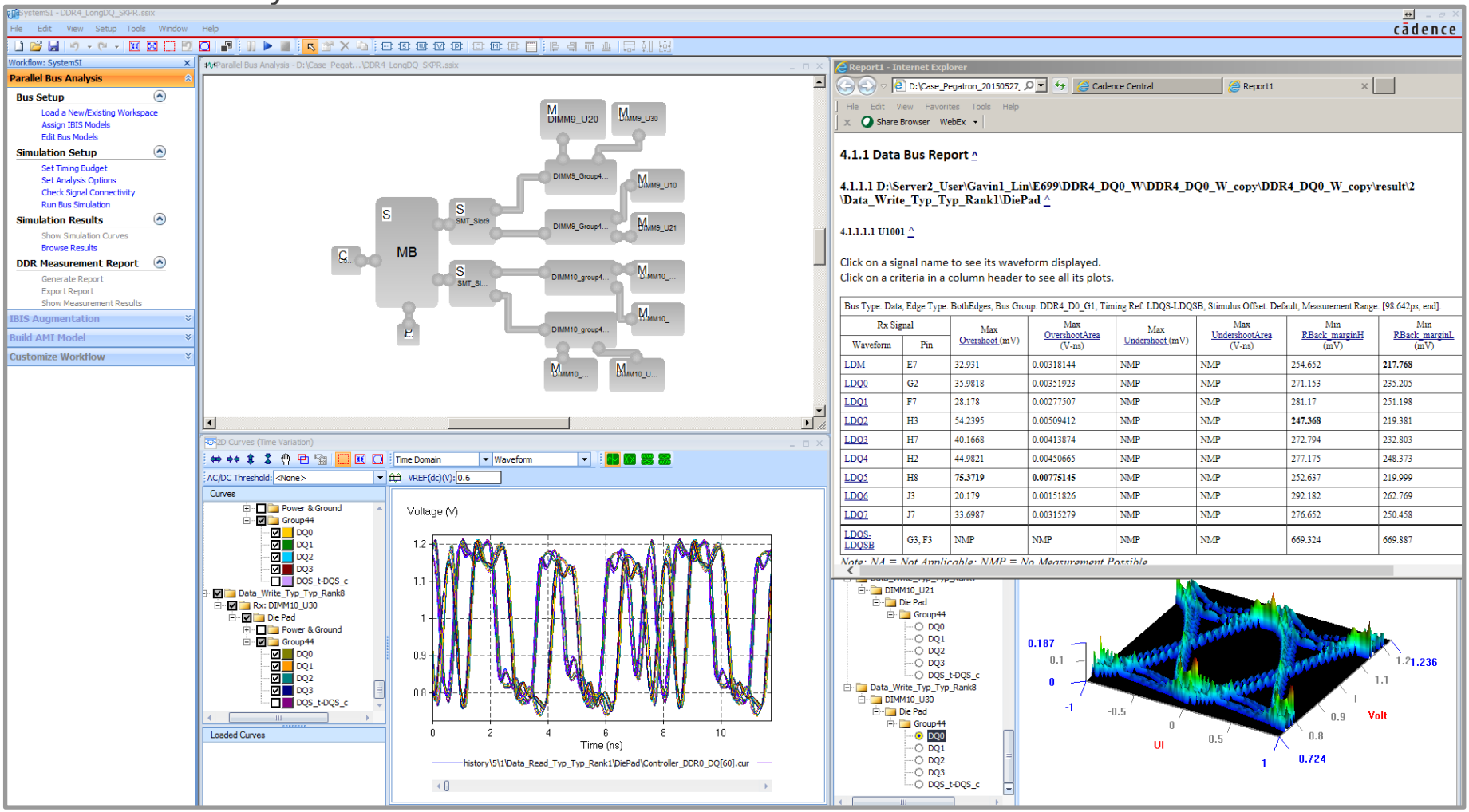
Bus simulation

- It refers to an automatic process
  - which includes simulation, measurement and report generation against a Bus, especially the memory interface in an EDA tool



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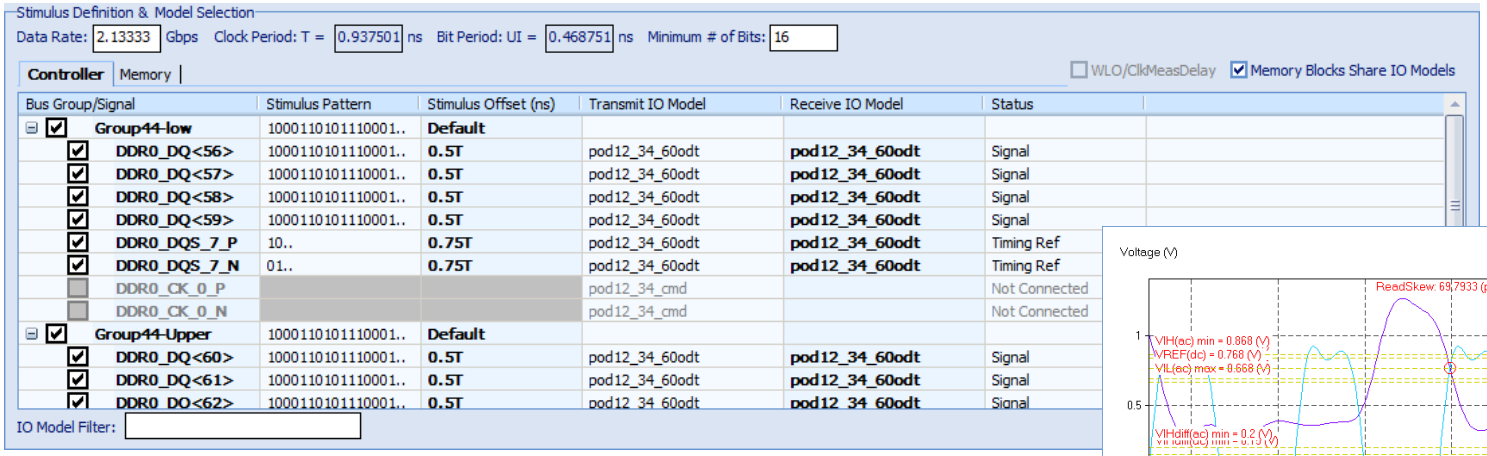
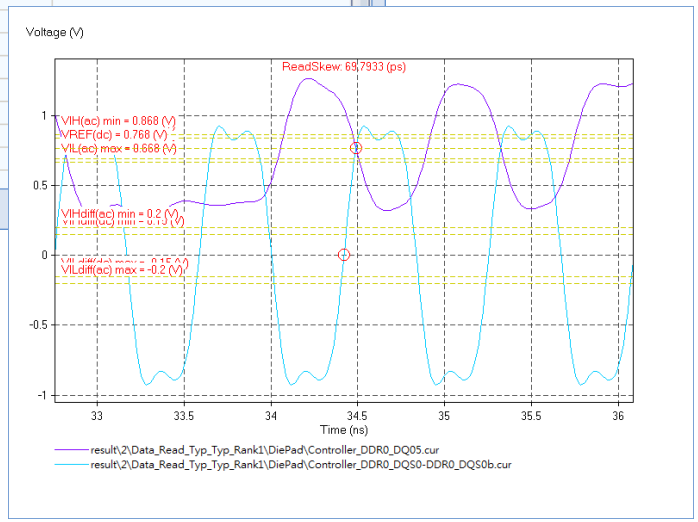
IBIS model

- Intrinsic format - the description of [Pin], [Diff Pin] and [Model Selector]
- IBIS makes Bus simulation possible in an EDA tool
  - easy to assign data groups with individual timing reference
  - Easy to change models and settings in batch mode





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SPICE netlist

- Maximum freedom in the circuit format but hard for Bus simulation to be implemented
- Has detailed characteristics of circuits which can't be fully described by IBIS model
  - Some IC designers prefer using SPICE netlist model than IBIS model

```
96  **********'termination load and voltage*********
97  'VRTT VTT GROUND '0.5'vdd15'
98  'R1 VTT PAD 25
99  'C1 PAD GROUND 4p
100 'C2 C GROUND 0.1p
101
102 **********'termination control ********
103
104 VODTEN ODTEN GROUND 0  'high-active for termination impedance control enable, or termination=none
105 VODT0 ODT0 GROUND vdd12      'ODT[2:0] termination impedance bits control, ex:3'b000=none (detail table as bellow)
106 VODT1 ODT1 GROUND 0
107 VODT2 ODT2 GROUND 0
108
109 ********'termination impedance table'****
110 'ODT2 ODT1 ODT0                ***
111
112 'mode=1'b0 (DDR2 mode)
113 '3'b000=none
114 '3'b001=150ohm
115 '3'b010=75ohm
116 '3'b011=50ohm
117
118 'mode=1'b1 (DDR3 mode)
119 '3'b000=none
120 '3'b001=120ohm
121 '3'b010=60ohm
122 '3'b011=40ohm
123 '3'b100=30ohm
124 '3'b101=20ohm
125
126 ****************************************
127
128
129 ***'unencrypted**********
130 '.inc
131
132 ***'e
133 .inc .
134
135
136
137 XDUT C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I MODE ODT0 ODT1 ODT2 ODTEN OE PAD PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
138
139 ***********************************************
140 * Parameter & Corner                  *
141 ***********************************************
142 '.TEMP 60
143 '.param fixed_cor_sw=1    vdd33='3.3'vratio' vdd15='1.5'vratio' vdd18='1.8'vratio' vdd12='1.2'vratio'
144 '.param vratio=1
145
```


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IBIS External Model

- Allow a spice netlist to be called by an IBIS model, which means:

- With IBIS format, easy for Bus-Sim to be implemented
- Include detailed characteristics of circuit

```
[External Model]
Language SPICE
|
| Corner corner_name  file name       circuit name (.subckt name)
Corner    Typ         buffer_typ.spi  buffer_io_typ
Corner    Min         buffer_min.spi  buffer_io_min
Corner    Max         buffer_max.spi  buffer_io_max
|
| Parameters - Not supported in SPICE
|
| Ports List of port names (in same order as in SPICE)
Ports A_signal my_drive my_enable my_receive my_ref
Ports A_puref A_pdref A_pcref A_gcref A_extref
|
| D_to_A d_port   port1     port2    vlow vhigh trise tfall corner_name
D_to_A   D_drive  my_drive   my_ref   0.0  3.3  0.5n  0.3n   Typ
D_to_A   D_enable my_enable  A_gcref  0.0  3.3  0.5n  0.3n   Typ
|
| A_to_D d_port    port1       port2       vlow  vhigh  corner_name
A_to_D   D_receive  my_receive  my_ref  0.8   2.0    Typ
|
| Note: A_signal might also be used instead of a user-defined interface port
| for measurements taken at the die pads
|
[End External Model]
```


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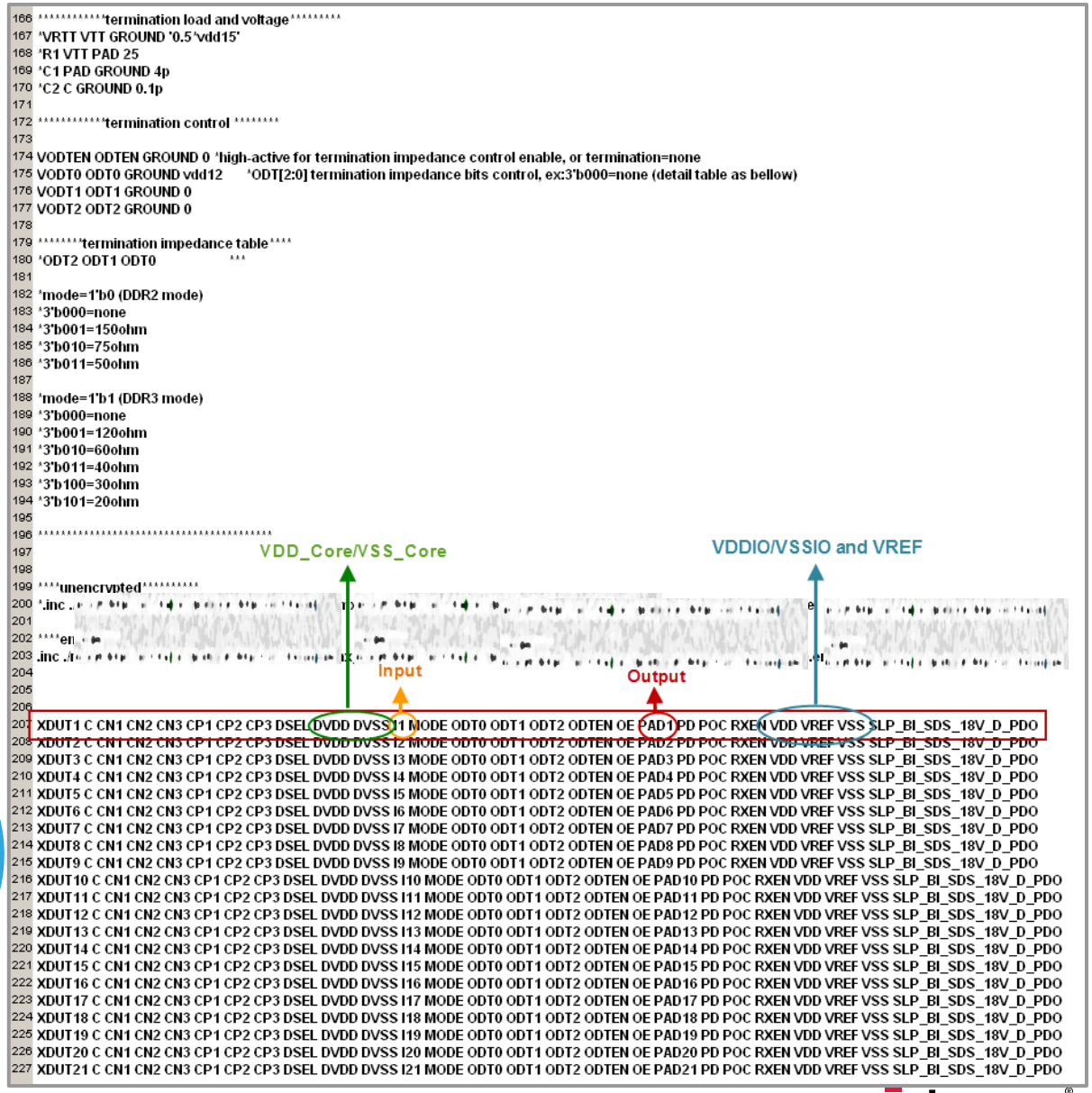
SPICE netlist of transistor based device model

- An example of SPICE netlist for a transistor based device model
- For power supply, there are:
  - VDD_Core/Vss_Core
  - VDDIO/VSSIO
  - VREF

Question: if we can use IBIS [External Model] to call this netlist to execute a fully power-aware Bus-Simulation?




```
**********termination load and voltage*********
'VRTT VTT GROUND '0.5*vdd15'
'R1 VTT PAD 25
'C1 PAD GROUND 4p
'C2 C GROUND 0.1p

**********termination control ********

VODTEN ODTEN GROUND 0  'high-active for termination impedance control enable, or termination=none
VODT0 ODT0 GROUND vdd12      'ODT[2:0] termination impedance bits control, ex:3'b000=none (detail table as bellow)
VODT1 ODT1 GROUND 0
VODT2 ODT2 GROUND 0

********termination impedance table****
'ODT2 ODT1 ODT0                ***

'mode=1'b0 (DDR2 mode)
'3'b000=none
'3'b001=150ohm
'3'b010=75ohm
'3'b011=50ohm

'mode=1'b1 (DDR3 mode)
'3'b000=none
'3'b001=120ohm
'3'b010=60ohm
'3'b011=40ohm
'3'b100=30ohm
'3'b101=20ohm

****************************************

****unencrypted**********
.inc ./
****en
.inc ./

XDUT1 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I1 MODE ODT0 ODT1 ODT2 ODTEN OE PAD1 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT2 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I2 MODE ODT0 ODT1 ODT2 ODTEN OE PAD2 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT3 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I3 MODE ODT0 ODT1 ODT2 ODTEN OE PAD3 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT4 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I4 MODE ODT0 ODT1 ODT2 ODTEN OE PAD4 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT5 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I5 MODE ODT0 ODT1 ODT2 ODTEN OE PAD5 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT6 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I6 MODE ODT0 ODT1 ODT2 ODTEN OE PAD6 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT7 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I7 MODE ODT0 ODT1 ODT2 ODTEN OE PAD7 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT8 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I8 MODE ODT0 ODT1 ODT2 ODTEN OE PAD8 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT9 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I9 MODE ODT0 ODT1 ODT2 ODTEN OE PAD9 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT10 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I10 MODE ODT0 ODT1 ODT2 ODTEN OE PAD10 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT11 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I11 MODE ODT0 ODT1 ODT2 ODTEN OE PAD11 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT12 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I12 MODE ODT0 ODT1 ODT2 ODTEN OE PAD12 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT13 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I13 MODE ODT0 ODT1 ODT2 ODTEN OE PAD13 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT14 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I14 MODE ODT0 ODT1 ODT2 ODTEN OE PAD14 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT15 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I15 MODE ODT0 ODT1 ODT2 ODTEN OE PAD15 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT16 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I16 MODE ODT0 ODT1 ODT2 ODTEN OE PAD16 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT17 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I17 MODE ODT0 ODT1 ODT2 ODTEN OE PAD17 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT18 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I18 MODE ODT0 ODT1 ODT2 ODTEN OE PAD18 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT19 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I19 MODE ODT0 ODT1 ODT2 ODTEN OE PAD19 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT20 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I20 MODE ODT0 ODT1 ODT2 ODTEN OE PAD20 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
XDUT21 C CN1 CN2 CN3 CP1 CP2 CP3 DSEL DVDD DVSS I21 MODE ODT0 ODT1 ODT2 ODTEN OE PAD21 PD POC RXEN VDD VREF VSS SLP_BI_SDS_18V_D_PDO
```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Approach 1: using IBIS [External Model]

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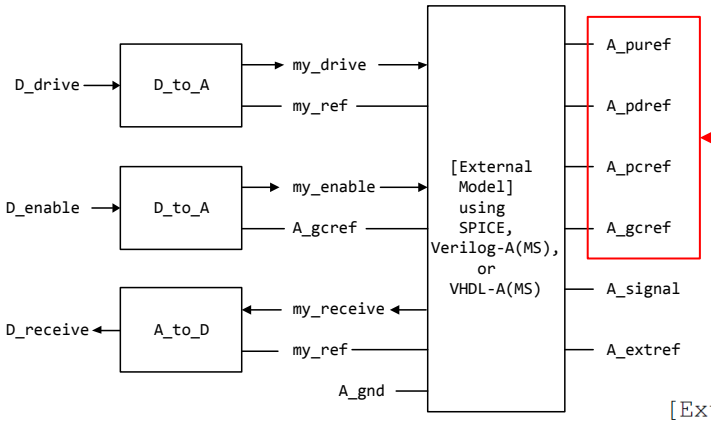
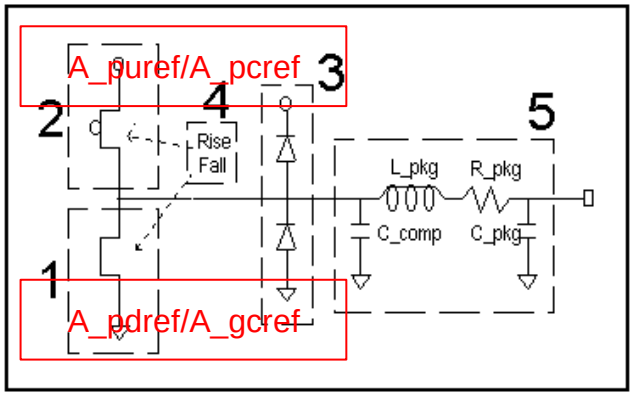
Multi-power nets in [External Model] Section?





- Same as a normal IBIS model, an IBIS model with [External Model] can connect to only one PWR / GND pair, usually the VDDIO and VSSIO.
- What will we do for the following:
  1. VDD_Core/Vss_Core
     - **A_puref, A_pdref, A_pcref, A_gcref**
  2. VDDIO/VSSIO
  3. VREF

```
[External Model]
Language SPICE
|
| Corner corner_name   file_name        circuit_name (.subckt name)
Corner    Typ           buffer_typ.spi   buffer_io_typ
Corner    Min           buffer_min.spi   buffer_io_min
Corner    Max           buffer_max.spi   buffer_io_max
|
| Parameters - Not supported in SPICE
|
| Ports List of port names (in same order as in SPICE)
Ports A_signal my_drive my_enable my_receive my_ref
Ports A_puref A_pdref A_pcref A_gcref A_extref
|
| D_to_A d_port    port1      port2     vlow vhigh trise tfall corner_name
D_to_A   D_drive   my_drive    my_ref    0.0  3.3   0.5n  0.3n   Typ
D_to_A   D_enable  my_enable   A_gcref   0.0  3.3   0.5n  0.3n   Typ
|
| A_to_D d_port     port1        port2        vlow  vhigh  corner_name
A_to_D   D_receive  my_receive   my_ref   0.8   2.0    Typ
|
| Note: A_signal might also be used instead of a user-defined interface port
| for measurements taken at the die pads
|
[End External Model]
```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Multi-power nets in [External Model] Section? (Cont')

(spice_io.ckt)

```
.subckt se_drv15_odtoff DVDD DVSS PAD I OE nd_out_of_in

.param vdd15='1.5'
.param vdd12='1.2'
VREF VREF GROUND '0.5*vdd15'  'reference voltage for the SSTL receiver @padring

.protect
.inc ./lib/design_io_pad.inc
.unprotect

*VDVDD DVDD GROUND vdd15       'power supply voltage
*VDVSS DVSS GROUND 0
VDDA12 VDD GROUND vdd12      'core power supply voltage
VSSA12 VSS GROUND 0

VMODE MODE GROUND vdd12       'mode select signal
            *1'b0 selects DDR2 mode
            *1'b1 selects DDR3 mode
VPOC POC GROUND 0     'power on control @padring

.connect OE RXEN


VPD PD GROUND vdd12      'active-high for receiver power down signal

VDSEL DSEL GROUND vdd12      'DDR2 drive slect signal
            *1'b0 60% drive (clasel)
            *1'b1 full drive (classII)

**********termination control ********

VODTEN ODTEN GROUND 0 'high-active for termination impedance control enable, or termination=none
VODT0 ODT0 GROUND vdd12      'ODT[2:0] termination impedance bits control, ex:3'b000=none (detail table as bellow)
VODT1 ODT1 GROUND 0
VODT2 ODT2 GROUND 0
```

```
|*****************************************************************
|                                        Model se_drv15_odtoff
|*****************************************************************
|
[Model] se_drv15_odtoff
Model_type I/O
Polarity       Non-Inverting
Enable         Active-High
[Voltage Range]        1.500V            1.425V              1.575V
[Ramp]
| variable       typ                 min                 max
dV/dt_r 0.720/0.006n        0.720/0.006n        0.720/0.006n
dV/dt_f 0.720/0.006n        0.720/0.006n        0.720/0.006n
R_load = 50.000
|
[External Model]
Language SPICE
|
| Corner  corner_name  file_name  circuit_name (.subckt name)
Corner    Typ          spice_io.ckt           se_drv15_odtoff
Corner    Min          spice_io_min.ckt          se_drv15_odtoff_min
Corner    Max          spice_io_max.ckt          se_drv15_odtoff_max
|
| Ports List of port names (in same order as in SPICE)
Ports A_puref A_pdref A_signal my_drive my_enable my_receive
|
| D_to_A d_port port1 port2 vlow vhigh trise tfall corner_name
D_to_A D_drive my_drive A_pdref 0.0 1.2 10p 10p Typ
D_to_A D_drive my_drive A_pdref 0.0 1.2 10p 10p Min
D_to_A D_drive my_drive A_pdref 0.0 1.2 10p 10p Max
D_to_A D_enable my_enable A_pdref 0.0 1.2 10p 10p Typ
D_to_A D_enable my_enable A_pdref 0.0 1.2 10p 10p Min
D_to_A D_enable my_enable A_pdref 0.0 1.2 10p 10p Max
| A_to_D d_port port1 port2 vlow vhigh corner_name
A_to_D D_receive my_receive A_pdref 0.0 1.0 Typ
A_to_D D_receive my_receive A_pdref 0.0 1.0 Min
A_to_D D_receive my_receive A_pdref 0.0 1.0 Max
|
[End External Model]
```

- Except the VDDIO and VSSIO, which will be connected to real power delivery network routing, the other PWR and GND will be connected to a "**IDEAL**" voltage source.

➡ **Not Fully Power-Aware**

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Approach 2: Using an IBIS model to drive the SPICE netlist

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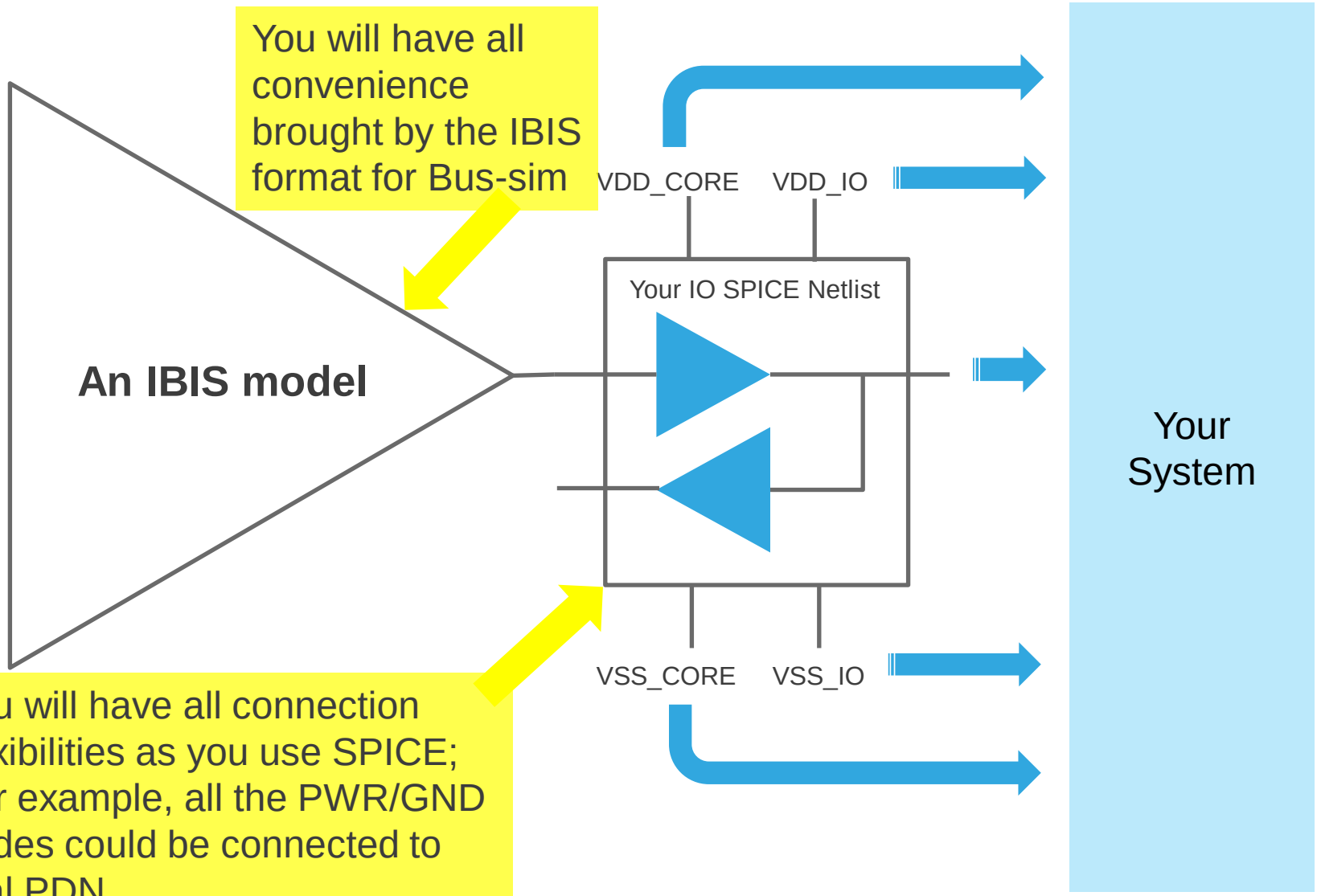
IBIS-drive SPICE netlist



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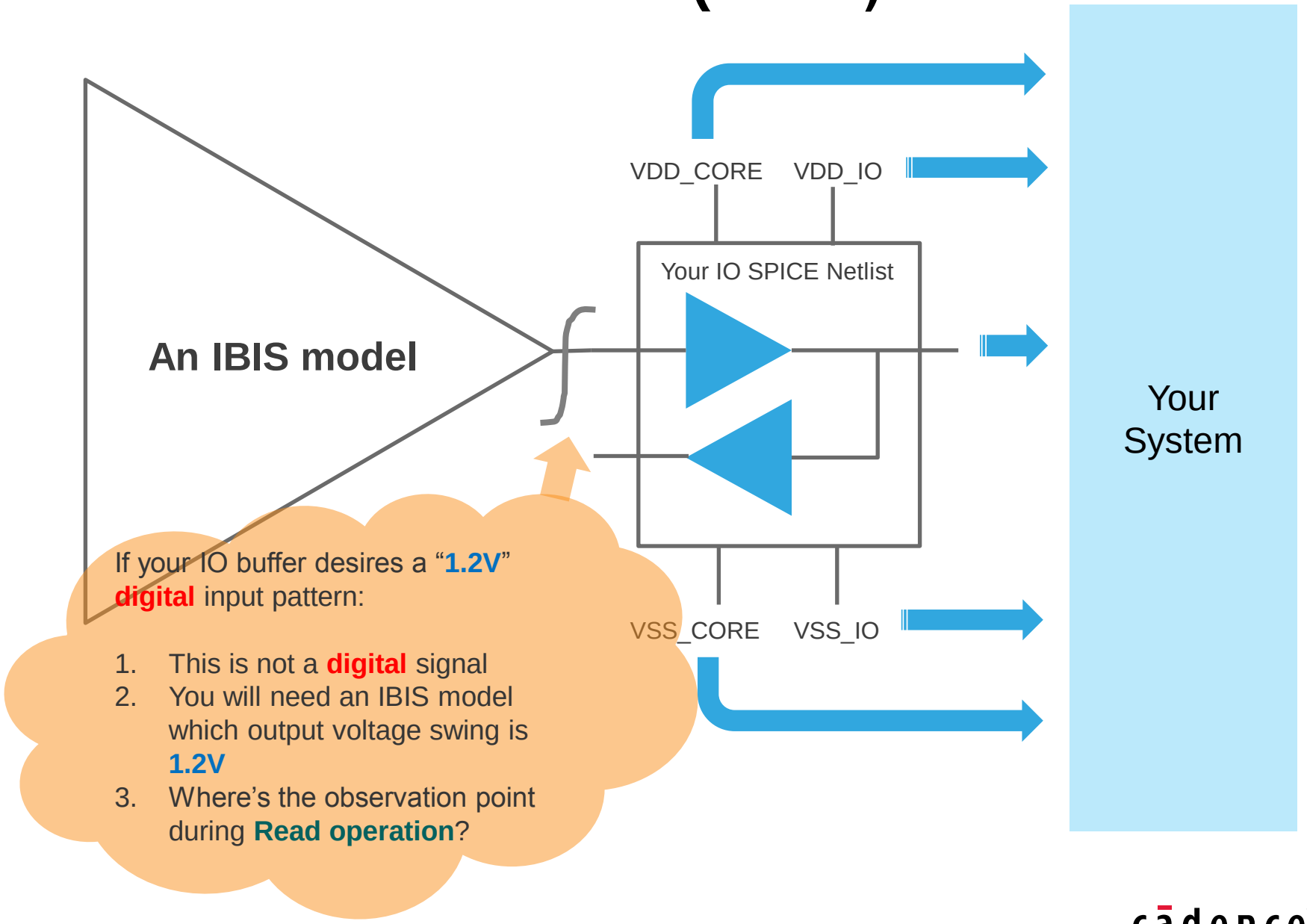
IBIS-drive SPICE netlist (Cont')



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Solution: A dummy IBIS model using [External Model] and additional circuits

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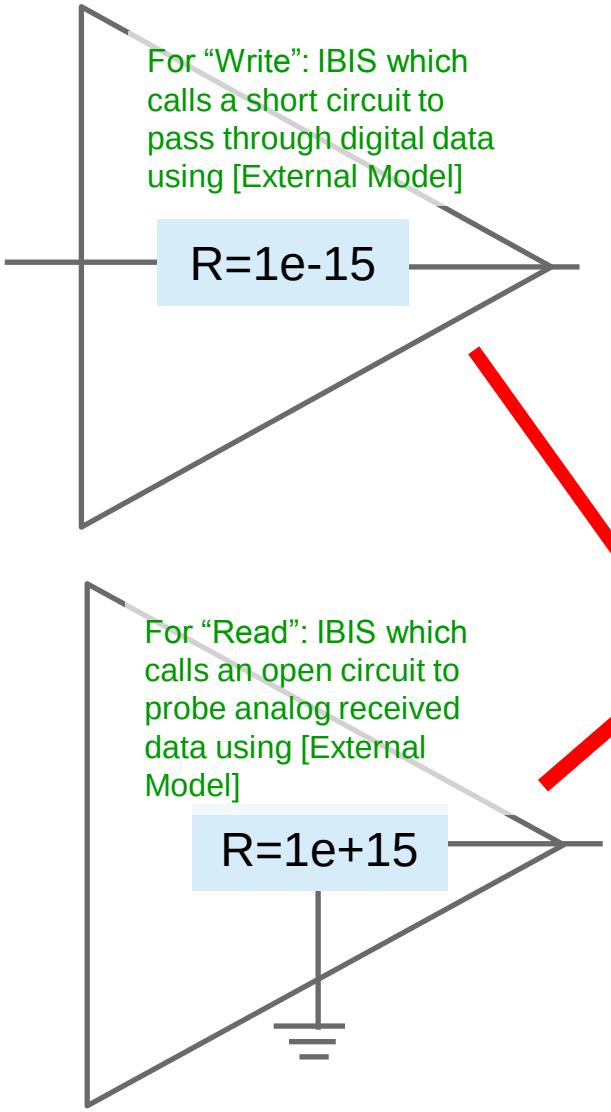
A simple kit




```
1       dq0                                     Dummy_IO
2       dq1                                     Dummy_IO
3       dq2                                     Dummy_IO
4       dq3                                     Dummy_IO
5       dq4                                     Dummy_IO
6       dq5                                     Dummy_IO
7       dq6                                     Dummy_IO
8       dq7                                     Dummy_IO
9       dq8                                     Dummy_IO
10      dq9                                     Dummy_IO
11      dq10                                    Dummy_IO
12      dq11                                    Dummy_IO
13      dq12                                    Dummy_IO
14      dq13                                    Dummy_IO
15      dq14                                    Dummy_IO
16      dq15                                    Dummy_IO
17      dm0                                     Dummy_IO
18      dm1                                     Dummy_IO
19      dqs0p                                   Dummy_IO
20      dqs0n                                   Dummy_IO
21      dqs1p                                   Dummy_IO
22      dqs1n                                   Dummy_IO
23      VSS0                                    GND
24      VDDQ0                                   POWER
|
[Diff pin]  inv_pin  vdiff   tdelay_typ   tdelay_min   tdelay_max
|
19        20      100.000mV  0.0s
21        22      100.000mV  0.0s
|*********************Component Bus Definitions ************************
|
[Model Selector] Dummy_IO
Write  single end driver
Read  single end Receiver
|
|*****************************************************************
|                                          Model Write
|*****************************************************************
|                                                              I
[Model] Write
Model_type I/O
Polarity       Non-Inverting
Enable        Active-High
[Voltage Range]        1.500V           1.425V             1.575V
[Ramp]
| variable       typ                 min                 max
dV/dt_r 0.120/0.001n        0.120/0.001n        0.120/0.001n
dV/dt_f 0.120/0.001n        0.120/0.001n        0.120/0.001n
R_load = 50.000
```

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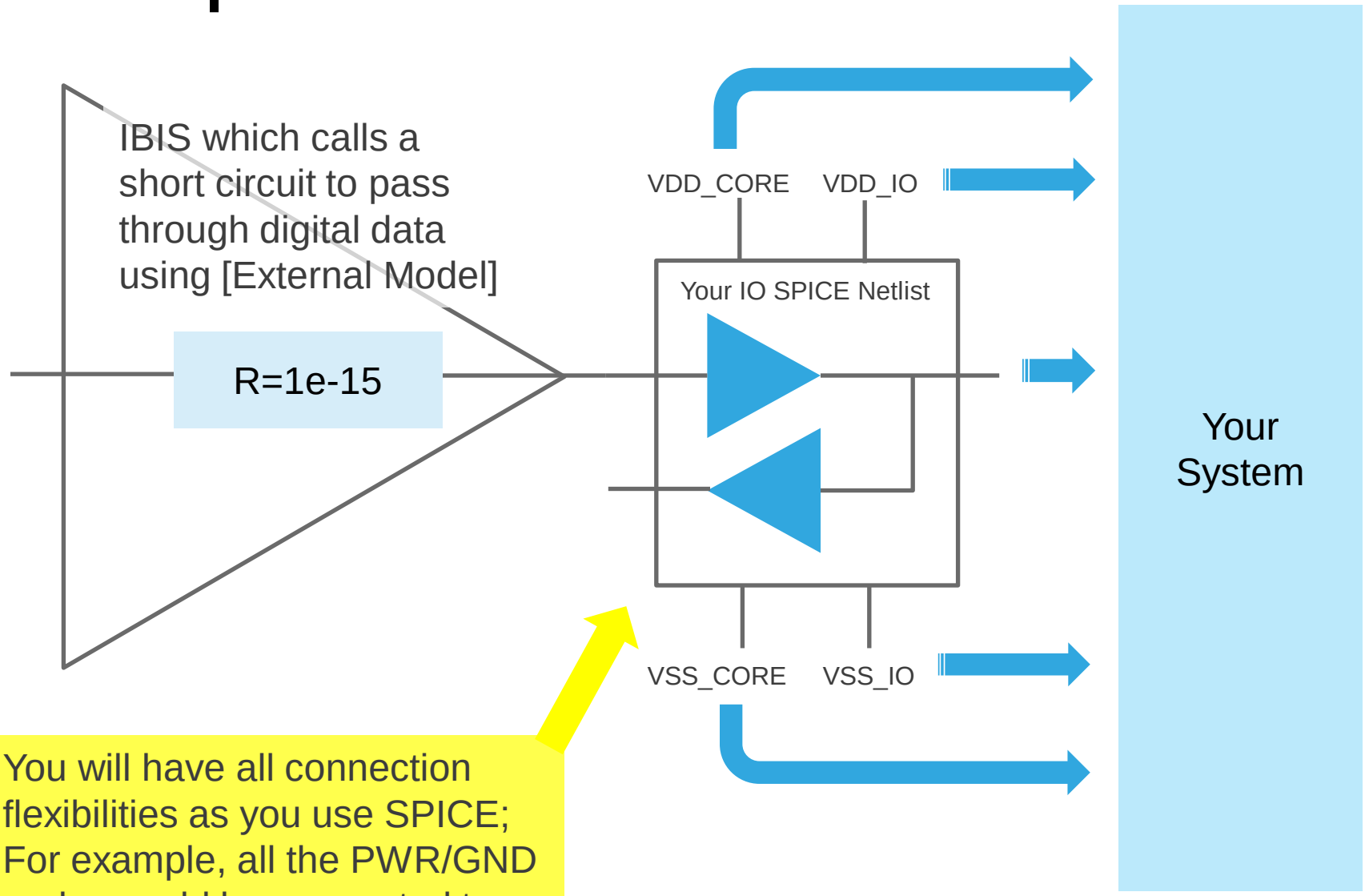
Write Operation



You will have all connection flexibilities as you use SPICE; For example, all the PWR/GND nodes could be connected to real PDN.

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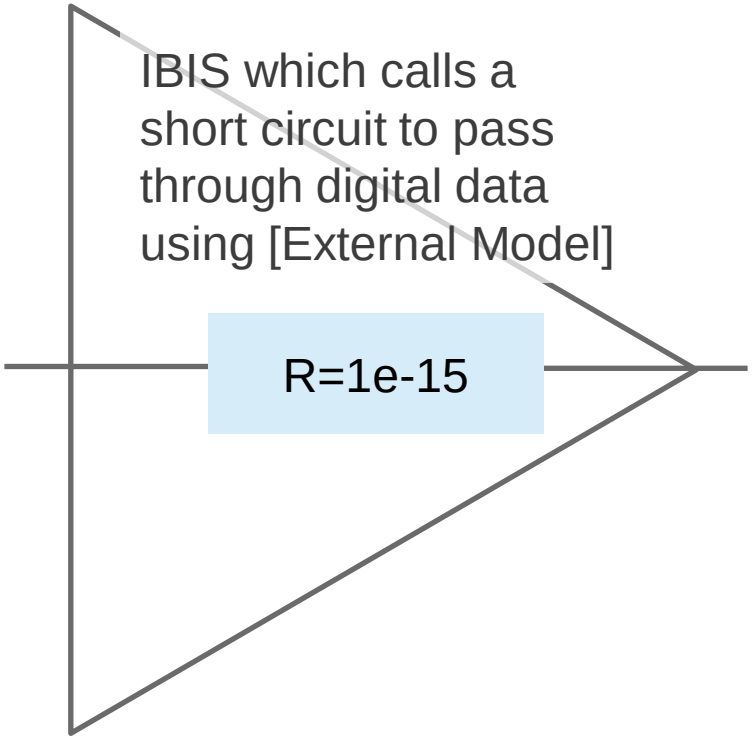
Write Operation (cont')




```
19        20      100.000mV  0.0s
21        22      100.000mV  0.0s
|********************Component Bus Definitions ***************************
|
[Model Selector] Dummy_IO
Write  single end driver
Read  single end Receiver
|
|*************************************************************************
|                                          Model Write
|*************************************************************************
|
[Model] Write
Model_type I/O
Polarity       Non-Inverting
Enable        Active-High
[Voltage Range]        1.500V            1.425V              1.575V
[Ramp]
| variable       typ                 min                 max
dV/dt_r 0.120/0.001n        0.120/0.001n        0.120/0.001n
dV/dt_f 0.120/0.001n        0.120/0.001n        0.120/0.001n
R_load = 50.000
|
[External Model]
Language SPICE
|
| Corner  corner_name  file_name  circuit_name (.subckt name)
Corner    Typ          write.ckt   write
Corner    Min          write.ckt   write
Corner    Max          write.ckt   write
|
| Ports List of port names (in same order as in SP   E)
Ports A_puref A_pdref A_signal my_drive my_enable my_receive
|
| D_to_A d_port port1
D_to_A D_drive my_driv
D_to_A D_drive my_driv
D_to_A D_drive my_driv
D_to_A D_enable my_ena
D_to_A D_enable my_ena
D_to_A D_enable my_ena
| A_to_D d_port port1 port2 vlow vhigh corner_name
A_to_D D_receive my_receive A_pdref 0.0
A_to_D D_receive my_receive A_pdref 0.0 1.0 Min
A_to_D D_receive my_receive A_pdref 0.0 1.0 Max
|
[End External Model]
|*************************************************************************
|                                          Model Read
```

```
.subckt write DVDD DVSS PAD I OE nd_out_of_in

R I PAD 1e-15

.ends
```

write.ckt

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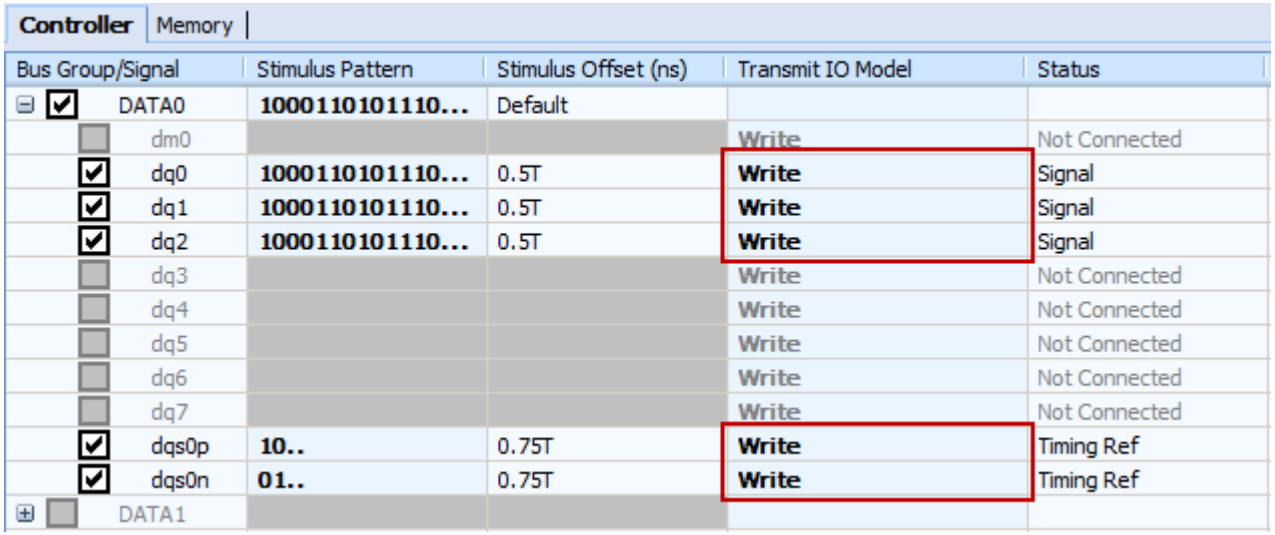
Write Operation (cont')

- In a bus simulation, user can easily switch the model of the Controller's buffer to "Write"



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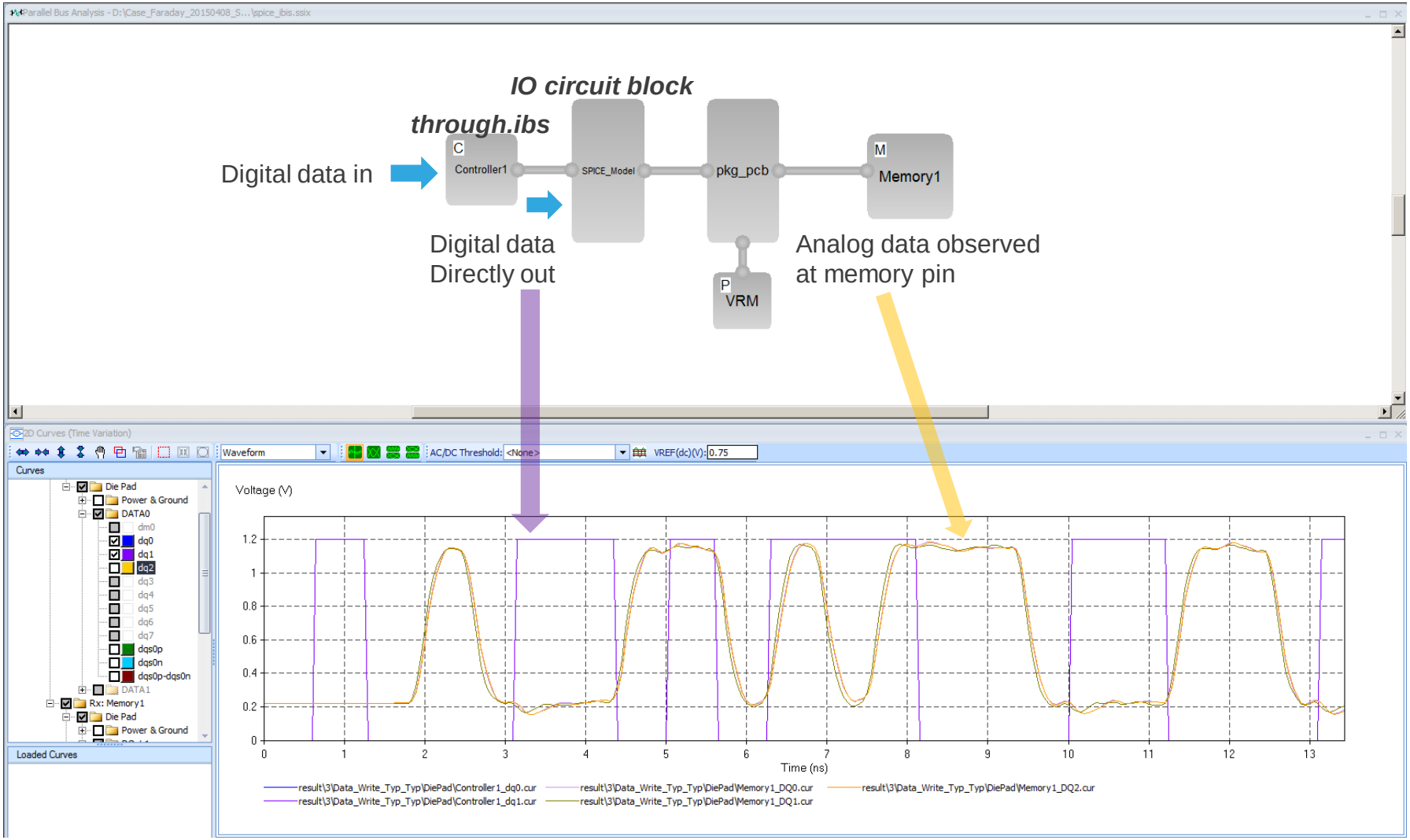
Write Operation (cont')



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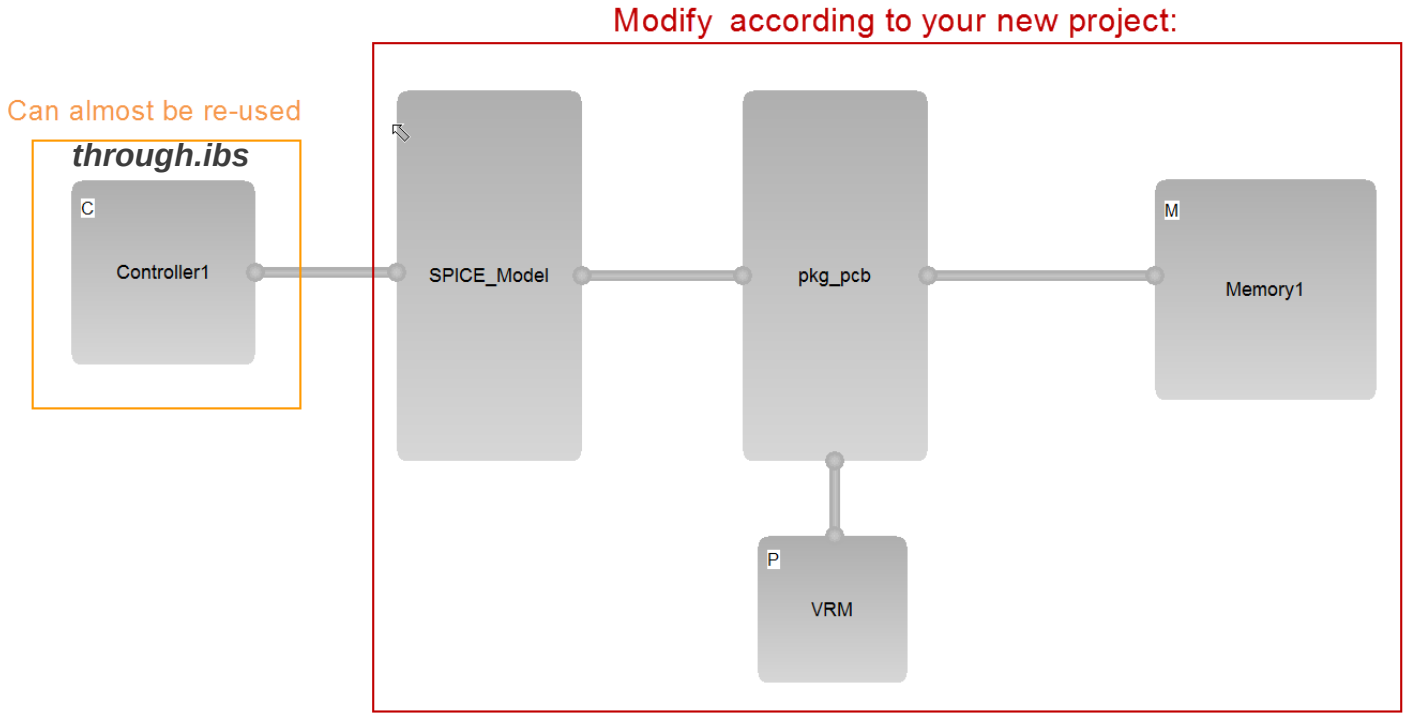
Write Operation (cont')

For a new project, the kit is re-usable with little modification



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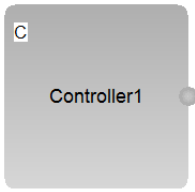
Write Operation (cont')

For a new project, the kit is re-usable with little modification

Can almost be re-used

through.ibs




```
21        22      100.000mV  0.0s
|**********************Component Bus Definitions ***************************
|
[Model Selector] Dummy_IO
Write  single end driver
Read  single end Receiver
|
|*****************************************************************************
|                                          Model Write
|*****************************************************************************
|
[Model] Write
Model_type I/O
Polarity       Non-Inverting
Enable         Active-High
[Voltage Range]         1.500V            1.425V             1.575V
[Ramp]
| variable       typ                 min                 max
dV/dt_r 0.120/0.001n        0.120/0.001n        0.120/0.001n
dV/dt_f 0.120/0.001n        0.120/0.001n        0.120/0.001n
R_load = 50.000
|
[External Model]
Language SPICE
|
| Corner  corner_name  file_name  circuit_name (.subckt name)
Corner    Typ          write.ckt   write
Corner    Min          write.ckt   write
Corner    Max          write.ckt   write
|
| Ports List of port names (in same order as in SPICE)
Ports A_puref A_pdref A_signal my_drive my_enable my_receive
|
| D_to_A d_port port1 port2 vlow vhigh trise tfall corner_name
D_to_A D_drive my_drive A_pdref 0.0 1.2 10p 10p Typ
D_to_A D_drive my_drive A_pdref 0.0 1.2 10p 10p Min
D_to_A D_drive my_drive A_pdref 0.0 1.2 10p 10p Max
D_to_A D_enable my_enable A_pdref 0.0 1.2 10p 10p Typ
D_to_A D_enable my_enable A_pdref 0.0 1.2 10p 10p Min
D_to_A D_enable my_enable A_pdref 0.0 1.2 10p 10p Max
| A_to_D d_port port1 port2 vlow vhigh corner_name
A_to_D D_receive my_receive A_pdref 0.0 1.0 Typ
A_to_D D_receive my_receive A_pdref 0.0 1.0 Min
A_to_D D_receive my_receive A_pdref 0.0 1.0 Max
|
[End External Model]
|*****************************************************************************
|                                          Model Read
|*****************************************************************************
```

Modify to the correct voltage level of your IO's Input node

Modify to the correct voltage level of your IO's Enable node

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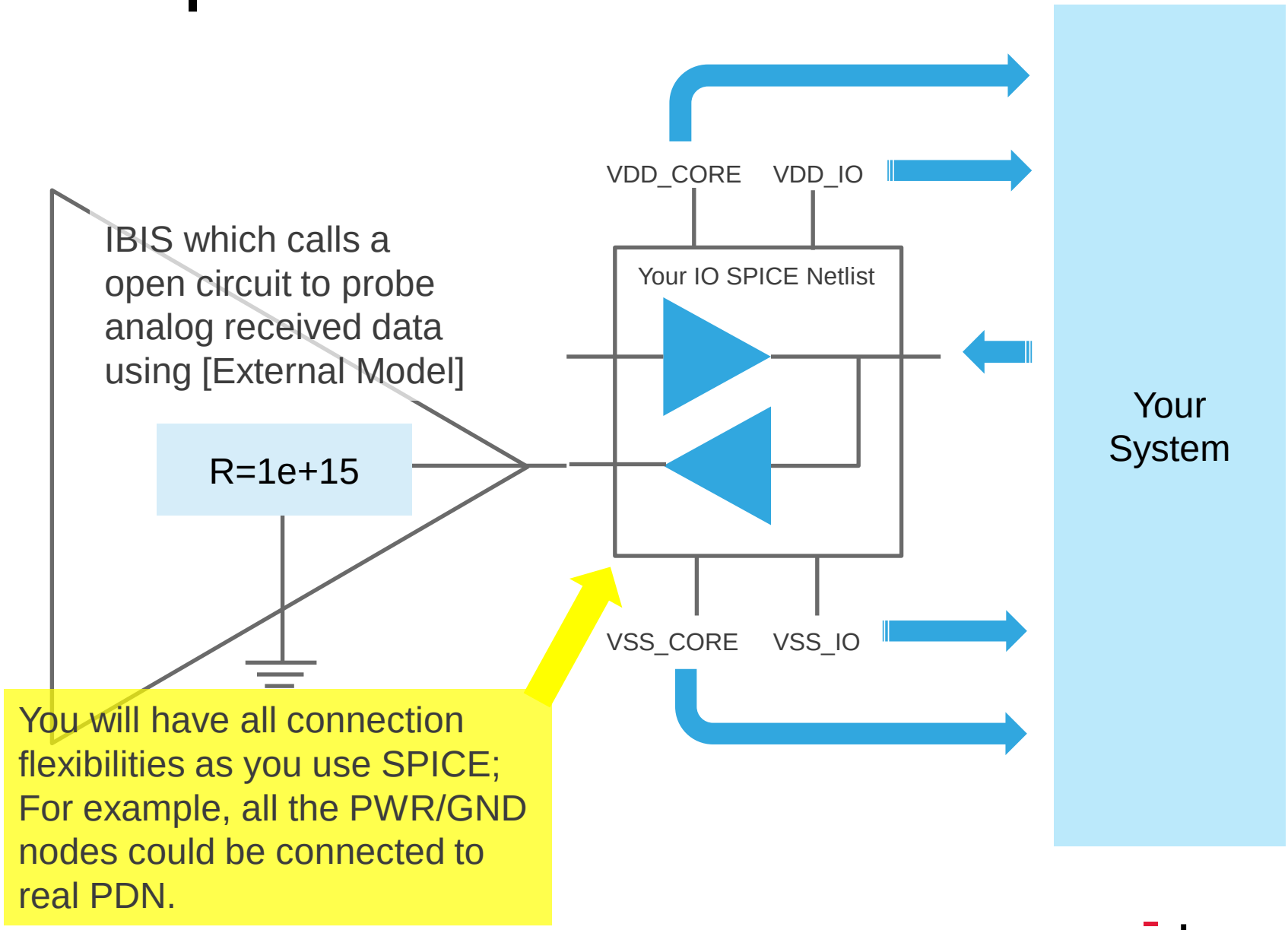
Read Operation



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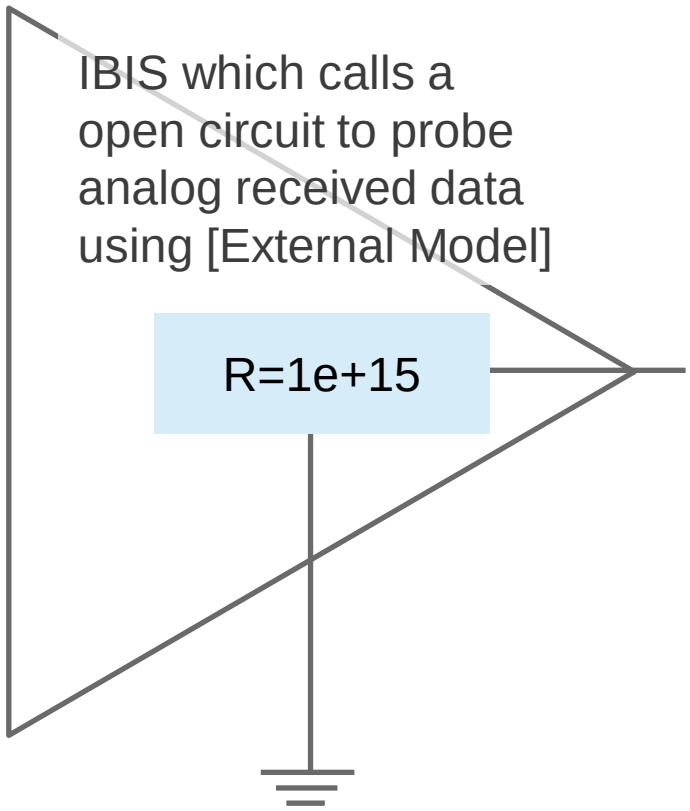
Read Operation (cont')




```
A_to_D D_receive my_receive A_pdref 0.0 1.0 Typ
A_to_D D_receive my_receive A_pdref 0.0 1.0 Min
A_to_D D_receive my_receive A_pdref 0.0 1.0 Max
|
[End External Model]
|*****************************************************************
|                                        Model Read
|*****************************************************************
|
[Model] Read
Model_type I/O
Polarity       Non-Inverting
Enable         Active-High
[Voltage Range]        1.500V            1.425V              1.575V
[Ramp]
| variable       typ                 min                 max
dV/dt_r 0.120/0.001n        0.120/0.001n        0.120/0.001n
dV/dt_f 0.120/0.001n        0.120/0.001n        0.120/0.001n
R_load = 50.000
|
[External Model]
Language SPICE
|
| Corner  corner_name  file_name  circuit_name (.subckt name)
Corner    Typ          read.ckt   read
Corner    Min          read.ckt   read
Corner    Max          read.ckt   read
|
| Ports List of port names (in same order as
Ports A_puref A_pdref A_signal my_drive my_enable
|
| D_to_A d_port port1 port2 vlow vhigh trise tfall
D_to_A D_drive my_driv
D_to_A D_drive my_driv
D_to_A D_drive my_driv
D_to_A D_enable my_ena
D_to_A D_enable my_ena
D_to_A D_enable my_ena
| A_to_D d_port port1
A_to_D D_receive my_re
A_to_D D_receive my_receive A_pdref 0.0 1.0 Min
A_to_D D_receive my_receive A_pdref 0.0
|
[End External Model]
|
[End]

|******Modified by Cadence Design Systems*****
|[ibischk5  V5.0.3]
```

```
.subckt read DVDD DVSS PAD I OE nd_out_of_in

R PAD DVSS 1e+15

.ends
```

read.ckt

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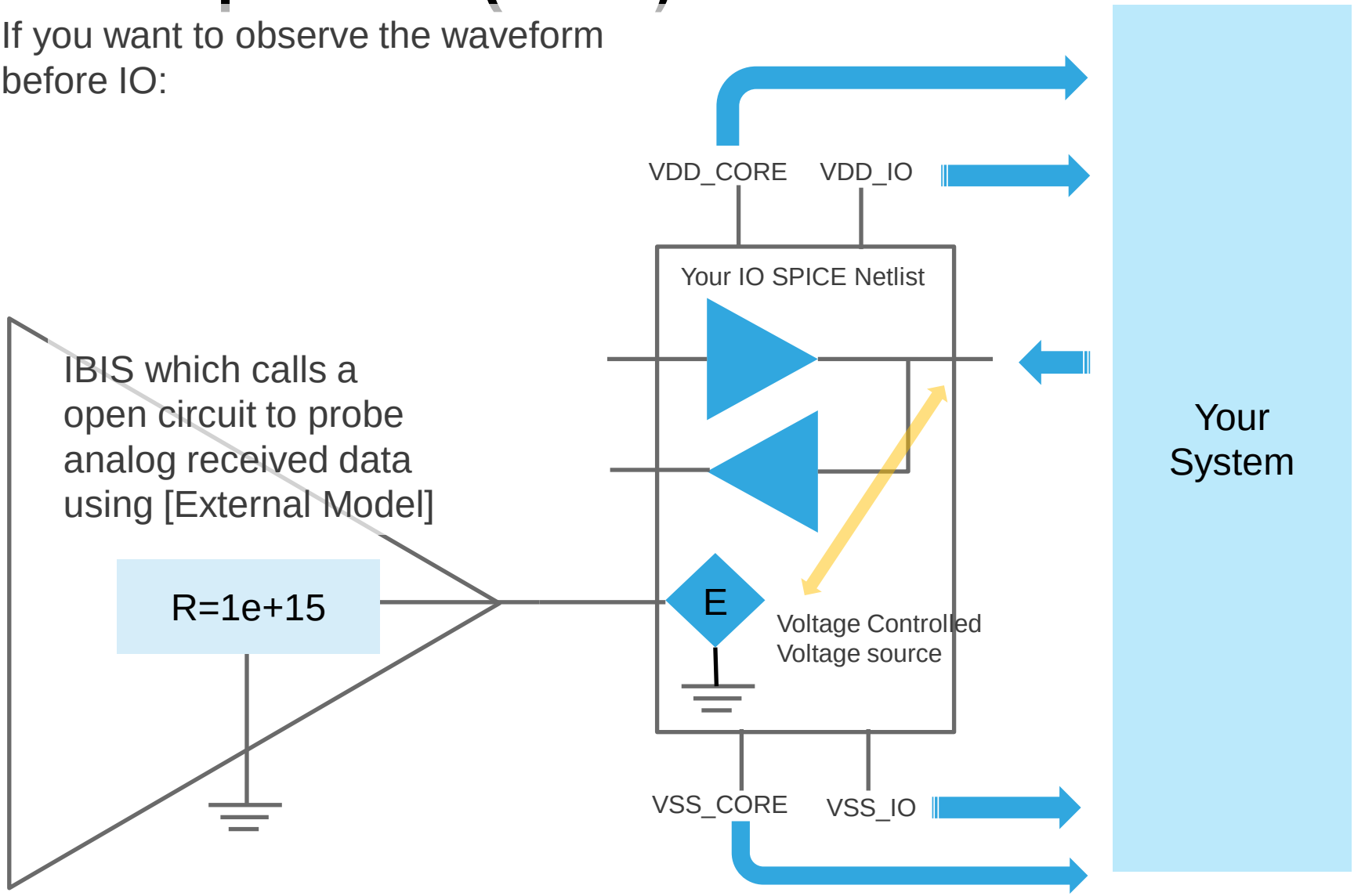
Read Operation (cont')

If you want to observe the waveform before IO:



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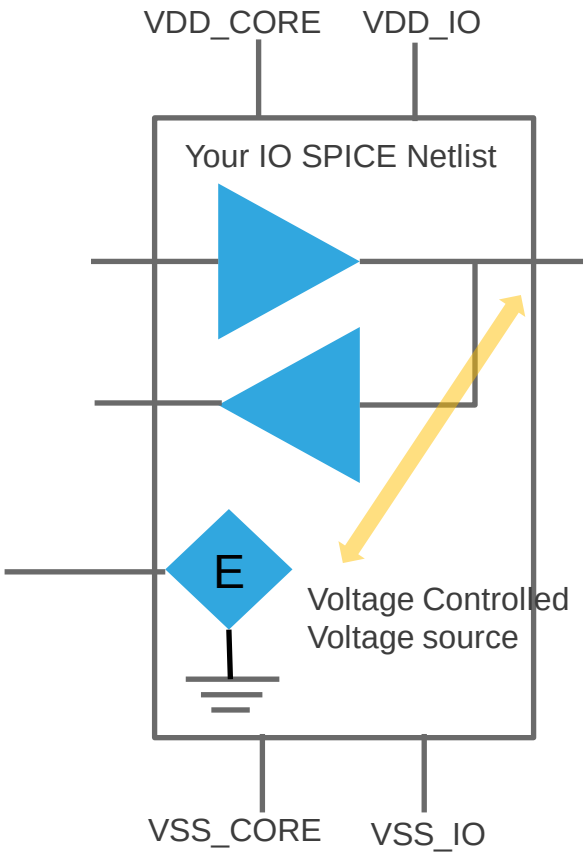
Read Operation (cont')

- You will need to modify the netlist of the IO circuit block by adding some "Voltage Controlled Voltage sources" which is controlled by the voltage on IO circuit block's PAD.
- Connect the dummy controller's output pad to these "Voltage Controlled Voltage sources"

```
*VCCT2B DVDD dum17854 DC 0.000000
*VVCCT2B dum17854 0 DC 1.500000
*VGNDT2B DVSS 0 DC 0.000000


*VENAT2B OE 0 DC 1.200000
*VINT2B I 0 PWL 0.0 0.000000
*+ 6.250000e-010 0.000000 6.350000e-010 1.200000
*+ 1.250000e-009 1.200000 1.260000e-009 0.000000
*+ 1.875000e-009 0.000000 1.885000e-009 1.200000
*+ 2.500000e-009 1.200000 2.510000e-009 0.000000
*+ 3.125000e-009 0.000000 3.135000e-009 1.200000
*+ 3.750000e-009 1.200000 3.760000e-009 0.000000
*+ 4.375000e-009 0.000000 4.385000e-009 1.200000
*+ 5.625000e-009 1.200000 5.635000e-009 0.000000
*+ 6.250000e-009 0.000000 6.260000e-009 1.200000
*+ 8.125000e-009 1.200000 8.135000e-009 0.000000

.TEMP 25.000000

.OPTIONS INGOLD=2 000000
.OPTIONS NUMDGT=8


*.OPTIONS DELMAX=1.000000e-011

*.TRAN 5.000000e-012 9.375000e-009
*.PRINT TRAN V(PAD) I(VCCT2B)
*.PRINT TRAN V(DVDD)
*.PRINT TRAN V(I)

*.END

E1 probe_PAD1 DVSS VOLT = "1*V(PAD1,DVSS)"
E2 probe_PAD2 DVSS VOLT = "1*V(PAD2,DVSS)"
E3 probe_PAD3 DVSS VOLT = "1*V(PAD3,DVSS)"
E4 probe_PAD4 DVSS VOLT = "1*V(PAD4,DVSS)"
E5 probe_PAD5 DVSS VOLT = "1*V(PAD5,DVSS)"
E6 probe_PAD6 DVSS VOLT = "1*V(PAD6,DVSS)"
E7 probe_PAD7 DVSS VOLT = "1*V(PAD7,DVSS)"
E8 probe_PAD8 DVSS VOLT = "1*V(PAD8,DVSS)"
E9 probe_PAD9 DVSS VOLT = "1*V(PAD9,DVSS)"
E10 probe_PAD10 DVSS VOLT = "1*V(PAD10,DVSS)"
E11 probe_PAD11 DVSS VOLT = "1*V(PAD11,DVSS)"
E12 probe_PAD12 DVSS VOLT = "1*V(PAD12,DVSS)"
E13 probe_PAD13 DVSS VOLT = "1*V(PAD13,DVSS)"
E14 probe_PAD14 DVSS VOLT = "1*V(PAD14,DVSS)"
E15 probe_PAD15 DVSS VOLT = "1*V(PAD15,DVSS)"
E16 probe_PAD16 DVSS VOLT = "1*V(PAD16,DVSS)"
E17 probe_PAD17 DVSS VOLT = "1*V(PAD17,DVSS)"
E18 probe_PAD18 DVSS VOLT = "1*V(PAD18,DVSS)"
E19 probe_PAD19 DVSS VOLT = "1*V(PAD19,DVSS)"
E20 probe_PAD20 DVSS VOLT = "1*V(PAD20,DVSS)"
E21 probe_PAD21 DVSS VOLT = "1*V(PAD21,DVSS)"
E22 probe_PAD22 DVSS VOLT = "1*V(PAD22,DVSS)"

.ends
*
```

spice_io_read.ckt



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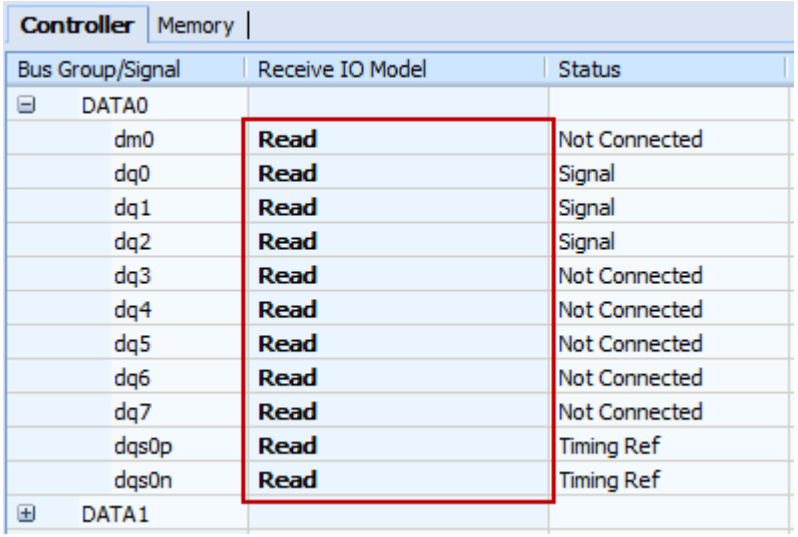
Read Operation (cont')

- In a bus simulation, user can easily switch the model of the Controller's buffer to "Read"



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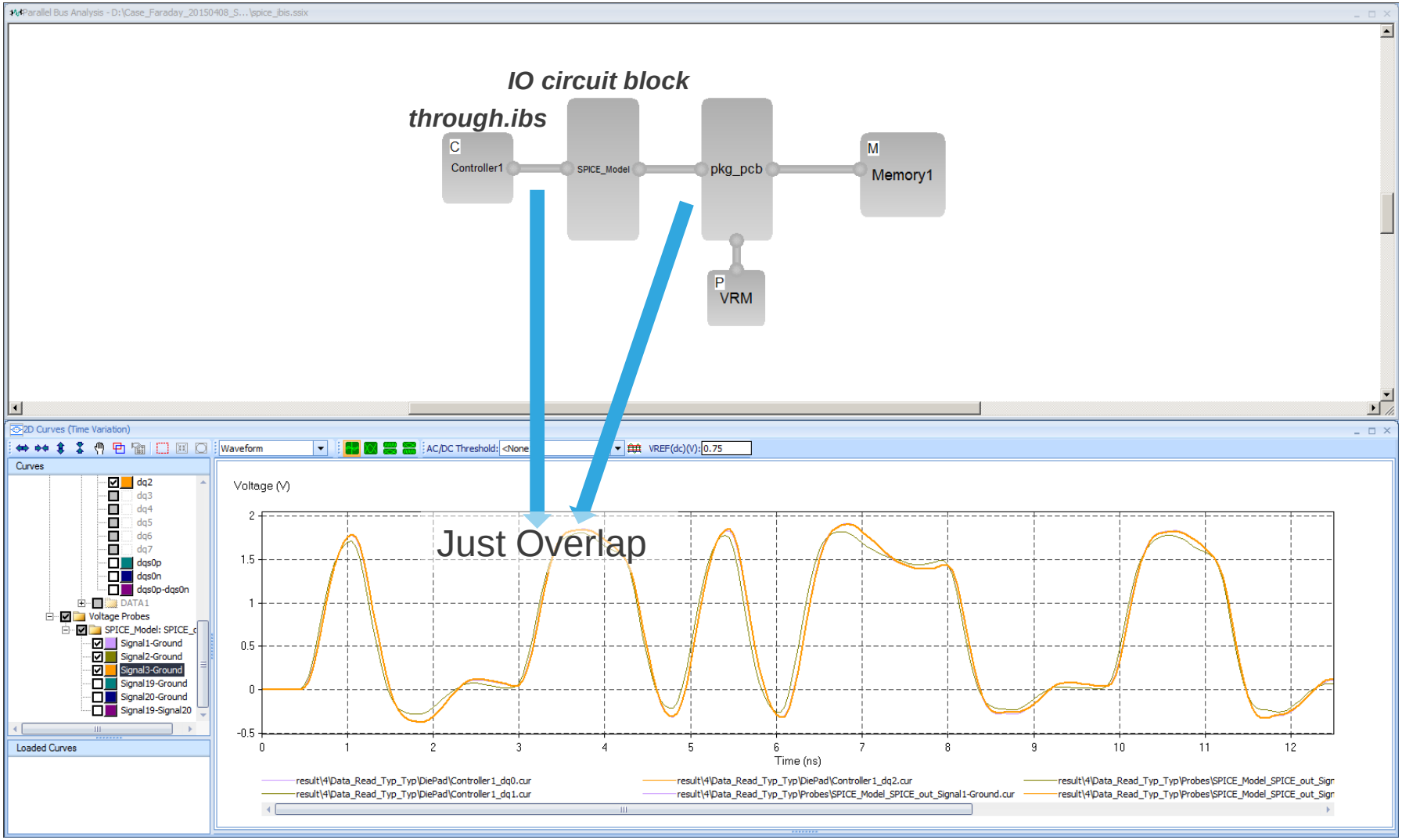
Read Operation (cont')



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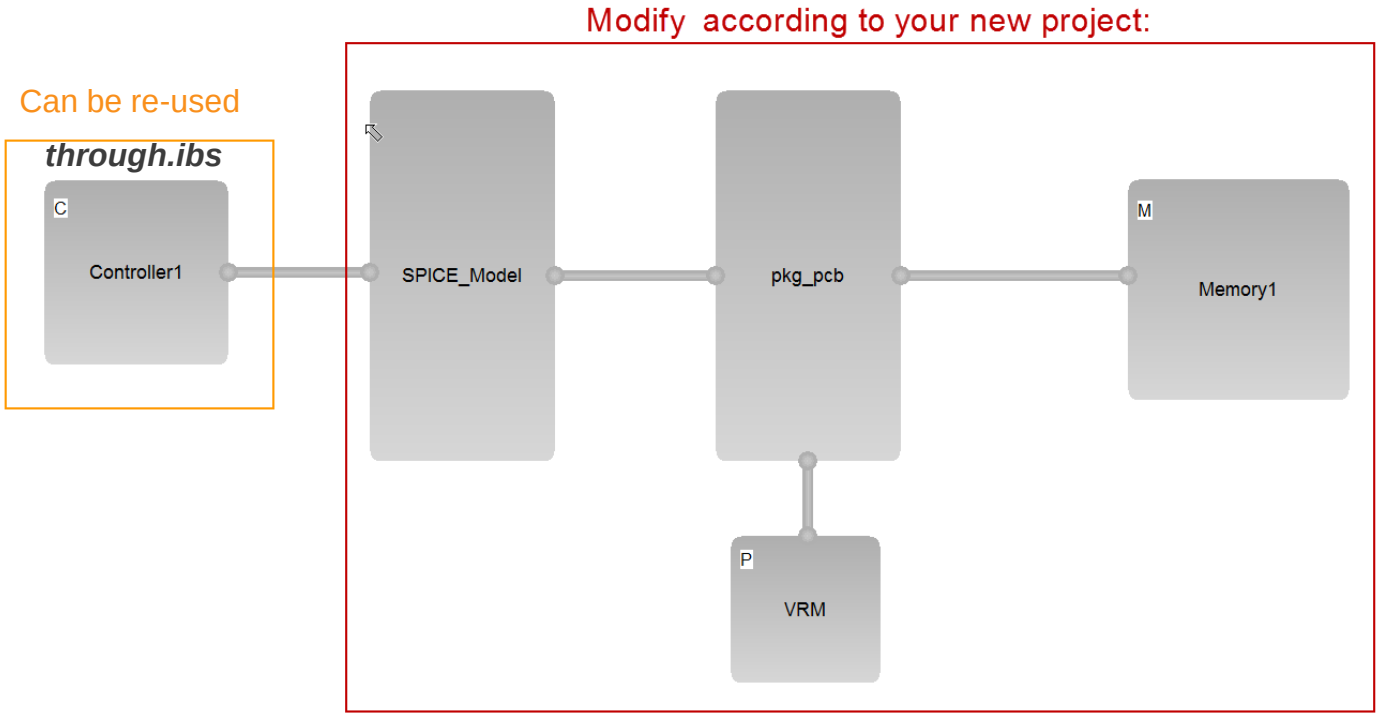
Read Operation (cont')

For a new project, the kit is re-usable with little modification



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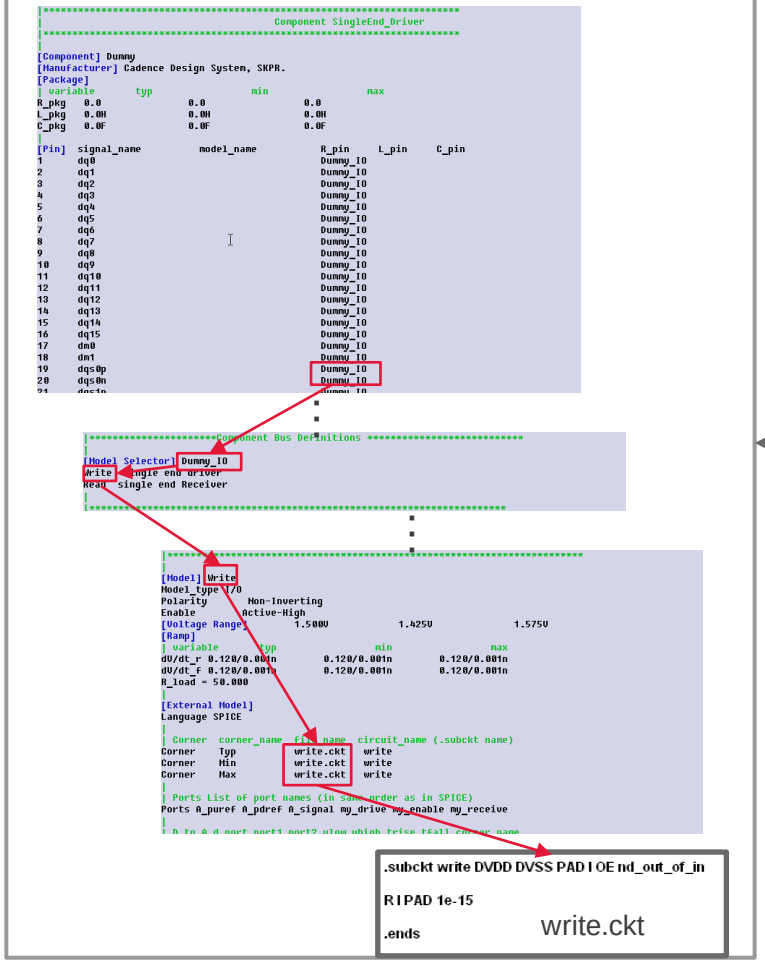
Differential Buffer

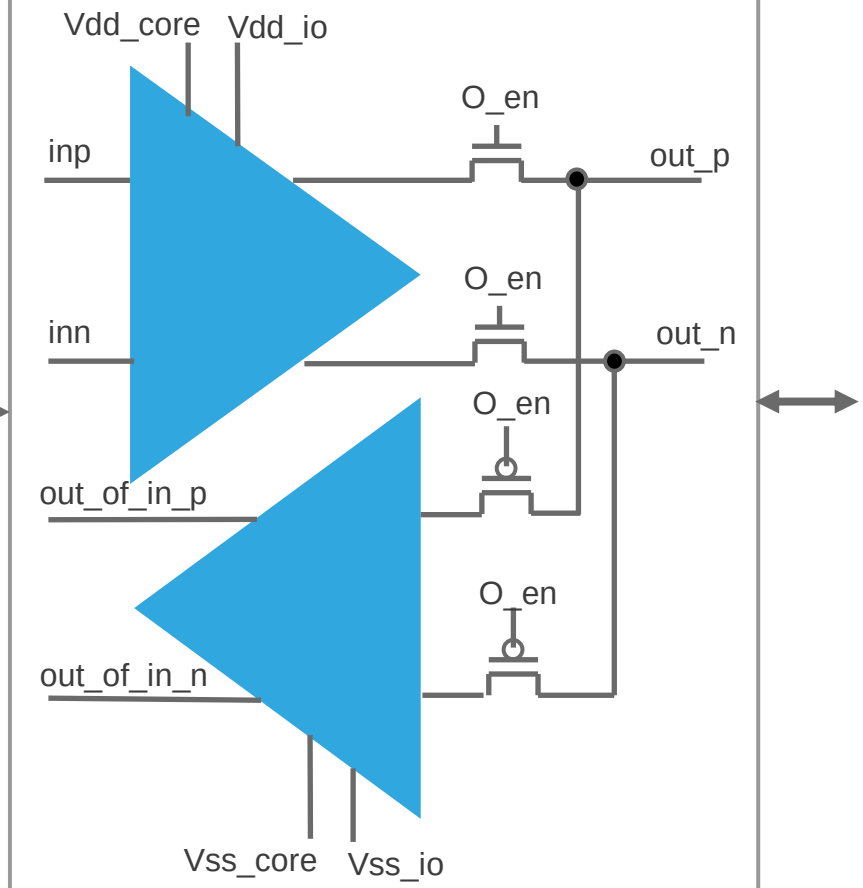
No matter true or pseudo, you can use the same kit without any modification because:

(take "**write operation**" as an example)

Controller (***through.ibs***)



SPICE Model Circuit Block
(Netlist-based IO Model)



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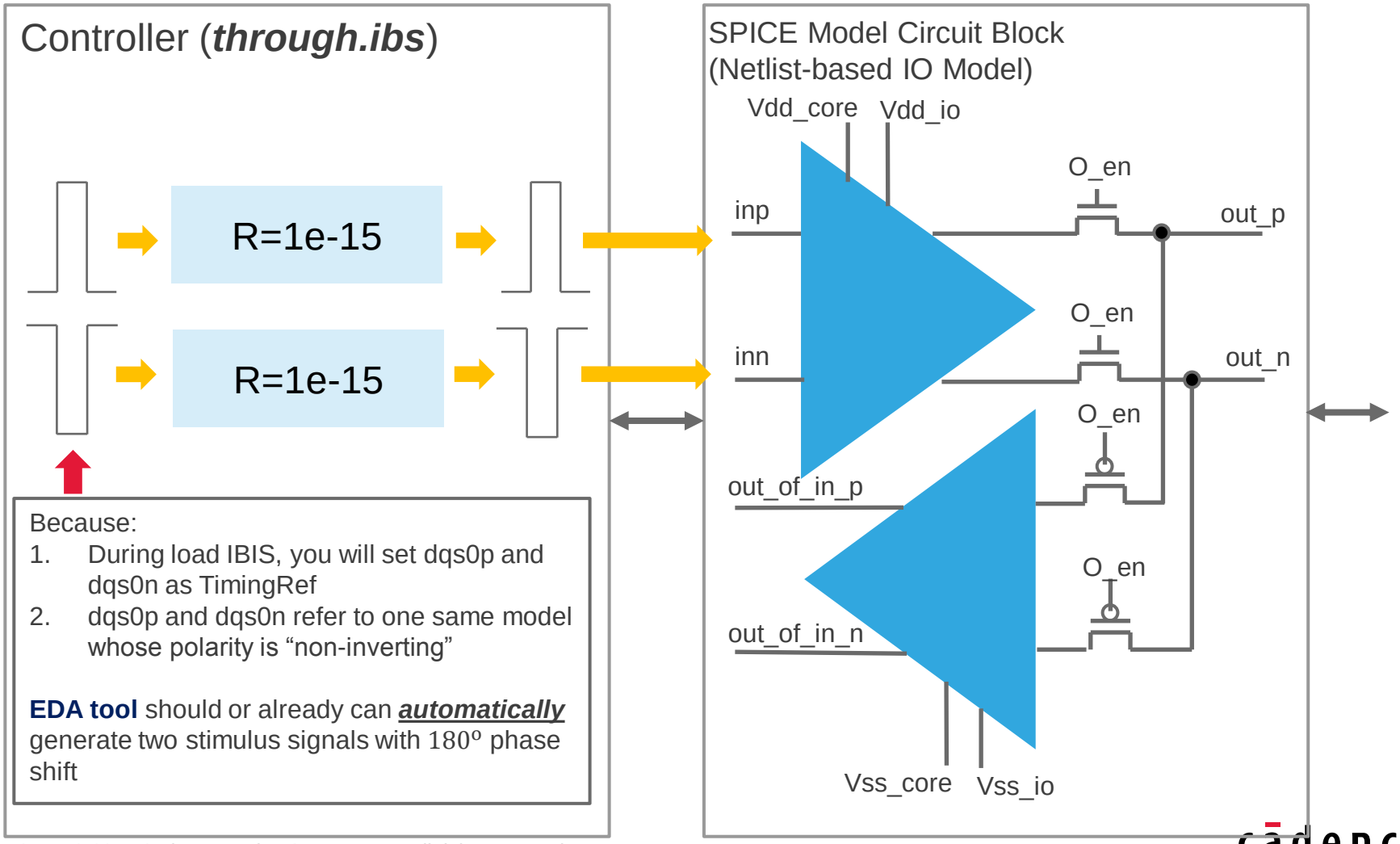
Differential Buffer (cont')

For Truly Differential Buffer type1:



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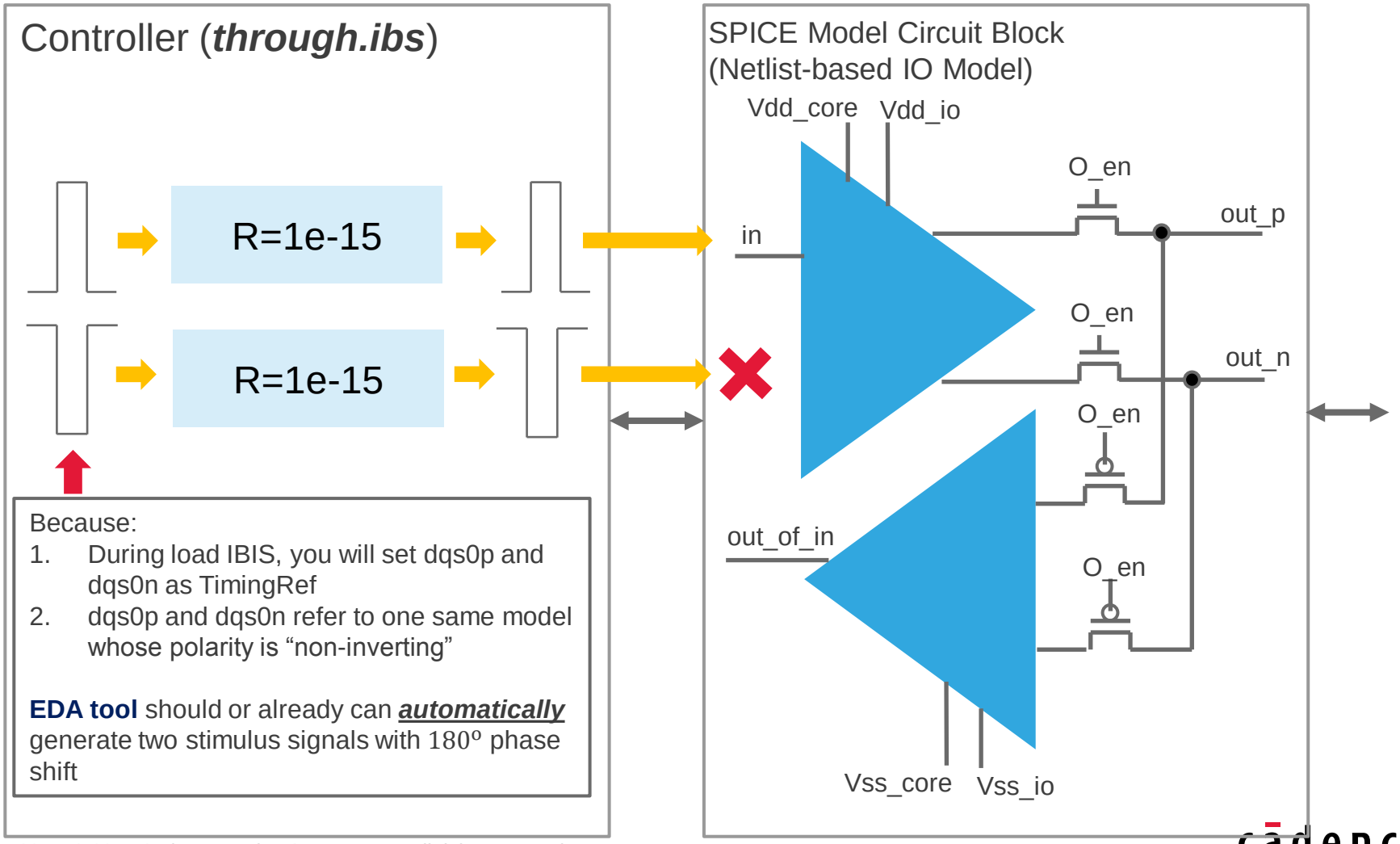
Differential Buffer (cont')

For Truly Differential Buffer type2:



Because:

1. During load IBIS, you will set dqs0p and dqs0n as TimingRef
2. dqs0p and dqs0n refer to one same model whose polarity is "non-inverting"

EDA tool should or already can ***automatically*** generate two stimulus signals with 180° phase shift

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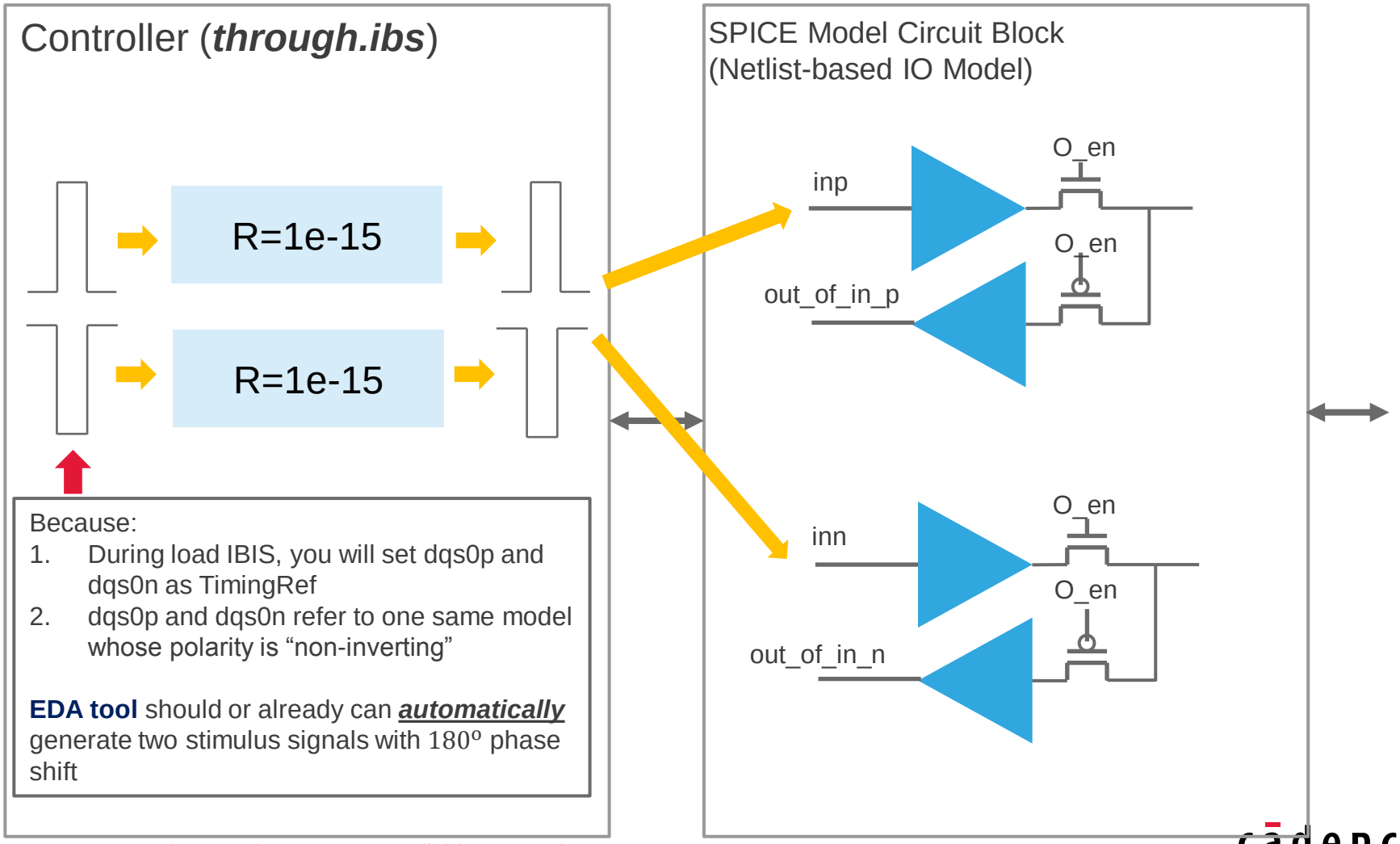
Differential Buffer (cont')

For Pseudo Differential Buffer:



Because:

1. During load IBIS, you will set dqs0p and dqs0n as TimingRef
2. dqs0p and dqs0n refer to one same model whose polarity is "non-inverting"

EDA tool should or already can ***automatically*** generate two stimulus signals with 180^{o} phase shift

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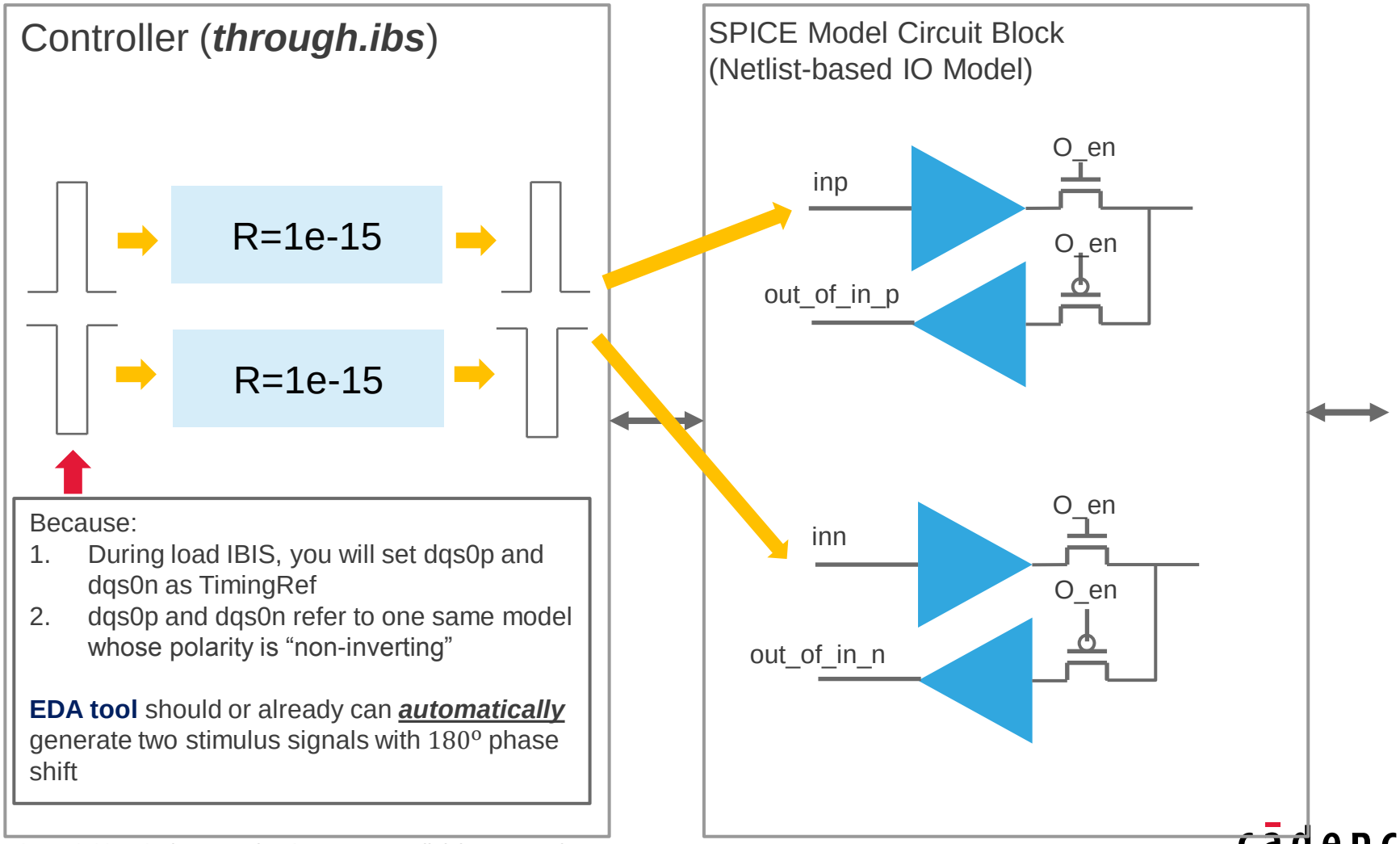
Differential Buffer (cont')

For Pseudo Differential Buffer:



Because:

1. During load IBIS, you will set dqs0p and dqs0n as TimingRef
2. dqs0p and dqs0n refer to one same model whose polarity is "non-inverting"

EDA tool should or already can ***automatically*** generate two stimulus signals with 180^{o} phase shift

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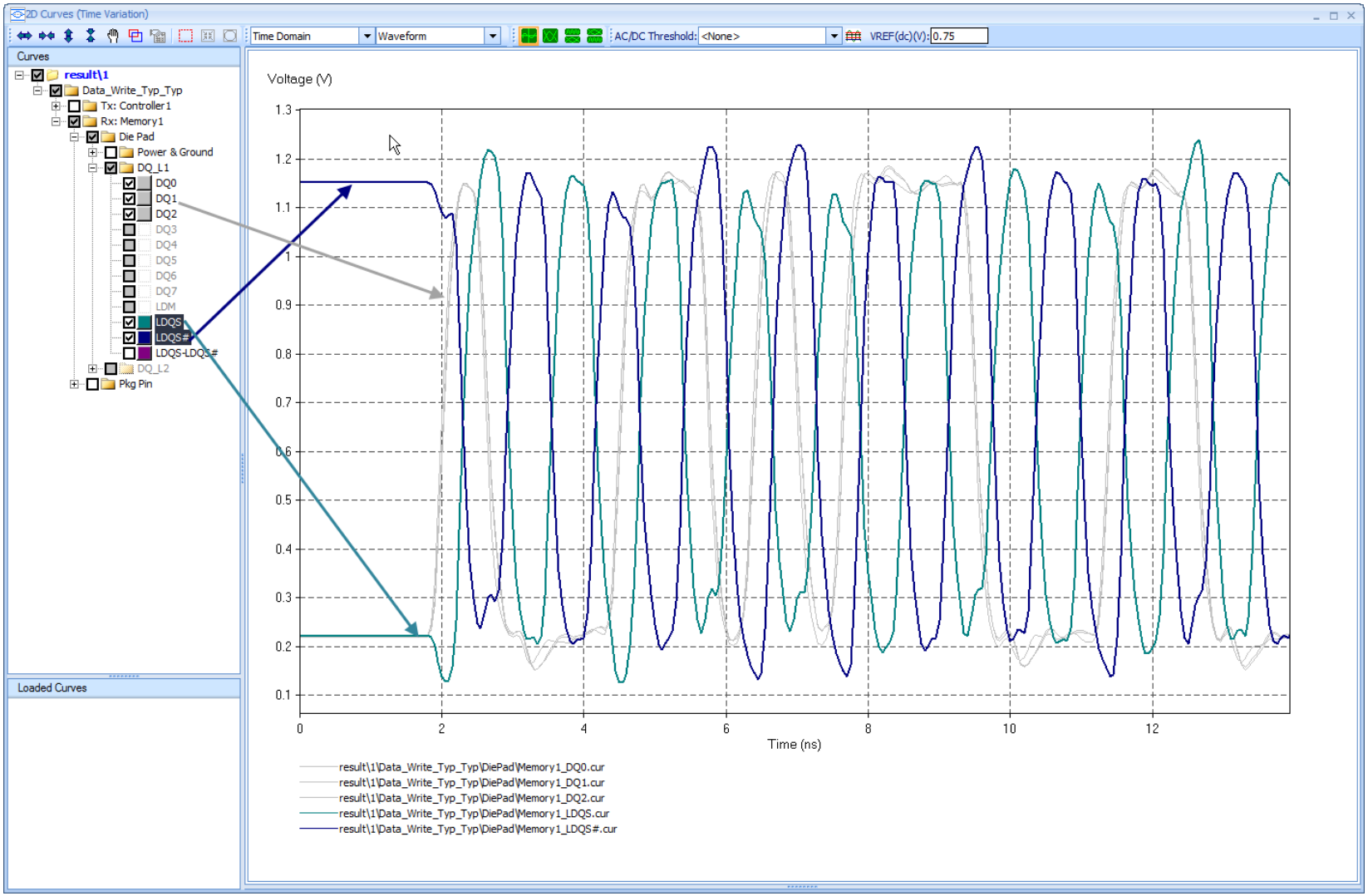
Differential Buffer (cont')

An example with method2: 3 DQ and 1 pair of DQS



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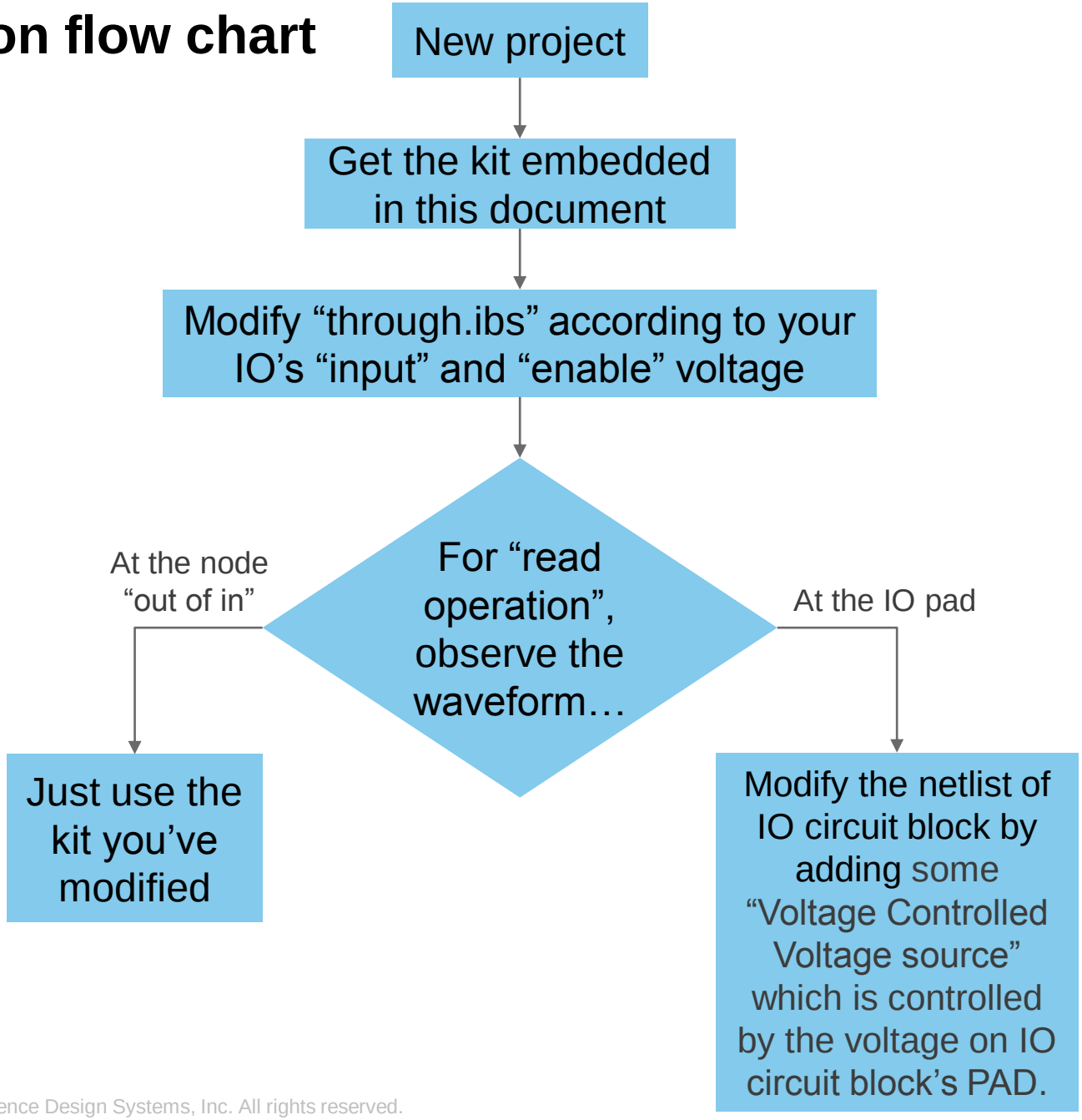
Solution flow chart



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Summary

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Notes

- For analysis of SSN
  - With the full flexibilities as using SPICE, this method allows user to do **a power-aware SSN analysis between multiple signals and multiple PDNs**, such as VDD_Core/VSS_Core, VDDIO/VSSIO, VTT and VREF together at the same time.
- Model modification and change of topology
  - This method requires the change of topology - inserting a Spice block but the wrapping .sp file according to the description in [External Model] is not necessary since it's ready for use in the kit - **easy for re-using** this kit in a new project of a new IO.
- Read Operation
  - As this method requires the change of topology when building topology, during the analysis of read operation, user will need to modify **the netlist of the IO circuit block** by adding some "Voltage Controlled Voltage source" which is controlled by the voltage on IO circuit block's PAD.
- Differential Buffer
  - This method can use the same kit without additional modification for both single-end and differential buffer, **no matter it's truly or pseudo**.

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References

- IBIS specification (v6.1)
  http://www.ibis.org/ver6.1/ver6_1.pdf

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