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FEC Applications for 25Gb/s Serial Link Systems

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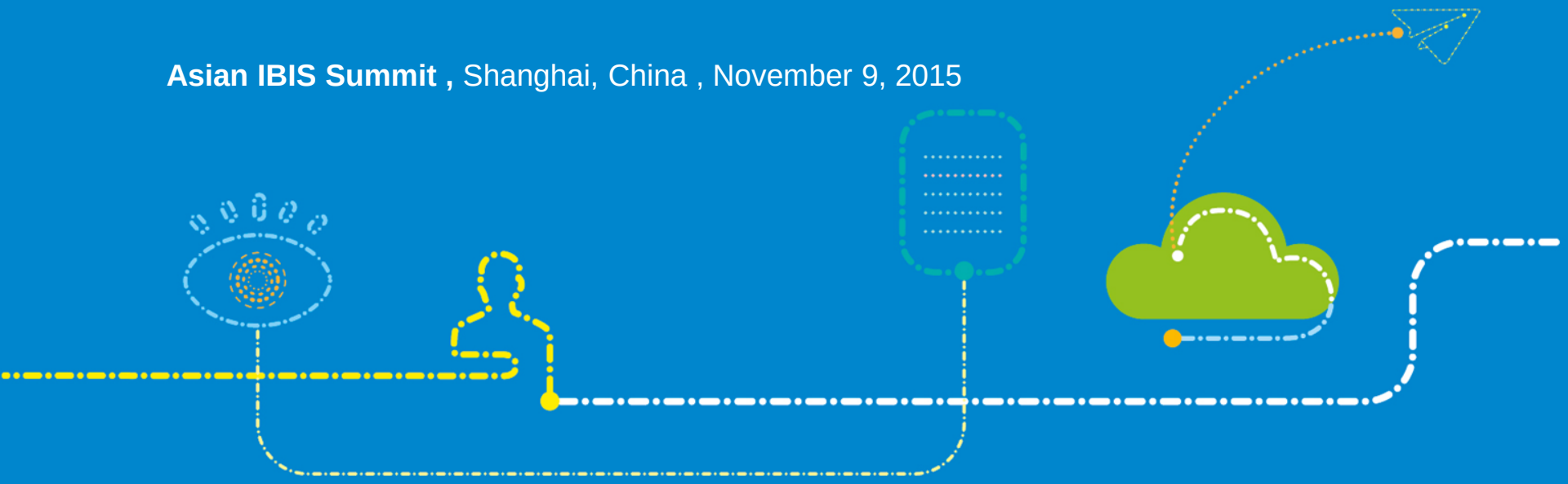
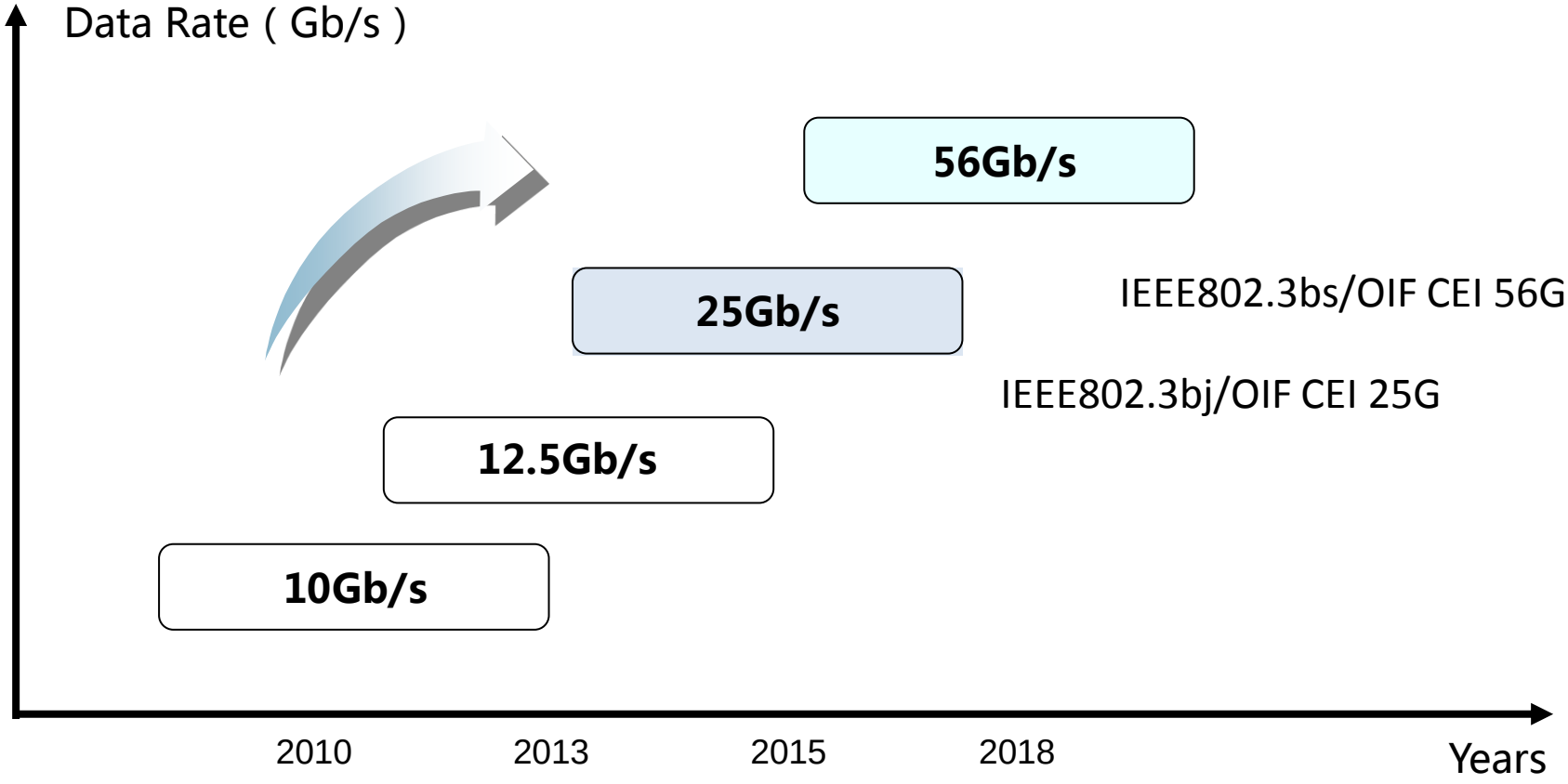


Agenda

- Introduction
- FEC Applications to Serial Link System
- FEC Simulations for 25Gb/s SerDes System
- A New Proposal for FEC Modeling and Simulation
- Summary

Introduction

100 Gigabit Ethernet will account for over half of all bandwidth deployed in carrier network in 2014，growing rapidly through 2018.



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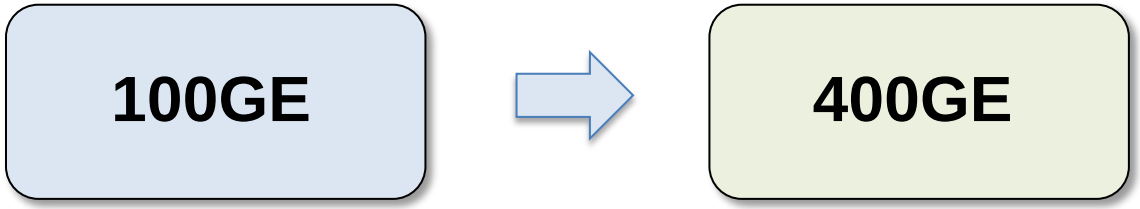
Introduction

Besides equalization techniques，some new techniques have been used for SerDes systems in order to meet 100GE- 400GE specs.

Higher Data Rate：25Gb/s to 56Gb/s



Equalization：
De-emphasis+CTLE+DFE

Forward Error Correction：**FEC**
Fanny Modulation：NRZ or PAM4

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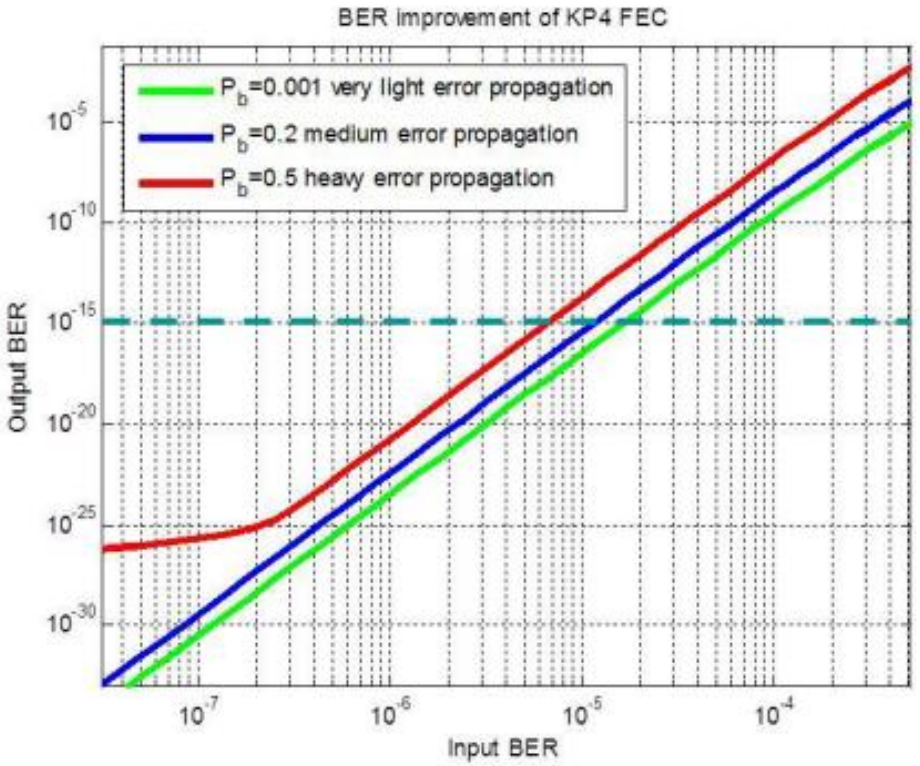
Introduction

The Forward Error Correction（FEC）has been used for Increasing serial link system budgets and relaxing BER requirements.

- Code Gain
  - Gain vs Higher Frequency
- Time
  - Serial Link Latency
- Complexity
  - Area and Power



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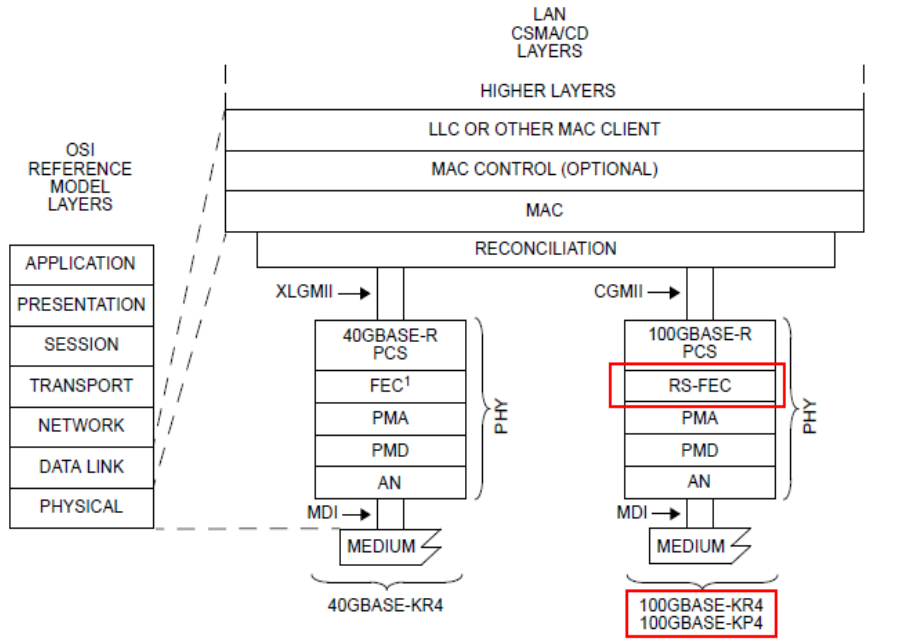
FEC Applications to Serial Link System

FEC Applications on the 100GE standard of IEEE802.3bj



- Backplane System —100GBASE-KR4
- FEC block is placed between PCS and PMA
- Reed-Solomon Code is suggested , defined in clause 91
- RS(528,514,7) — about 5dB gain

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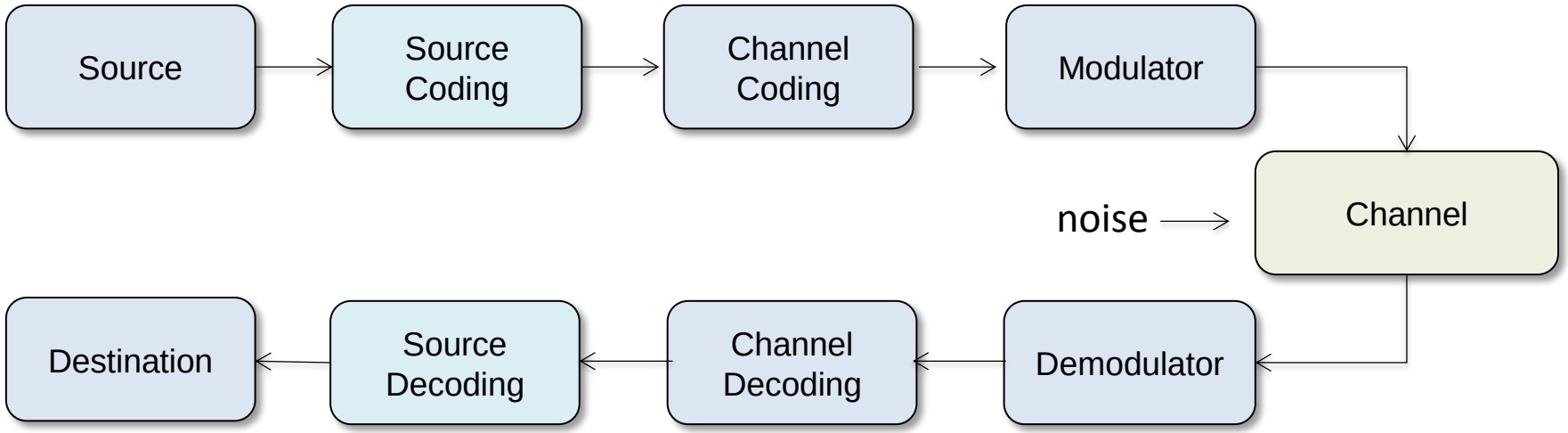
FEC Applications to Serial Link System



Recently adopted FEC

- Fire Code （1604, 1584） – OIF CEI-P
- QC Code （2112, 2080） – 10GBASE-KR
- RS（528, 514, 7） over GF(210) – 100GBASE-KR4
- RS（544, 514, 15） over GF(210) – 100GBASE-KP4

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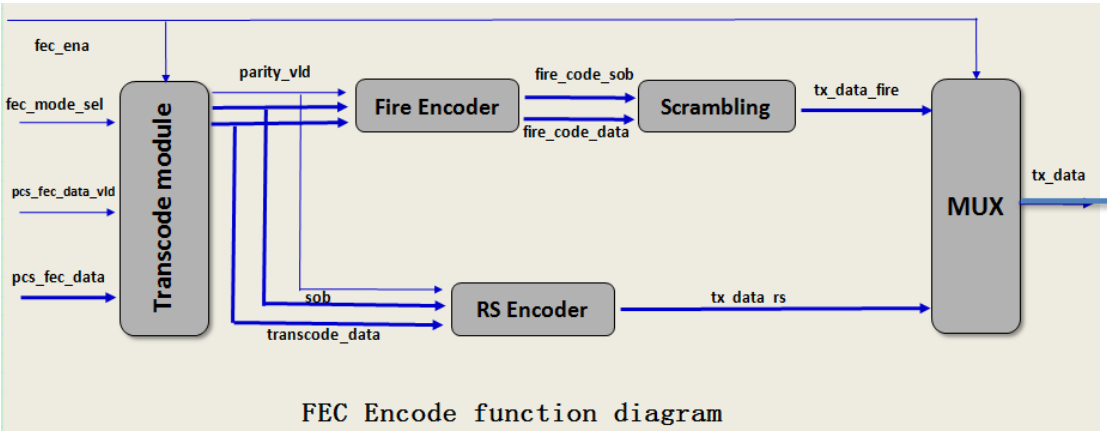
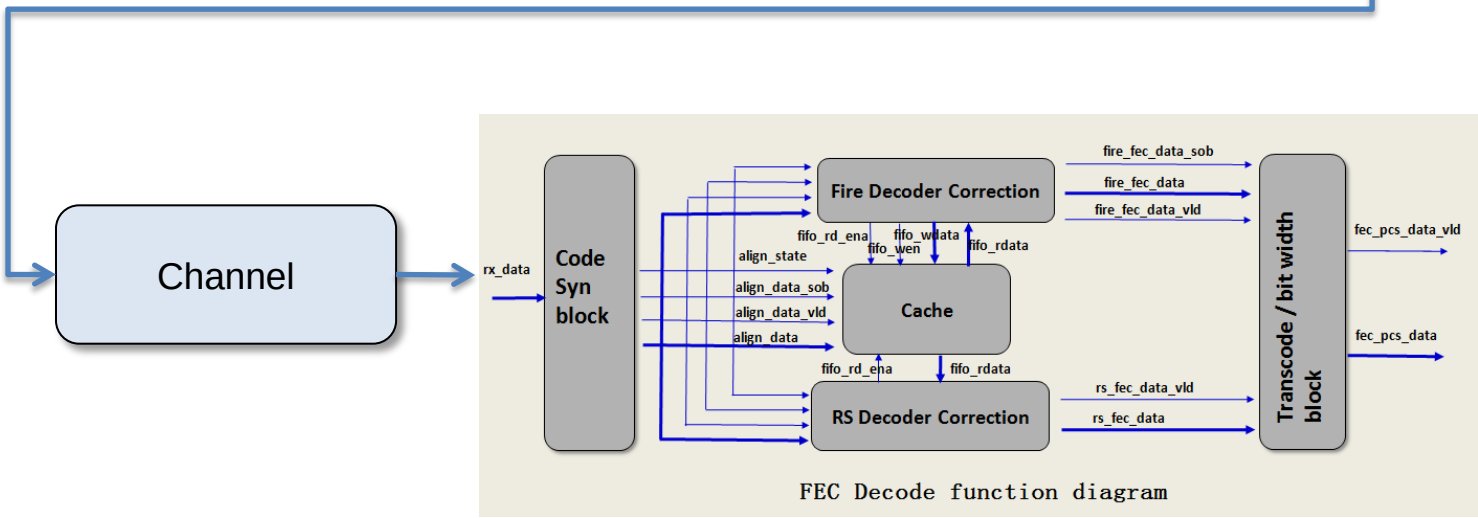
FEC Applications to Serial Link System

FEC Encoding & Decoding diagram





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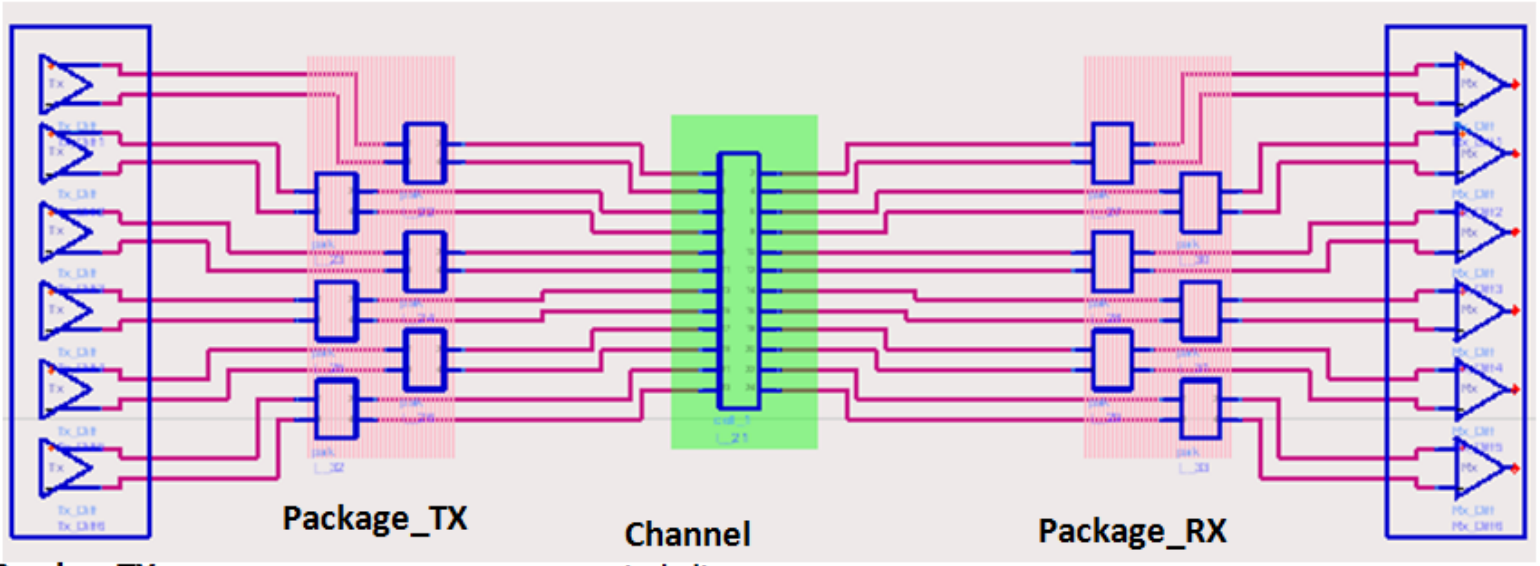
FEC Simulations for 25Gb/s SerDes System

Simulation Setup :

Data rate:25.78125Gb/s
BER:~1e-15
Pattern : PRBS 31
Number of bits: 1million



Serdes_TX
Including
Pattern
prbs31;FEC;
FFE ...

Channel
including
Backplane*1;
Daughter Card*2;
Connector*2
Channel length:30inch

Serdes_RX
Including
CTLE;DFE ;
FEC; ...

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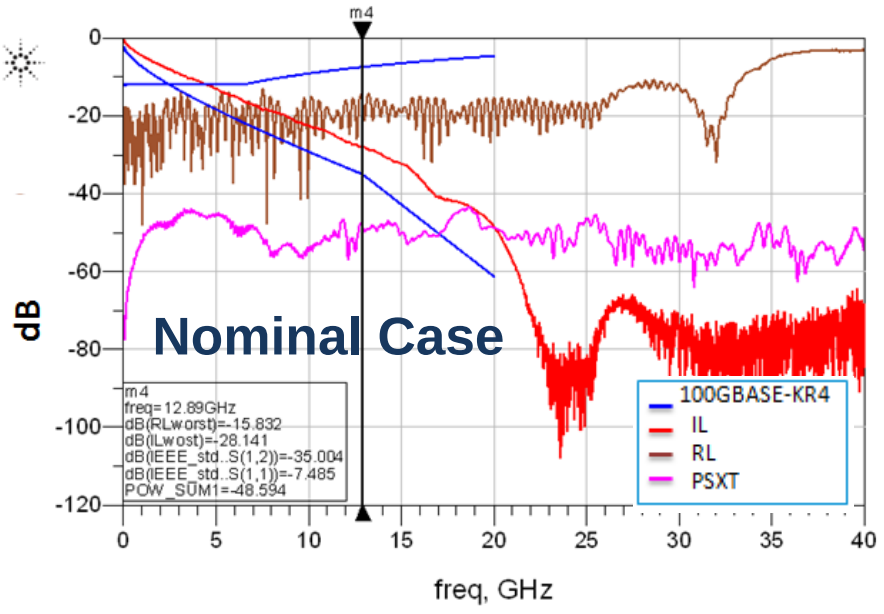
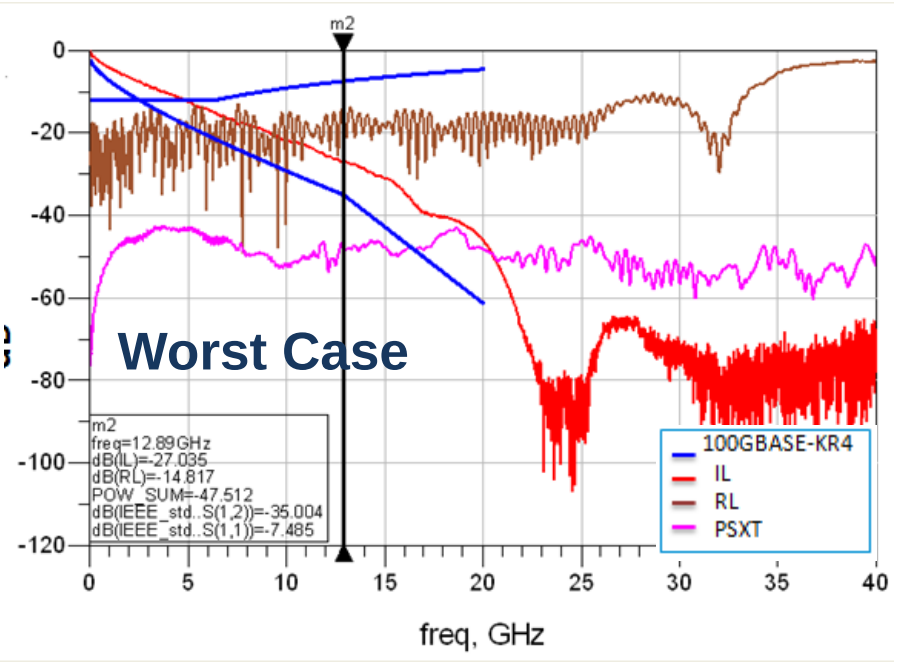
FEC Simulations for 25Gb/s SerDes System





	IL/dB	RL/dB	PSXT/dB
Nominal	-26.3	-16.8	-47.51
Worst	-28.1	-15.83	-48.59

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FEC Simulations for 25Gb/s SerDes System

Comparison between with and without FEC

	Nominal Case		Worst Case		
AtBER	Width/*UI	Height/mV	Width/%*UI	Height/mV	Condition
^1e-12	16.2%	23.1	4.51%	5.39	With emphasis/DFE ; Without FEC
^1e-15	12.2%	17.4	0.07%	0.00	
^1e-17	9.92%	14.2	0.00%	0.00	
^1e-12	42.5%	57.0	42.2%	48.6	With emphasis/DFE ; With FEC
^1e-15	40.6%	54.8	40.2%	46.4	
^1e-17	39.5%	53.4	38.9%	45.1	

Eye diagram at the BER of 1e-12 of the channel simulation can not meet the requirement of 100GE Standard without FEC.
Crosstalk must be concerned in the channel simulation.

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FEC Simulations for 25Gb/s SerDes System

Comparison between with and without FEC

	Nominal Case		Worst Case		
AtBER	Width/*UI	Height/mV	Width/%*UI	Height/mV	Condition
^1e-5	33.5%	63.6	32.6%	54.6	With emphasis/DFE ; Without FEC;
^1e-6	29.1%	62.4	23.2%	53.5	
^1e-7	25.9%	61.4	17.1%	52.6	
^1e-12	42.5%	57.0	42.2%	48.6	With emphasis/DFE ; With FEC;
^1e-15	40.6%	54.8	40.2%	46.4	
^1e-17	39.5%	53.4	38.9%	45.1	

Eye diagram at the BER of 1e-15 of the channel simulation can meet the requirement of 100GE Standard with FEC, while relaxing the BER requirement from 1e-15 to 1e-5 or 1e-6.

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A New Proposal for FEC Modeling and Simulation

Current Situation:

- IBIS-AMI model

```
(my_AMIname                  | Header,such as AMI_version …
                             | Function such as, GetWave_Exists …
     (Reserved_Parameters    | Modulation such as, NRZ, PAM4 …
                             | Jitter such as, Dj …
                             | Repeater …
```

- EDA Tool

  FEC blocks are not supported in IBIS-AMI model nor in EDA tool

- System Simulation

  Uses the same Serdes IP on the TX and RX end supported by the IC Vendor

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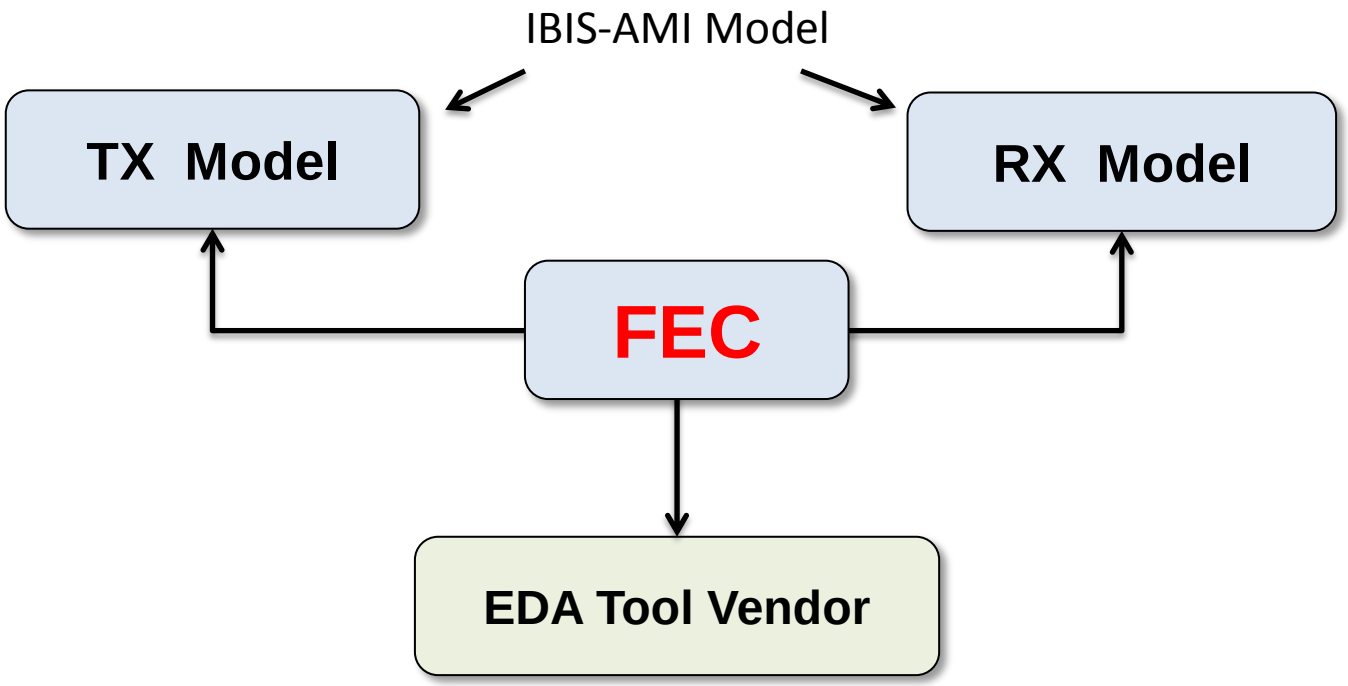
A New Proposal for FEC Modeling and Simulation



System vendors strongly expect that IBIS-AMI models can be used for FEC simulations.

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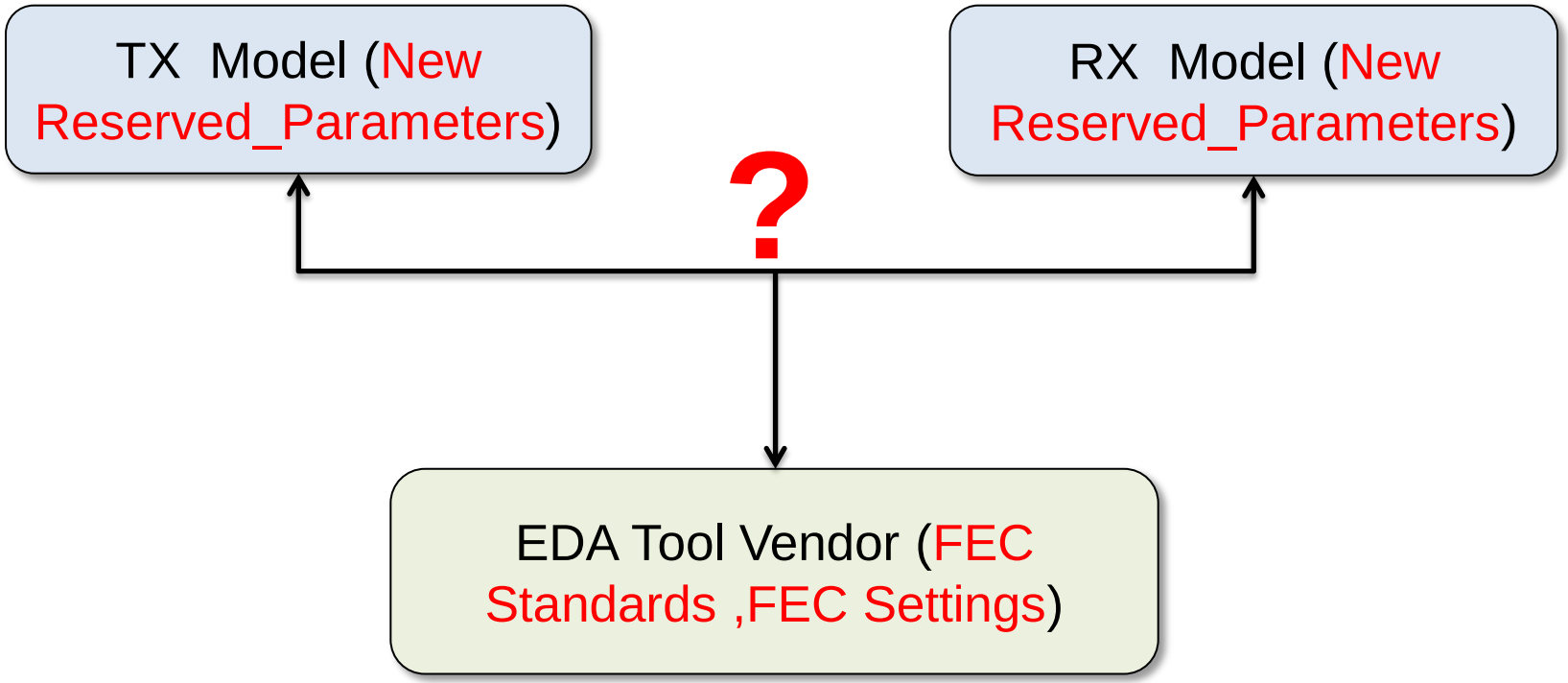
A New Proposal for FEC Modeling and Simulation



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A New Proposal for FEC Modeling and Simulation

[Reserved_Parameters] / [Model_Specific] → tx_fec / rx_fec ?

On the transmit end
Add the branch 'tx_fec' into Model_Specific, then add parameters, config min/typ/max, mode on/off, such as

```
(Model_Specific
  (tx_fec
    (config (Usage In)(List "min" "typ" "max")(Type String)
      (Default "typ")(Description "enable fec function setting"))
    (mode (Usage In)(Format List "on" "off")(Type String)
      (Default "off")(Description "fec control mode"))
```

On the receiver end,
Add the branch 'rx_fec' into Model_Specific, then add the same parameters to respond the tx configuration, such as

```
(Model_Specific
  (rx_fec
    (config (Usage In)(List "min" "typ" "max")(Type String)
      (Default "typ")(Description "enable fec function setting"))
    (mode (Usage In)(Format List "on" "off")(Type String)
      (Default "off")(Description "fec control mode"))
```


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Summary

- FEC can be used for many dispersion and noise limited systems, such as high-speed serial link systems in order to meet 100GE- 400GE specs.
- FEC relaxes PHY BER requirement from 1e-15 to 1e-06 for serial link systems.
- FEC is one of critical techniques for 25-56Gb/s SerDes systems and IBIS-AMI model is an efficient solution for complex IO modeling.
- System vendors strongly expect that IBIS-AMI models can be used for FEC simulations.
- “One model, one platform, one simulator” needed for both passive and active components, such as FFE，DFE，FEC …

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Thank you

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