WELCOME FROM MIKE LABONTE, SIGNAL INTEGRITY SOFTWARE

Ladies and Gentlemen,

As chair of the IBIS Open Forum it is my pleasure to welcome you to the 2015 Asian IBIS Summit in Shanghai, and to thank you for your presentations and participation. We are grateful to our sponsors Huawei Technologies, Cadence Design Systems, IO Methodology, Keysight Technologies, Synopsys, Teledyne LeCroy, and ZTE Corporation for making this event possible.

Since 1993 IBIS has provided the digital electronics industry with specifications to make signal, timing, and power integrity analyses much easier and faster. The challenges keep changing and the IBIS community keeps responding with new enhancements to the IBIS family of specifications, which the IC vendors, EDA tool companies, and system designers adopt readily.

Support for IBIS in Asia has been strong, and the IBIS Open Forum looks forward to continued innovation and contributions from technology companies in this part of the world. Thank you!

Mike LaBonte
Signal Integrity Software (SiSoft)
Chair, IBIS Open Forum

WELCOME FROM MIKE LABONTE, SIGNAL INTEGRITY SOFTWARE

女士们，先生们，

作为 IBIS 开放论坛的主席我很高兴地欢迎大家来到 2015 年亚洲 IBIS 上海峰会，并感谢您的演讲和参与。我们特别要感谢我们的赞助商华为技术，Cadence Design Systems，IO Methodology Inc， Keysight Technologies，Synopsys，Teledyne LeCroy 和 ZTE 中兴通讯，是他们使本次活动成为可能。

从 1993 年至今，IBIS 为高速数字电路设计的信号，时序和功率完整性分析方面提供了更加容易和快捷电子模型行业规范。为适应不断变化的挑战，在 IC 供应商， EDA 工具公司和系统设计师的共同努力下， IBIS 正在继续不断加入新的功能和完善已有的 IBIS 系列规范。

在亚洲， IBIS 一直受到广泛的支持。 从世界的这一部分， IBIS 开放论坛期待着有更多的技术创新和贡献。

谢谢！

Mike LaBonte (迈克 拉邦地)
SiSoft 公司
主席，IBIS 开放论坛

WELCOME FROM LI JINJUN, HUAWEI TECHNOLOGIES

Ladies and Gentlemen,

On behalf of Huawei Technologies, welcome to the 11th annual Asian IBIS Summit (China). I would like to express my appreciation to IBIS Open Forum and all the sponsors for co-organizing this event.

Since 2005, IBIS Asian Summit in China has been the top-level international conference in high speed digital design society in China. I am looking forward to work with IBIS members in China, and to expand our participations in the region.

Huawei has actively involved in all IBIS society's events. We hope to resolve high speed link issues with IBIS Open Forum, EDA vendors and IC vendors. Your comments and suggestions will be deeply appreciated!

Welcome all of you to Shanghai! Hope you will enjoy all the technical discussions and sharing throughout the meeting, and have a nice journey !

Thank you!
Jinjun Li
Huawei Technologies

各位专家，各位来宾：

我代表华为公司，欢迎大家来参加第 11 届亚洲 IBIS 技术研讨会，衷心地感谢 IBIS 协会组织本次会议。

自从 2005 年以来，IBIS 技术研讨会已经成为了中国高速设计领域的一次盛会。我很高兴有机会与 IBIS 协会一起促进和扩大在该领域的分享。

华为积极参与各项 IBIS 活动，希望与 IBIS 协会、EDA 软件、芯片公司一道来共同解决许多高速链路设计上的挑战，欢迎大家会上讨论和建议。

欢迎 IBIS 专家来到上海，希望你们能够喜欢所有的技术讨论和会议分享，度过美好一天。

谢谢大家
华为公司 厉进军

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

8:15 **SIGN IN**
- Vendor Tables Open at 8:30

8:45 **WELCOME**
- Li, JinJun
  (Huawei Technologies, China)
- LaBonte, Mike (Chair, IBIS Open Forum
  (Signal Integrity Software (SiSoft), USA)

9:00 **IBIS Chair's Report** **7**
(LaBonte, Mike (Signal Integrity Software (SiSoft), USA)

9:25 **Introducing IBIS Version 6.1** **16**
Mirmak, Michael (Intel Corporation, USA)

9:45 **Enabling Full Power-aware Bus Simulation with Non-IBIS Device Model - A Kit Using IBIS [External Model]** . . . **21**
Liang, Skipper (Cadence Design Systems, China)

10:35 **BREAK** (Refreshments and Vendor Tables)

11:25 **A Practical DOE Application in Statistical SI Analysis Using IBIS & How Can We Make IBIS Work Beyond Best Case/Worst Case?** **41**
Shi*, Feng; Ekholm**, Anders; Mahmod**, Zilwan and
Zhang*, David (Ericson, *China, **Sweden)

11:20 **IBIS Interconnect BIRD Update** **48**
Katz, Walter (Signal Integrity Software (SiSoft), USA)

12:00 **FREE BUFFET LUNCH** (Hosted by Sponsors)
- Vendor Tables

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

IBIS Chair's Report

http://ibis.org/

Mike LaBonte
SiSoft
Chair, IBIS Open Forum

Asian IBIS Summit
Shanghai, China
November 9, 2015

Specification Development

IBIS Milestones

I/O Buffer Information Specification

- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
  - Dynamic buffers
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power aware
- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
  - Power delivery package models

Other Work

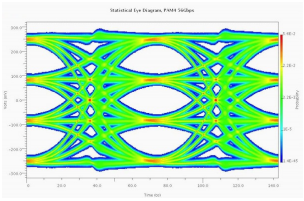
- 1995: **ANSI/EIA-656**
  - IBIS 2.1
- 1999: **ANSI/EIA-656-A**
  - IBIS 3.2
- 2001: **IEC 62014-1**
  - IBIS 3.2
- 2003: **ICM 1.0**
  - Interconnect Model Specification
- 2006: **ANSI/EIA-656-B**
  - IBIS 4.2
- 2009: **Touchstone® 2.0***
- 2011: **IBIS-ISS 1.0**
  - Interconnect SPICE Subcircuit specification

**Touchstone® is a registered trademark of Agilent Technologies, Inc.*

Specification Development

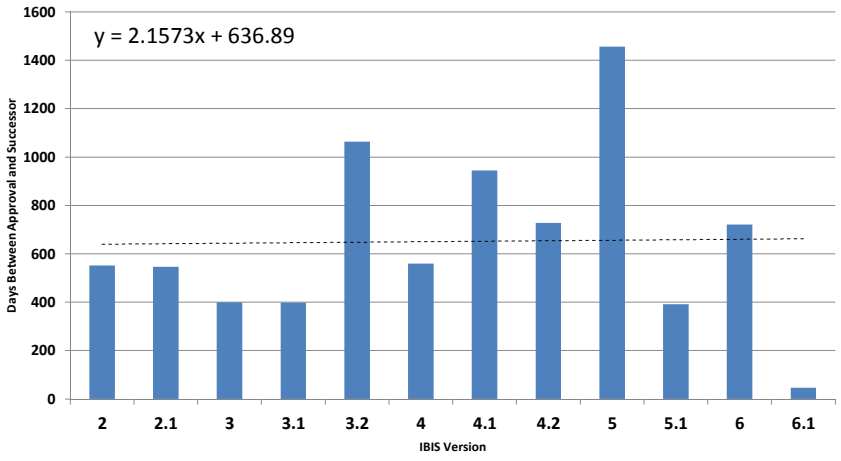
Progress: IBIS 6.1 Ratified

- Ratified 11 September 2015
- Support for PAM4
- IBIS-AMI Parameters Simplified
- Package Models for Power Integrity
- and more …



Specification Development

Lifespan of IBIS Versions



Specification Development

In The Works

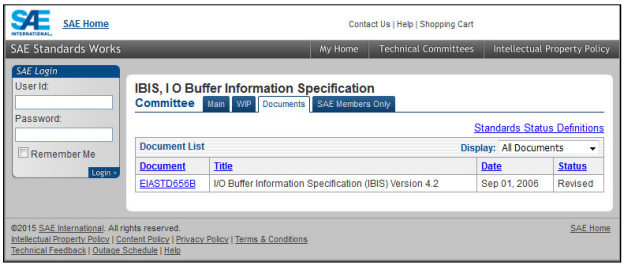
- IBIS 6.2 dedicated to reference node clarifications
  - Potential SAE standard
- Advance Technology Modeling Task Group
  - Optimization/Back-channel support
  - External circuit enhancements
- Interconnect Task Group
  - External Package/on-die models using IBIS-ISS
- IBIS Quality Task Group
  - IBISCHK enhancements and documentation

Specification Development

Status of IBIS Standards

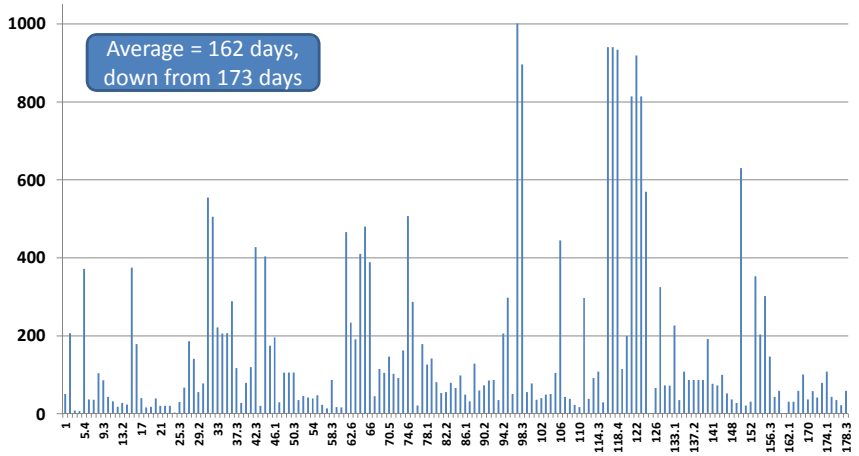
I/O Buffer Information Specification	IBIS 4.2: SAE/EIA-STD-656-B IBIS 3.2: IEC-62014-1
IBIS Interconnect Modeling Specification	ICM 1.1: ANSI/GEIA-STD-0001)

IBIS 6.2 might be next …



Specification Development

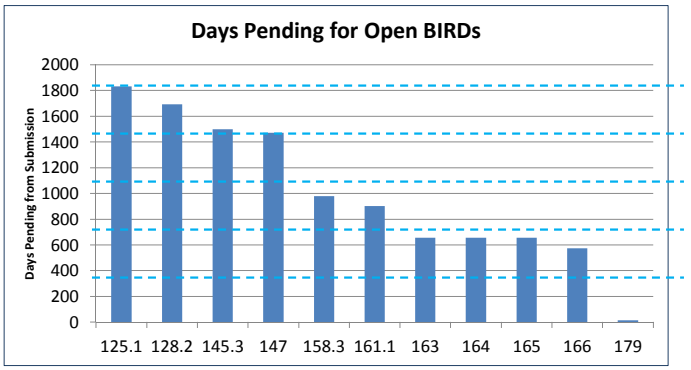
Days To Resolve BIRDs



Specification Development

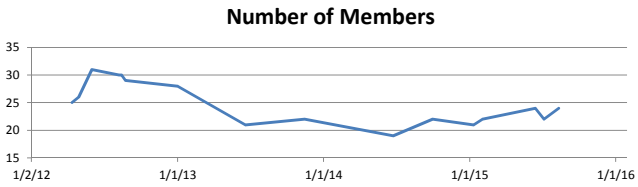
Pending BIRDs

BIRD125.1 pending for 5 years, a new "record"



Organization

24 IBIS Members



Organization

IBIS Officers 2015-2016

- New Chair, Treasurer and Postmaster elected 15 June 2015
- Many thanks to incumbent IBIS officers for their continued service

A special thank you to outgoing chair Michael Mirmak
(Total of 11 terms!)

Chair:	*Mike LaBonte, Signal Integrity Software*
Vice-Chair:	*Lance Wang, IO Methodology Inc.*
Secretary:	*Randy Wolff, Micron Technology*
Treasurer:	*Bob Ross, Teraspeed Labs*
Librarian:	*Anders Ekholm, Ericsson*
Webmaster:	*Mike LaBonte, Signal Integrity Software*
Postmaster:	*Curtis Clark, ANSYS*

Organization

Organizational Activities

- So far in 2015:
  - 15 Open Forum teleconferences
  - 3 Summit meetings (including this one)
    - 2015 first year for EPEPS IBIS summit
  - 38 ATM Task Group teleconferences
  - 10 Editorial Task Group teleconferences
  - 10 Interconnect Task Group teleconferences
  - 35 Quality Task Group teleconferences

Organization

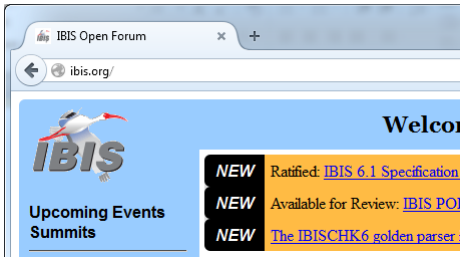
Upcoming Summits

- Asian IBIS Summit, Taipei, Taiwan
  - November 13, 2015
- Asian IBIS Summit, Tokyo, Japan
  - November 16, 2015
- DesignCon IBIS Summit, Santa Clara, CA
  - January 22, 2016
- SPI IBIS Summit, Torino, Italy
  - May 11, 2016

Infrastructure

We Have Moved!

- Our gratitude to Accellera for eda.org web and email service from 1993 to 2015
- Email lists have moved to freelists.org
- Website has moved to http://ibis.org



Infrastructure

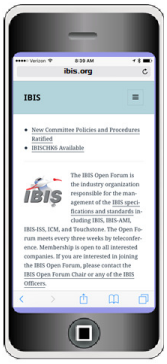
Same Website For Now

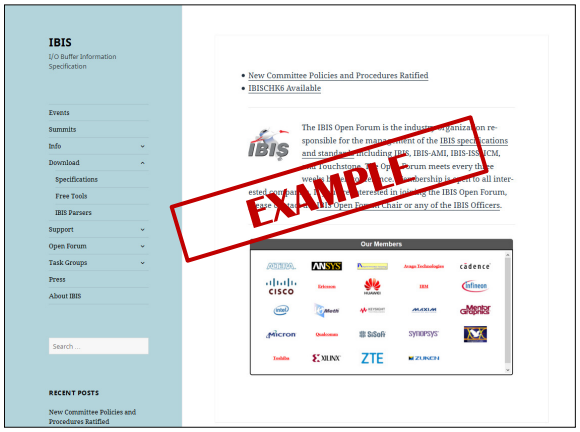
- Manually edited HTML
- Perl scripts

Infrastructure

New Website In The Works

- WordPress
- Bug trackers
- Live Calendar
- Responsive Design





[Thank You]

IBIS Open Forum:
Web: http://ibis.org
Email: ibis-info@freelists.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.

Open BIRDs

125.1	Make IBIS-ISS Available for IBIS Package Modeling	Arpad Muranyi, Mentor Graphics	21-Oct-10
128.2	Allow AMI_parameters_out to pass AMI_parameters_in data on calls to AMI_GetWave	Walter Katz, SiSoft	11-Mar-11
145.3	Cascading IBIS I/O buffers with [External Circuit]s using the [Model Call] keyword	Taranjit Kukal, Ambrish Varma, Cadence Design Systems, Inc. Arpad Muranyi, Mentor Graphics.	19-Sep-11
147	Back-channel support	Marcus Van Ierssel, Snowbush IP; Kumar Keshavan, Sigrity, Inc.; Ken Willis, Sigrity, Inc.; Walter Katz, SiSoft	18-Oct-11
158.3	AMI Touchstonefile (R) Analog Buffer Models	Walter Katz, Signal Integriity Software, Inc.	20-Feb-13
161.1	Supporting Incomplete and Buffer-only [Component] Descriptions	Michael Mirmak, Intel Corp.	8-May-13
163	Instantiating and Connecting [External Circuit] Package Models with [Circuit Call]	Arpad Muranyi & John Angulo, Mentor Graphics; Ambrish Varma & Brad Brim, Cadence Design Systems, Inc.	9-Jan-14
164	Allowing Package Models to be defined in [External Circuit]	Ambrish Varma & Brad Brim, Cadence Design Systems, Inc.; Arpad Muranyi, Mentor Graphics	9-Jan-14
165	Parameter Passing Improvements for [External Circuit]s	Arpad Muranyi & John Angulo, Mentor Graphics; Ambrish Varma & Brad Brim, Cadence Design Systems, Inc	9-Jan-14
166	Resolving problems with Redriver Init Flow	Walter Katz, Signal Integrity Software, Inc. Darshan Shah, F5Networks, Inc.	2-Apr-14
179	New IBIS-AMI Reserved Parameter Special_Param_Names	Arpad Muranyi, Mentor Graphics	13-Oct-15

Introducing IBIS Version 6.1

Michael Mirmak
Intel Corporation

http://www.ibis.org/

ASIAN IBIS Summit
Shanghai, China
November 9, 2015

1

Agenda

IBIS 6.1 Overview and Development

Key Features
- AMI Improvements
- Traditional IBIS Improvements

Methods for Providing Feedback

References

* Other names and brands may be claimed as the property of others

2

Specifications and Activities

- IBIS Version 6.1 approved Sept. 11, 2015
  - Nearly two years to the day after Ver. 6.0 approval
  - Freely available at http://www.ibis.org/ver6.1/
- Waiting for IBIS 6.2 for possible SAE standardization
- A free syntax checker/parser under development
  - Release tentatively expected in November
  - Source code license is available for purchase
  - Current ibischk6 licensees will receive a free update

Key Features of IBIS 6.1

- AMI improvements
  - Extending IBIS-AMI for PAM4 Analysis
  - Model dependencies are supported through a new API
  - Buffer directionality for AMI models
- "Traditional" IBIS improvements
  - V-t table delay and overclocking
  - Package RLC Matrix Diagonals
  - Power Pin Package Modeling
  - New keyword [Initial Delay] for Submodels and Driver Schedules
- Plus corrections, clarifications, and a recommendation

AMI Improvements

- PAM4 Signaling
  - Expands IBIS's AMI support beyond 2 levels (NRZ) to 4 (PAM4)
  - Adds "Modulation", "PAM4_Mapping", offset and threshold Reserved Parameters
  - Re-defines bit-time and clock-times concepts
- Model Dependencies
  - Allows the final values of some .ami parameters to depend on the values of others, or of IBIS [Model]s
  - New flow resolves dependencies before simulation
  - Adds "AMI_Resolve" and "AMI_Resolve_Close" functions
  - Adds "Resolve_Exists" and "Model_Name" Reserved Parameters
  - Adds "Dep" Usage Type

AMI Improvements (2)

- Buffer Directionality
  - Paving the way for DDR4 and beyond under AMI
  - Associates all Reserved Parameters and Model_Types with directions (Tx, Rx)
    - Most Serdes buffers are Tx-only or Rx-only
    - DDR4 DQ buffers are I/O (bi-directional)
  - Enables explicit information to be used by EDA tools about the direction for a given I/O buffer in a particular simulation
  - Adds "Direction" descriptor to all Reserved Parameters
  - Adds "Executable_Tx" and "Executable_Rx" subparameters to the [Algorithmic Model] keyword

Traditional IBIS Improvements

- Overclocking and delay
  - [Initial Delay] defines the explicit amount of time, before transitions, embedded in the V-t and any I-t tables
  - Supported for both single-Model and [Driver Schedule] structures
- Package and Power Pin Modeling
  - Diagonal package matrix values are enforced positive-only, and more mathematical assumptions are documented
  - More rigorous rules are defined for EDA tool interpretation of partial Package Models which do not cover the entire [Pin] list
  - Added support for [Merged Pins] where a single pin covers the parasitics of multiple physical pins

Feedback is Welcome

- Anyone may submit IBIS specification change proposals (BIRDs – Buffer Issue Resolution Documents)
  - This is the primary mechanism for making IBIS changes
  - http://ibis.org/birds/
- Bugs and enhancement requests may also be proposed
  - The BUG report covers both
  - http://ibis.org/bugs/ibischk
- The IBIS Open Forum and Task Group teleconferences welcome public participation

Your feedback is vital for keeping IBIS relevant and useful to the industry!

References

- IBIS Web site: www.ibis.org
  - Links to Task Groups available there
- Specifications
  - IBIS 6.1: www.ibis.org/ver6.1/
  - IBISCHK6 parser (6.1 in progress): www.ibis.org/ibischk6/
  - Touchstone: www.ibis.org/touchstone_ver2.0/
- Summit Presentations
  - www.ibis.org/summits/
- IBIS 4.0 Cookbook
  - www.ibis.org/cookbook/
- Training
  - www.ibis.org/training/

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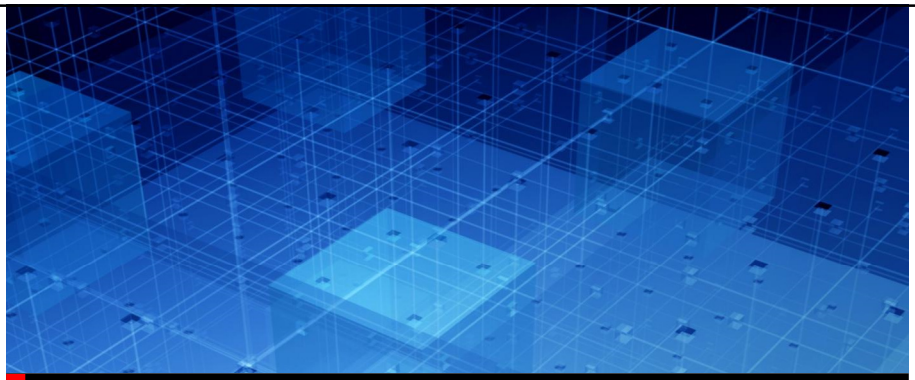


Enabling Full Power-aware Bus Simulation with Non-IBIS Device Model - A Kit using IBIS [External Model]

Skipper Liang
Cadence Design Systems
Asian IBIS Summit, Shanghai, China
November 9, 2015

cadence

Agenda

- Introduction
- Approach 1: Using IBIS [External Model]
- Approach 2: Using an IBIS model to drive the SPICE netlist
- Solution: A dummy IBIS model using [External Model] and additional circuit
- Summary

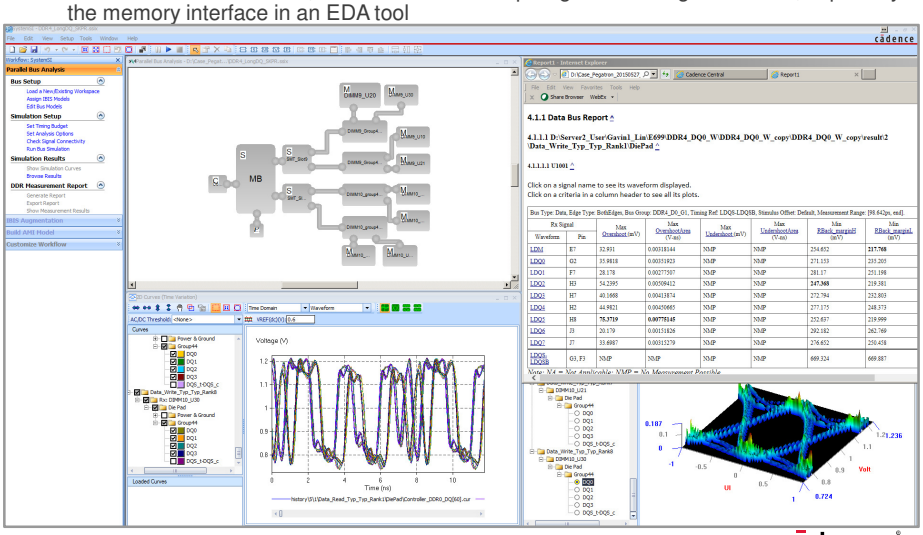
cadence

Introduction

cadence

Bus simulation

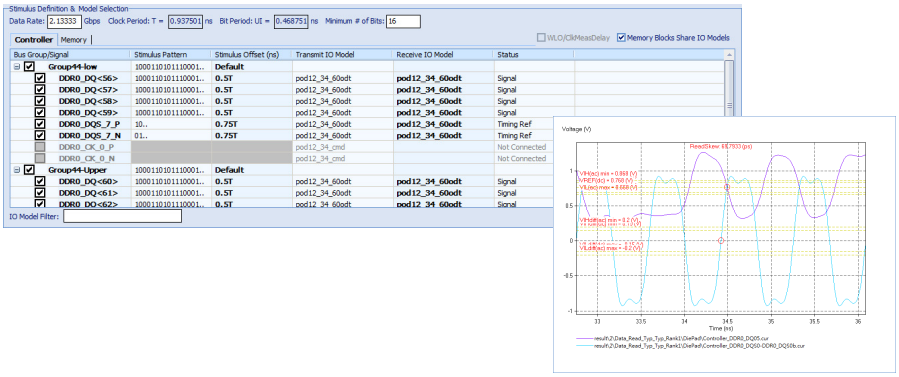
- It refers to an automatic process
  - which includes simulation, measurement and report generation against a Bus, especially the memory interface in an EDA tool



cadence

IBIS model

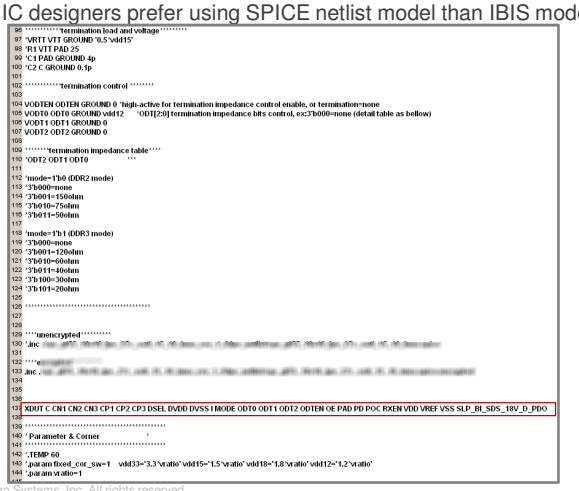
- Intrinsic format - the description of [Pin], [Diff Pin] and [Model Selector]
- IBIS makes Bus simulation possible in an EDA tool
  - easy to assign data groups with individual timing reference
  - Easy to change models and settings in batch mode



cadence

SPICE netlist

- Maximum freedom in the circuit format but hard for Bus simulation to be implemented
- Has detailed characteristics of circuits which can't be fully described by IBIS model
  - Some IC designers prefer using SPICE netlist model than IBIS model



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IBIS External Model

- Allow a spice netlist to be called by an IBIS model, which means:

- With IBIS format, easy for Bus-Sim to be implemented
- Include detailed characteristics of circuit

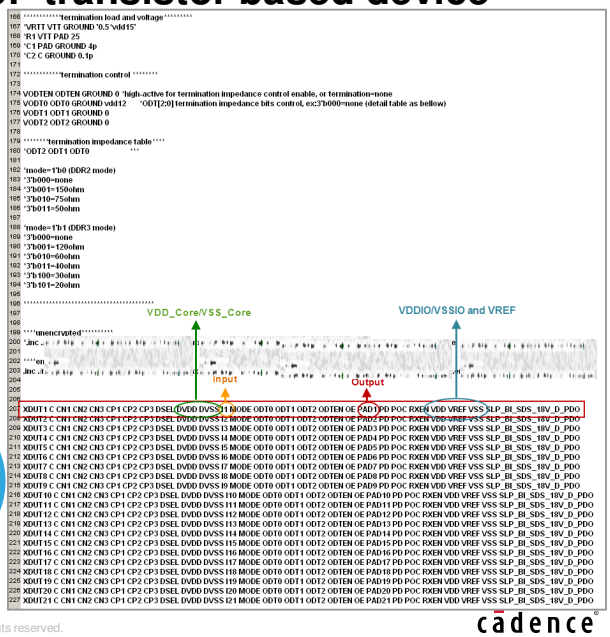
```
[External Model]
Language SPICE
|
| Corner corner_name  file_name        circuit_name (.subckt name)
Corner    Typ          buffer_typ.spi  buffer_io_typ
Corner    Min          buffer_min.spi  buffer_io_min
Corner    Max          buffer_max.spi  buffer_io_max
|
| Parameters - Not supported in SPICE
|
| Ports List of port names (in same order as in SPICE)
Ports A_signal my_drive my_enable my_receive my_ref
Ports A_puref A_pdref A_pcref A_gcref A_extref
|
| D_to_A d_port   port1     port2     vlow vhigh trise tfall corner_name
D_to_A   D_drive  my_drive   my_ref    0.0  3.3  0.5n  0.3n   Typ
D_to_A   D_enable my_enable  A_gcref   0.0  3.3  0.5n  0.3n   Typ
|
| A_to_D d_port    port1       port2       vlow  vhigh  corner_name
A_to_D   D_receive  my_receive  my_ref  0.8   2.0    Typ
|
| Note: A_signal might also be used instead of a user-defined interface port
| for measurements taken at the die pads
|
[End External Model]
```


cadence

SPICE netlist of transistor based device model

- An example of SPICE netlist for a transistor based device model
- For power supply, there are:
  - VDD_Core/Vss_Core
  - VDDIO/VSSIO
  - VREF

Question: if we can use IBIS [External Model] to call this netlist to execute a fully power-aware Bus-Simulation?



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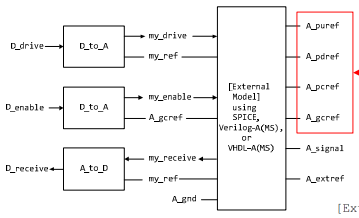
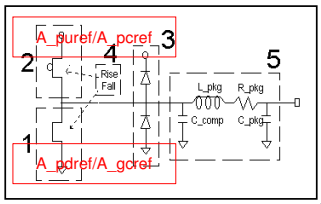
Approach 1: using IBIS [External Model]

cadence

Multi-power nets in [External Model] Section?





- Same as a normal IBIS model, an IBIS model with [External Model] can connect to only one PWR / GND pair, usually the VDDIO and VSSIO.
- What will we do for the following:
  1. VDD_Core/Vss_Core
     ➡ **A_puref, A_pdref, A_pcref, A_gcref**
  2. VDDIO/VSSIO
     ➡ ?
  3. VREF
     ➡ ?

```
[External Model]
Language SPICE
|
| Corner corner_name  file_name       circuit_name (.subckt name)
Corner    Typ          buffer_typ.spi  buffer_io_typ
Corner    Min          buffer_min.spi  buffer_io_min
Corner    Max          buffer_max.spi  buffer_io_max
|
| Parameters - Not supported in SPICE
|
| Ports List of port names (in same order as in SPICE)
Ports A_signal my_drive my_enable my_receive my_ref
Ports A_puref A_pdref A_pcref A_gcref A_extref
|
| D_to_A d_port   port1     port2     vlow vhigh trise tfall corner_name
D_to_A   D_drive  my_drive   my_ref   0.0  3.3  0.5n  0.3n   Typ
D_to_A   D_enable my_enable  A_gcref  0.0  3.3  0.5n  0.3n   Typ
|
| A_to_D d_port    port1       port2       vlow  vhigh  corner_name
A_to_D   D_receive  my_receive  my_ref  0.8   2.0    Typ
|
| Note: A_signal might also be used instead of a user-defined interface port
| for measurements taken at the die pads
|
[End External Model]
```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Multi-power nets in [External Model] Section? (Cont')

(spice_io.ckt)

```
.subckt se_drv15_odtoff DVDD DVSS PAD I OE nd_out_of_in

.param vdd15='1.5'
.param vdd12='1.2'
VREF VREF GROUND '0.5*vdd15' *reference voltage for the SSTL receiver @padring

.protect
.inc ./lib/design_io_pad.inc
.unprotect

*VDVDD DVDD GROUND vdd15       *power supply voltage
*VDVSS DVSS GROUND 0
VDDA12 VDD GROUND vdd12      *core power supply voltage
VSSA12 VSS GROUND 0

VMODE MODE GROUND vdd12       *mode select signal
            *1'b0 selects DDR2 mode
            *1'b1 selects DDR3 mode
VPOC POC GROUND 0     *power on control @padring

.connect OE RXEN


VPD PD GROUND vdd12      *active-high for receiver power down signal

VDSEL DSEL GROUND vdd12      *DDR2 drive slect signal
            *1'b0 60% drive (classII)
            *1'b1 full drive (classI)

**********termination control ********

VODTEN ODTEN GROUND 0 *high-active for termination impedance control enable, or termination=none
VODT0 ODT0 GROUND vdd12      *ODT[2:0] termination impedance bits control, ex:3'b000=none (detail table as bellow)
VODT1 ODT1 GROUND 0
VODT2 ODT2 GROUND 0
```

```
|*****************************************************************
|                                        Model se_drv15_odtoff
|*****************************************************************
|
[Model] se_drv15_odtoff
Model_type I/O
Polarity        Non-Inverting
Enable          Active-High
[Voltage Range]         1.500V              1.425V              1.575V
[Ramp]
| variable        typ                 min                 max
dV/dt_r 0.720/0.006n        0.720/0.006n        0.720/0.006n
dV/dt_f 0.720/0.006n        0.720/0.006n        0.720/0.006n
R_load = 50.000
|
[External Model]
Language SPICE
|
| Corner  corner_name  file_name  circuit_name (.subckt name)
Corner    Typ           spice_io.ckt          se_drv15_odtoff
Corner    Min           spice_io_min.ckt        se_drv15_odtoff_min
Corner    Max           spice_io_max.ckt        se_drv15_odtoff_max
|
| Ports List of port names (in same order as in SPICE)
Ports A_pureF A_pdref A_signal my_drive my_enable my_receive
|
| D_to_A d_port port1 port2 vlow vhigh trise tfall corner_name
D_to_A D_drive my_drive A_pdref 0.0 1.2 10p 10p Typ
D_to_A D_drive my_drive A_pdref 0.0 1.2 10p 10p Min
D_to_A D_drive my_drive A_pdref 0.0 1.2 10p 10p Max
D_to_A D_enable my_enable A_pdref 0.0 1.2 10p 10p Typ
D_to_A D_enable my_enable A_pdref 0.0 1.2 10p 10p Min
D_to_A D_enable my_enable A_pdref 0.0 1.2 10p 10p Max
| A_to_D d_port port1 port2 vlow vhigh corner_name
A_to_D D_receive my_receive A_pdref 0.0 1.0 Typ
A_to_D D_receive my_receive A_pdref 0.0 1.0 Min
A_to_D D_receive my_receive A_pdref 0.0 1.0 Max
|
[End External Model]
```

- Except the VDDIO and VSSIO, which will be connected to real power delivery network routing, the other PWR and GND will be connected to a "**IDEAL**" voltage source.

  ➡ **Not Fully Power-Aware**

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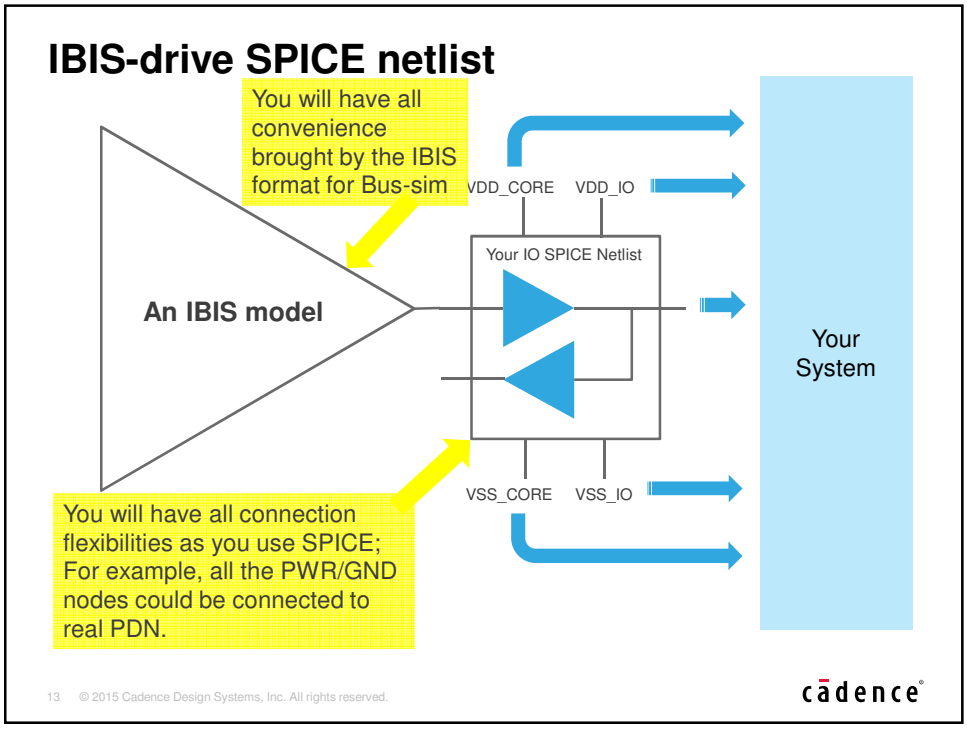
IBIS-drive SPICE netlist
You will have all convenience brought by the IBIS format for Bus-sim
An IBIS model
VDD_CORE
VDD_IO
Your IO SPICE Netlist
VSS_CORE
VSS_IO
Your System
You will have all connection flexibilities as you use SPICE; For example, all the PWR/GND nodes could be connected to real PDN.
13
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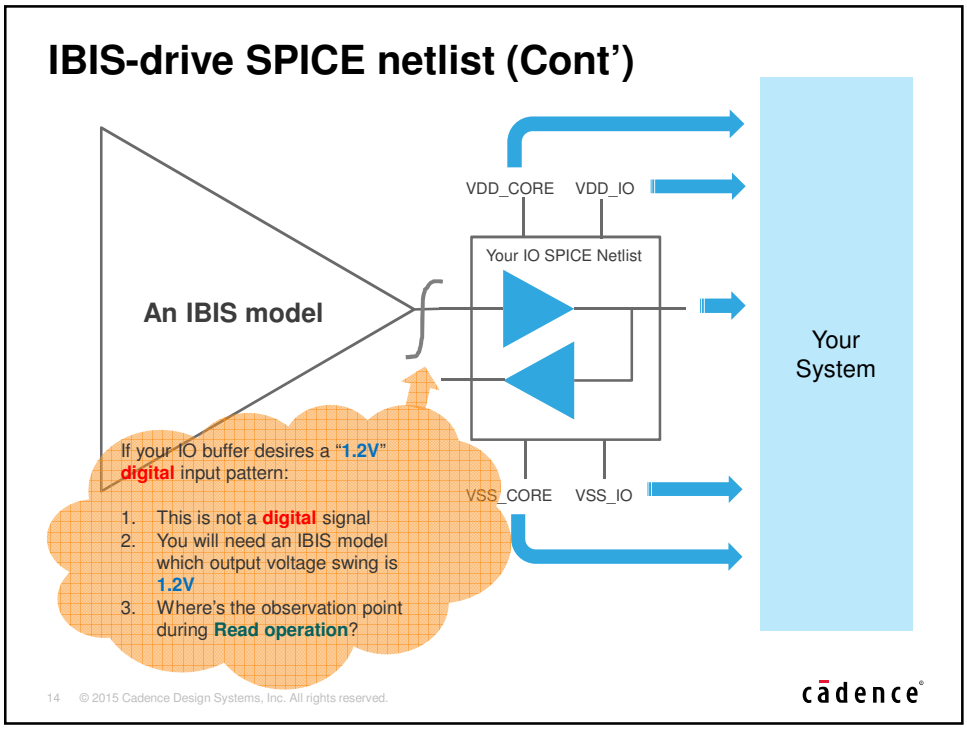
IBIS-drive SPICE netlist (Cont')
An IBIS model
VDD_CORE
VDD_IO
Your IO SPICE Netlist
VSS_CORE
VSS_IO
Your System
If your IO buffer desires a "1.2V" digital input pattern:
1. This is not a digital signal
2. You will need an IBIS model which output voltage swing is 1.2V
3. Where's the observation point during Read operation?
14
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Solution: A dummy IBIS model using [External Model] and additional circuits

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A simple kit

For "Write": IBIS which calls a short circuit to pass through digital data using [External Model]

R=1e-15

For "Read": IBIS which calls an open circuit to probe analog received data using [External Model]

R=1e+15

```
1       dq0                                     Dummy_IO
2       dq1                                     Dummy_IO
3       dq2                                     Dummy_IO
4       dq3                                     Dummy_IO
5       dq4                                     Dummy_IO
6       dq5                                     Dummy_IO
7       dq6                                     Dummy_IO
8       dq7                                     Dummy_IO
9       dq8                                     Dummy_IO
10      dq9                                     Dummy_IO
11      dq10                                    Dummy_IO
12      dq11                                    Dummy_IO
13      dq12                                    Dummy_IO
14      dq13                                    Dummy_IO
15      dq14                                    Dummy_IO
16      dq15                                    Dummy_IO
17      dm0                                     Dummy_IO
18      dm1                                     Dummy_IO
19      dqs0p                                   Dummy_IO
20      dqs0n                                   Dummy_IO
21      dqs1p                                   Dummy_IO
22      dqs1n                                   Dummy_IO
23      VSS0                                    GND
24      VDDQ0                                   POWER
|
[Diff pin]  inv_pin  vdiff   tdelay_typ   tdelay_min   tdelay_max
|
19        20      100.000mV  0.0s
21        22      100.000mV  0.0s
|*********************Component Bus Definitions ************************
|
[Model Selector] Dummy_IO
Write  single end driver
Read  single end Receiver
|
|*************************************************************
|                                        Model Write
|*************************************************************
|
[Model] Write
Model_type I/O
Polarity       Non-Inverting
Enable         Active-High
[Voltage Range]         1.500V              1.425V              1.575V
[Ramp]
| variable       typ                 min                 max
dV/dt_r 0.120/0.001n        0.120/0.001n        0.120/0.001n
dV/dt_f 0.120/0.001n        0.120/0.001n        0.120/0.001n
R_load = 50.000
```

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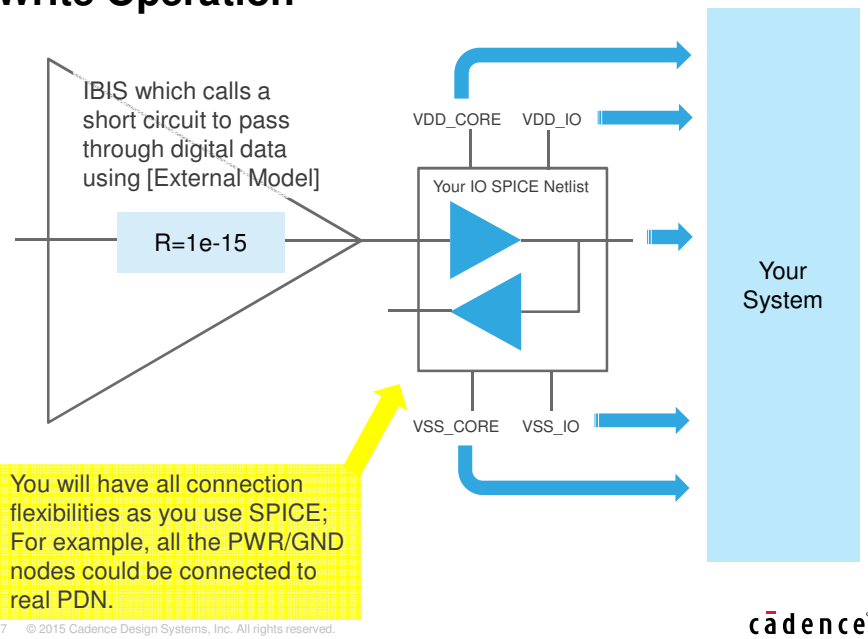
Write Operation



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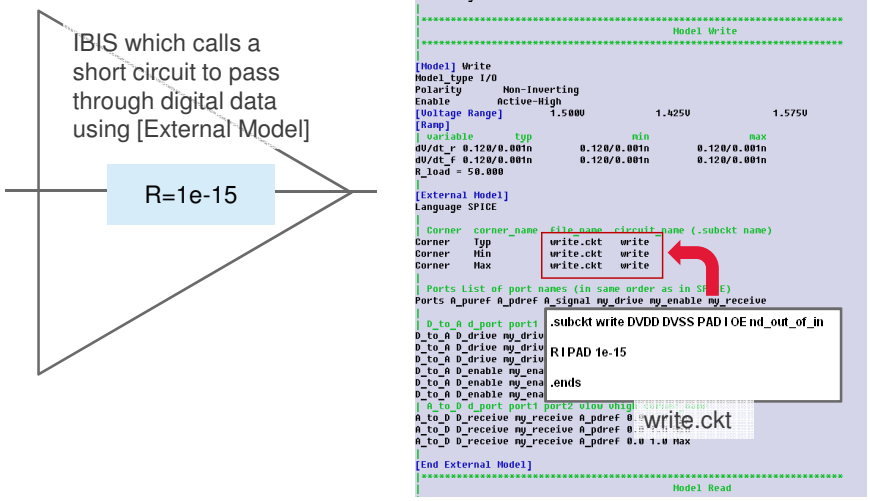
Write Operation (cont')



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Write Operation (cont')

- In a bus simulation, user can easily switch the model of the Controller's buffer to "Write"

Controller | Memory

Bus Group/Signal	Stimulus Pattern	Stimulus Offset (ns)	Transmit IO Model	Status
DATA0	1000110101110...	Default		
dm0			Write	Not Connected
dq0	1000110101110...	0.5T	Write	Signal
dq1	1000110101110...	0.5T	Write	Signal
dq2	1000110101110...	0.5T	Write	Signal
dq3			Write	Not Connected
dq4			Write	Not Connected
dq5			Write	Not Connected
dq6			Write	Not Connected
dq7			Write	Not Connected
dqs0p	10..	0.75T	Write	Timing Ref
dqs0n	01..	0.75T	Write	Timing Ref
DATA1				

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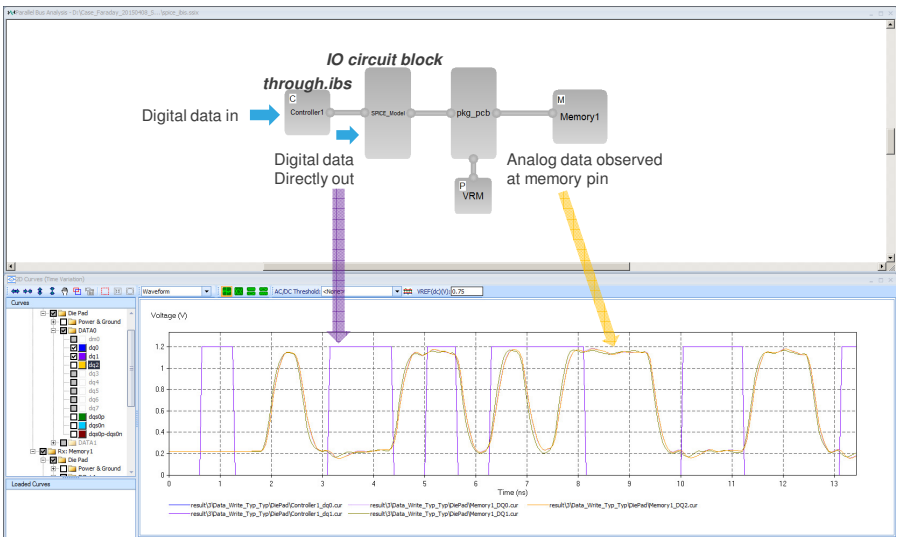
Write Operation (cont')



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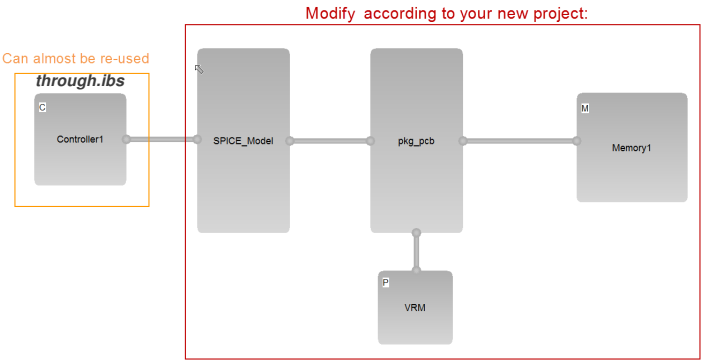
Write Operation (cont')

For a new project, the kit is re-usable with little modification



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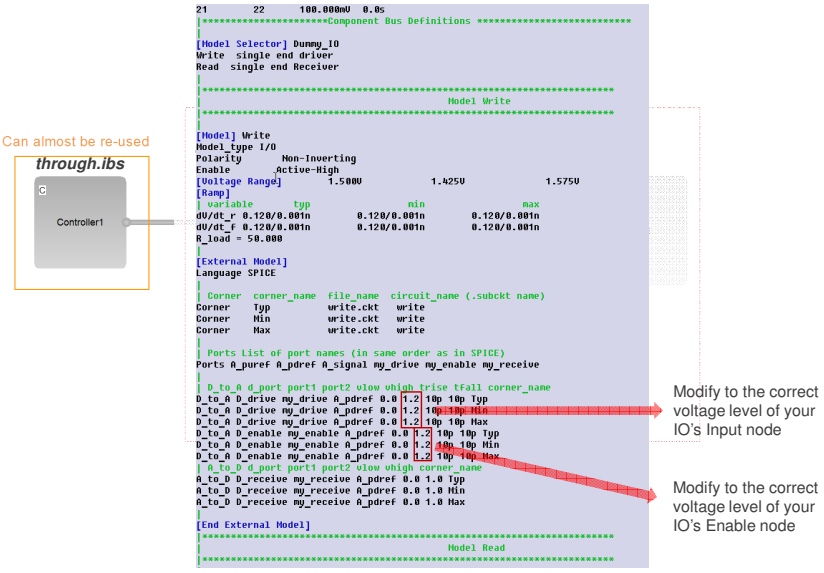
Write Operation (cont')

For a new project, the kit is re-usable with little modification



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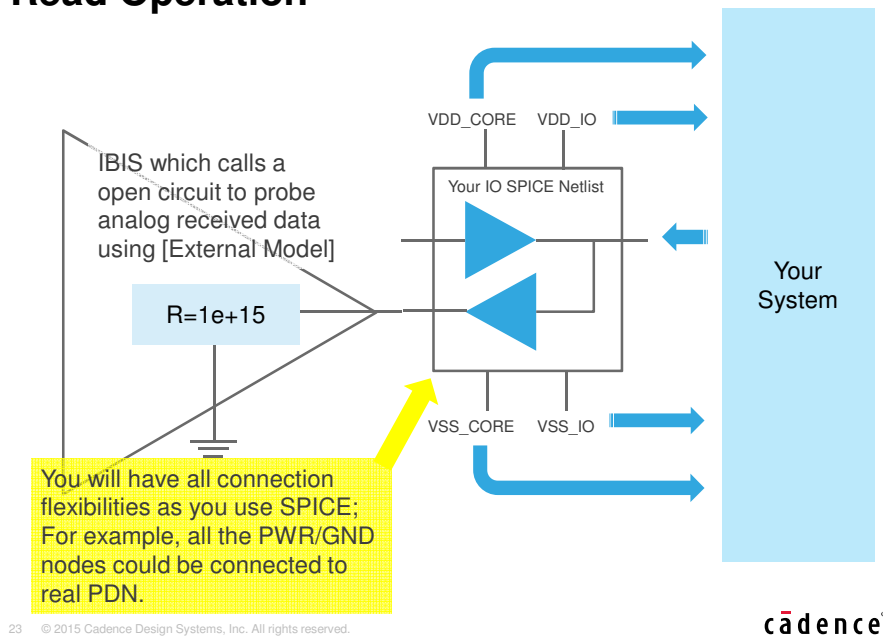
Read Operation



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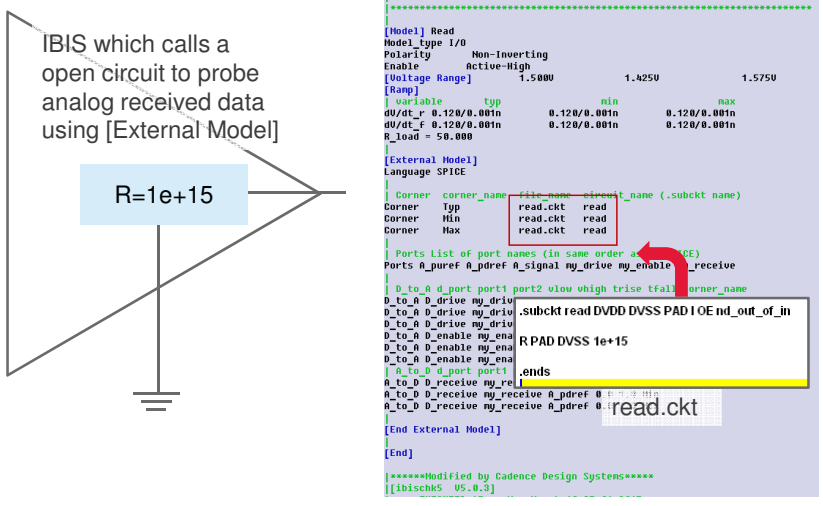
Read Operation (cont')



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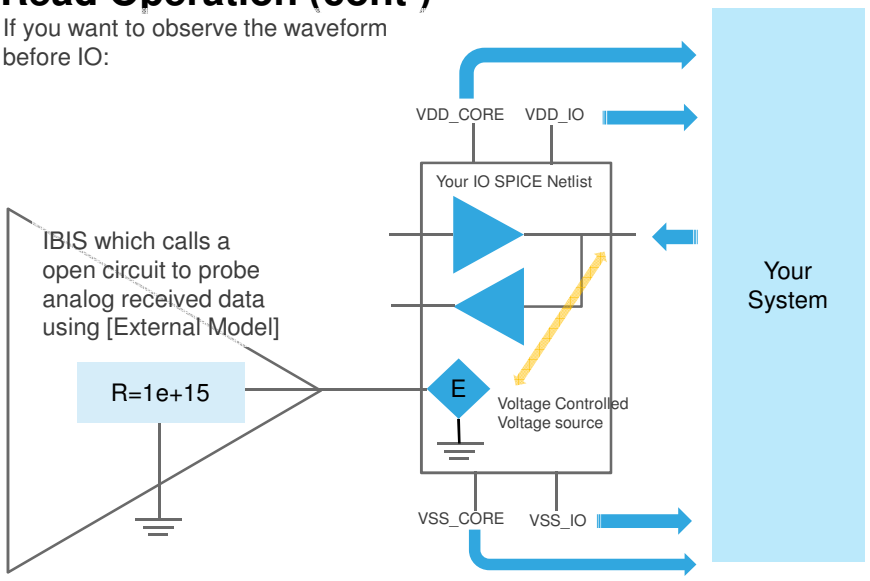
Read Operation (cont')

If you want to observe the waveform before IO:



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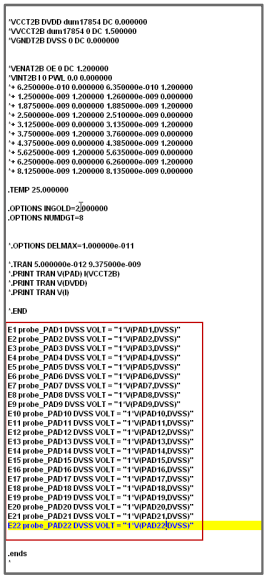
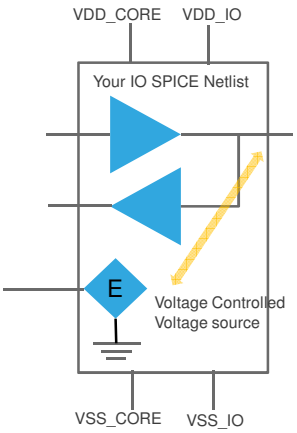
Read Operation (cont')

- You will need to modify the netlist of the IO circuit block by adding some "Voltage Controlled Voltage sources" which is controlled by the voltage on IO circuit block's PAD.
- Connect the dummy controller's output pad to these "Voltage Controlled Voltage sources"



```
'VCCT2B DVDD dum17854 DC 0.000000
'VVCCT2B dum17854 0 DC 1.500000
'VGNDT2B DVSS 0 DC 0.000000

'VENAT2B OE 0 DC 1.200000
'VINT2B I 0 PWL 0.0 0.000000
'+ 6.250000e-010 0.000000 6.350000e-010 1.200000
'+ 1.250000e-009 1.200000 1.260000e-009 0.000000
'+ 1.875000e-009 0.000000 1.885000e-009 1.200000
'+ 2.500000e-009 1.200000 2.510000e-009 0.000000
'+ 3.125000e-009 0.000000 3.135000e-009 1.200000
'+ 3.750000e-009 1.200000 3.760000e-009 0.000000
'+ 4.375000e-009 0.000000 4.385000e-009 1.200000
'+ 5.625000e-009 1.200000 5.635000e-009 0.000000
'+ 6.250000e-009 0.000000 6.260000e-009 1.200000
'+ 8.125000e-009 1.200000 8.135000e-009 0.000000

.TEMP 25.000000

.OPTIONS INGOLD=2000000
.OPTIONS NUMDGT=8

'.OPTIONS DELMAX=1.000000e-011

'.TRAN 5.000000e-012 9.375000e-009
'.PRINT TRAN V(PAD) I(VCCT2B)
'.PRINT TRAN V(DVDD)
'.PRINT TRAN V(I)

'.END

E1 probe_PAD1 DVSS VOLT = "1*V(PAD1,DVSS)"
E2 probe_PAD2 DVSS VOLT = "1*V(PAD2,DVSS)"
E3 probe_PAD3 DVSS VOLT = "1*V(PAD3,DVSS)"
E4 probe_PAD4 DVSS VOLT = "1*V(PAD4,DVSS)"
E5 probe_PAD5 DVSS VOLT = "1*V(PAD5,DVSS)"
E6 probe_PAD6 DVSS VOLT = "1*V(PAD6,DVSS)"
E7 probe_PAD7 DVSS VOLT = "1*V(PAD7,DVSS)"
E8 probe_PAD8 DVSS VOLT = "1*V(PAD8,DVSS)"
E9 probe_PAD9 DVSS VOLT = "1*V(PAD9,DVSS)"
E10 probe_PAD10 DVSS VOLT = "1*V(PAD10,DVSS)"
E11 probe_PAD11 DVSS VOLT = "1*V(PAD11,DVSS)"
E12 probe_PAD12 DVSS VOLT = "1*V(PAD12,DVSS)"
E13 probe_PAD13 DVSS VOLT = "1*V(PAD13,DVSS)"
E14 probe_PAD14 DVSS VOLT = "1*V(PAD14,DVSS)"
E15 probe_PAD15 DVSS VOLT = "1*V(PAD15,DVSS)"
E16 probe_PAD16 DVSS VOLT = "1*V(PAD16,DVSS)"
E17 probe_PAD17 DVSS VOLT = "1*V(PAD17,DVSS)"
E18 probe_PAD18 DVSS VOLT = "1*V(PAD18,DVSS)"
E19 probe_PAD19 DVSS VOLT = "1*V(PAD19,DVSS)"
E20 probe_PAD20 DVSS VOLT = "1*V(PAD20,DVSS)"
E21 probe_PAD21 DVSS VOLT = "1*V(PAD21,DVSS)"
E22 probe_PAD22 DVSS VOLT = "1*V(PAD22,DVSS)"

.ends
```

spice_io_read.ckt



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Read Operation (cont')

- In a bus simulation, user can easily switch the model of the Controller's buffer to "Read"

Controller | Memory

Bus Group/Signal	Receive IO Model	Status
DATA0		
dm0	Read	Not Connected
dq0	Read	Signal
dq1	Read	Signal
dq2	Read	Signal
dq3	Read	Not Connected
dq4	Read	Not Connected
dq5	Read	Not Connected
dq6	Read	Not Connected
dq7	Read	Not Connected
dqs0p	Read	Timing Ref
dqs0n	Read	Timing Ref
DATA1		

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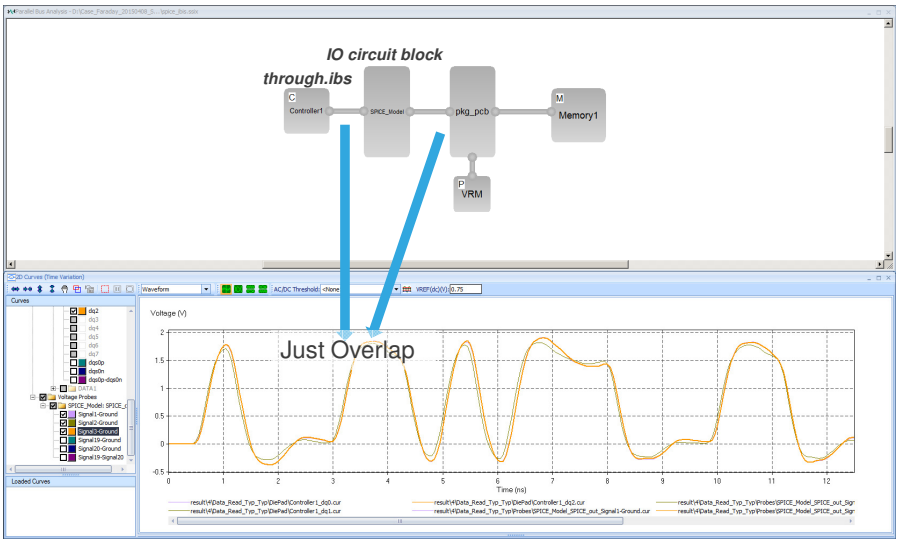
Read Operation (cont')



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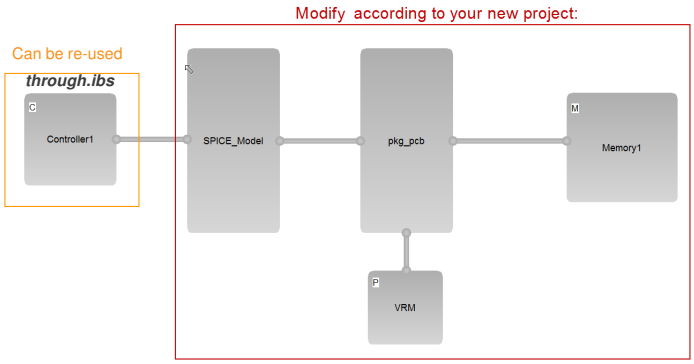
Read Operation (cont')

For a new project, the kit is re-usable with little modification



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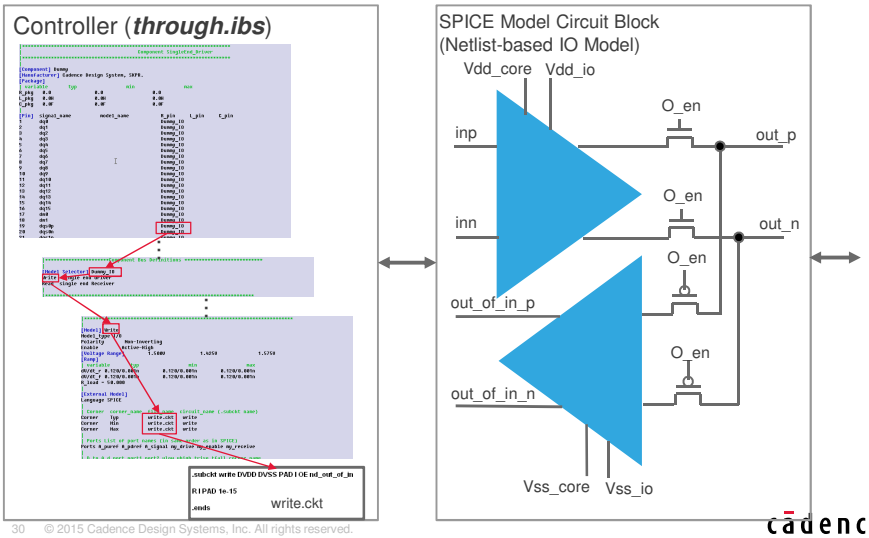
Differential Buffer

No matter true or pseudo, you can use the same kit without any modification because:
(take "**write operation**" as an example)



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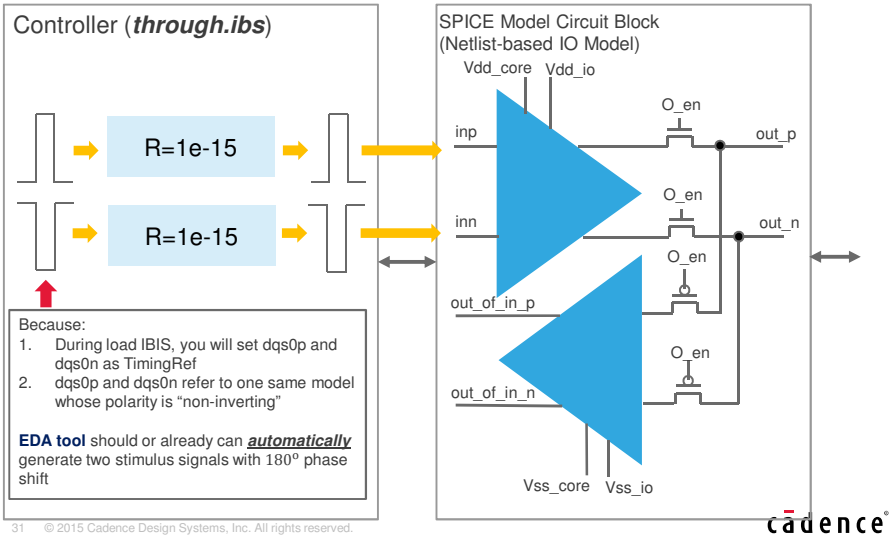
Differential Buffer (cont')

For Truly Differential Buffer type1:



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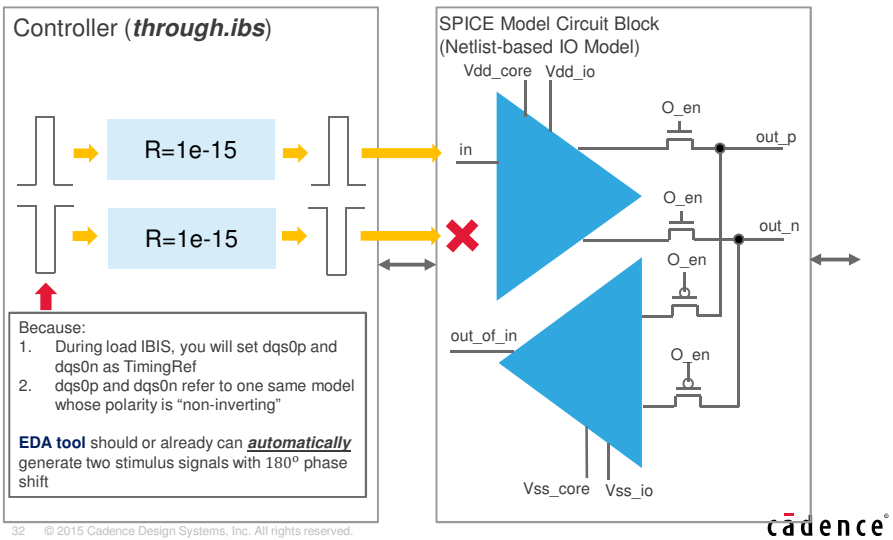
Differential Buffer (cont')

For Truly Differential Buffer type2:



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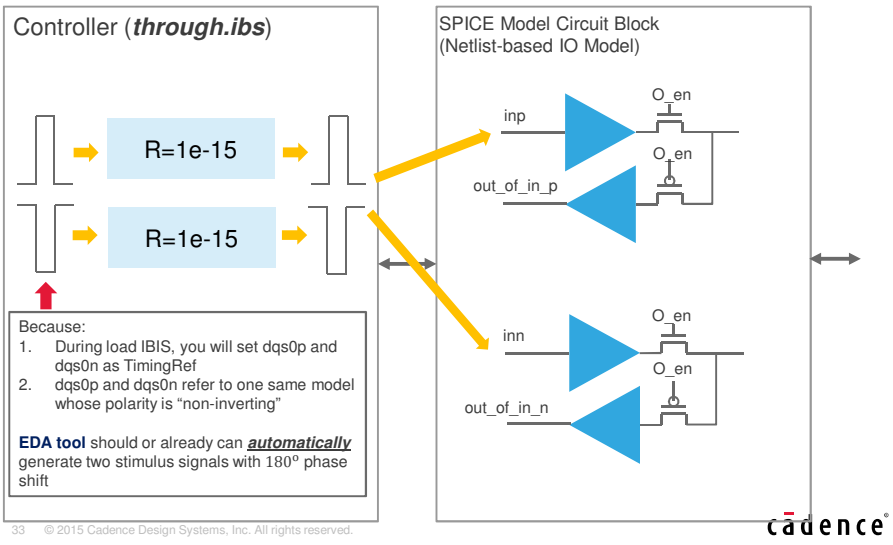
Differential Buffer (cont')

For Pseudo Differential Buffer:



Because:
1. During load IBIS, you will set dqs0p and dqs0n as TimingRef
2. dqs0p and dqs0n refer to one same model whose polarity is "non-inverting"

EDA tool should or already can ***automatically*** generate two stimulus signals with 180° phase shift

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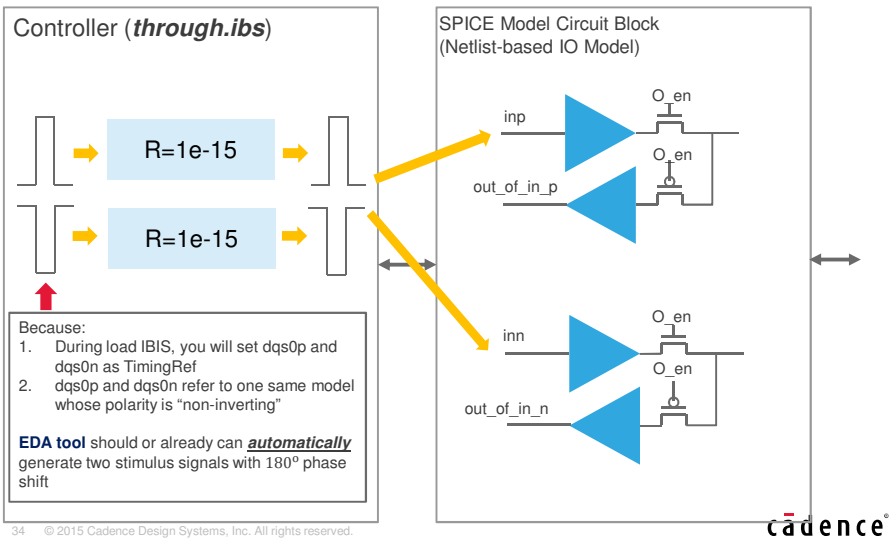
Differential Buffer (cont')

For Pseudo Differential Buffer:



Because:
1. During load IBIS, you will set dqs0p and dqs0n as TimingRef
2. dqs0p and dqs0n refer to one same model whose polarity is "non-inverting"

EDA tool should or already can ***automatically*** generate two stimulus signals with 180° phase shift

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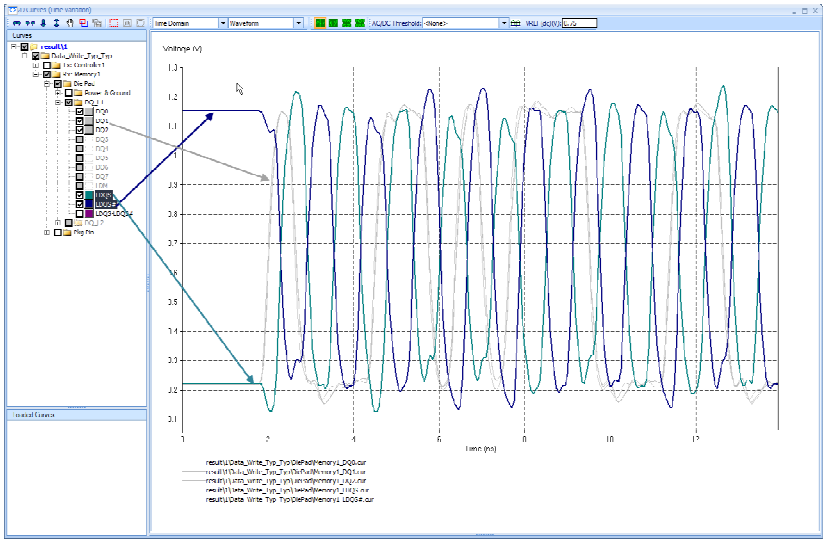
Differential Buffer (cont')

An example with method2: 3 DQ and 1 pair of DQS



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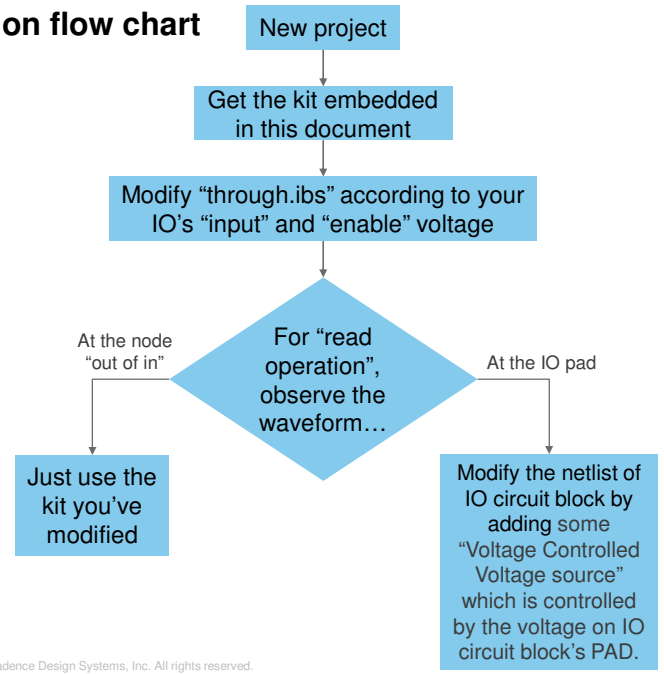
Solution flow chart



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Summary

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Notes

- For analysis of SSN
  - With the full flexibilities as using SPICE, this method allows user to do **a power-aware SSN analysis between multiple signals and multiple PDNs**, such as VDD_Core/VSS_Core, VDDIO/VSSIO, VTT and VREF together at the same time.
- Model modification and change of topology
  - This method requires the change of topology - inserting a Spice block but the wrapping .sp file according to the description in [External Model] is not necessary since it's ready for use in the kit - **easy for re-using** this kit in a new project of a new IO.
- Read Operation
  - As this method requires the change of topology when building topology, during the analysis of read operation, user will need to modify **the netlist of the IO circuit block** by adding some "Voltage Controlled Voltage source" which is controlled by the voltage on IO circuit block's PAD.
- Differential Buffer
  - This method can use the same kit without additional modification for both single-end and differential buffer, **no matter it's truly or pseudo**.

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References

- IBIS specification (v6.1)
  http://www.ibis.org/ver6.1/ver6_1.pdf

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ERICSSON

A PRACTICAL DOE APPLICATION IN STATISTICAL SI ANALYSIS USING IBIS & HOW CAN WE MAKE IBIS WORK BEYOND BEST CASE/WORST CASE?

ASIAN IBIS SUMMIT NOVEMBER 9, 2015 SHANGHAI, CHINA

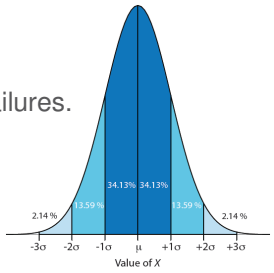
Authors:
Feng Shi, Anders Ekholm, Zilwan Mahmod & David Zhang.

AGENDA

- IBIS & Statistical analysis
- DOE as a statistical methodology
- Practical DDR3/DDR4 Topology problem solved by DOE
- How can we extend IBIS to support confidence interval analysis.
- Suggestion to enhance IBIS typ, min, max corners with distribution data.
- Conclusion

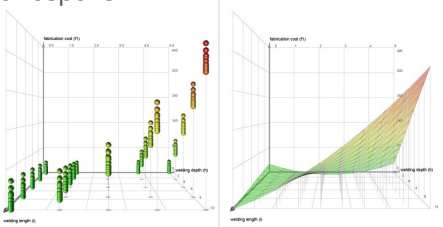
IBIS & STATISTICAL ANALYSIS

- IBIS based SI analysis uses:
  - Behavioral buffer models. typ, min, max (BC/WC)
  - Trace modeling of topology BC/WC
  - Via modeling BC/WC
- Best Case / Worst case analysis assumes:
  - 100% confidence interval. Every produced individual works.
- Statistical SI analysis predicts:
  - Defects at a given confidence interval.
  - Help manage overdesign and possible BC/WC failures.



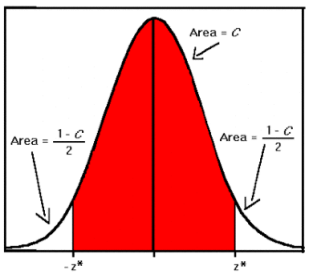
DOE AS A STATISTICAL METHODOLOGY

- DOE Design Of Experiments will fit a model to our solutions space (often used is a RSM Response Surface Model)
- Uses much fewer simulation than sweep analysis or Monte Carlo analysis.
- Catches cross term interaction missed by OFAT analysis.
  - (OFAT, One Factor At a Time)
- RSM used to predict the fitted part of the solutions space and to give Confidence Intervals for the predicted respons.



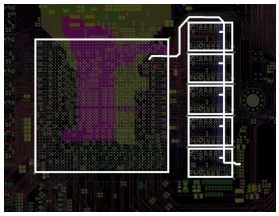
PRACTICAL DDR TOPOLOGY PROBLEM SOLVED BY DOE

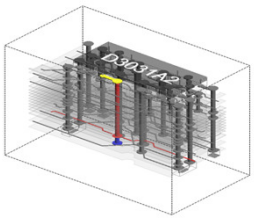
- Problem of ringing in a high speed DDR3/DDR4 address/command/control bus in memory down solutions with thick PCB's >1mm.
- Find an optimal topology that solves the problem with a given confidence e.g. 95%

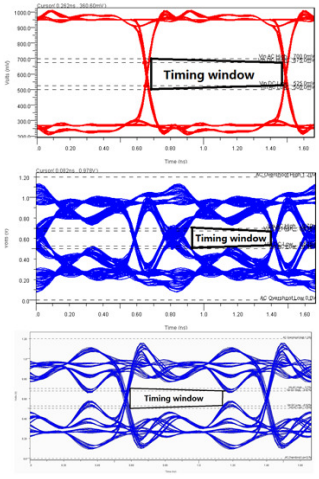


PRACTICAL DDR TOPOLOGY PROBLEM SOLVED BY DOE

- DDR3/DDR4 address/command/control bus topology
  - Flyby? Daisy-chain. →Reflection
  - Thick PCB's >1mm. →Ringback





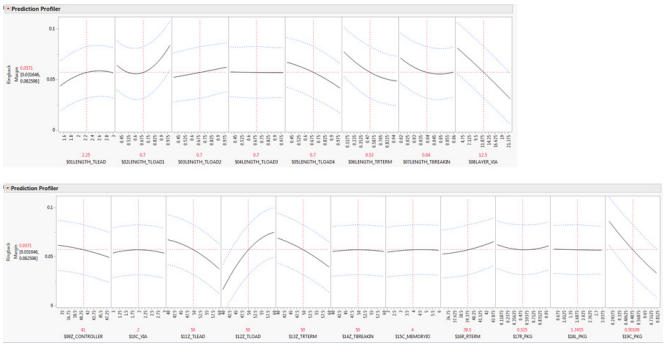


PRACTICAL DDR TOPOLOGY PROBLEM SOLVED BY DOE

Design Parameter	Factor	Factor Type	Min	Typ	Max	Analysis Type
Length of lead Tline	01Length_TLead	Continuous	1.5inch	2.25inch	3 inch	Design
Length of first load Tline	02Length_TLoad1	Continuous	0.4inch	0.7inch	1 inch	Design
Length of second load Tline	03Length_TLoad2	Continuous	0.4 inch	0.7inch	1 inch	Design
Length of third load Tline	04Length_TLoad3	Continuous	0.4 inch	0.7inch	1 inch	Design
Length of forth load Tline	05Length_TLoad4	Continuous	0.4 inch	0.7inch	1 inch	Design
Length of Tline to the termination resistor	06Length_TRterm	Continuous	0.06 inch	0.53inch	1 inch	Design
Length of memory fanout Tline	07Length_TBreakin	Continuous	0.02 inch	0.04inch	0.06 inch	Design
Routing layer/ Via barrel length	08Layer_Via	Categorical	3, 5, 7, 18, 20, 22 layer			Design
Driver impedance of controller	09Z_Controller	Categorical	34ohm	40 ohm	48 ohm	Design
Via anti-pad size	10C_Via	Categorical	1=hiC	2=typC	3=lowC	Design
Impedance of lead Tline	11Z_TLead	Categorical	40 ohm	50 ohm	60 ohm	Design& Manufacturing
Impedance of load Tline	12Z_TLoad	Categorical	40 ohm	50 ohm	60 ohm	Design& Manufacturing
Impedance of Tline to the termination resistor	13Z_TRterm	Categorical	40 ohm	50 ohm	60 ohm	Design& Manufacturing
Impedance of memory fanout Tline	14Z_TBreakin	Categorical	40 ohm	50 ohm	60 ohm	Design& Manufacturing
Input capacitance of memory IO buffer	15C_MemoryIO	Categorical	2=0.2	4=0.4	6=0.6	Manufacturing
Termination resistor	16R_Rterm	Continuous	36 ohm	39 ohm	43 ohm	Design
Packaging resistance of_memory	17R_Pkg	Continuous	0.05 ohm	0.525 ohm	1 ohm	Manufacturing
Packaging inductance of_memory	18L_Pkg	Continuous	0.5nH	1.75nH	3nH	Manufacturing
Packaging capacitance of_memory	19C_Pkg	Continuous	0.2pF	0.5pF	0.8pF	Manufacturing

PRACTICAL DDR TOPOLOGY PROBLEM SOLVED BY DOE

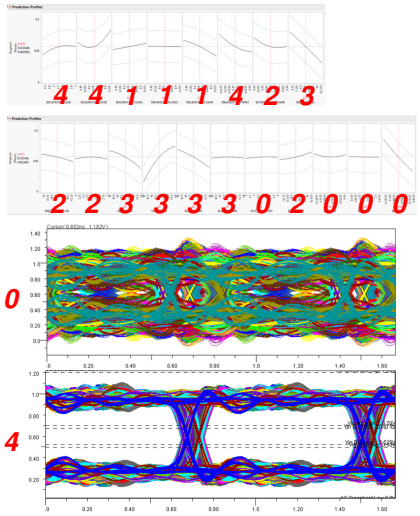
- Prediction Profiler

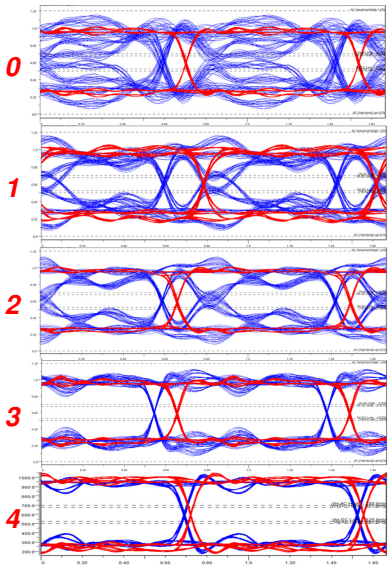


  - Confidence interval ------> Quality
  - Slope ------> Influence /Importance
  - Vertical red line ------> “What if ” analysis & Interactions
  - Desirability function ------> Optimization

PRACTICAL DDR TOPOLOGY PROBLEM SOLVED BY DOE

- DOE Optimization

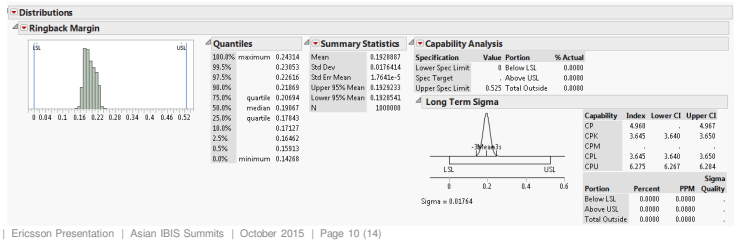




PRACTICAL DDR TOPOLOGY PROBLEM SOLVED BY DOE

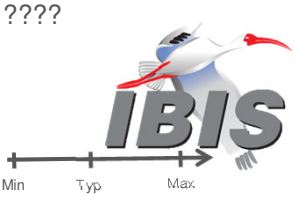
- DPM (Defects per Million)
  - Equation Simulator to evaluate the response equation at millions of conditions.

  - Realistic predicted yield plots obtained in seconds .



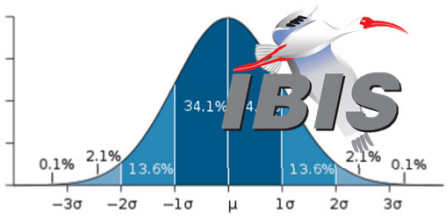
HOW CAN WE EXTEND IBIS TO SUPPORT CONFIDENCE INTERVAL ANALYSIS.

- IBIS currently and traditionally uses a typ, min, max parameter definition.
- This is based on a Best/Worst case scenario analysis. E.g. 100% confidence.
- Best/Worst case analysis has served us well during the years and still does in some cases, however more and more cases will not reach design closure using Best/Worst case analysis.
- When it does not reach design closure how will we know how many of our produced units will fail ????



ADD AN OPTION TO IBIS TYP, MIN, MAX CORNERS TO USE DISTRIBUTION DATA AS A PARAMETER DEFINITION.

- If we add an option to IBIS to support distribution data for parameters as an average/mean and a variation/sigma.
- If we feel we can not assume a standard distribution we could even add support for other distributions.
- These parameters could be used in DOE analysis scenarios and could help us predict confidence intervals for our products as well as DPM (Defect Per million) predictions.



CONCLUSIONS.

- Our design work is moving beyond Best case, Worst case analysis.
- We need to start working on an infrastructure both in modeling and tool support for statistical analysis.
- Many of us EE's need to go back to our statistics books and review statistical analysis.
- We need to secure that we can get the correct information from IC and PCB vendors on parameter distributions.
- SI/PI statistical analysis is the next step to secure our product quality.

ERICSSON

IBIS Interconnect BIRD Update

Walter Katz
Signal Integrity Software, Inc.
Asian IBIS Summit
Shanghai, China
November 9, 2015

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Overview

- IBIS Interconnect Task Group
- Models Represent Package and On-Die Interconnect
- On Die, Package, Supply and Signal Interconnect can be Combined or Kept Separate
- IBIS Interconnect Model Terminals
- Examples

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IBIS Interconnect Task Group

- Meets Wednesdays 8AM PDT
- http://www.ibis.org/interconnect_wip/
- Major Contributors

– Altera	David Banas
– Cadence Design Systems	Bradley Brim
– Intel Corp	Michael Mirmak (Chair)
– Keysight Technologies	Radek Biernacki
– Mentor Graphics	Arpad Muranyi
– Micron Technology	Justin Butterfield, Randy Wolff
– Signal Integrity Software	Walter Katz, Mike LaBonte
– Synopsys	Rita Horner
– Teraspeed Labs	Bob Ross

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Models Represent Package and On-Die Interconnect

- Currently IBIS supports lumped coupled RLC models or lossless uncoupled distributed models.
- New modeling will support broadband, coupled, signal interconnect and power distribution models.
- Languages Supported
  - IBIS-ISS
    - IBIS Interconnect SPICE Subcircuit (IBIS-ISS) Specification, Version 1.0, October 7th 2011 http://www.ibis.org/ibis-iss_ver1.0/ibis-iss_ver1_0.pdf
  - Touchstone ®
    - http://www.ibis.org/touchstone_ver2.0/

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On Die, Package, Supply and Signal Interconnect can be Combined or Kept Separate

- Supports separate on-die and package interconnect models and combined on-die and package interconnect models
- Independent Supply and Signal Interconnect Models
- Coupled Supply and Signal Interconnect Models
- Singled Ended and Differential Interconnect Models

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Similar Approach for Both IBIS and EBD

- IBIS (.ibs) Interconnect Model Terminals
  - Pins ([Pins])
  - Die Pads
  - Buffers
- EBD (.ebd) Interconnect Model Terminals
  - A similar approach will be used to update EBD (Electrical Board Description) or EMD (Electrical Module Description) to support broadband, coupled interconnect models

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IBIS Interconnect Model Terminals

- Pins
  - Pin_name (aka Pin Number)
  - Signal_name (assumes signal_name pins shorted)
  - Bus_label (allows sub-groups of rail signal_name pins)
- Pads (Die/Package Interface)
  - Pin_name (aka Pin Number) for I/O connections
  - Pad_name for rail connections
  - Signal_name (assumes signal_name pads shorted)
  - Bus_label (allows sub-groups of rail signal_name pads)
- Buffers
  - Signal (I/O)
  - Rails
    - Pin_name and (puref/pdref/pcref/gcref)
    - Signal_name (assumes signal_name terminals shorted)
    - Bus_label (allows sub-groups of rail buffer terminals)

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Interconnect Model Terminals

- <Terminal Number> <Terminal Type> <Qualifier>
  - X: I/O pin_name
  - Y: Supply pin_name, signal_name or bus_label
  - Z: Supply pad_name

Terminal_Type	pin_name	signal_name	bus_label	pad_name
Buffer_I/O	X			
Puref	X			
Pdref	X			
Pcref	X			
Gcref	X			
Extref	X			
Buffer_rail		Y	Y	
Pad_I/O	X			
Pad_rail		Y	Y	Z
Pin_I/O	X			
Pin_rail	Y	Y	Y	

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Interconnect Model Examples

```
[Interconnect Model]   DQ1   | IBIS-ISS Model
File_IBIS-ISS  DQ.iss  DQ
Param  Length  Value   0.1
Number_of_Terminals =  2
1 Pin_I/O      pin_name     A1
2 Buffer_I/O   pin_name     A1
[End Interconnect Model]

[Interconnect Model]   A1    | Touchstone File Shortcut
File_TS        A1.s2p
Number_of_Terminals =  3
1 Pin_I/O      pin_name     A1
2 Buffer_I/O   pin_name     A1
3 Pin_rail     signal_name  VSS
[End Interconnect Model]
```

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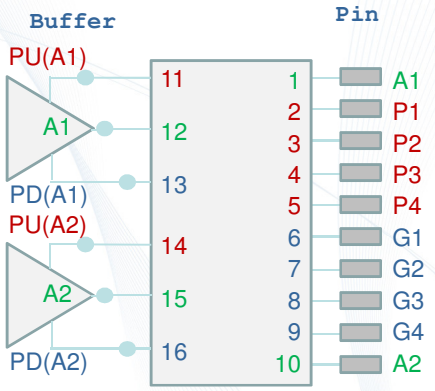
Full Package, All Pins to All Buffers

```
[Pin]   signal_name  model_name
A1      DQ1          DQ
A2      DQ2          DQ
P1      VDD          POWER
P2      VDD          POWER
P3      VDD          POWER
P4      VDD          POWER
G1      VSS          GND
G2      VSS          GND
G3      VSS          GND
G4      VSS          GND

[Begin Interconnect Model]
…
1  Pin_I/O     pin_name    A1
2  Pin_rail    pin_name    P1
3  Pin_rail    pin_name    P2
4  Pin_rail    pin_name    P3
5  Pin_rail    pin_name    P4
6  Pin_rail    pin_name    G1
7  Pin_rail    pin_name    G2
8  Pin_rail    pin_name    G3
9  Pin_rail    pin_name    G4
10 Pin_I/O     pin_name    A2
11 Puref       pin_name    A1
12 Buffer_I/O  pin_name    A1
13 Pdref       pin_name    A1
14 Puref       pin_name    A2
15 Buffer_I/O  pin_name    A2
16 Pdref       pin_name    A2
[End Interconnect Model]
```




```
.subckt AllPinsAllBuffers 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
```

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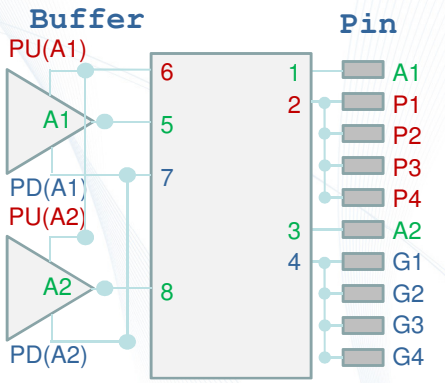
Full Package, All VDD and VSS Pins Shorted
All Buffer Rail Connections Shorted on Die

```
[Pin]    signal_name  model_name
A1       DQ1          DQ
A2       DQ2          DQ
P1       VDD          POWER
P2       VDD          POWER
P3       VDD          POWER
P4       VDD          POWER
G1       VSS          GND
G2       VSS          GND
G3       VSS          GND
G4       VSS          GND

[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal_name
A1             VSS          VDD
A2             VSS          VDD

[Begin Interconnect Model]
…
1  Pin_I/O      pin_name     A1
2  Pin_rail     signal_name  VDD
3  Pin_I/O      pin_name     A2
4  Pin_rail     signal_name  VSS
5  Buffer_I/O   pin_name     A1
6  Buffer_rail  signal_name  VDD
7  Buffer_rail  signal_name  VSS
8  Buffer_I/O   pin_name     A2
[End Interconnect Model]
```




```
.subckt AllPinsRailsShorted 1 2 3 4 5 6 7 8
```

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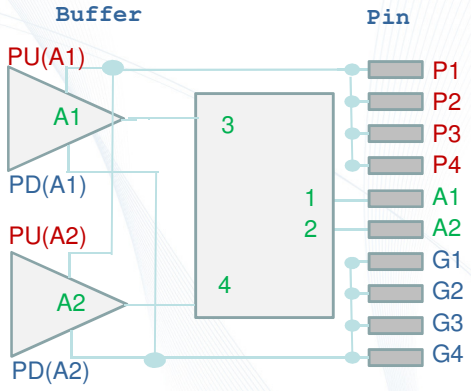
Crosstalk Model, Signal I/O Only

```
[Pin]    signal_name  model_name
A1       DQ1          DQ
A2       DQ2          DQ
P1       VDD          POWER
P2       VDD          POWER
P3       VDD          POWER
P4       VDD          POWER
G1       VSS          GND
G2       VSS          GND
G3       VSS          GND
G4       VSS          GND

[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal_name
A1             VSS          VDD
A2             VSS          VDD

[Begin Interconnect Model]
…
1  Pin_I/O      pin_name     A1
2  Pin_I/O      pin_name     A2
3  Buffer_I/O   pin_name     A1
4  Buffer_I/O   pin_name     A2
[End Interconnect Model]
```




```
.subckt XtalkNoRail 1 2 3 4
```

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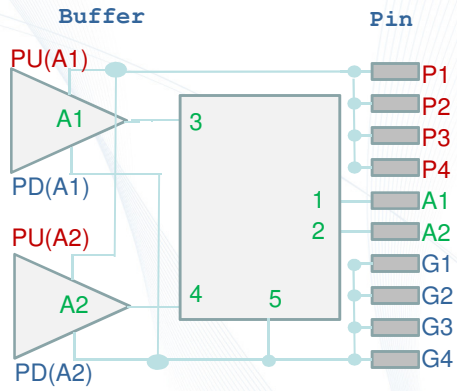
Crosstalk Model, Signal I/O Only, Touchstone Model

```
[Pin]    signal_name  model_name
A1       DQ1          DQ
A2       DQ2          DQ
P1       VDD          POWER
P2       VDD          POWER
P3       VDD          POWER
P4       VDD          POWER
G1       VSS          GND
G2       VSS          GND
G3       VSS          GND
G4       VSS          GND

[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal_name
A1             VSS          VDD
A2             VSS          VDD

[Begin Interconnect Model]
File_TS xyz.s4p
1  Pin_I/O     pin_name     A1
2  Pin_I/O     pin_name     A2
3  Buffer_I/O  pin_name     A1
4  Buffer_I/O  pin_name     A2
5  Pin_rail    signal_name  VSS
[End Interconnect Model]
```




```
.subckt XtalkNoRail_s4p 1 2 3 4
```

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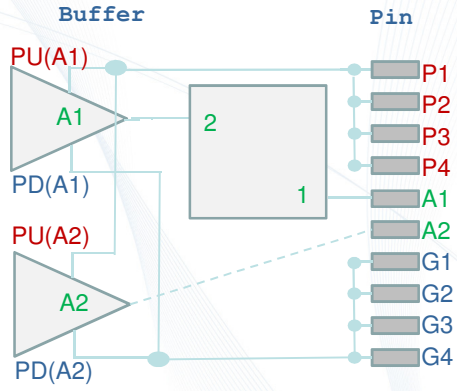
DQ1 Pin to Buffer

```
[Pin]    signal_name  model_name
A1       DQ1          DQ
A2       DQ2          DQ
P1       VDD          POWER
P2       VDD          POWER
P3       VDD          POWER
P4       VDD          POWER
G1       VSS          GND
G2       VSS          GND
G3       VSS          GND
G4       VSS          GND

[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal_name
A1             VSS          VDD
A2             VSS          VDD

[Begin Interconnect Model]
…
1  Pin_I/O     pin_name     A1
2  Buffer_I/O  pin_name     A1
[End Interconnect Model]
```




```
.subckt DQ1Pin2Buffer 1 2
```

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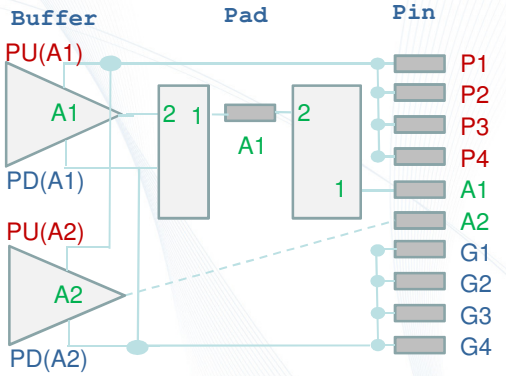
DQ1 Pin to Pad, DQ1 Pad to Buffer

```
[Pin]    signal_name  model_name
A1       DQ1          DQ
A2       DQ2          DQ
P1       VDD          POWER
P2       VDD          POWER
P3       VDD          POWER
P4       VDD          POWER
G1       VSS          GND
G2       VSS          GND
G3       VSS          GND
G4       VSS          GND

[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal_name
A1             VSS          VDD
A2             VSS          VDD

[Begin Interconnect Model]
…
1  Pin_I/O     pin_name     A1
2  Pad_I/O     pin_name     A1
[End Interconnect Model]

[Begin Interconnect Model]
…
1  Pad_I/O     pin_name     A1
2  Buffer_I/O  pin_name     A1
[End Interconnect Model]
```




```
.subckt DQ1Pin2Pad 1 2
.subckt DQ1Pad2Buffer 1 2

XPinPad PinA1 PadA1 DQ1Pin2Pad
XPadBuf PadA1 BufA1 DQ1Pad2Buffer
```

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VDD Pad by signal_name

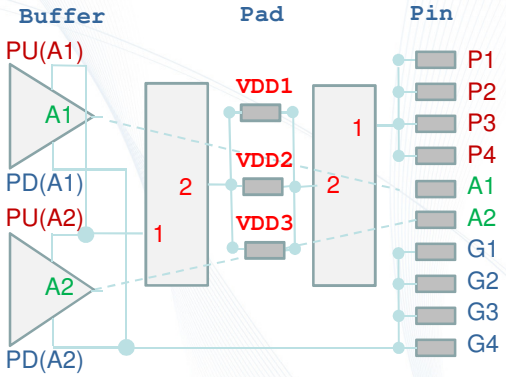
```
[Pin]    signal_name  model_name
A1       DQ1          DQ
A2       DQ2          DQ
P1       VDD          POWER
P2       VDD          POWER
P3       VDD          POWER
P4       VDD          POWER
G1       VSS          GND
G2       VSS          GND
G3       VSS          GND
G4       VSS          GND

[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal_name
A1             VSS          VDD
A2             VSS          VDD

[Die Supply Pads] signal_name bus_label
VDD1           VDD          VDDa
VDD2           VDD          VDDa
VDD3           VDD          VDDb
[End Die Supply Pads]

[Begin Interconnect Model]
…
1  Pin_rail    signal_name  VDD
2  Pad_rail    signal_name  VDD
[End Interconnect Model]

[Begin Interconnect Model]
…
1  Buffer_rail signal_name  VDD
2  Pad_rail    signal_name  VDD
[End Interconnect Model]
```




```
.subckt VDDPin2Pad_sn 1 2
.subckt VDDBuf2Pad_sn 1 2

XPinPad VDDPin VDDPad VDDPin2Pad_sn
XBufPad VDDPad VDDBuf VDDBuf2Pad_sn
```

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VDD Pad by pad_name

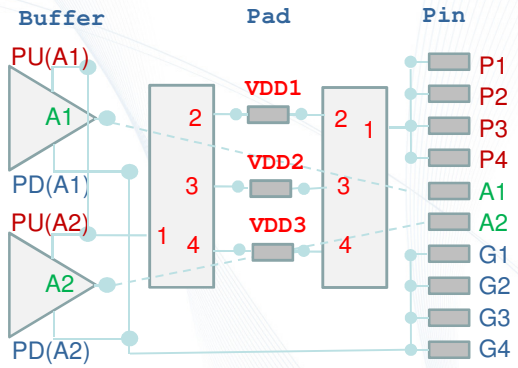
```
[Pin]    signal_name  model_name
A1       DQ1          DQ
A2       DQ2          DQ
P1       VDD          POWER
P2       VDD          POWER
P3       VDD          POWER
P4       VDD          POWER
G1       VSS          GND
G2       VSS          GND
G3       VSS          GND
G4       VSS          GND

[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal_name
A1             VSS          VDD
A2             VSS          VDD

[Die Supply Pads] signal_name bus_label
VDD1               VDD          VDDa
VDD2               VDD          VDDa
VDD3               VDD          VDDb
[End Die Supply Pads]

[Begin Interconnect Model]
…
1 Pin_rail     signal_name     VDD
2 Pad_rail     pad_name        VDD1
3 Pad_rail     pad_name        VDD2
4 Pad_rail     pad_name        VDD3
[End Interconnect Model]

[Begin Interconnect Model]
…
1 Buffer_rail signal_name     VDD
2 Pad_rail     pad_name        VDD1
3 Pad_rail     pad_name        VDD2
4 Pad_rail     pad_name        VDD3
[End Interconnect Model]
```




```
.subckt VDDPin2Pad 1 2 3 4
.subckt VDDBuf2Pad 1 2 3 4

XPinPad VDDPin VDD1 VDD2 VDD3 VDDPin2Pad
XBufPad VDDBuf VDD1 VDD2 VDD3 VDDBuf2Pad
```

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VDD Pad by bus_label

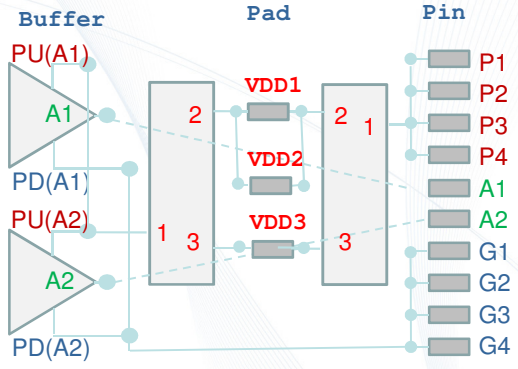
```
[Pin]    signal_name  model_name
A1       DQ1          DQ
A2       DQ2          DQ
P1       VDD          POWER
P2       VDD          POWER
P3       VDD          POWER
P4       VDD          POWER
G1       VSS          GND
G2       VSS          GND
G3       VSS          GND
G4       VSS          GND

[Pin Mapping] pulldown_ref pullup_ref
Bus_label_signal_name
A1             VSS          VDD
A2             VSS          VDD

[Die Supply Pads] signal_name bus_label
VDD1               VDD          VDDa
VDD2               VDD          VDDa
VDD3               VDD          VDDb
[End Die Supply Pads]

[Begin Interconnect Model]
…
1 Pin_rail     signal_name     VDD
2 Pad_rail     bus_label       VDDa
3 Pad_rail     bus_label       VDDb
[End Interconnect Model]

[Begin Interconnect Model]
…
1 Buffer_rail signal_name     VDD
1 Pin_rail     signal_name     VDD
2 Pad_rail     bus_label       VDDa
3 Pad_rail     bus_label       VDDb
[End Interconnect Model]
```




```
.subckt VDDPin2Pad_bl 1 2 3
.subckt VDDBuf2Pad_bl 1 2 3

XPinPad VDDPin VDDa VDDb VDDPin2Pad_bl
XBufPad VDDBuf VDDa VDDb VDDBuf2Pad_bl
```

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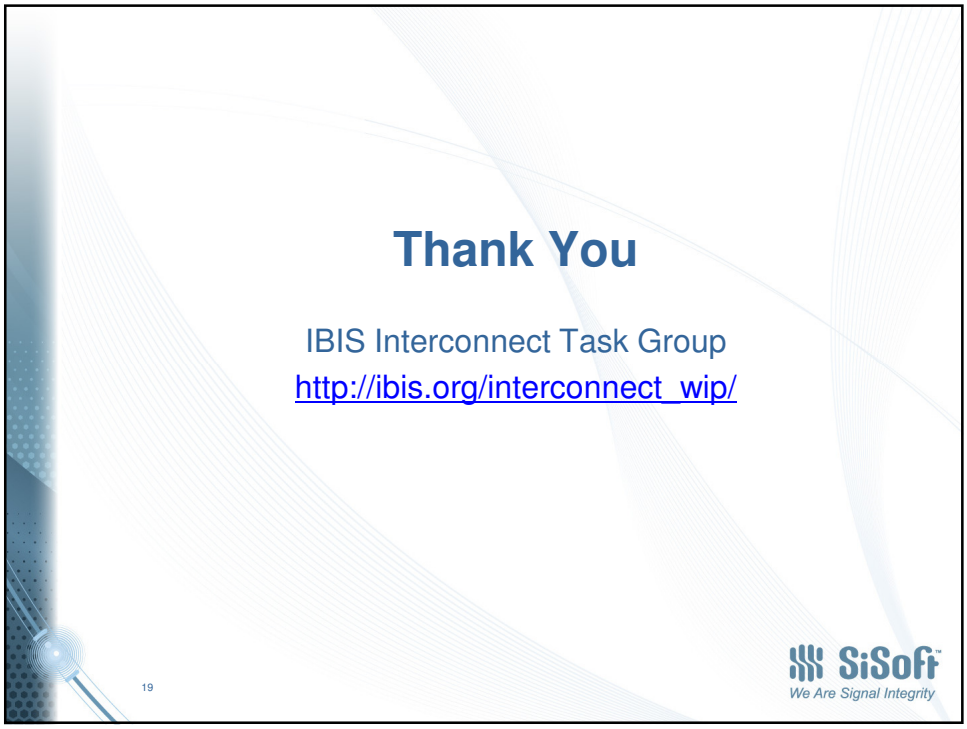
We Are Signal Integrity

18


Thank You
IBIS Interconnect Task Group
http://ibis.org/interconnect_wip/
19
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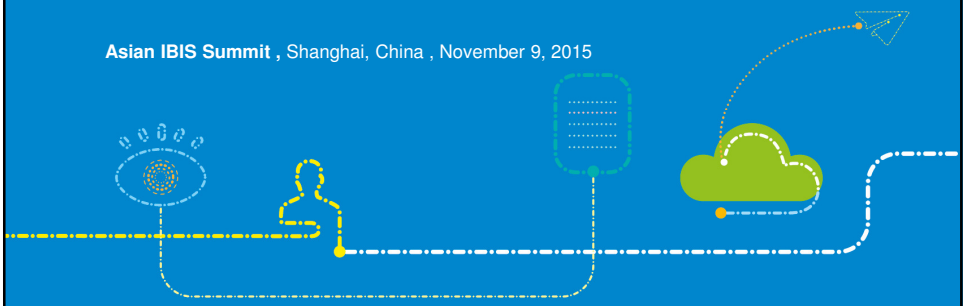
Tomorrow never waits

FEC Applications for 25Gb/s Serial Link Systems

Guo Tao，Zhu Shunlin
Guo.tao6@zte.com.cn, zhu.shunlin@zte.com.cn

Asian IBIS Summit , Shanghai, China , November 9, 2015

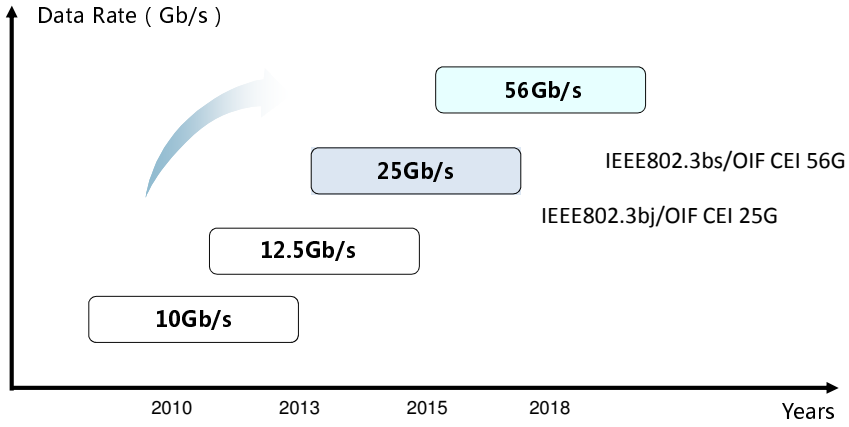


Agenda

- Introduction
- FEC Applications to Serial Link System
- FEC Simulations for 25Gb/s SerDes System
- A New Proposal for FEC Modeling and Simulation
- Summary

Introduction

100 Gigabit Ethernet will account for over half of all bandwidth deployed in carrier network in 2014，growing rapidly through 2018.

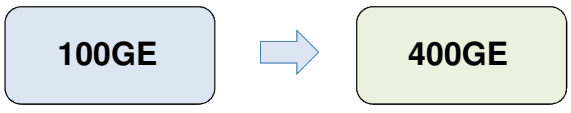


ZTE

Introduction

Besides equalization techniques，some new techniques have been used for SerDes systems in order to meet 100GE- 400GE specs.

Higher Data Rate：25Gb/s to 56Gb/s



Equalization：
De-emphasis+CTLE+DFE

Forward Error Correction：**FEC**
Fanny Modulation：NRZ or PAM4

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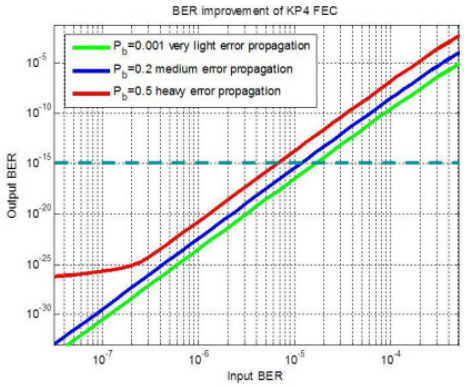
Introduction

The Forward Error Correction（FEC）has been used for Increasing serial link system budgets and relaxing BER requirements.

- Code Gain
  - Gain vs Higher Frequency
- Time
  - Serial Link Latency
- Complexity
  - Area and Power



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Agenda

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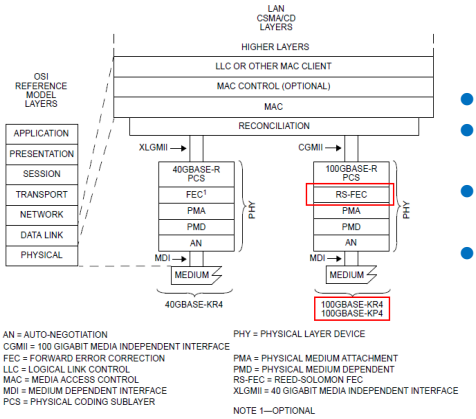
FEC Applications to Serial Link System

FEC Applications on the 100GE standard of IEEE802.3bj



- Backplane System —100GBASE-KR4
- FEC block is placed between PCS and PMA
- Reed-Solomon Code is suggested , defined in clause 91
- RS(528,514,7) — about 5dB gain

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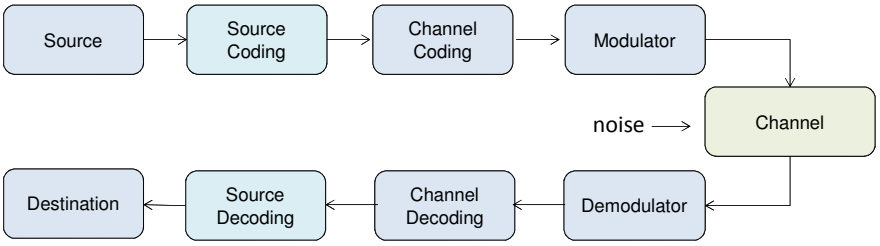
FEC Applications to Serial Link System



Recently adopted FEC

- Fire Code （1604, 1584） – OIF CEI-P
- QC Code （2112, 2080） – 10GBASE-KR
- RS（528, 514, 7） over GF(210) – 100GBASE-KR4
- RS（544, 514, 15） over GF(210) – 100GBASE-KP4

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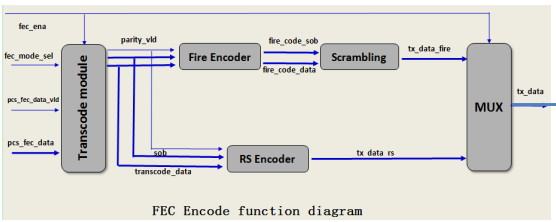
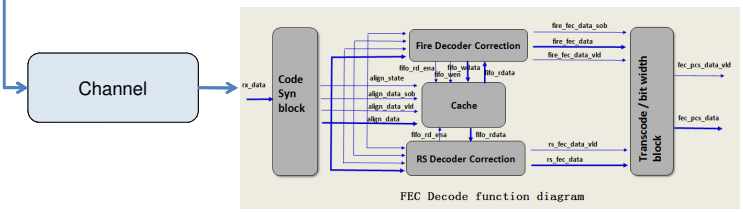
FEC Applications to Serial Link System

FEC Encoding & Decoding diagram



FEC Encode function diagram



FEC Decode function diagram

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Agenda

- Introduction
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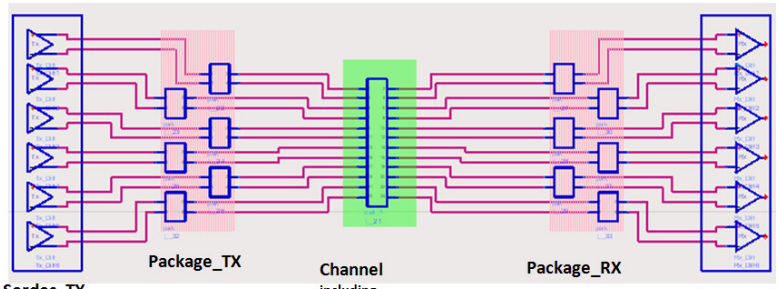
FEC Simulations for 25Gb/s SerDes System

Simulation Setup :

Data rate:25.78125Gb/s
BER:~1e-15
Pattern : PRBS 31
Number of bits: 1million



Serdes_TX
Including
Pattern
prbs31;FEC;
FFE ...

Channel
including
Backplane*1;
Daughter Card*2;
Connector*2
Channel length:30inch

Serdes_RX
Including
CTLE;DFE ;
FEC; ...

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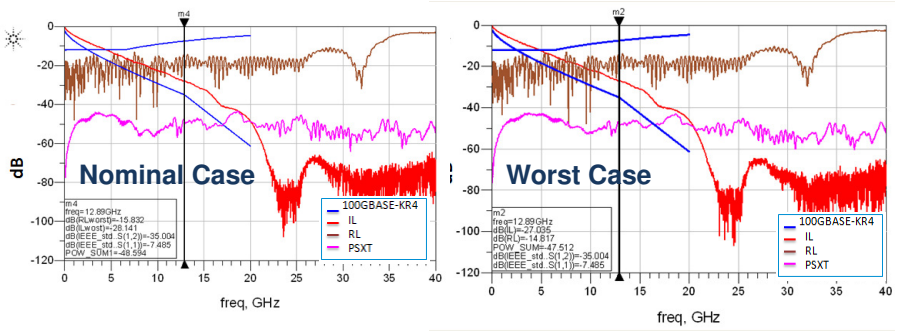
FEC Simulations for 25Gb/s SerDes System



	IL/dB	RL/dB	PSXT/dB
Nominal	-26.3	-16.8	-47.51
Worst	-28.1	-15.83	-48.59

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FEC Simulations for 25Gb/s SerDes System

Comparison between with and without FEC

	Nominal Case		Worst Case		
AtBER	Width/*UI	Height/mV	Width/%*UI	Height/mV	Condition
^1e-12	16.2%	23.1	4.51%	5.39	With emphasis/DFE ; Without FEC
^1e-15	12.2%	17.4	0.07%	0.00	
^1e-17	9.92%	14.2	0.00%	0.00	
^1e-12	42.5%	57.0	42.2%	48.6	With emphasis/DFE ; With FEC
^1e-15	40.6%	54.8	40.2%	46.4	
^1e-17	39.5%	53.4	38.9%	45.1	

Eye diagram at the BER of 1e-12 of the channel simulation can not meet the requirement of 100GE Standard without FEC.
Crosstalk must be concerned in the channel simulation.

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FEC Simulations for 25Gb/s SerDes System

Comparison between with and without FEC

	Nominal Case		Worst Case		
AtBER	Width/*UI	Height/mV	Width/%*UI	Height/mV	Condition
^1e-5	33.5%	63.6	32.6%	54.6	
^1e-6	29.1%	62.4	23.2%	53.5	With emphasis/DFE ; Without FEC;
^1e-7	25.9%	61.4	17.1%	52.6	
^1e-12	42.5%	57.0	42.2%	48.6	
^1e-15	40.6%	54.8	40.2%	46.4	With emphasis/DFE ; With FEC;
^1e-17	39.5%	53.4	38.9%	45.1	

Eye diagram at the BER of 1e-15 of the channel simulation can meet the requirement of 100GE Standard with FEC, while relaxing the BER requirement from 1e-15 to 1e-5 or 1e-6.

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Agenda

- Introduction
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- Summary

A New Proposal for FEC Modeling and Simulation

Current Situation:

- IBIS-AMI model

```
(my_AMIname                | Header,such as AMI_version …
                           | Function such as, GetWave_Exists …
     (Reserved_Parameters  | Modulation such as, NRZ, PAM4 …
                           | Jitter such as, Dj …
                           | Repeater …
```

- EDA Tool

  FEC blocks are not supported in IBIS-AMI model nor in EDA tool

- System Simulation

  Uses the same Serdes IP on the TX and RX end supported by the IC Vendor

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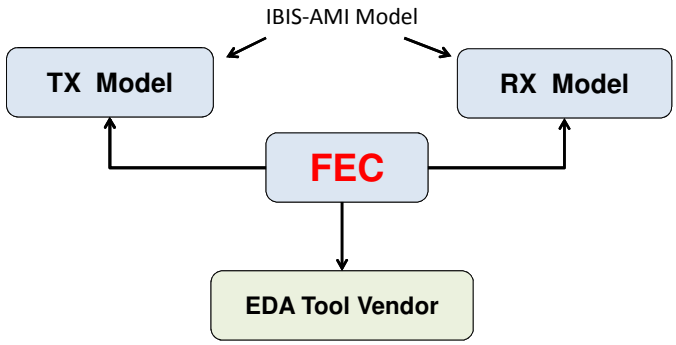
A New Proposal for FEC Modeling and Simulation



System vendors strongly expect that IBIS-AMI models can be used for FEC simulations.

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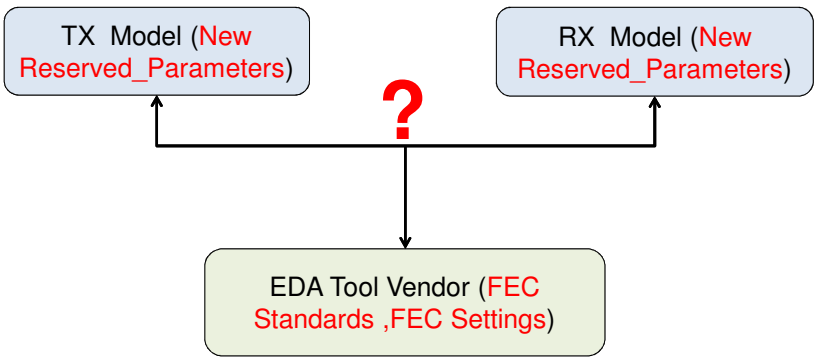
A New Proposal for FEC Modeling and Simulation



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A New Proposal for FEC Modeling and Simulation

[Reserved_Parameters] / [Model_Specific] → tx_fec / rx_fec ?

On the transmit end
Add the branch 'tx_fec' into Model_Specific, then add parameters, config min/typ/max, mode on/off, such as

```
(Model_Specific
  (tx_fec
    (config (Usage In)(List "min" "typ" "max")(Type String)
      (Default "typ")(Description "enable fec function setting"))
    (mode (Usage In)(Format List "on" "off")(Type String)
      (Default "off")(Description "fec control mode"))
```

On the receiver end,
Add the branch 'rx_fec' into Model_Specific, then add the same parameters to respond the tx configuration, such as

```
(Model_Specific
  (rx_fec
    (config (Usage In)(List "min" "typ" "max")(Type String)
      (Default "typ")(Description "enable fec function setting"))
    (mode (Usage In)(Format List "on" "off")(Type String)
      (Default "off")(Description "fec control mode"))
```


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Agenda

- Introduction
- FEC Applications to Serial link System
- FEC Simulations for 25Gb/s SerDes System
- A New Proposal for FEC Modeling and Simulation
- Summary

Summary

- FEC can be used for many dispersion and noise limited systems, such as high-speed serial link systems in order to meet 100GE- 400GE specs.
- FEC relaxes PHY BER requirement from 1e-15 to 1e-06 for serial link systems.
- FEC is one of critical techniques for 25-56Gb/s SerDes systems and IBIS-AMI model is an efficient solution for complex IO modeling.
- System vendors strongly expect that IBIS-AMI models can be used for FEC simulations.
- “One model, one platform, one simulator” needed for both passive and active components, such as FFE，DFE，FEC …

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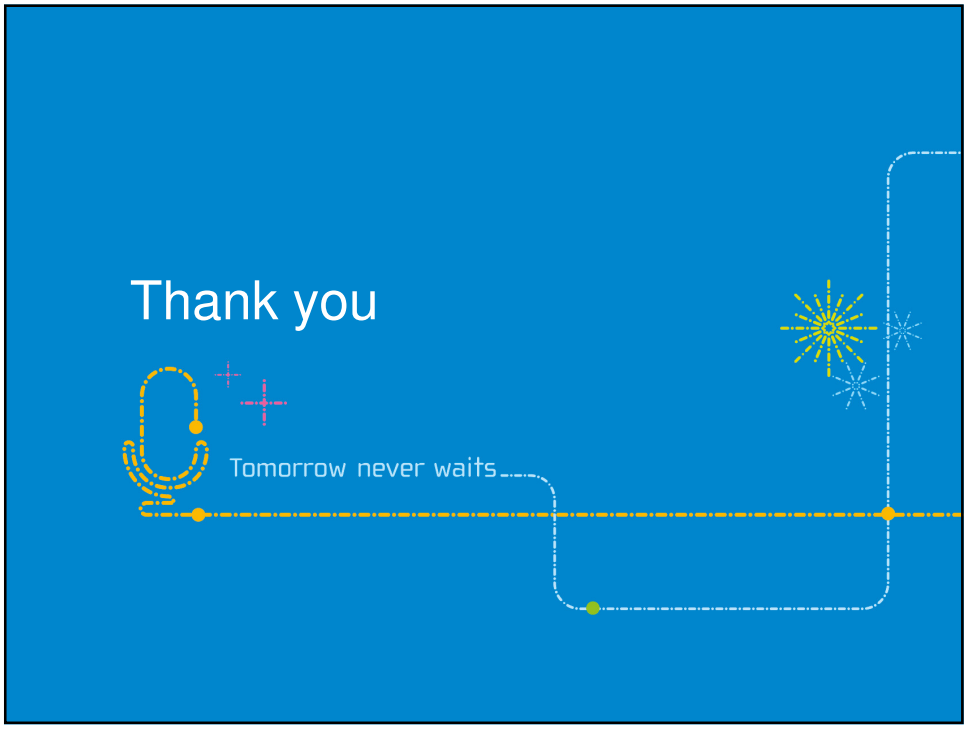


PAM4 System Simulation using AMI models

Fangyi RAO

Asian IBIS Summit
Shanghai, China
November 9, 2015

Presented by Yi WANG

KEYSIGHT TECHNOLOGIES

Agenda

- Overview of PAM4
- Challenges in PAM-4 Link Designs
- Solutions for Simulating PAM-4 Links with IBIS-AMI Models

KEYSIGHT TECHNOLOGIES

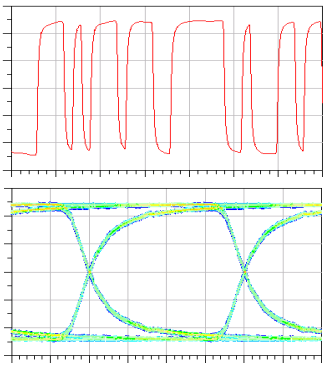
Enabling the next step in link data rate

- 56 Gb/s lane data rate will be the principle enabler for 400GbE
- Two contenders for implementing 56Gb/s lane data rate:
  - 56G NRZ
    - + No new science – linear evolution from 25/28G lanes
    - - Difficult to manage channel loss & channel reflections
  - 28 Gbaud PAM-4
    - + Channel loss problems worked out with 28 Gb/s NRZ
    - - 30% chip real estate, 35+% more power
    - - Lose 9.6 dB usable SNR
    - - Lots of new challenges – little experience to draw from
  - Both signaling technologies will be utilized to enable 400GbE

KEYSIGHT TECHNOLOGIES

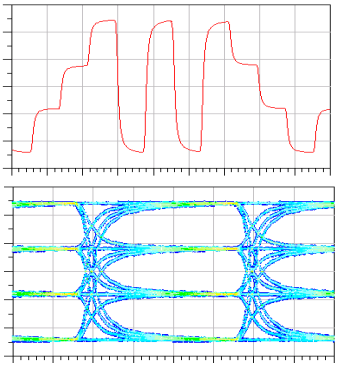
NRZ (Non-Return-to-Zero) vs. PAM (Pulse Amplitude Modulation)

NRZ (PAM-2)



- 2 amplitude levels
- 1 bit of information in every symbol
- 56 Gbaud for 56 Gb/s

PAM-4



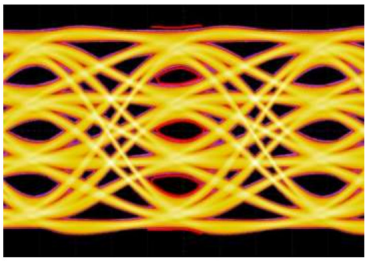
- 4 amplitude levels
- 2 bits of information in every symbol
  - ✓ 2x throughput for the same Baud rate
  - ✓ 28 Gbaud for 56 Gb/s, half of the loss in dB
- Lower SNR, more susceptible to jitter & noise
- More complex TX/RX design, higher cost

KEYSIGHT TECHNOLOGIES

Moving from NRZ to PAM-4

Revolutionary – not Evolutionary

- Jump from 10G NRZ to 25G introduced many new concepts....
  - Still a linear transition (more or less)
- Multi-Level signaling changes all the rules – in place for 50+ years!
  - Saturating to linear output stages
  - *More complex (and precise) level threshold detection for inputs*
  - Finite rise time creates inherent ISI
  - How to implement clock recovery?
  - How will DFE need to change?
  - ....
  - ....



KEYSIGHT TECHNOLOGIES

Agenda

6

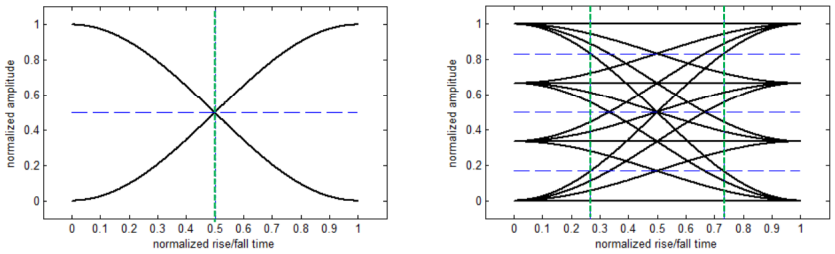
- Overview of PAM4
- Challenges in PAM-4 Link Designs
- Solutions for Simulating PAM-4 Links with IBIS-AMI Models

KEYSIGHT TECHNOLOGIES

6

Implementing PAM-4 links = "New Science"

- Inherent ISI requires receivers to be less susceptible to pattern dependent jitter

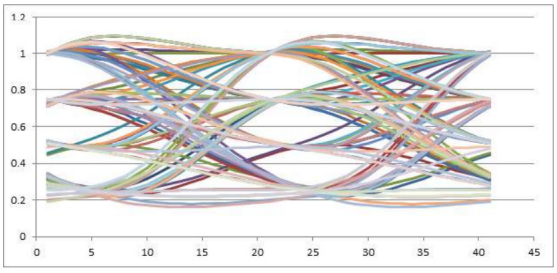


decision threshold
Amount of switching jitter

KEYSIGHT TECHNOLOGIES

Implementing PAM-4 links = "New Science" (2)

- Some of the other challenges learned so far include...
  - Eye time skew from linear drive of VCSELs
    - Upper eyes arrive sooner than lower transitions
    - Each eye needs to be sampled with independent delay



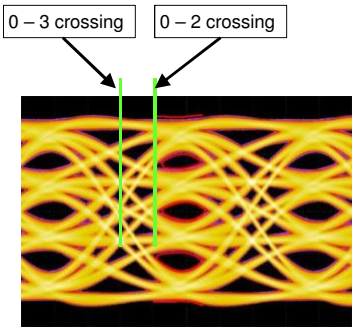
KEYSIGHT TECHNOLOGIES

Challenges shifting from NRZ to PAM

PAM-4 is one of the enablers of 56 G lane rate supporting 400G links

Multi-level signaling changes all the rules that have in place for 50+ years!

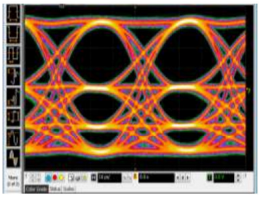
- Saturating to linear output stages
- More complex (and precise) level threshold detection for inputs
- Finite rise time creates inherent ISI
- How to implement clock recovery?
- How will DFE need to change?



KEYSIGHT TECHNOLOGIES

Other impairments that challenge PAM-4 receivers

- Non-linearity - Amplitude compression in lower eyes
  - Non uniform effective SNR across individual eyes



- Receivers sensitive to additional artifacts beyond “traditional” jitter types in NRZ
  - Still learning what impairments cause problems
    - New measurements WILL be defined for Tx Outputs
    - New stress types WILL be defined for Rx Input testing

KEYSIGHT TECHNOLOGIES

Challenges in PAM-4 SerDes Design

- Nonlinearity between levels due to saturation
- CDR
- Upper and lower eye slicer reference level tuning
- Timing skews between three slicers for optimal sampling
- Analog based architecture vs ADC based architecture
- …

Challenges in PAM-4 Link Simulation

- How to capture PAM-4 SerDes behaviors
- How to measure PAM-4 eyes (three stacking eyes vs single eye in NRZ)

KEYSIGHT TECHNOLOGIES

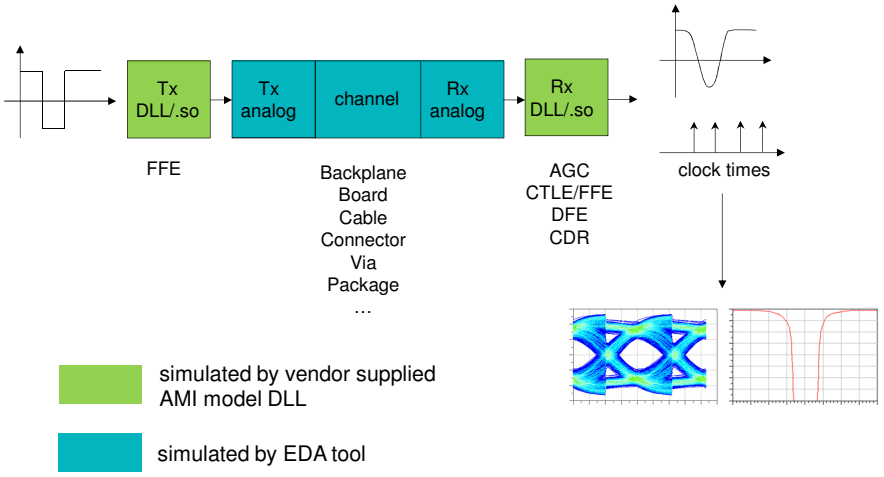
Agenda

12

- Overview of PAM4
- Challenges in PAM-4 Link Designs
- Solutions for Simulating PAM-4 Links with IBIS-AMI Models

KEYSIGHT TECHNOLOGIES

AMI Simulation Flow for NRZ



KEYSIGHT TECHNOLOGIES

IBIS-AMI Based PAM-4 Link Simulation

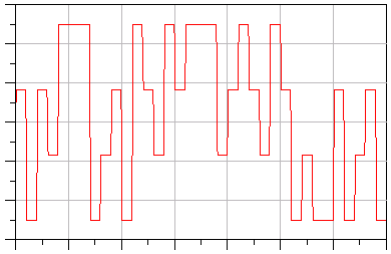
- AMI successfully brings SerDes vendors' models and EDA tools together
- **Interoperability**: AMI defines a common interface between SerDes model and channel simulator
- **IP protection**: SerDes behavior is concealed in model DLL/shared object
- Superior simulation speed
- AMI has been widely adopted by IC, system and EDA companies

http://www.ibis.org/

KEYSIGHT TECHNOLOGIES

AMI Modeling for PAM4 Signaling: Tx

- For NRZ, input stimulus to Tx DLL has two levels (0.5 and -0.5V), representing 1 and 0 bits
- For PAM4, input to Tx DLL has four levels (0.5, 0.5/3, -0.5/3 and -0.5V), representing symbols 0, 1, 2 and 3
- Tx DLL/.so interface is unchanged for PAM4



KEYSIGHT TECHNOLOGIES

Tx AMI Reserved Parameters

Modulation

- String. Allowed values are “NRZ” and “PAM4”
- Optional. Default is “NRZ”

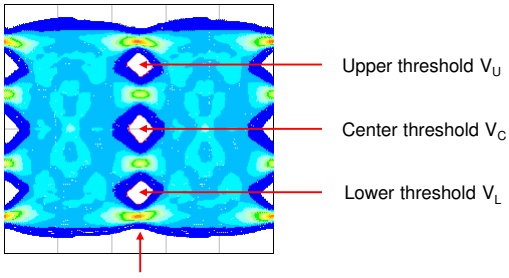
PAM4_Mapping

- String of four non-repeated integers 0, 1, 2 and 3 (e.g. “0123”)
- Bit pairs 00, 01, 10 and 11 map to symbol levels specified by 1st, 2nd, 3rd and 4th integers, respectively
- Optional. Default is “0132” (Gray coding)

KEYSIGHT TECHNOLOGIES

AMI Modeling for PAM4 Signaling: Rx

- PAM4 Rx symbol decision relies on three slicers
- Slicer thresholds can be adjusted adaptively and can vary with time
- Sampling time skew can be applied independently to each slicer for optimal result and can vary with time
- Rx model should provide transient slicer threshold and timing skew information



KEYSIGHT TECHNOLOGIES

Rx AMI Reserved Parameters

PAM4_UpperThreshold, PAM4_CenterThreshold, PAM4_LowerThreshold

- Float. Upper, center and lower slicer thresholds
- Optional. If not provided by models, EDA tools have to guess their values for SER calculations

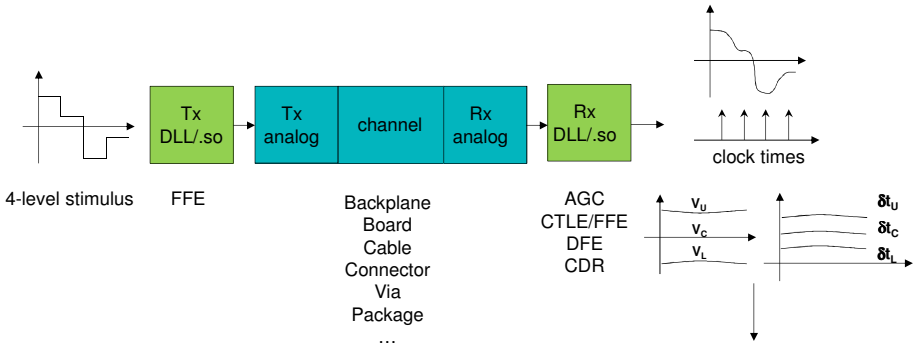
PAM4_UpperEyeOffset, PAM4_CenterEyeOffset, PAM4_LowerEyeOffset

- Float. Upper, center and lower slicer sample time offsets relative to clock times
- Optional. Default is 0

Rx model can update values of these parameters in AMI_Init and AMI_GetWave and return them through the *AMI_parameters_out* string argument

KEYSIGHT TECHNOLOGIES

AMI Simulation Flow for PAM4



simulated by vendor supplied AMI model DLL

simulated by EDA tool

V_U, V_C, V_L: upper, center and lower eye thresholds
δt_U, δt_C, δt_L: upper, center and lower eye sample time offsets

KEYSIGHT TECHNOLOGIES

Symbol Error Rate (SER) Measurement

- Measure bathtubs and SER contours individually for each of the three stacking eyes
- Horizontal eye center is placed at clock time + offset to capture CDR behavior and skew
- Vertical eye center is placed at threshold V_U/ V_C/ V_L to capture slicer level fluctuation

	Logic high traces	Logic low traces
Upper eye	$v_3(t) - V_U(t)$	$v_2(t) - V_U(t)$
Center eye	$v_2(t) - V_C(t)$	$v_1(t) - V_C(t)$
Lower eye	$v_1(t) - V_L(t)$	$v_0(t) - V_L(t)$

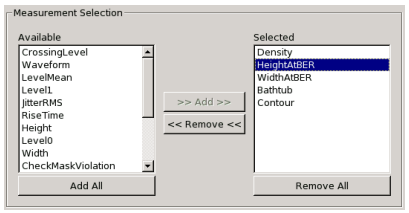
(v_0, v_1, v_2 and v_3 are waveforms of expected 0, 1, 2 and 3 symbols, respectively)

KEYSIGHT TECHNOLOGIES

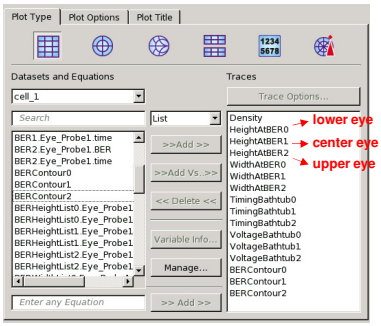
SER Measurements in Eye Probe

A set of bathtub, contour, HeightAtBER and WidthAtBER are calculated individually for each of the three eyes if selected

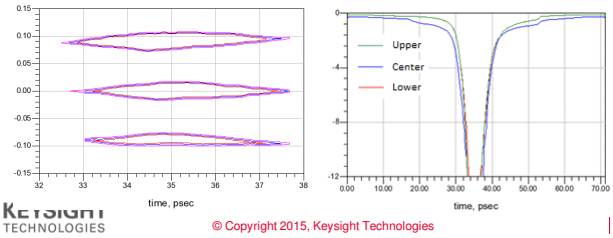
<Eye probe measurement tab>



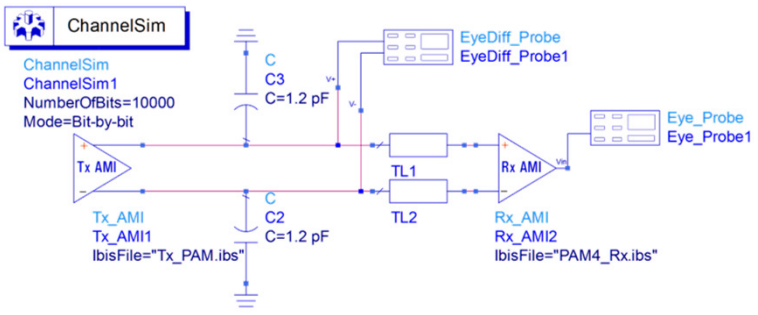
<Dataset>



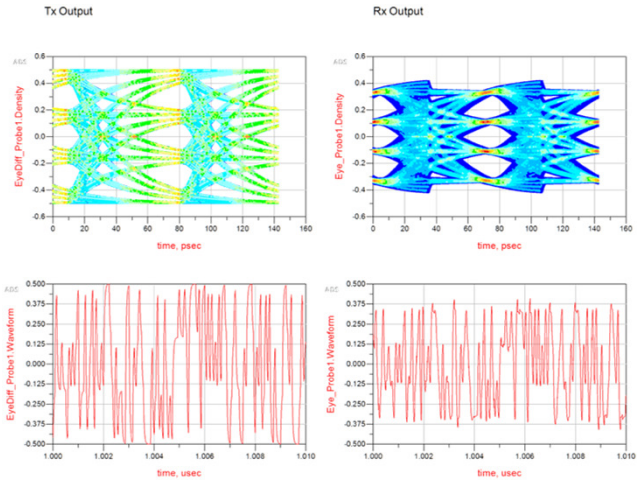
<SER>



PAM4 System Simulation using AMI models



PAM4 System Simulation using AMI models



KEYSIGHT TECHNOLOGIES

Thank you

KEYSIGHT TECHNOLOGIES

Some Results for General K-table Extraction Proposal Using SPICE

Bob Ross, Teraspeed Labs
bob@teraspeedlabs.com
Xuefeng Chen, Synopsys
xfchen@synospsys.com

Asian IBIS Summit
Shanghai, China
November 9, 2015

(From material originally presented January 30, 2015,
this presentation given Oct. 28, 2015)

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Updated Material

- **More derivation detail: January 30, 2015, "General K-Table Extraction Proposal Using SPICE"**
  - **http://www.ibis.org/summits/jan15/ross2.pdf**
  - **Contains Summit references**
- **Some results and other observations here**
- **Purpose – Use SPICE for PROTOTYPING IBIS extraction algorithms (with general C_comp, on-die, package structures and fixture loads)**

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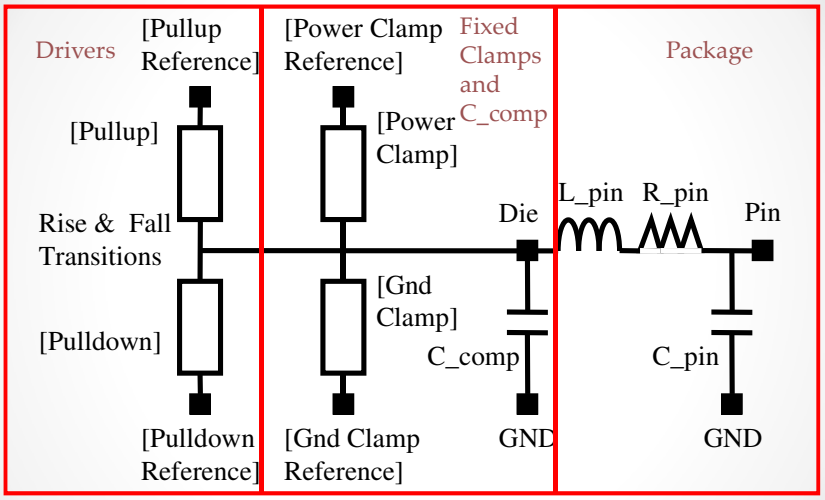
Overview

- Fixed C_comp to local GND for extraction
- Detailed C_comp model from S-parameters or IBIS-ISS allowed
- IBIS Interconnect BIRD proposal adds on-die and package models
- SPICE-based extraction proposal supports total path measurement with more detailed C_comp/on-die/package structures
- Limitations exist

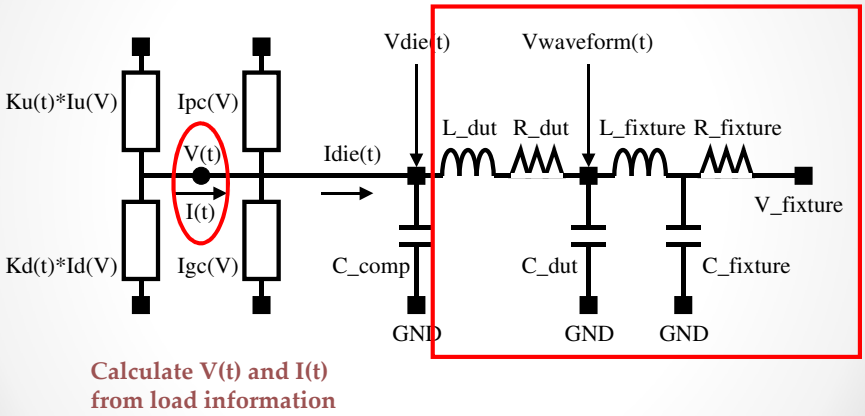
SYNOPSYS® Silicon to Software™ 3

Standard IBIS Model



SYNOPSYS® Silicon to Software™ 4

Generalized V-T Extraction Load (with L/R/C_dut)



Calculate V(t) and I(t) from load information

Direct V(t), I(t) Solution

- Xuefeng Chen, Asian IBIS Summit (China), September 11, 2007: V(t), I(t) extracted directly for L/R/C/V_fixture by applying i=C*dv(t)/dt and v=L*di(t)/dt
- Extension can include L/R/C_dut (where L/R/C_dut replaces the L/R/C_pin values for the measured pin)
- Ku(t) and Kd(t) tables extracted using the 2-equations/2-unknowns (2EQ/2UK) method (later)

Indirect Feedback Solution Next

- Avoids encoding equations for complex structures
- Calculates K-tables with high-gain (e.g., 1E7) feedback loop multiplier
  - Kur(t), Kdr(t) from two rising V-T waveforms and fixtures
  - Kuf(t), Kdf(t) from two falling V-T waveforms and fixtures
- Calculated and specified responses converge
- Requires vendor-specific SPICEs (versus IBIS-ISS)
  - Tables
  - Feedback loop issues with tables

SYNOPSYS® Silicon to Software™

Partial SPICE Circuit Showing 2EQ/2UK K-Table Extraction

```
*
* FEEDBACK TABLE ADJUSTMENT ............................. VVV
GDET    NDET  GND  CUR='(I(VDN2)*I(VUP1)-I(VDN1)*I(VUP2))/(1E7)'
VDET    NDET  GND  0
*
GKUR    NKU   GND
+ CUR='(V(IN2)-V(PIN2))*I(VDN1)-(V(IN1)-V(PIN1))*I(VDN2))/I(VDET)'
VKUR    NKU   GND  0
*                  Kur
GKDR    NKD   GND
+ CUR='(V(IN1)-V(PIN1))*I(VUP2)-(V(IN2)-V(PIN2))*I(VUP1))/I(VDET)'
VKDR    NKD   GND  0
*                  Kdr
```

$$I_1(t) = Ku(t)*Iu(V_1(t)) + Kd(t)*Id(V_1(t))$$

$$I_2(t) = Ku(t)*Iu(V_2(t)) + Kd(t)*Id(V_2(t))$$

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SPICE Encoding

- I-V tables: G elements (VCCS)
- V-T tables: PWL voltage sources
- Voltage rails: Entered
- SPICE interpolation
  - Allows higher resolution time steps in V-T tables
  - Interpolates G table currents
- I-V and V-T tables extended from final values
- Convergence criteria adjustable
- K-tables printed for Kur(t), Kdr(t); Kuf(t), Kdf(t)
- Simulation done with K-table drivers:
  - G elements for K-tables
  - Scaled controlled ramp (1V/nS)
  - Step stimuli (0 to 1, 1 to 0)

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Part of SPICE Encoded IBIS Prototype for Simulation

```
* HIGH SIDE
XUP     OUT1   VCC   NU1           PULLUP
VUP     NU1    VCC   0
GUP     OUT1   VCC   CUR='-I(VUP)*(I(VKUR)*I(VON)+I(VKUF)*(1-I(VON)))'
XPC     OUT1   VCC                 POWER_CLAMP
*
* LOW SIDE
XDN     OUT1   GRD   ND1           PULLDOWN
VDN     ND1    GRD   0
GDN     OUT1   GRD   CUR='-I(VDN)*(I(VKDR)*I(VON)+I(VKDF)*(1-I(VON)))'
XGC     OUT1   GNDC                GND_CLAMP
*
* C_COMP AND DUT PACKAGE
XCAP    OUT1   GRD                 C_COMP
XPKG    OUT1   GRD   PIN1          PACKAGE
*
* LOAD
TLOAD   PIN1   GRD   PIN9    GRD   Z0=50 TD=1N
RLOAD   PIN9   GND   50G
*
* VOLTAGE CONTROL (AMPLITUDE (0 TO 1), PULSE WIDTH & PERIOD)
VPULSE STEP    GRD   0   PULSE (1 0 0P 1P 1P 5N 10N)
```

Kur, Kdr

Kuf, Kdf

Table switching control

Enter simulation load

Ideal Step Stimulus

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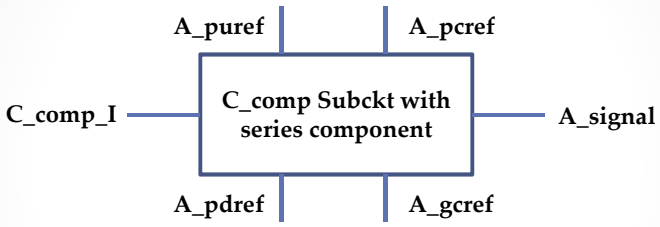
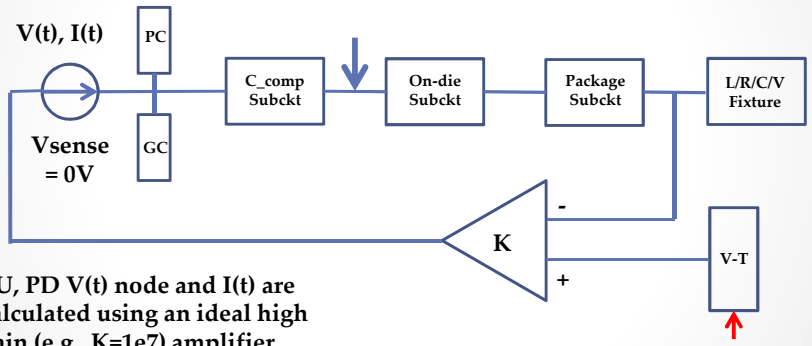
General Proposed Single-ended C_comp Subckt Model



- (Notation and details under development)
- C_comp_I: If needed for series path
  - Resistance needs to be de-embedded from I-V tables
- A_signal: Output
- Extend model for differential connections

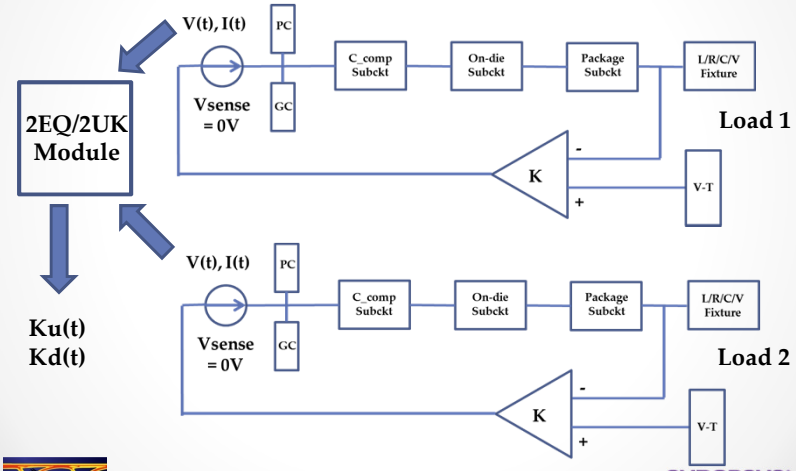
SPICE Extraction of V(t), I(t) Setup and C_comp A_signal Node



PU, PD V(t) node and I(t) are calculated using an ideal high gain (e.g., K=1e7) amplifier

V-T table (originally extracted at the Fixture) is now a PWL driver

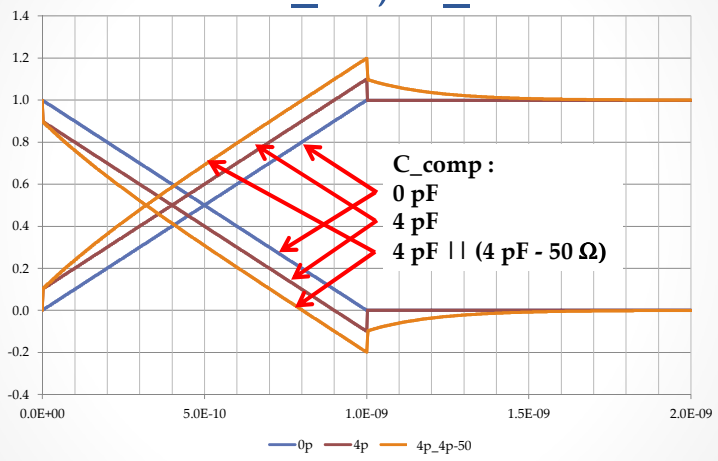
2EQ/2UK SPICE Setup to Generate Ku(t), Kd(t) Tables



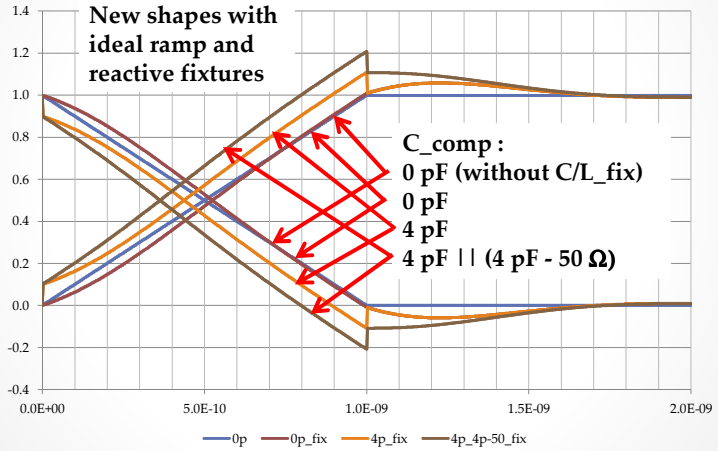
Ideal Ramp Test Cases

- **Reference Waveforms**
  - 1 ns ramp (0% to 100%) into 50 Ω-to-gnd and 50 Ω-to-vcc loads
  - 5 V supply
  - 2 ns duration
- **C_comp cases**
  - 0 pF (0p)
  - 4 pF (4p)
  - 4 pF || (4 pF – 50 Ω) (4p_4p-50)
- **Pullup/Pulldown I-V tables**
  - 50 Ω straight lines
- **1001 point extractions (not critical)**

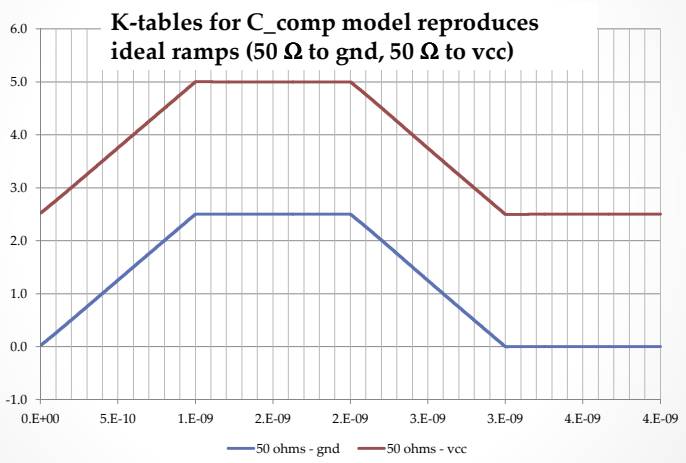
K-tables Shapes Versus Time (s)
No L_fix, C_fix



K-tables Versus Time (s) – With
L_fix=10 nH, C_fix=4 pF Fixtures

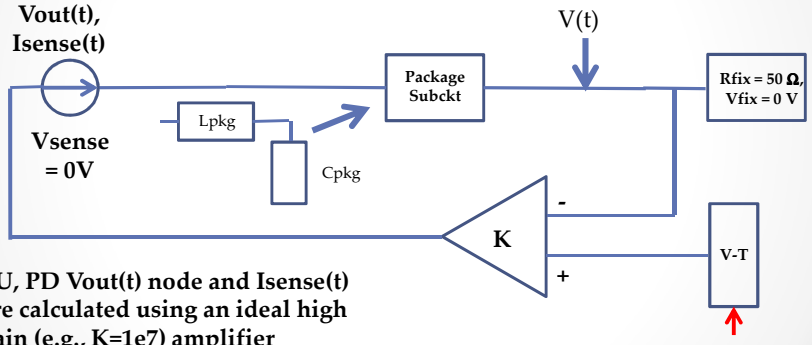


4 ns Cycle Simulations for 4p_4p-50 C_comp Model



Test Case Notation Change for Vout(t) & Isense(t); Given V(t)

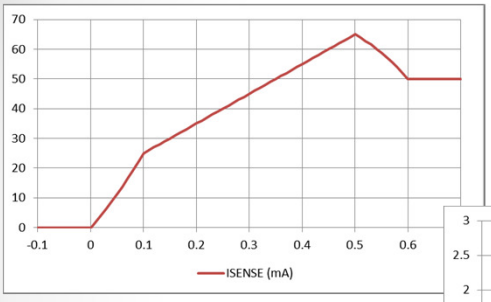
No C_comp, no clamps, just a Package model which could be a C_comp model or an on-die model



PU, PD Vout(t) node and Isense(t) are calculated using an ideal high gain (e.g., K=1e7) amplifier

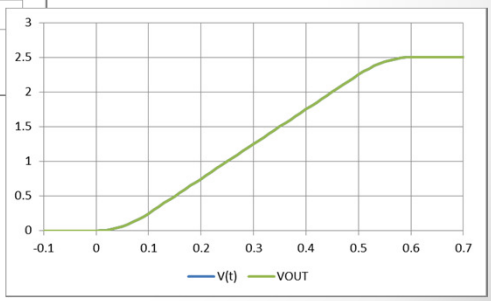
V-T table (originally extracted at the Fixture) is now a PWL driver

Lpkg = 0 nH, Cpkg = 0.004 nF



Closed-form references (50 Ω to GND)

Continuous V(t) and dV(t)/dt



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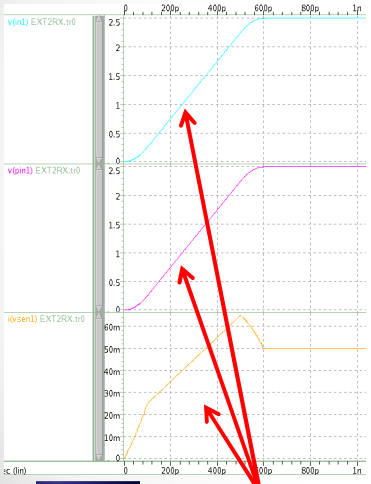
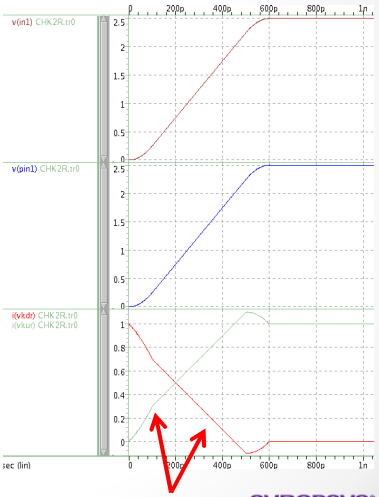
Extractions using Laplace Element





Same as closed-form references

K-tables

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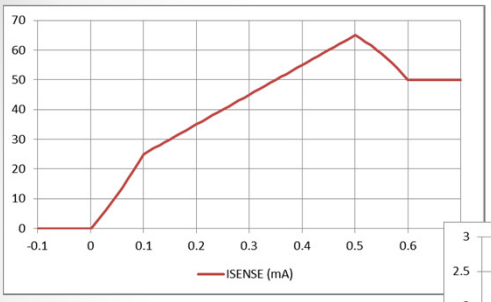
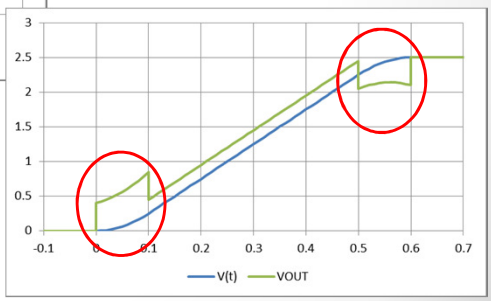
Lpkg = 2 nH, Cpkg = 0.004 nF



VOUT discontinuities: Feedback loop fails



Closed-form references (50 Ω to GND)

Observations and Conclusions

- Result accuracy
  - K-table extraction insensitive to K=1e5 to K=1e9 feedback multipliers
  - Requires SPICE maximum accuracy settings
  - Not sensitive to number of extraction points
- Severe test cases
  - Sharp waveform derivative discontinuity in ideal ramp
  - Large C_comp model load can be used
  - Large L_fixture, C_fixture reactive loads are ok
  - BOTH L_pkg, and C_pkg do not converge (even with smooth waveforms) – therefore topology limited and must use tool-dependent methods
  - Fails for T-line models (delay in feedback loop)
  - Works for S-parameter, Laplace transform, lumped models

IBIS Simulation Case Study:
Unexpected Glitch and Using C_fixture

Lance Wang
Asian IBIS Summit
Shanghai, China
Nov. 9th, 2015

Outline

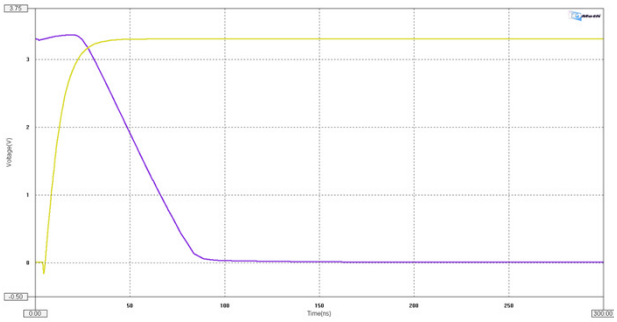
- Motivation
  - Unexpected glitch issue in the IBIS simulation
  - Seeking for solutions
- Case study and solutions
  - The root cause of glitch issue
  - Possible solutions
- Using C_fixture in IBIS V-T curves
- Conclusions

Motivation

- An unexpected glitch found when doing an IBIS model validation (transient analysis simulations)
  - An unexpected glitch found when we used < 450ps time step setting (called resolution setting in some EDA tools)
  - Everything is correct when we used bigger time step in the simulations
- Want to find out the root cause of this issue and solutions

The case study

- IBIS buffer model
  - This is normal I^2C pad buffer (Open Drain type)
  - It is relatively low speed buffer
    - About 60ns for rising and 300ns for falling to be settled with 4.7K ohm load and 3.3v to pull up

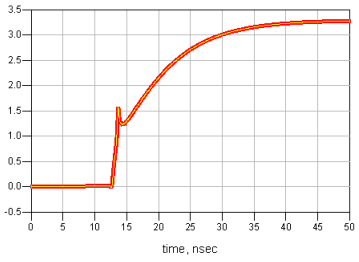


The case study

- Simulation results with the same condition as V-T fixture settings

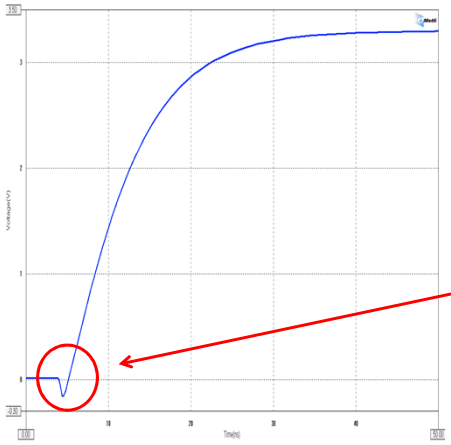
The case study

- A simulator bug?
  - We tried to use 5 different simulators and found all the results have the glitch issues. Only differences are the glitch levels



This is from another simulator

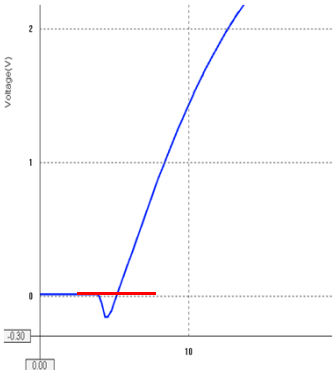
The case study



- IBIS Model issue?
  - IBIS curves are normal
  - 0 error, 0 warning from IBISCHK
  - Only Rising curve has a small “dip”

The case study

- We manually removed the “dip”. The simulation results are normal for all simulators
- So, this is the root cause. But WHY?

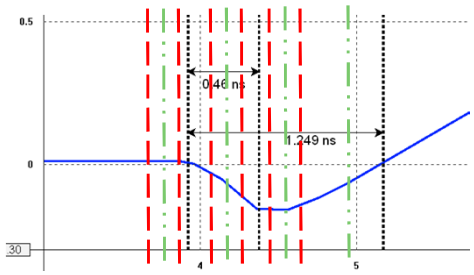


The root cause

Simulator works fine when the time step is bigger than the “dip down” period. It produces only 1 or 0 step in the “dip down” region. It would be “skipped” when it leads to a wrong direction

Simulator got confused when the time step is less than the “dip down” period when it produces 2 or more steps in the “dip down” region. It leads to a wrong direction without any information from I-V curves

The “dip” width is about 1.25ns. The dip down period is about 460ps.

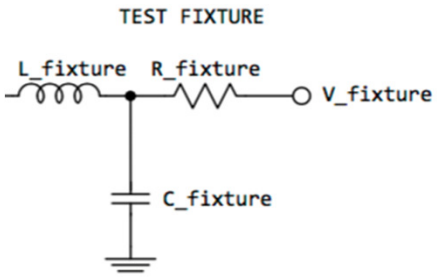


Solutions

- Using large time step size in transient analysis
  - It could lead to an inaccurate result
  - The setting needs to be manually forced. A dynamic step setting feature might not work.
- Manually remove the “dip” area in IBIS Model
- Adding C_fixture to reduce or make the “dip” area “lighter” or to disappear
  - This method leads to another discussion topic in this presentation

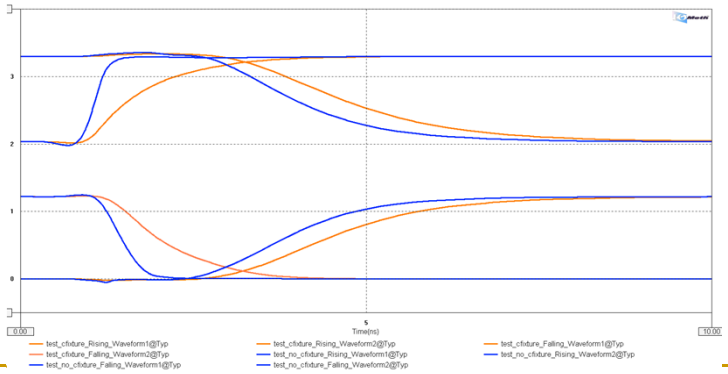
C_fixture setting in IBIS V-T section

- C_fixture optionally can be used in IBIS V-T waveforms
- We normally do not recommend using C_fixture in V-T curves



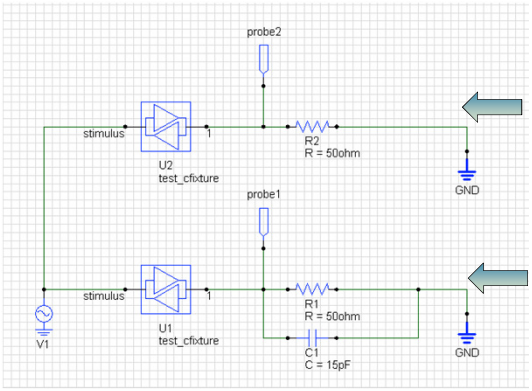
C_fixture test case

- We used the same Spice netlist to create 2 IBIS Models. All settings are the same except C_fixture
  - Blue – without C_fixture (C_fixture = 0)
  - Orange – with C_fixture (C_fixture = 15pF)



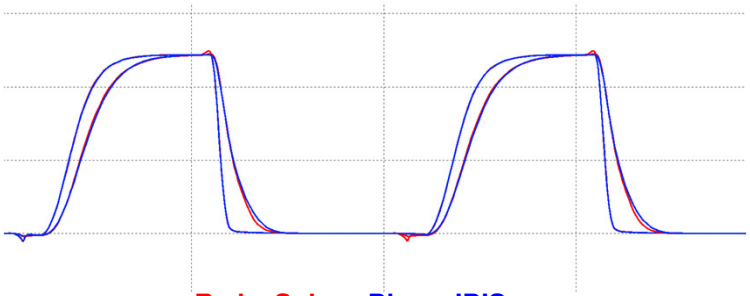
C_fixture test case

- Use both Models with this topology



C_fixture test case

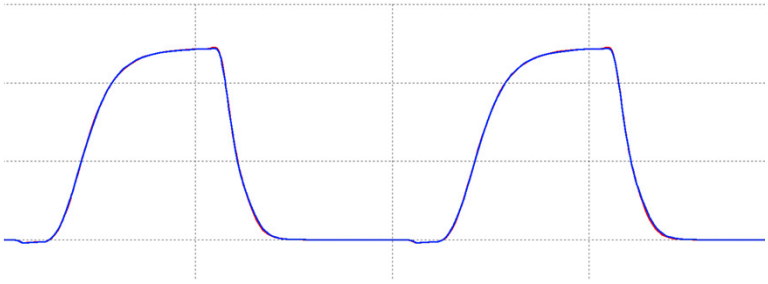
- Both cases correlate well with Spice simulations for C_fixture=0 IBIS Model



Red – Spice Blue – IBIS

C_fixture test case

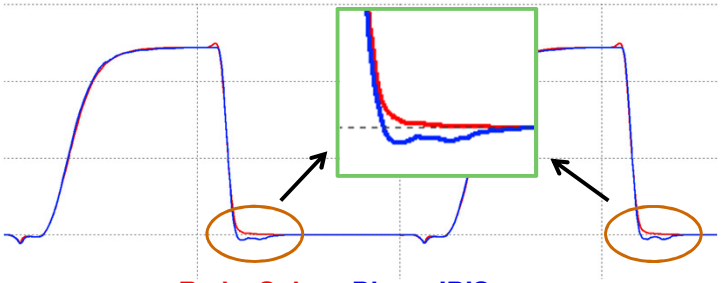
- The result from the load with capacitance correlates well with Spice simulations for C_fixture=15pF IBIS Model



Red – Spice Blue – IBIS

C_fixture test case

- The slight difference in results from the load without capacitance for C_fixture=15pF IBIS Model



Red – Spice Blue – IBIS

C_fixture test case

- C_fixture can be used in IBIS V-T curves
- Simulators need to use a de-capacitance algorithm when C_fixture is present in the V-T curves. C_fixture may reduce simulation accuracy
- It is better that IBIS V-T curves only have resistance load (linear load)

Supporting C_fixture in simulations

- This is a surprise!

3 out of 6 major simulators don't support C_fixture in IBIS Model.
It got ignored!

Summary

- In some simulations for a slow IBIS model, we found unexpected glitch in the result
  - It is due to a “dip down” area and it could be solved by using larger time step size (resolution value)
  - The “dip down” period could be removed manually or use C_fixture to reduce “dip down” area (size)
- Be careful when using C_fixture
  - It might cause some inaccurate simulation results
  - Some simulators do not support C_fixture in IBIS model
  - Recommend using linear load for V-T curves in IBIS model.

The Modeling Specialist

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http://www.iometh.com

Laplace Transform Time Response Utility

Bob Ross, Teraspeed Labs
bob@teraspeedlabs.com

Asian IBIS Summit
Shanghai, China
November 9, 2015

(Presented by Anders Ekholm, Ericsson)
Originally presented May 13, 2015

Some Applications

- **Show step and impulse response for network analysis**
- **Show step and impulse response for lower-order, reduced order (or pole-zero) Touchstone formulations in IBIS-AMI analysis**
- **Embed for time-response displays in analysis applications by inserting calculations at top**

Notation and Introduction

Laplace Transform

$$X(s) = \frac{a_{n-1}s^{n-1} + \cdots + a_0}{s^n + b_{n-1}s^{n-1} + \cdots + b_0},$$

Differential Equation

$$x^n(t) + b_{n-1}x^{n-1}(t) + \cdots + b_0 x(t) = 0$$

initial conditions, $x(0), \cdots, x^{n-1}(0),$

Utility calculates and displays immediately 101 points for $x^i(t)$, i=0 to i=26 for the time response and all of its derivatives

Extended for more time points by copying and pasting last row

Can be used as an embedded utility involving other Laplace Transform calculations

Enter Laplace Transform Num. and Den. Coefficients and Time-Step

Laplace Transform Numerator and Denominator Coefficients

a7	a6	a5	a4	a3	a2	a1	a0
0	1	-21	210	-1260	4725	-10395	10395
b7	b6	b5	b4	b3	b2	b1	b0
1	21	210	1260	4725	10395	10395	0

T-Step s

Select 0.08

Step Response of 6th order Bessel (maximally flat envelope delay, MFED) all-pass function

Change time-step to zoom-in or zoom-out and to change resolution

The graph auto-scales over 101 points

6th Order MFED All-Pass Step Response

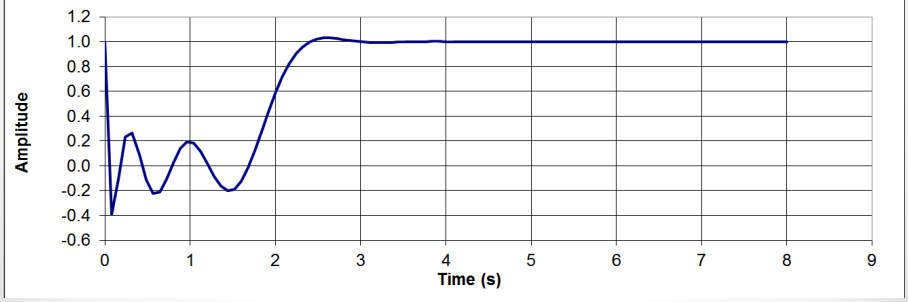
Laplace Transform Numerator and Denominator Coefficients

	a6	a5	a4	a3	a2	a1	a0
a7 0	1	-21	210	-1260	4725	-10395	10395
b7 1	b6 21	b5 210	b4 1260	b3 4725	b2 10395	b1 10395	b0 0

T-Step s
Select 0.08

Copy for Pasting

a6	a5	a4	a3	a2	a1	a0
1	-21	210	-1260	4725	-10395	10395
b6	b5	b4	b3	b2	b1	b0
21	210	1260	4725	10395	10395	0



6th Order MFED Low-Pass Step Response Input

Laplace Transform Numerator and Denominator Coefficients

	a6	a5	a4	a3	a2	a1	a0
a7 0							10395
b7 1	b6 21	b5 210	b4 1260	b3 4725	b2 10395	b1 10395	b0 0

T-Step s
Select 0.08

Convert all-pass to low-pass filter by zeroing out numerator coefficients (click/back-space or enter 0) for real-time modification

6th Order MFED Low-Pass Step Response

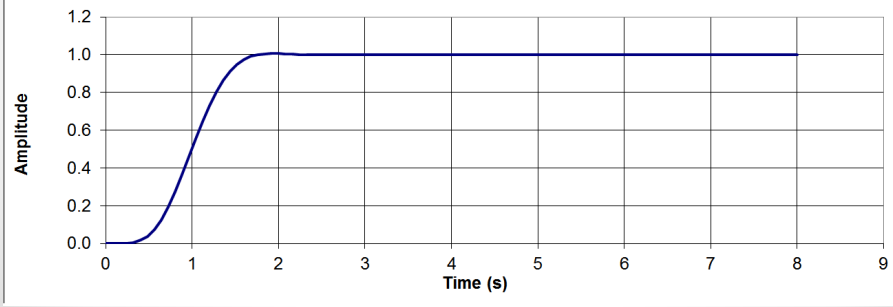
Laplace Transform Numerator and Denominator Coefficients

	a6	a5	a4	a3	a2	a1	a0
0							10395
b7	b6	b5	b4	b3	b2	b1	b0
1	21	210	1260	4725	10395	10395	0

T-Step s
Select 0.08

Copy for Pasting

a6	a5	a4	a3	a2	a1	a0
1	-21	210	-1260	4725	-10395	10395
b6	b5	b4	b3	b2	b1	b0
21	210	1260	4725	10395	10395	0



7th Order MFED Low-Pass Impulse Response Input

Laplace Transform Numerator and Denominator Coefficients

	a6	a5	a4	a3	a2	a1	a0
0	0	0	0	0	0	0	135135
b7	b6	b5	b4	b3	b2	b1	b0
1	28	378	3150	17325	62370	135135	135135

T-Step s
Select 0.025

7th Order MFED Low-Pass Impulse Response

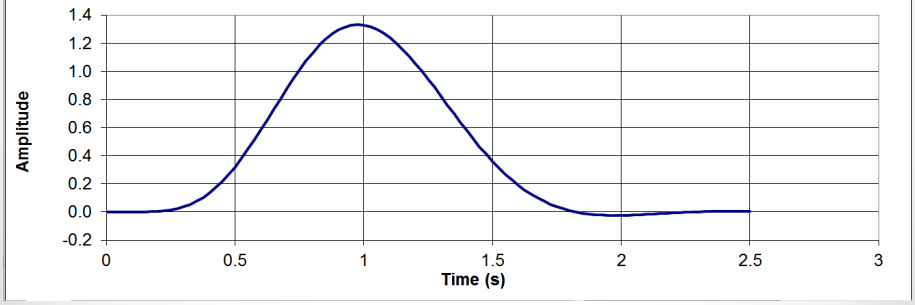
Laplace Transform Numerator and Denominator Coefficients

	a7	a6	a5	a4	a3	a2	a1	a0
	0	0	0	0	0	0	0	135135
	b7	b6	b5	b4	b3	b2	b1	b0
	1	28	378	3150	17325	62370	135135	135135

T-Step s
Select 0.025

Copy for Pasting

a6	a5	a4	a3	a2	a1	a0
1	-21	210	-1260	4725	-10395	10395
b6	b5	b4	b3	b2	b1	b0
21	210	1260	4725	10395	10395	0



X(s) = 1/(s² + 1) Sine Wave with Left-Shifted Coefficients

Laplace Transform Numerator and Denominator Coefficients

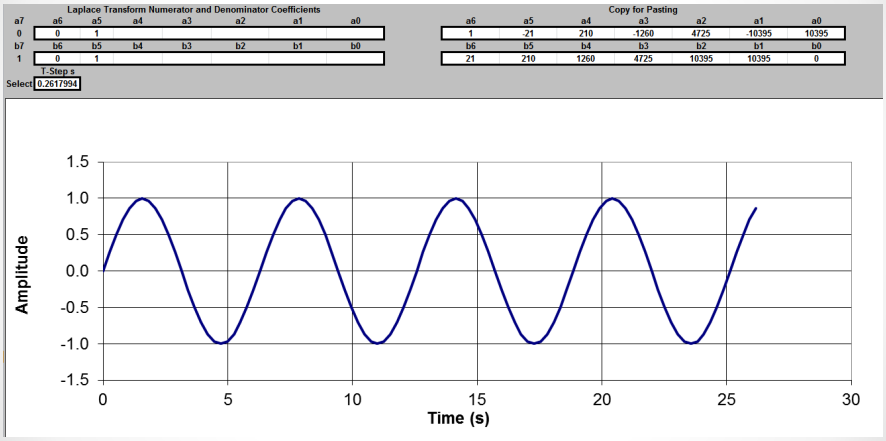
	a7	a6	a5	a4	a3	a2	a1	a0
	0	0	1					
	b7	b6	b5	b4	b3	b2	b1	b0
	1	0	1					

T-Step s
Select 0.2617994

Set Time-Step =PI()/12 for exact π/12 (15 degree) steps

Can compare response with exact solution: x(t) = sin(πt/12)

Sine Wave Response



Recursive Taylor Series Method (Repeat b and c)

a) Initialize: *i* = 1, … , *n*-1 (n = 7)

$$x(0) = a_{n-1} \qquad x^i(0) = a_{n-1-i} - \sum_{j=0}^{i-1} b_{n-i-j}\, x^j(0)$$

b) Extend: *i* = *n*, … , *p* (p = 26)

$$x^i(t) = - \sum_{j=0}^{n-1} b_j\, x^{i-n-j}\,(t)$$

c) Next time step: *i* = 0, … , *n*-1 (Taylor Series)

$$x^i(t+T) = \sum_{j=i}^{p} x^j(t) \frac{T^{j-i}}{(j-i)!}$$

R. I. Ross, "Evaluating the Transient Response of a Network Function," *Proc. IEEE*, vol.55, pp. 615-616, May 1967

Spread Sheet Details

Laplace Transform Numerator and Denominator Coefficients

a7	a6	a5	a4	a3	a2	a1	a0
0	0	1					
b7	b6	b5	b4	b3	b2	b1	b0
1	0	1					

Copy for Pastin

a6	a5	a4	a3
1	-21	210	-1260
b6	b5	b4	b3
21	210	1260	4725

T-Step s
Select 0.2617994

(a) Initialize

Copy to Reset Sheet

N	0	1	2	3	4	5	6	7	8	9	10
T^n/n!	1	0.2617994	0.0342695	0.002990575	0.000195733	1.02485E-05	4.47177E-07	1.67244E-08	5.47304E-10	1.59204E-11	4.16796E-13

$V^{(N)}(t)$ / t	0	1	2	3	4	5	6	7	8	9	10
0	0.0000	1.000E+00	0.000E+00	-1.000E+00	0.000E+00	1.000E+00	0.000E+00	-1.000E+00	0.000E+00	1.000E+00	0.000E+00
0.2617994	0.2588	9.659E-01	-2.588E-01	-9.659E-01	2.588E-01	9.659E-01	-2.588E-01	-9.659E-01	2.588E-01	9.659E-01	-2.588E-01
0.5235988	0.5000	8.660E-01	-5.000E-01	-8.660E-01	5.000E-01	8.660E-01	-5.000E-01	-8.660E-01	5.000E-01	8.660E-01	-5.000E-01
0.7853982	0.7071	7.071E-01	-7.071E-01	-7.071E-01	7.071E-01	7.071E-01	-7.071E-01	-7.071E-01	7.071E-01	7.071E-01	-7.071E-01
1.0471976	0.8660	5.000E-01	-8.660E-01	-5.000E-01	8.660E-01	5.000E-01	-8.660E-01	-5.000E-01	8.660E-01	5.000E-01	-8.660E-01
1.3089969	0.9659	2.588E-01	-9.659E-01	-2.588E-01	9.659E-01	2.588E-01	-9.659E-01	-2.588E-01	9.659E-01	2.588E-01	-9.659E-01
1.5707963	1.0000	7.342E-16	-1.000E+00	-7.342E-16	1.000E+00	7.342E-16	-1.000E+00	-7.342E-16	1.000E+00	7.342E-16	-1.000E+00
1.8325957	0.9659	-2.588E-01	-9.659E-01	2.588E-01	9.659E-01	-2.588E-01	-9.659E-01	2.588E-01	9.659E-01	-2.588E-01	-9.659E-01
2.0943951	0.8660	-5.000E-01	-8.660E-01	5.000E-01	8.660E-01	-5.000E-01	-8.660E-01	5.000E-01	8.660E-01	-5.000E-01	-8.660E-01
2.3561945	0.7071	-7.071E-01	-7.071E-01	7.071E-01	7.071E-01	-7.071E-01	-7.071E-01	7.071E-01	7.071E-01	-7.071E-01	-7.071E-01
2.6179939	0.5000	-8.660E-01	-5.000E-01	8.660E-01	5.000E-01	-8.660E-01	-5.000E-01	8.660E-01	5.000E-01	-8.660E-01	-5.000E-01

(c) x(t+T) Taylor Series for new row

(b) Extend thru N=26

Accurate Time Response for $X(s) = 1/(s^2 + 1)$; $x(t) = \sin(\pi t/12)$

	X	Y	Z	AA	AB	AC
103	-1.05412673E-14	1.00000000E+00	1.05412673E-14	-1.00000000E+00	-1.05412673E-14	1.00000000E+00
104	2.58819045E-01	9.65925826E-01	-2.58819045E-01	-9.65925826E-01	2.58819045E-01	9.65925826E-01
105	5.00000000E-01	8.66025404E-01	-5.00000000E-01	-8.66025404E-01	5.00000000E-01	8.66025404E-01
106	7.07106781E-01	7.07106781E-01	-7.07106781E-01	-7.07106781E-01	7.07106781E-01	7.07106781E-01
107	8.66025404E-01	5.00000000E-01	-8.66025404E-01	-5.00000000E-01	8.66025404E-01	5.00000000E-01
108	9.65925826E-01	2.58819045E-01	-9.65925826E-01	-2.58819045E-01	9.65925826E-01	2.58819045E-01
109	1.00000000E+00	1.10769747E-14	-1.00000000E+00	-1.10769747E-14	1.00000000E+00	1.10769747E-14
110	9.65925826E-01	-2.58819045E-01	-9.65925826E-01	2.58819045E-01	9.65925826E-01	-2.58819045E-01
111	8.66025404E-01	-5.00000000E-01	-8.66025404E-01	5.00000000E-01	8.66025404E-01	-5.00000000E-01
112	7.07106781E-01	-7.07106781E-01	-7.07106781E-01	7.07106781E-01	7.07106781E-01	-7.07106781E-01
113	5.00000000E-01	-8.66025404E-01	-5.00000000E-01	8.66025404E-01	5.00000000E-01	-8.66025404E-01

Iterative calculation = exact response to 9 digits
- **up to 101 data points**
- **up to the 26th derivative**

(Table resolution increased to 9 digits to show accuracy)

5th-order Step Response

Laplace Transform Numerator and Denominator Coefficients

a7	a6	a5	a4	a3	a2	a1	a0
0				-4	4		
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
1	6	13	12	4	0		

T-Step s
Select 0.25

$X(s) = 4(-s + 1)/[(s + 1)^2 (s + 2)^2 s] = (-4s + 4)/(s^5 + 6s^4 + 13s^3 + 12s^2 + 4s)$

Laplace transform is normalized ($b_7 = 1$)
Left-shift the numerator and denominator coefficients
Step response means b_2 is 0
Right-hand plane zero creates pre-shoot

5th-Order Step Response

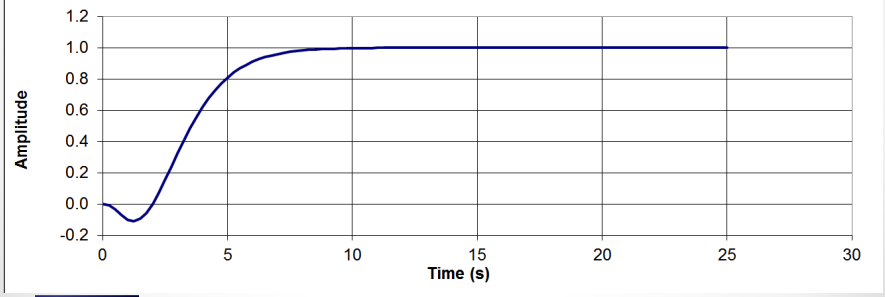
Laplace Transform Numerator and Denominator Coefficients

a7	a6	a5	a4	a3	a2	a1	a0
0				-4	4		
b7	b6	b5	b4	b3	b2	b1	b0
1	6	13	12	4	0		

T-Step s
Select 0.25

Copy for Pasting

a6	a5	a4	a3	a2	a1	a0
1	-21	210	-1260	4725	-10395	10395
b6	b5	b4	b3	b2	b1	b0
21	210	1260	4725	10395	10395	0



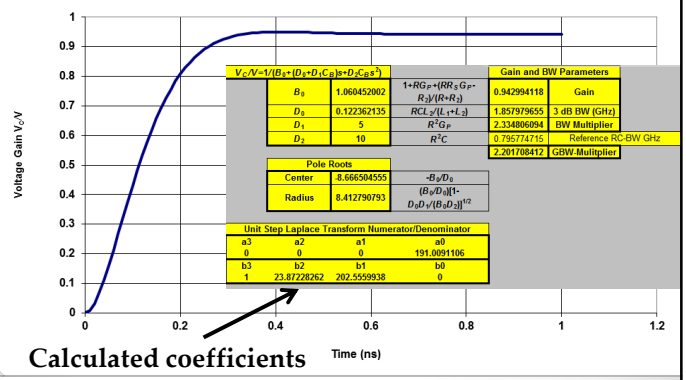
Embedded with Constant-R Bridged T-Coil Calculations

Bridged T-Coil Input	
R	50
C (pF)	4
R_S	10
G_P (1/R_P)	0.002
R_1	1.9073

C (nF)	0.004
R_P	500

T-step (ns)	0.01
Theta (deg)	33

Calculated Values		Value, Formulas
C_B (pF)	0.523535237	C_B (nF) 0.000523535
R_1	1.9073	Choose R_1 above so that R_2 >= 0
R_2 (Check R_2>=0)	3.099998636	$R_2=[R^2G_P-R_1(1+G_P(R_S+R))]/(1+G_P(R_1+R_S-R))$
L_1+L_2 (nH)	10.01459727	$\{(R-R_1)^2/[1+G_P(R_1+R_S-R)]\}C$
L_1 (nH)	3.887559745	$(R_1-R)(R_1+R_S-R)/\{1+[(1+G_P(R_1+R_S-R)]+[1+G_P(R_1+R_S-R)]^{1/2}\}$*C
L_2 (nH)	6.127037527	
L_3 (nH)	-1.069612463	$R^2C_B-L_1L_2/(L_1+L_2)$



Scaled Time (ns), L (nH), C (nF) with 3rd order Laplace Transform sheet

Closed-form equations inserted above Time Response

Guidance

- Normalize coefficients (highest order denominator coefficient set to 1)
- Scale coefficients so that values are meaningful for time-steps between 0.01 and 1 (because of Taylor Series expansion)
- Left-shift the entries for lower-order functions
- Change time-step to zoom-in or zoom-out
- Get numerical values from spread sheet
- Copy and paste last row to extend spread sheet for more time rows (also adjust display range)

Final Remarks

- Works with real, complex, multiple roots, pole-zero canceled roots, and right-hand plane zeros
- Response fast even though spread-sheet implementation is based on inefficient storage
- Recursive routine (slide 11) can be done in-place for better storage efficiency in other programming applications
- Display shows changes as coefficients are modified
- Display diverges if Laplace Transform close-form response diverges

IBIS Summit
Downloads and References

- www.ibis.org/summits/nov15a/
  - ross2.xls (time-response utility)
  - ross2.pdf (this presentation for instructions, examples)
- www.ibis.org/summits/may11/
  - ross3.pdf, "Continuous and Discrete Modeling for IBIS-AMI" (gives theoretical background for both differential and difference equations)
  - ross2.pdf, "T-Coils and Bridged-T Networks" (gives general T-coil derivations)