IBIS Package Model
(Past, Present, What's Next)

Asian IBIS Summit
Yokohama, Japan
November 20, 2014

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IBIS Model Version

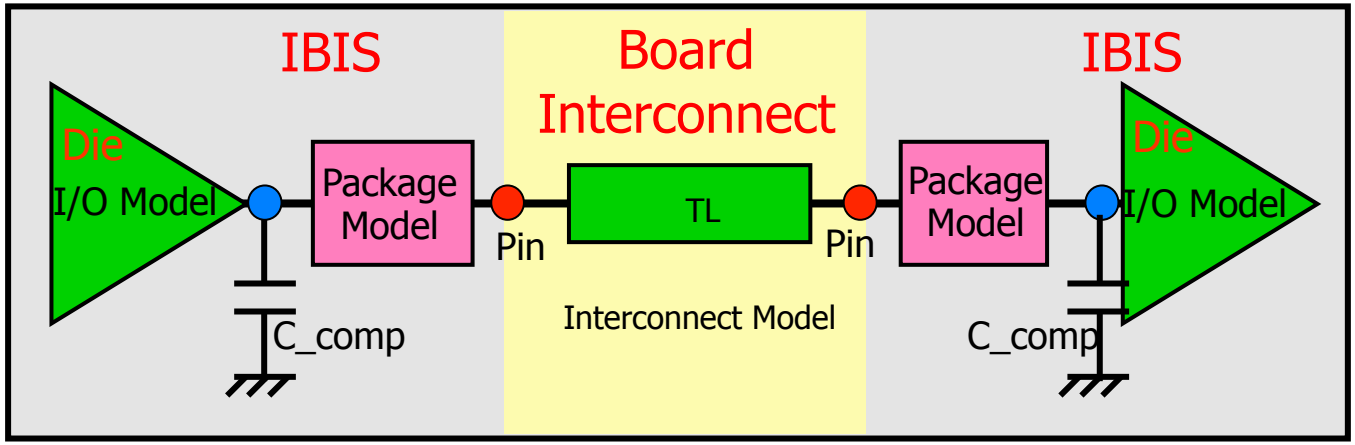
• Version 1.0	1993.04	
• Version 1.1	1993.06	
• Version 2.0	1994.06	
• Version 2.1	1995.12	ANSI/EIA-656
• Version 3.0	1997.06	
• Version 3.2	1999.09	ANSI/EIA-656A
• Version 4.0	2002.07	
• Version 4.1	2003.02	
• Version 4.2	2006.06	ANSI/EIA-656B
• Version 5.0	2008.08	IBIS AMI
• Version 5.1	2012.08	
• Version 6.0	2013.09	

IBIS vs. Signal Speed

			PCI 1.0/2.0	33 MHz
• Version 1.0	1993.04	R,L,C		
• Version 1.1	1993.06			
			PCI 2.1	66 MHz
• Version 2.0	1994.06			
• Version 2.1	1995.12			
• Version 3.0	1997.06	EBD		
• Version 3.2	1999.09			
			DDR SDRAM	100-200 MHz
			PCI Express Gen1	1.25 GHz
• Version 4.0	2002.07			
• Version 4.1	2003.02			
			DDR2	200-533 MHz
• Version 4.2	2006.06			
			DDR3	400-1066 MHz
			PCI Express Gen2	2.5 GHz
• Version 5.0	2008.08	IBIS AMI		
			PCI Express Gen3	4 GHz
			DDR4	1066-2133 MHz
• Version 5.1	2012.08			
• Version 6.0	2013.09			
			PCI Express Gen4	8 GHz

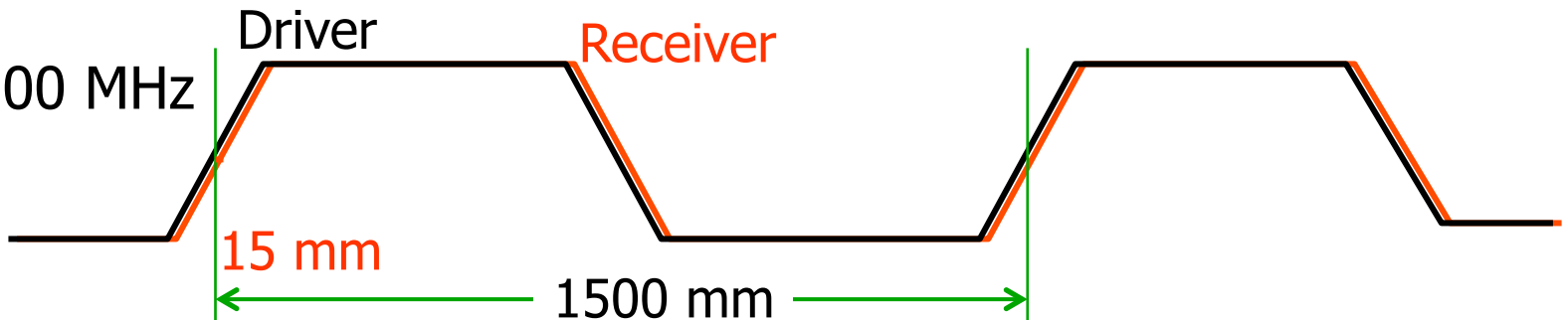
IBIS Model

- I/O Buffer + Chip Capacitor + Connection inside Package
  (I/O Model) (C_comp) (Package Model)

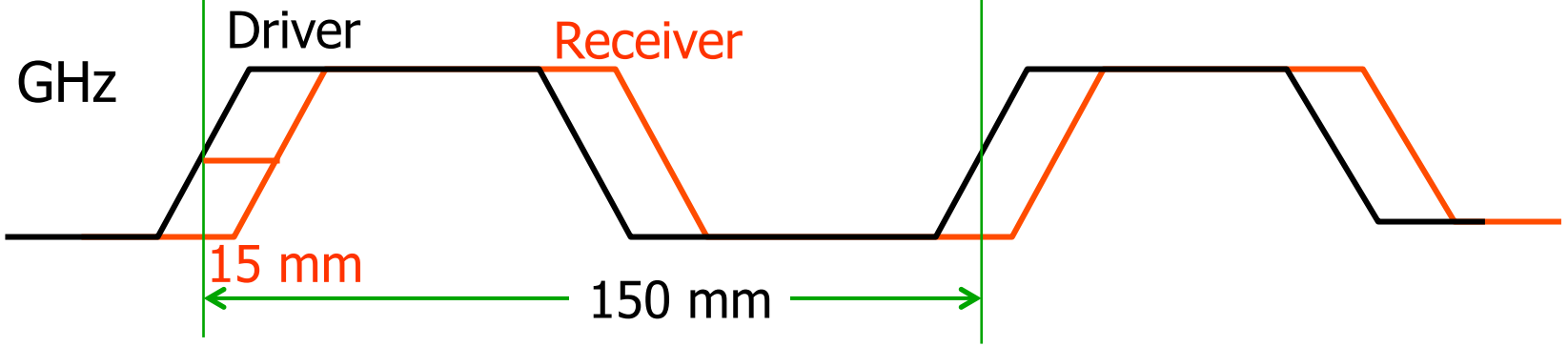


Effect of Connection inside Package

- Etch Length: 5 ~ 20 mm
- 100 MHz



- 1 GHz



Version 1.0 - 2.1

- Package Model

[Package]

variable	typ	min	max
R_pkg	250.0m	225.0m	275.0m
L_pkg	15.0nH	12.0nH	18.0nH
C_pkg	18.0pF	15.0pF	20.0pF

Individual Pin Model

[Pin]	signal_name	model_name	R_pin	L_pin	C_pin
1	RAS0#	Buffer1	200.0m	5.0nH	2.0pF
2	RAS1#	Buffer2	209.0m	NA	2.5pF
3	EN1#	Input1	NA	6.3nH	NA
4	A0	3-state			
5	D0	I/O1			
6	RD#	Input2	310.0m	3.0nH	2.0pF
7	WR#	Input2			
8	A1	I/O2			
9	D1	I/O2			
10	GND	GND	297.0m	6.7nH	3.4pF
11	RDY#	Input2			
12	GND	GND	270.0m	5.3nH	4.0pF
.					
.					
.					
18	VCC3	POWER			
19	NC	NC			
20	Vcc5	POWER	226.0m	NA	1.0pF

Version 3.0

- Enhancement To The Package Model

| [Package Model]
| •
| •
| [Define Package Model] Required if the [Package Model] keyword is used
| [Manufacturer] (note 1)
| [OEM] (note 1)
| [Description] (note 1)
| [Number Of Sections] (Optional)
| [Number Of Pins] (note 1)
| [Pin Numbers] (note 1)
| [Model Data] (note 1)
| [Resistance Matrix] Optional
| [Inductance Matrix] (note 1)
| [Capacitance Matrix] (note 1)
| [Bandwidth] Required (for Banded_matrix matrices only)
| [Row] (note 1)
| [End Model Data] (note 1)
| [End Package Model] (note 1)

Two Different Definitions

- Physical Layout Definition
  [Number of Sections]
- Electrical Effect Matrix
  [Model Data]
  •
  •
  [End Model Data]

Ver3.2

Either the [Number Of Sections] or the [Model Data]/[End Model Data] keywords are required.

Note that [Number of Sections] and the [Model Data]/[End Model Data] keywords are mutually exclusive.

[Number Of Sections]

- Physical Layout

```
[Number Of Sections] 2
[Number Of Pins]   4
[Pin Numbers]
A1 Len=0 L=1.2n/ Len=1.2 L=2.0n C=0.5p R=0.05/ Len=0 L=2.0n C=1.0p/
|
A2 Len=0 L=1.2n/ Len=0/ Len=1.2 L=2.0n C=0.5p R=0.05/ Len=0 L=2.0n C=1.0p/
|
B1 Len=0 L=2.3n /                  | bondwire
Len=1.2 L=1.0n C=2.5p /            | first section
 Fork                              | indicates the starting of a branch
 Len=1.0 L=2.0n C=1.5p /           | section
 Endfork                           | ending of the branch
Len=0.5 L=1.0 C=2.5p/              | second section
Len=0.0 L=1.5n /                   | pin
|
B13 Len=0 L=2.3n /                 | bondwire
Len=1.2 L=1.0n C=2.5p /            | first section
Len=0.5 L=1.0 C=2.5/               | second section, pin connects here
Fork                               | indicates the starting of a branch
Len=1.0 L=2.0n C=1.5p /            | section
Endfork                            | ending of the branch
```

[Number Of Sections]

- Physical Layout

A1 Len=0 L=1.2n/ Len=1.2 L=2.0n C=0.5p R=0.05/ Len=0 L=2.0n C=1.0p/

Bonding Wire L=1.2nH

Etch length = 1.2
L=2.0nH x 1.2
C=0.5pF x 1.2
R=0.05Ω x 1.2

Via
L=2.0nH
C=1.0pF

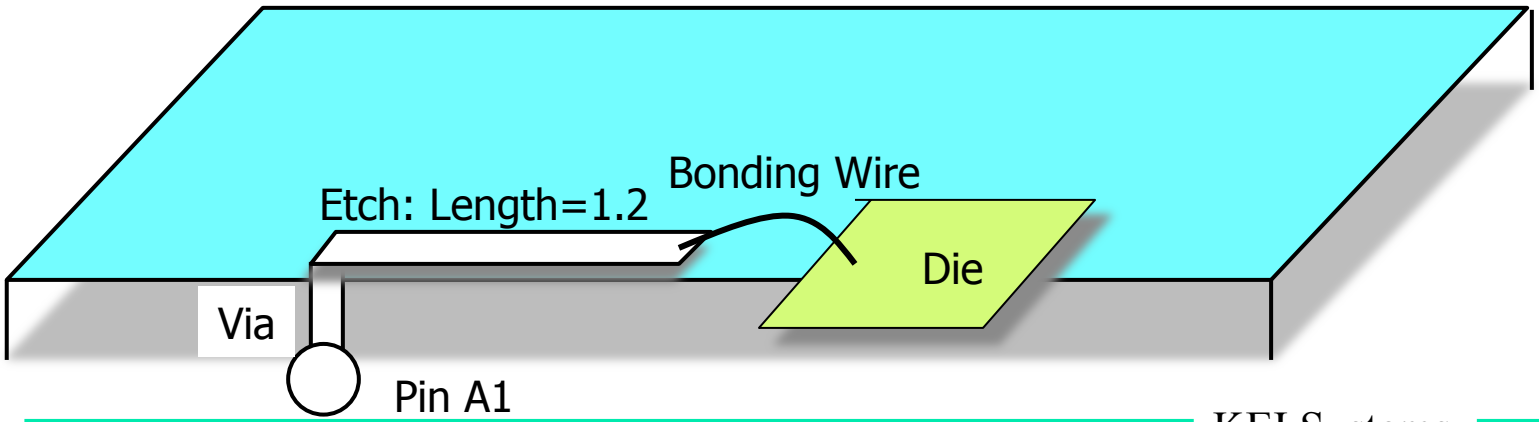
A2 Len=0 L=1.2n/ Len=0/ Len=1.2 L=2.0n C=0.5p R=0.05/ Len=0 L=2.0n C=1.0p/

Bonding Wire L=1.2nH

No data

Etch length = 1.2
L=2.0nH x 1.2
C=0.5pF x 1.2
R=0.05Ω x 1.2

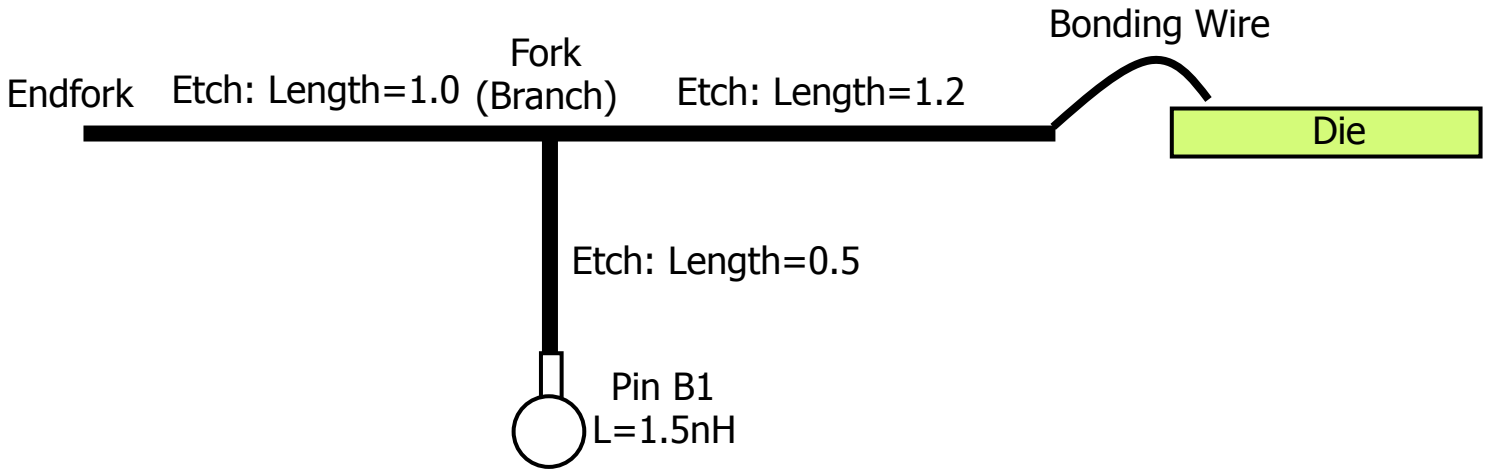
Via
L=2.0nH
C=1.0pF



[Number Of Sections]

- Physical Layout

```
B1 Len=0 L=2.3n /          | bondwire
Len=1.2 L=1.0n C=2.5p /    | first section
  Fork                     | indicates the starting of a branch
  Len=1.0 L=2.0n C=1.5p /  | section
  Endfork                  | ending of the branch
Len=0.5 L=1.0 C=2.5p/      | second section
Len=0.0 L=1.5n /           | pin
```



[Model Data]

- Electrical Effect Matrix

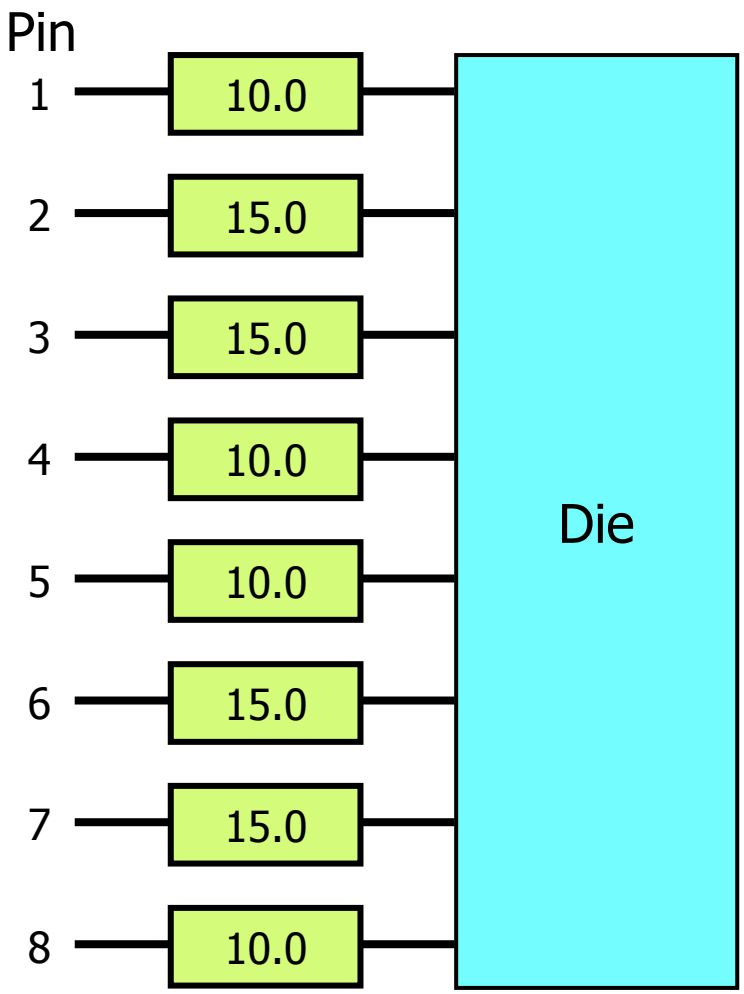
[Model Data]
[Resistance Matrix]
[Inductance Matrix]
[Capacitance Matrix]
| [Bandwidth] Banded_matrix matrices only
[Row]

[Number Of Pins] 8
|
[Pin Numbers]
1
2
.
.
8
|
[Model Data]
|
[Resistance Matrix] Banded_matrix
[Bandwidth] 0
.
.
[Inductance Matrix] Full_matrix
.
.
[Capacitance Matrix] Sparse_matrix
.
.
[End Model Data]
[End Package Model]

Banded_Matrix

- No Coupling

[Resistance Matrix] Banded_matrix
[Bandwidth] 0
[Row] 1
10.0
[Row] 2
15.0
[Row] 3
15.0
[Row] 4
10.0
[Row] 5
10.0
[Row] 6
15.0
[Row] 7
15.0
[Row] 8
10.0



Full_Matrix

- All Pins Coupling Together

[Inductance Matrix] Full_matrix

[Row] 1

3.04859e-07	4.73185e-08	1.3428e-08	6.12191e-09
1.74022e-07	7.35469e-08	2.73201e-08	1.33807e-08

[Row] 2

3.04859e-07	4.73185e-08	1.3428e-08	7.35469e-08
1.74022e-07	7.35469e-08	2.73201e-08	

[Row] 3

3.04859e-07	4.73185e-08	2.73201e-08	7.35469e-08
1.74022e-07	7.35469e-08		

[Row] 4

3.04859e-07	1.33807e-08	2.73201e-08	7.35469e-08
1.74022e-07			

[Row] 5

4.70049e-07	1.43791e-07	5.75805e-08	2.95088e-08

[Row] 6

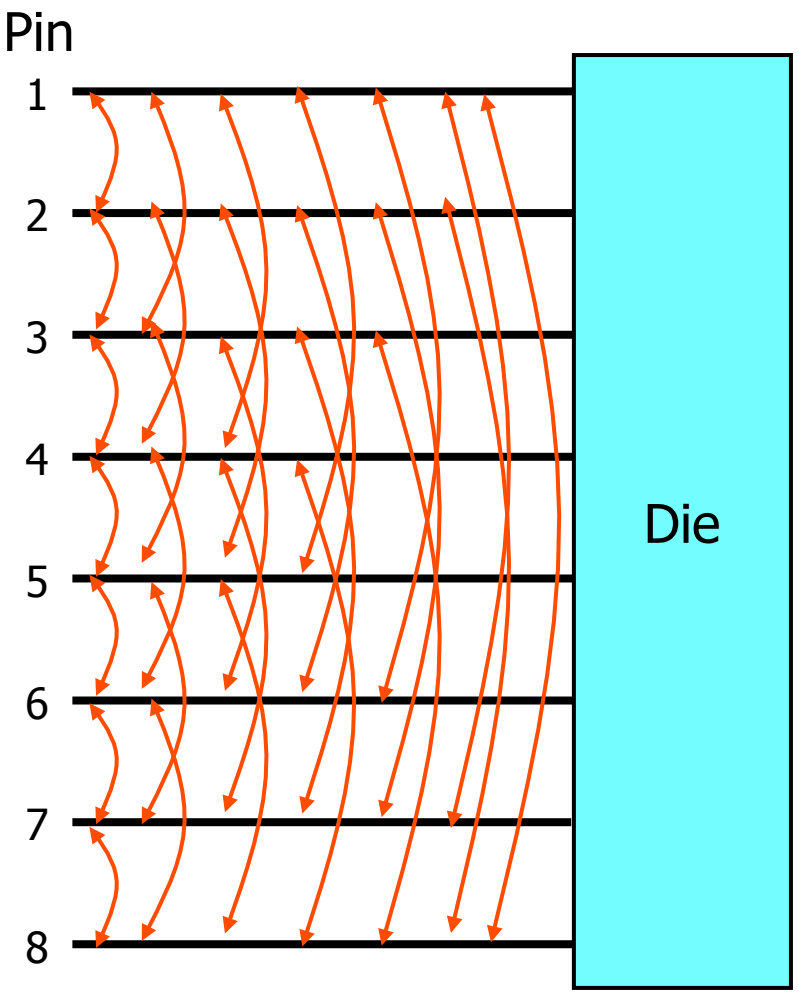
4.70049e-07	1.43791e-07	5.75805e-08	

[Row] 7

4.70049e-07	1.43791e-07		

[Row] 8

4.70049e-07



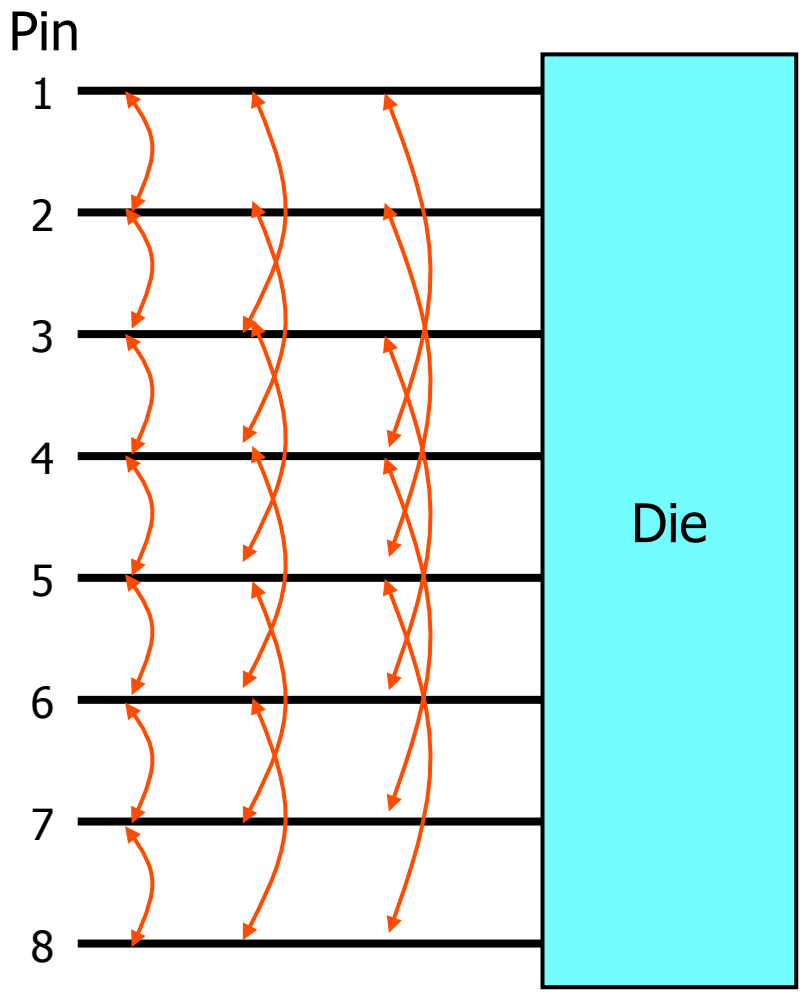
Sparse_Matrix

- Matrix between selected pins

[Capacitance Matrix] Sparse_matrix

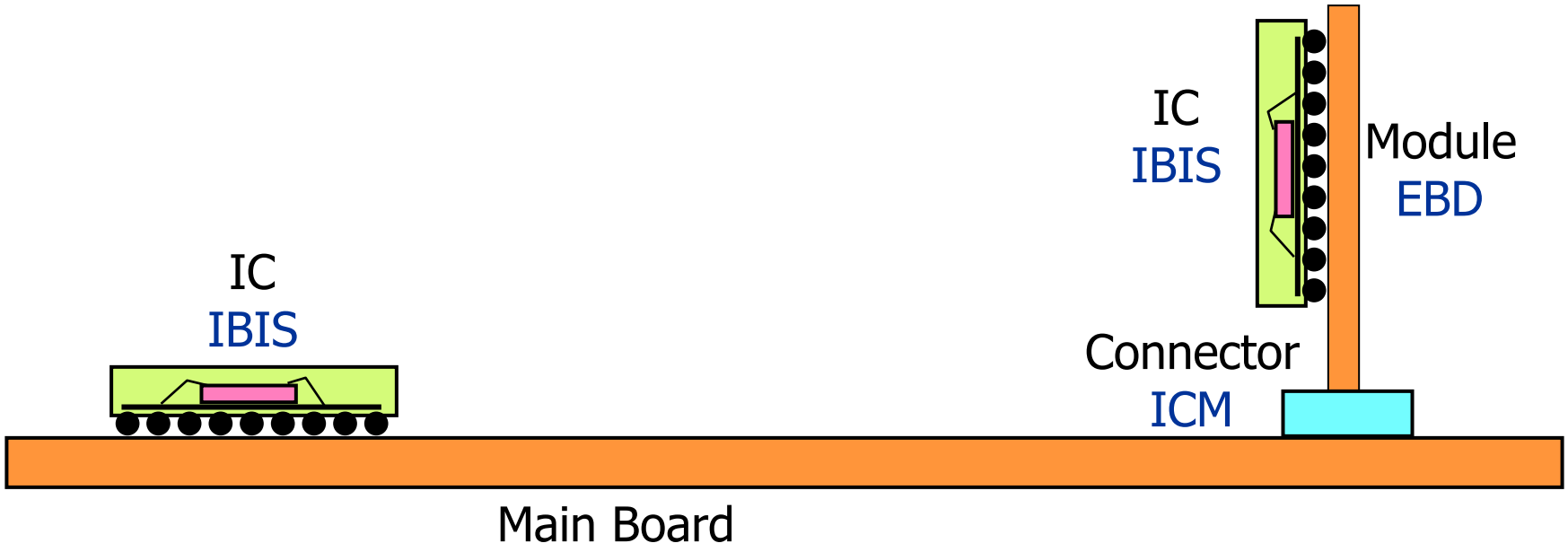
[Row] 1
1 2.48227e-10
2 -1.56651e-11
3 -9.54158e-11
[Row] 2
2 2.51798e-10
3 -1.56552e-11
4 -6.85199e-12
[Row] 3
3 2.51798e-10
4 -1.56651e-11
5 -6.82003e-12
[Row] 4
4 2.48227e-10
5 -7.15684e-12
6 -9.54158e-11

[Row] 5
5 1.73542e-10
6 -3.38247e-11
7 -9.0486e-11
[Row] 6
6 1.86833e-10
7 -3.27226e-11
8 -6.85199e-12
[Row] 7
7 1.86833e-10
8 -3.38247e-11
[Row] 8
8 1.73542e-10



Electric Board Description (EBD)

- .EBD File
  - Description of Sub-circuit Module on Board



EBD Sample

- SIMM

```
[Begin Board Description]
[Manufacturer]
[Number Of Pins]     240
[Pin List]  signal_name
1          POWER          |
2          GND            |
3          DQ0R           |
4          DQ1R           |
.
.
240      DQ1N             |
 |
[Path Description] 3
Pin 3
Len=0.07450 L=9.01289e-009 C=2.78361e-012 R=0.09740 /
Len=0 R=22.00000 /
Len=0.68672 L=9.01289e-009 C=2.78361e-012 R=0.09740 /
Len=0 C=2.18420e-013 /
Len=0.06746 L=9.01289e-009 C=2.78361e-012 R=0.09740 /
Node U1.K8
.  ⇩
.
.  ⇩
.
[Path Description] DQ1R
Pin 4
Len = 0   L=2.0n /
Len = 2.1 L=6.0n C=2.0p /
 Fork
 Len = 1.0 L = 1.0n C= 2.0p /
 Node U2.15
 Endfork
Len = 1.0 L = 6.0n C=2.0p /
Pin 240
|
[Reference Designator Map]
| Ref Des  File name   Component
R1         r_200.ibs          resistor_series
R2         r_200.ibs          resistor_series
U1         u58a.ibs           processor
U2        eeprom_nc.ibs      eeprom

[End Board Description]

[End]
```

Other IBIS Open Forum Works

- ICM 1.1　　2005.07 (ANSI/SEIA-STD-0001)
  - IBIS Interconnect Modeling Specification
- Touchstone 2.0 (2009.04)
- IBIS-ISS 1.0 2011.10
  - IBIS Interconnect SPICE Subcircuit Specification

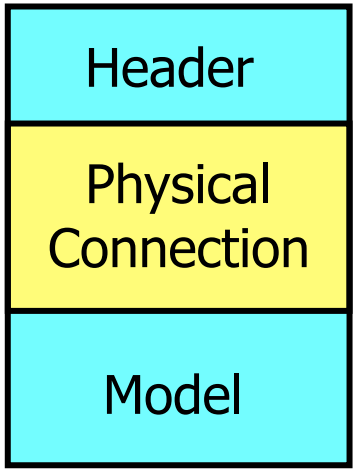
IBIS vs. Signal Speed

			PCI 1.0/2.0	33 MHz
• Version 1.0	1993.04	R,L,C		
• Version 1.1	1993.06			
			PCI 2.1	66 MHz
• Version 2.0	1994.06			
• Version 2.1	1995.12			
• Version 3.0	1997.06	EBD		
• Version 3.2	1999.09			
			DDR SDRAM	100-200 MHz
			PCIe Gen1	1.25 GHz
• Version 4.0	2002.07			
• Version 4.1	2003.02			
	ICM		DDR2	200-533 MHz
• Version 4.2	2006.06			
			DDR3	400-1066 MHz
			PCIe Gen2	2.5 GHz
• Version 5.0	2008.08	IBIS AMI		
	Touchstone		PCIe Gen3	4 GHz
	IBIS-ISS		DDR4	1066-2133 MHz
• Version 5.1	2012.08			
• Version 6.0	2013.09			
			PCIe Gen4	8 GHz

ICM

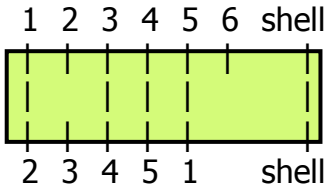
- IBIS Interconnect Modeling Specification

  This specification for general purpose interconnect modeling in an IBIS compatible format.
  It was written to provide means for modeling all electrical interconnect types, including connectors, cables, packages, and printed circuit boards.



Fork - Endfork
Map List

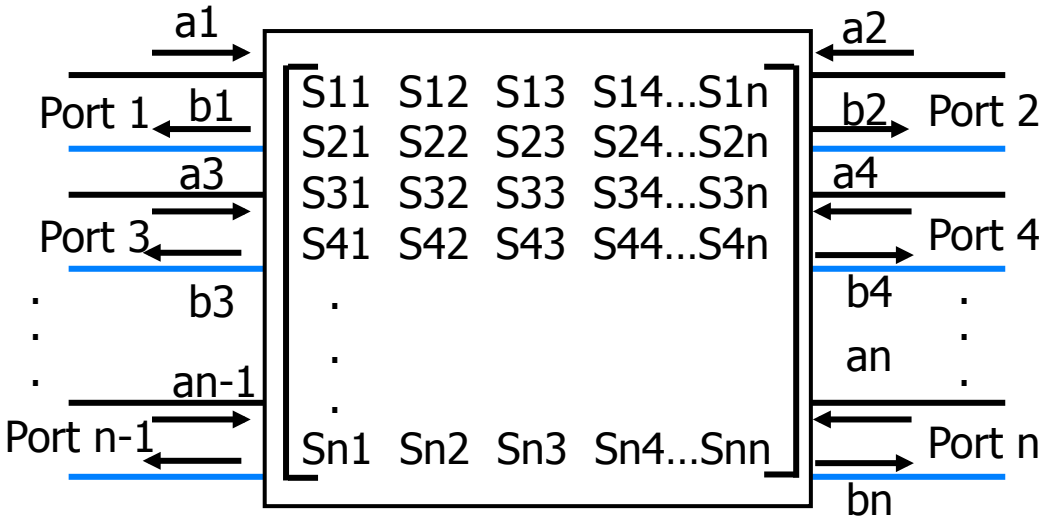
R-L-C Matrix
S-Parameter



PS2 6-pin female mini DIN
Section for connector pins
Section for wiring
Section for connector pins
5-pin male DIN

Touchstone

- S(Y,Z,H,G)-Parameter
- S Parameter
  - Reflection-Transfer
  - Frequency Depend
  - n-Ports



This document, based upon information from Agilent Corporation (the originator of Touchstone), is a formal specification of the Touchstone file format, intended for use with documents and specifications produced by the EIA/IBIS Open Forum.

IBIS-ISS

- **IBIS Interconnect SPICE Subcircuit (IBIS-ISS)**
  - **Support**
    - Subset of HSPICE Language
    - elementary circuit elements (resistors, capacitors, inductors)
    - transmission line elements (lossless and lossy)
    - frequency-domain network parameters (e.g., S-parameters)
    - parameter/variable passing to elements and subcircuits
    - dependent and limited independent sources
    - string-based node naming
    - user-defined comments
    - abstraction through modular, user-defined subcircuit definitions

IBIS-ISS

- Transmission Line Element
  - T-element: Ideal Transmission Line
  - W-element: Coupled Transmission Line (Frequency Domain Table Model)
  - S-element: S-parameter

BIRD (Buffer Issue Resolution Document)

- 173.3 Package RLC Matrix Diagonals 2014
- 164 Allowing Package Models to be defined in [External Circuit] 2014
- 163 Instantiating and Connecting
  [External Circuit] Package Models with [Circuit Call]