



IBIS Open Forum Minutes

Meeting Date: **November 20, 2014**

Meeting Location: **Yokohama, Japan**

VOTING MEMBERS AND 2014 PARTICIPANTS

Altera	David Banas, Kundan Chand, Hsinho Wu
ANSYS	Lan Chen, Minggang Hou, Jianbo Liu, Peng Wang Shulong Wu, Guoli Yin, Jizhi Zhao, Tommy Chien Elly Dong, Milkman Hsuan, Winny Huang Stanley Hangwei Kuo, James Wang Jean Yacchin Wang, Jerry Wang, Benson Peishen Wei Jack Wu, Tinghao Yeh, Tohru Watanabe*, Shigeru Sano*
Applied Simulation Technology	Fred Balistreri, Norio Matsui
Cadence Design Systems	Ambrish Varma, Brad Brim, Joy Li, Kumar Keshavan Ken Willis, Yingxin Sun, Joshua Luo, John Phillips Aileen Chen, Lanbing Chen, Zhiyu Guo, Jinsong Hu Rachel Li, Lavia Liu, Ping Liu, Yubao Meng Feng Miao, Zuli Qin, Haisan Wang, Hui Wang Yitong Wen, Clark Wu, Benny Yan Rong Zhang, Wenjian Zhang, Alex Zhao Zhangmin Zhong, Kent Ho, Thunder Lay, Skipper Liang Paddy Wu, Candy Yu, Ian Yu, Ikuo Masuko* Morihiro Nakazato*
Ericsson	Anders Ekholm*, Zilwan Mahmood*, Feng Shi Wenyan Xei
Huawei Technologies	Jinjun Li, Xiaoqing Dong, Zanglin Yuan, Han Li Haiping Cao, Yu Chen, Peng Huang, Hongxing Jiang Xueping Jiao, Aojie Li, Xusheng Liu, Zipeng Luo Longfang Lv, Luya Ma, Xiao Peng, Wenju Sheng Jianhua Wang, Shengli Wang, Huichao Weng Zhengrong Xu, Gezi Zhang, Zhenyi Zhu
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak, Jon Powell, Riaz Naseer Udy Shrivastava, Mustafa Yousuf, Jimmy Jackson Pietro Brenner, Todd Bermensolo, Denis Chen Jimmy Hsu, Cucumber Lin, Jeff Loyer, Thomas Su
IO Methodology	Lance Wang*, Michelle Coombs
Keysight Technologies (Agilent)	Radek Biernacki, Nilesh Kamdar, Colin Warwick Graham Riley, Pegah Alavi, Fangyi Rao Heidi Barnes, Dimitrios Drogoudis, Tao Zhang Xianzhao Zhao
LSI (Avago)	Xingdong Dai, Min Huang, Anaam Ansari, Brian Burdick Venkatesh Avula
Maxim Integrated Products	Hassan Rafat

Mentor Graphics	Arpad Muranyi, John Angulo, Fadi Deek, Chuck Ferry Thomas Groebli, Larry Shi, Kenji Kushima* Kazuhiro Kadota*
Micron Technology	Randy Wolff
Micron Akita	Katsunobu Noguchi*
Micron Memory Japan	Fumiyuki Osanai*, Hiromasa Takeda*
Qualcomm	Jaimeen Shah, Srinivasa Rao, Senthil Nagarathinam
Signal Integrity Software	Mike LaBonte, Walter Katz, Todd Westerhoff, Michael Steinberger
Synopsys	Ted Mido, Scott Wedge, Kevin Cameron, Rita Horner Xuefeng Chen, Jinghua Huang, Lianpeng Sang Deng Shi
Teraspeed Labs	Bob Ross, Tom Dagostino, Scott McMorro
(Teraspeed Consulting Group)	
Toshiba	Hiroyuki Ikegami, Toshihiro Tsujimura*, Hideo Oie Masato Kanie*, Atsushi Tomishima* Yasuki Torigoshi*
Toshiba Information Systems	Yasuyuki Inaba*, Mari Kuroki*
Toshiba Microelectronics	Jyunya Masumi*
Toshiba Semiconductor & Storage	Toru Amamoto*, Yoshinori Fukuba*, Shinya Harada* Yasunobu Umemoto*
Xilinx	Ravindra Gali
ZTE Corporation	Fengling Gao, Lili Wei, Zhongmin Wei Changgang Yin, Shunlin Zhu
Zuken	Michael Schaefer, Amir Wallrabenstein, Griff Derryberry Reinhard Remmert, Kiyohisa Hasegawa*

OTHER PARTICIPANTS IN 2014

3M	Shiang Yao
Advanet	Kohji Tomita*
Advantest Corporation	Yasutaka Aoki*
ADVLSI	Pierre Dermey, Juanna Gao
AET	Chihiro Ueda*
Alcatel-Lucent	Yishan Li
AMD	Tadashi Arai*
Amlogic	Jiaying Ye, Weiguo Zhu
Apollo Giken Co.	Naoya Iisaka*, Satoshi Endo*
Avant Technology	Jiaying Sun, Jyam Huang, Chloe Yang
Azuma Co.	Teruaki Hirose*
Canon	Yuji Ishikawa*, Kenta Koshida*, Syoji Matsumoto* Takeshi Nagata*
Carleton University	Ramachandra Achar
Casio Computer	Yasuhisa Hayashi*, Ikuo Imada*
Celestica	Lei Liu, Xu Yan

Chinese Academy of Engineering Physics (CAEP), Institute of Electronic Engineering (5th Institute)	Anju Tan, Liang Yin
Cisco Systems	Hongxian Yin
Continental Automotive	Catalin Negrea
CST	Stefan Paret
Cybernet Systems	Shinobu Koakutsu*
Design Methodology Lab	Motoh Tanaka*
ECL Advantage	Thomas Iddings
EMC Corporation	Sherman Chen
Flatoak Co.	Hiroshi Sakai*
Freescale Semiconductor	Asher Berkovitz, Takahiro Sato*
Fujitsu Advanced Technologies	Shogo Fujimori*, Kazuhiro Kanai*, Kumiko Teramae* Hidenobu Shiihara*
Fujitsu Interconnect Technologies	Syunsuke Fujisawa*
Fujitsu Laboratories	Toshiki Iwai*
Fujitsu Limited	Kohichi Yoshimi*
Fujitsu Microelectronics Solutions	Yutaka Ide*
Fujitsu Semiconductor	Jyunko Nakamoto*, Yu Kamata*, Fumiyo Kawafuji*
Fujitsu VLSI	Hiroki Kubota*, Yuji Nakagawa*, Hajime Ohmi*
Fuji Xerox Advanced Technology	Ryota Seki*, Satoshi Kodama*
Fuji Xerox Manufacturing	Rumi Maeda*
Fuzhou Rockchip Electronics	Xinjun Wang
Gigabyte Technology	Eric Chien, Mountain Lin, Alex Lu
Giga Hertz Technology	Chisato Kawamura*
H3C	Xinyi Hu, Xiaoqun Li
Hamamatsu Photonics K.K.	Akahiho Inoguchi*
Hangzhou Hikvision Digital Technology	Wenquan Hu, Jia Zhang
Hewlett Packard	Ting Zhu
Himax Technologies	Brian Kuo, Ren-Yu Wang, Josh Wu
Hisense Group	Golden Qian
Hitachi Information & Communication Engineering	Yoshifumi Takada*
Hitachi ULSI Systems Co.	Hiroshi Uematsu*, Sadahiro Nonoyama*
Hoei Co.	Tatsuya Chiba*
Hong Kong University	Lijun Jiang
Hon-Hai Precision (Foxconn)	Ryan Lung-Yu Hou, Daniel Ying-Tso Lai Chris Chia-Nan Pai
IBM	Adge Hawes
ILI Technology Corp.	Chia-Cheng Wu
Innotech Corporation	Sinobu Seki*
Instituto de Telecomunicações	Wael Dghais
Japan Radio Co.	Hiroto Katakura*
JEITA	Yousuke Kanamaru*, Ryosuke Miyagawa*

JONHON	Akahito Nagamoto*, Kyouji Yamazaki*
JVC Kenwood Corporation	Guoqi Zhou
KEI Systems	Hidetoshi Suzuki*
KSK Co.	Shinichi Maeda*
Lapis Semiconductor	Yutaka Shishido*
Lattice Semiconductor	Katsuhiro Hisaka*
Lenovo	Xu Jiang
LUXSHARE-ICT	John Lin, Alan Sun
Macronix Microelectronics	Jet Shen, Chenhui Zeng
Marvell	Donghe Tang
	Weizhe Li, Xike Liu, Fang Lv, Banglong Qian
MD Systems	Yuyang Wang, Liang Wu
Mediatek	Hidetoshi Ogawa*
Megachips Corp.	Alice Lin, Delbert Liao
Mellanok Technologies	Kenichiro Kobayashi*
Microsemi	Piers Dawe
Modech	Nizar Abdallah, Ann Lau
Montage Technology	Yasuo Kawahara*, Masanori Shimasue*, Minoru Tanaka*
Murata Manufacturing	Xiaoliang Xu
Nanium	Satoshi Arai*, Naoki Iida*, Kingo Kurotani*
Nanya Technology Corp.	Abel Janeiro
	Chi-Wei Chen, Aiden Hsu, Tingshuo Hsu, Andre Huang
NEC Corp.	Raphael Huang, Tian-De Huang, Zuo Xin
NEC Engineering	Yasuyuki Chiba*
Nikon Corporation	Masahiko Kuroda*
Olympus Corp.	Kazuomi Tominaga*, Manabu Matsumoto*
Oracle	Kazuhiro Sakamoto*
Panasonic Semiconductor	Stephan Mueller
Solutions Co.	Daisuke Matsuoka*, Masaya Sumita*
Pangya	
Pegatron Corp.	Edgar Aguirre
Pioneer Corp.	Lance Chang, Stanley Chu, Gavin Lin
Pioneer Micro Technology Corp.	Kenji Sakamoto*
Private	Minoru Nakahara*
Proficient Design	Seijyu Ichijyo*
Renesas Electronics	Kishor Patel
	Genichi Tanaka, Masayasu Koumyo*, Ryuichi Oikawa*
Renesas System Design Corp.	Kenzo Tan*, Hiroyuki Uchida*
Ricoh Company	Kazunori Yamada*
	Yasuhiro Akita*, Kazumasa Aoki*, Masahiko Banno*
Rockchip	Miyoko Goto*, Takefumi Takizawa*
Rohm Co.	Jiayi Song
SAE International	Noboru Takizawa*
Sanei Hytechs Co.	Chris Denham
	Hiroyuki Kai*

Seiko Instruments	Masaya Murata*
Shimadzu Corp.	Kazuo Nakajima*
Sony LSI Design	Satoshi Tago*
Success International Corporation	Tatsuo Futai*
Sunplus Technology	Forest Hsu, Yi-Tzeng Lin
Tabula	Ben Zhou
Technische Universität Hamburg	Torsten Reuschel
Teledyne LeCroy	Larry Cao, Derek Hu, Joyce Yin
Towa Electronics	Yoshikazu Suzuki*
University of Illinois	José Schutt-Ainé
VIA	Terence Hsieh, Justin Hsu
Via CPU	Leon Liang
Vitesse	Siris Tsang
Wadow	Kazuhiko Kusunoki*
Winbond Electronics	Albert Lee
Wiwynn Corp.	Scott CH Lee, Kevin TK Wang
Xpeedic Technology	Wenliang Dia, Feng Ling, Zhouxiang Su
Yamanashi Avionics Co.	Yasunori Yamashita*
Zhejiang Uniview Technologies	Fei Ye, Feng Ye

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
December 5, 2014	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

<https://ciscosales.webex.com/ciscosales/j.php?J=205475958>

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The IBIS Open Forum summit was held in Yokohama, Japan, co-located with the Electronics Design Solutions Fair (EDS Fair) at the Pacifico Yokohama Conference Center. Approximately 111 people representing 69 organizations attended.

The statements below summarize the material presented. More details are available through the summit presentations posted online at:

<http://www.eda.org/ibis/summits/nov14c/>

Lance Wang opened the Summit. Shogo Fujimori (Fujitsu Advanced Technology and JEITA IBIS Promotion Working Group Chair) provided introductions and welcomes.

Lance continued by thanking the co-sponsors: the major sponsors JEITA and the IBIS Open Forum and also the co-sponsors ANSYS, Cadence Design Systems, Cybernet Systems, Mentor Graphics, MoDeCH and Zuken.

ACTIVITIES AND DIRECTION OF IBIS

Michael Mirmak (Intel Corporation, USA)

[Presented by Lance Wang (IO Methodology, USA)]

Lance Wang began by noting that the current version of IBIS is IBIS 6.0, and a parser, IBISCHK6, was released in June 2014. A user's guide for IBISCHK6 is in development from the IBIS Quality task group and a work-in-progress document is available for review. An IBIS model review service is also available. As of today, three approved BIRDs propose major changes to IBIS 6.0, while five other approved BIRDs make clarifications or corrections. Eleven other BIRDs are proposed but not approved, and these cover areas including backchannel adaptation for equalization, expanded package modeling capabilities, Touchstone support for AMI analog buffer models and parameter passing for External Circuits. A major revision of the IBIS Open Forum basic policies and procedures is also underway. Changes to the IBIS Open Forum charter will allow for greater involvement in votes and officer elections by membership companies worldwide.

INTRODUCTION OF IBIS PROMOTION WORKING GROUP

Shogo Fujimori (Fujitsu Advanced Technologies, Japan)

Shogo Fujimori began by introducing the Japan Electronics and Information Technology Industries Association (JEITA) and Electronic Commerce Center committee organization. He continued with a summary of the IBIS Quality Working Group's progress from 2007 to June 2014. That WG developed processes for testing, verifying and distributing quality IBIS models. Shogo noted that the IBIS Promotion Working Group is new. Their objective is to promote the use of IBIS models in simulation. Their action plan is to review the IBIS specification, summarize which keywords should be used for target applications, provide guidance on which versions of IBIS models should be used for specific simulation cases, and look at IBIS model inconsistencies. Their proposed activities include supporting logistics for the IBIS Summit in Japan, promoting IBIS model utilization including providing IBIS-related information, defining

IBIS simulation guidelines and maintaining the IBIS Quality WG results. Shogo concluded by inviting more participation in the IBIS Promotion WG.

INCONSISTENCY OF EBD (ELECTRICAL BOARD DESCRIPTION) SPECIFICATION IN DDR3 DIMM

Shogo Fujimori (Fujitsu Advanced Technologies, Japan)

Shogo Fujimori gave an overview of the Electrical Board Description (EBD) modeling in IBIS. He showed an example from the IBIS specification of syntax for a differential clock-type circuit including a series termination. He introduced some problems encountered with EBD modeling of DDR3 fly-by topology clock nets including differential termination and AC termination. For differential terminations, description styles are vendor dependent. He noted an EBD that commented that the capacitor termination must be added external to the EBD, but it is not clear how to do this. Until IBIS 5.0, series components could not connect two separate [Path Description]s. This was allowed in IBIS 5.1, but it may not be supported in all EDA tools yet. Another issue is that the IBIS Terminator model cannot define AC terminations connected to the power terminal. Shogo proposed adding a Rac/Cac type termination to the Terminator model that connects to the power terminal. He would also like to see an EBD section added to the IBIS Cookbook.

IBIS PACKAGE MODEL (PAST, PRESENT, WHAT'S NEXT)

Shinichi Maeda (KEI Systems, Japan)

Shinichi Maeda gave an overview of package modeling in IBIS beginning with IBIS 1.0 through IBIS 6.0. This included [Package], [Pin], [Package Model] and EBD. IBIS has also released other interconnect modeling specifications including ICM, Touchstone 2.0 and IBIS-ISS. Several BIRDs have yet to be approved that relate to improving package and interconnect modeling in IBIS.

DIFFERENTIAL BUFFER USING IBIS MODELS FOR PDN SIMULATIONS

Lance Wang (IO Methodology, USA)

Lance Wang presented a case study of differential pair buffers in Power Delivery Network (PDN) simulations. The IBIS specification does not indicate how to make an IBIS power aware model for true differential pair buffers. Lance used a 1.5V LVDS true-differential buffer with balanced pullup and pulldowns for his study. The buffer also had access to the power supply connections for both the positive and negative signal drivers. The simulation correlated well to the transistor model when the IBIS model was extracted from separate power supplies for each of the positive and negative pins. If one doesn't have access to each buffer's power pins separately, this creates a problem. For this model, one can get a combined ISSO curve by setting up both pullup and pulldown, then taking the average for each buffer. For [Composite Current] waveforms, one can take one rising edge and one falling edge curve at the same time for the differential pair and add the results together. The resulting model is not a perfect correlation to the transistor model, but the results are better than using an IBIS model without the power aware features.

TRUE DIFFERENTIAL IBIS MODEL FOR SERDES ANALOG BUFFER

Shivani Sharma, Tushar Malik and Taranjit Kukal (Cadence Design Systems, India)
[Presented by Morihiro Nakazato, (Cadence Design Systems, Japan)]

Morihiro Nakazato gave an overview of current differential buffer modeling techniques in IBIS. An alternative approach to S-parameter characterization was shown using standard IBIS tabular data formats along with series elements to model differential current. This extended the approach suggested in the IBIS cookbook suggesting modeling of differential current using series resistance. A modeling flow was shown for extraction of common and differential mode impedances. From the impedance at a specific frequency one can calculate series and common mode reactances and resistances. Depending on the sign the reactance could be inductive or capacitive. A parallel RL network is then modeled using the series model type. A parallel RC network is modeled using C_comp and clamp I-V tables. The true differential model provides much better accuracy than a pseudo differential IBIS model for channel simulation in terms of jitter, eye opening and reflection losses.

IBIS AMI VALIDATION

Zilwan Mahmud and Anders Ekholm (Ericsson, Sweden)
[Presented by Zilwan Mahmud (Ericsson, Sweden)]

Zilwan Mahmud began by describing design goals he has with IBIS AMI analysis. IBIS AMI models must be validated, as correct and validated models are needed. Certification is the first step a model must go through to check that the model behavior is reasonable. Zilwan presented a long checklist of items to verify. To do active correlation, the PCB model in simulation must be adjusted to match the real channel characteristics as seen in measurements. S-parameters from measurement can be used in the correlation exercise, but the PCB models need to be adjusted for later use in post-layout simulation. TX active validation is feasible, but RX active validation is not, because measurements at the decision point are not possible.

Zilwan's experience shows that many models fail certification for various reasons such as syntax errors, run time errors, simulated DC levels that don't match measured DC levels, idealized analog models, etc.

IBIS MODEL ENGINEERING APPLICATION POSSIBILITY

Kazuhiko Kusunoki (Wadow, Japan)

Kazuhiko Kusunoki noted that IBIS models are good for SI simulation but wondered how useful they could be for PI and EMI simulation. IBIS models contain useful information such as V-T waveforms, I-V data, [Ramp] data and RLC package data. V-T waveforms can be very useful for EMI by doing an FFT and looking at the spectral content. IBIS models can be a useful datasheet for PI and EMI because they contain information not usually found in the device datasheet. Kazuhiko looked at a case study of using models to estimate EMI on a PCB. He started with a Chip Power Model (CPM) to represent current flow in the power supply for the die. With use of only the CPM, no EMI was seen from the signal trace on the PCB. With a signal current model based on the datasheet and using the CPM, the simulation result showed unrealistically high radiation. Using an ideal current model based on the I-V data in the IBIS model and the CPM did not show any high frequency content in the radiation. The most realistic

results were obtained by generating a signal current model from the FFT of the current waveform from an SI simulation using the IBIS model.

INTRODUCTION OF P2401 LSI-PACKAGE-BOARD STANDARD FORMAT

Yoshinori Fukuba (Toshiba Semiconductor & Storage, Japan)

Yoshinori Fukuba opened his presentation by stating that IEEE P2401 work started earlier this year, with working group membership being entity-based, for advanced IEEE Standards Association members. Several Japanese companies are currently represented in the working group. The group was formed because sometimes LSI (large-scale integrated circuits), package, and board designers work independently, but coordination of their work is needed. The industry generally wants to have a shared format for exchanging information in these areas, to shorten design and production cycles. Product development phases are long, and sometimes miss market windows. Having IBIS model simulations at each stage is desirable, but simulations take more time at each stage as development progresses. Simulation under LPB would take place from product planning, through circuit design, layout and SI/PI/EMC checking.

LPB is JEITA's first formal international standard effort. The LPB approach contains five different formats within it, including netlist, geometry, project, component and rule, identified by leading letters (i.e., M-, N-, C-, R-, and G-format). The C- and G- formats are used by CAD/CAE teams, while the N-format is used by system designers.

N-format is netlist, using Verilog. The R-format covers design rules, and is constraint-based, including material characteristics and constraints. G-format covers geometries using XFL, while the C-format covers components, in its own unique language approach. IBIS would fall under the C-format.

Files can be modified throughout life cycle stages by different engineers. This format standardization avoids issues with human error.

The LPB group's objective is to have an IEEE standard by December 2015.

CONCLUDING ITEMS

Lance Wang thanked the co-sponsors, presenters and attendees for their participation and support. The meeting adjourned at 4:30 PM.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held December 5, 2014.

=====

NOTES

IBIS CHAIR: Michael Mirmak (916) 356-4261, Fax (916) 377-3788
michael.mirmak@intel.com
Data Center Platform Applications Engineering

Intel Corporation
FM5-239
1900 Prairie City Rd.,
Folsom, CA 95630

VICE CHAIR: Lance Wang (978) 633-3388
lwang@iometh.com
President/CEO, IO Methodology, Inc.
PO Box 2099
Acton, MA 01720

SECRETARY: Randy Wolff (208) 363-1764, Fax: (208) 368-3475
rrwolff@micron.com
Principal Engineer, Silicon SI Group Lead, Micron Technology, Inc.
8000 S. Federal Way
Mail Stop: 01-711
Boise, ID 83707-0006

LIBRARIAN: Anders Ekholm (46) 10 714 27 58, Fax: (46) 8 757 23 40
ibis-librarian@eda.org
Digital Modules Design, PDU Base Stations, Ericsson AB
BU Network
Färögatan 6
164 80 Stockholm, Sweden

WEBMASTER: Mike LaBonte
mikelabonte@eda.org
IBIS-AMI Modeling Specialist, Signal Integrity Software
6 Clock Tower Place
Maynard, MA 01754

POSTMASTER: Mike LaBonte
mikelabonte@eda.org
IBIS-AMI Modeling Specialist, Signal Integrity Software
6 Clock Tower Place
Maynard, MA 01754

This meeting was conducted in accordance with ANSI guidance.

The following e-mail addresses are used:

majordomo@eda.org

In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:

subscribe ibis-users <your e-mail address>

Help and other commands:

help

ibis-request@eda.org

To join, change, or drop from either or both:

IBIS Open Forum Reflector (ibis@eda.org)

IBIS Users' Group Reflector (ibis-users@eda.org)

State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

<http://www.eda.org/ibis/bugs/ibischk/>

<http://www.eda.org/ibis/bugs/ibischk/bugform.txt>

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/

http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/

http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

<http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt>

<http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt>
<http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt>

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

<http://www.eda.org/ibis>

Check the IBIS file directory on eda.org for more information on previous discussions and results:

<http://www.eda.org/ibis/directory.html>

Other trademarks, brands and names are the property of their respective owners.

IBIS – SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status				
			October 24, 2014	November 14, 2014	November 17, 2014	November 20, 2014
Altera	Producer	Inactive	X	-	-	-
ANSYS	User	Active	-	X	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	X	X	X
Ericsson	Producer	Active	-	X	X	X
Huawei Technologies	Producer	Inactive	-	X	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Inactive	-	-	X	-
IO Methodology	User	Active	X	-	X	X
Keysight Technologies (Agilent)	User	Inactive	X	X	-	-
LSI (Avago)	Producer	Inactive	-	-	-	-
Maxim Integrated Products	Producer	Inactive	-	-	-	-
Mentor Graphics	User	Active	X	X	-	X
Micron Technology	Producer	Inactive	X	-	-	X
Qualcomm	Producer	Inactive	-	-	-	-
Signal Integrity Software	User	Inactive	X	-	-	-
Synopsys	User	Inactive	X	X	-	-
Teraspeed Labs	General Interest	Inactive	X	-	-	-
Toshiba	Producer	Inactive	-	-	-	X
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	X	-	-
Zuken	User	Inactive	-	-	-	X

I/O Buffer Information Specification Committee (IBIS)

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH SAE BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.