Inconsistency of EBD (Electrical Board Description) specification in DDR3 DIMM

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— Agenda —

1. IBIS EBD Model
2. Problems in DDR3 DIMM
   - Differential termination
   - AC termination
3. Proposal
4. Summary

1. IBIS EBD Model

- Electrical Board Description

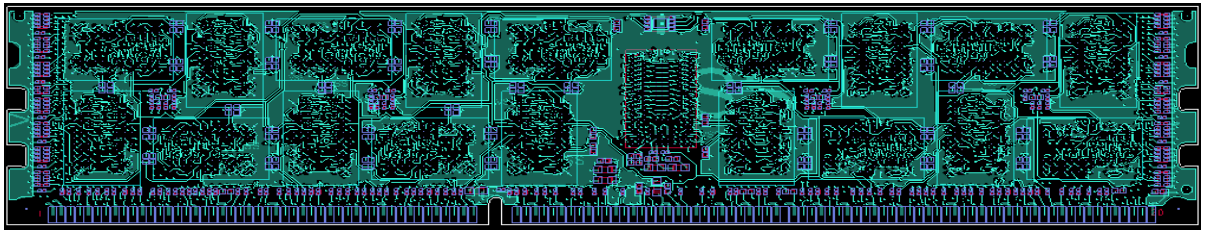
・The electrical connectivity of a Board level component
  - PCB
  - Components
  - User visible pins
・Example: DIMM

IBIS Version 6.0

8 ELECTRICAL BOARD DESCRIPTION

INTRODUCTION

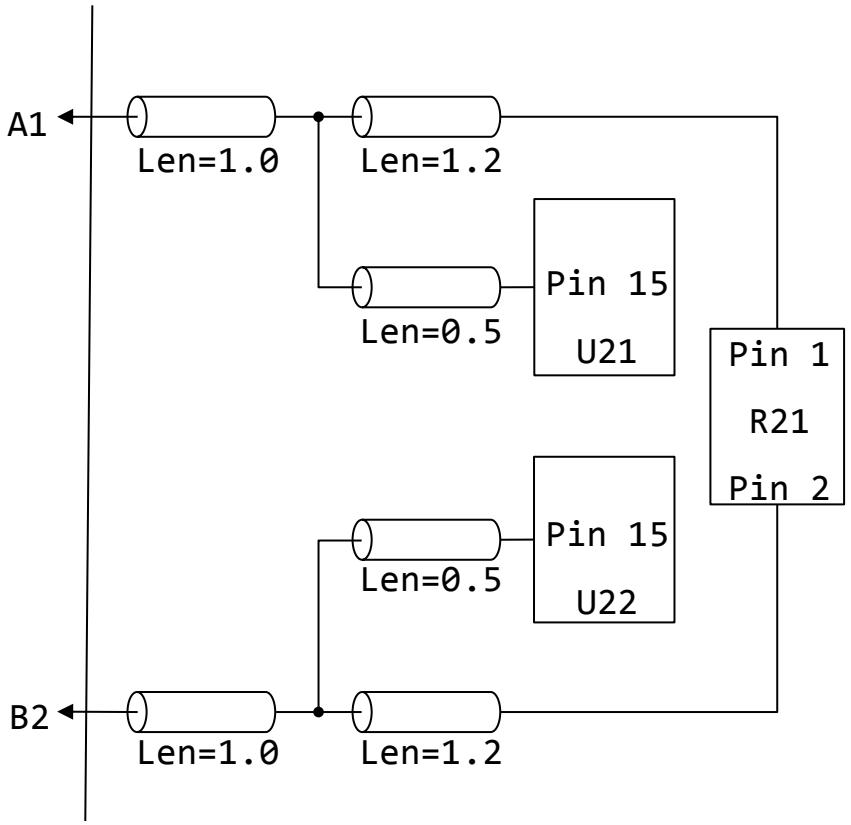
A “board level component” is the generic term to be used to describe a printed circuit board (PCB) or substrate which can contain components or even other boards, and which can connect to another board through a set of user visible pins. The electrical connectivity of such a board level component is referred to as an “Electrical Board Description”. For example, a SIMM module is a board level component that is used to attach several DRAM components on the PCB to another board through edge connector pins. An electrical board description file (a .ebd file) is defined to describe the connections of a board level component between the board pins and its components on the board.



1. IBIS EBD Model

- Example

```
|
[Path Description] Example
Pin A1
Len = 1.0 L=6.0n C=2.0p /
  Fork
  Len = 0.5 L = 1.0n C= 2.0p /
  Node U21.15
  Endfork
Len = 1.2 L=6.0n C=2.0p /
Node R21.1
Node R21.2
Len = 1.2 L=6.0n C=2.0p /
  Fork
  Len = 0.5 L = 1.0n C= 2.0p /
  Node U22.15
  Endfork
Len = 1.0 L = 6.0n C=2.0p /
Pin B2
|
```



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Node R21.1
Node R21.2
Len = 1.2 L=6.0n C=2.0p /
  Fork
  Len = 0.5 L = 1.0n C= 2.0p /
  Node U22.15
  Endfork
Len = 1.0 L = 6.0n C=2.0p /
Pin B2
|
```

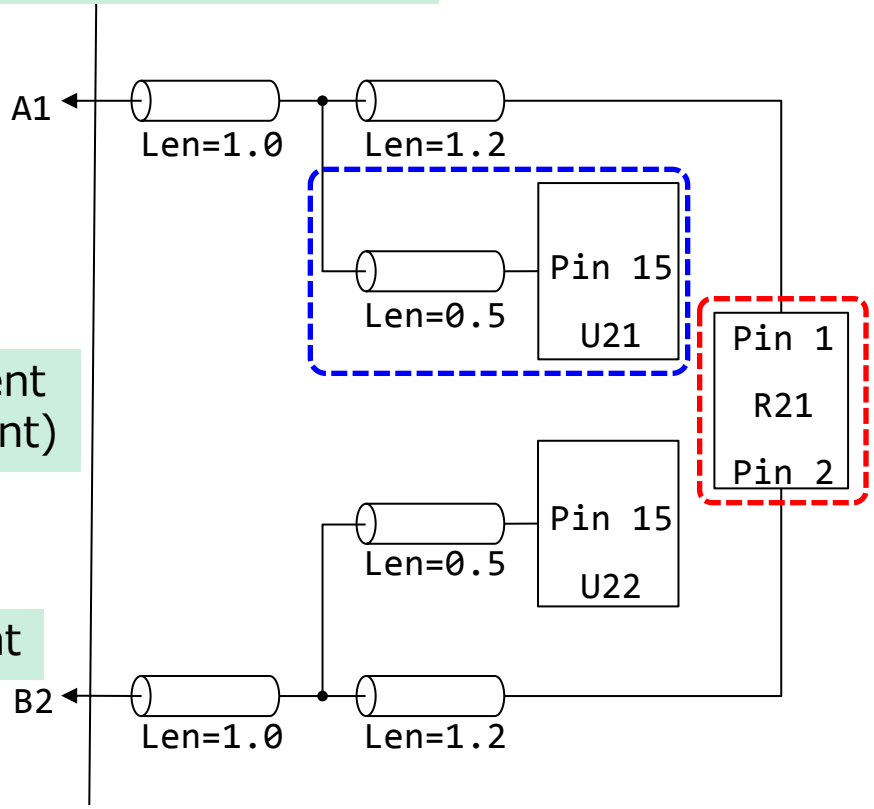
User accessible pin

Branch off of the main path

Passive component (Series component)

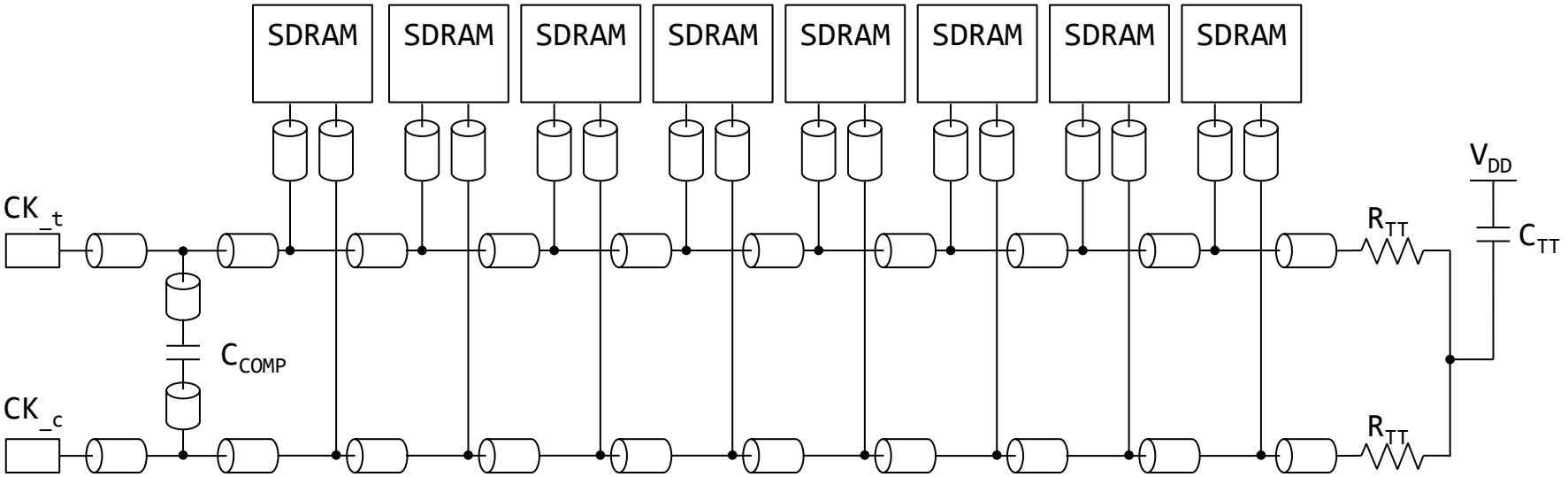
Active component

User accessible pin



2. Problem in DDR3 DIMM

- DDR3 Clock Net (Fly-by)

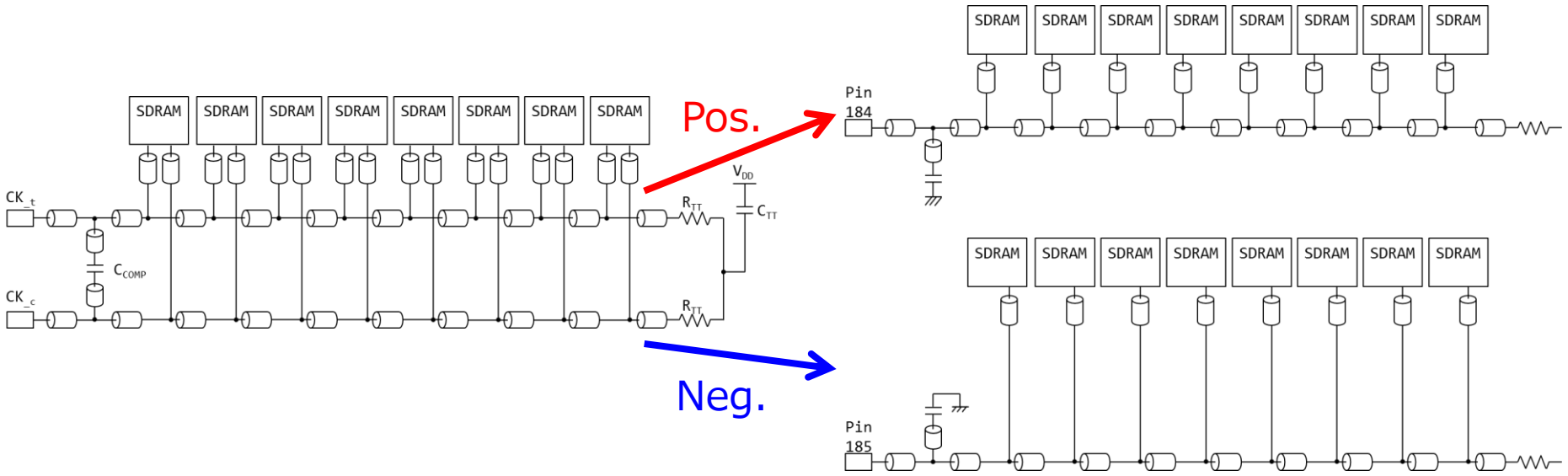


- Problems of EBD
  - ① Differential termination
  - ② AC termination
  - ③ Differential lines Coupling

← This presentation

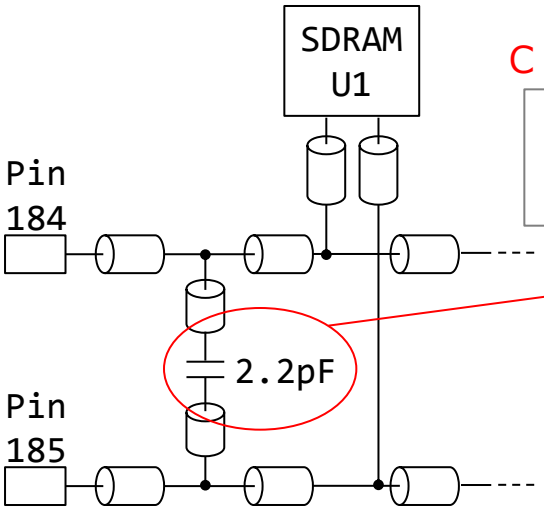
2.1 Differential termination

- Description styles of differential terminations are vendor dependent
  - Case1: A single [Path Description] including differential pair nets
  - Case2: Two separate [Path Description]s for each differential pair nets. (See below figure)

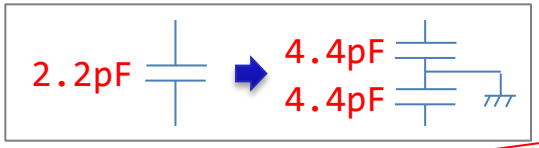


Problem case of differential termination

- Problem case of two separate [Path Description]s
  - Two paths are completely separated



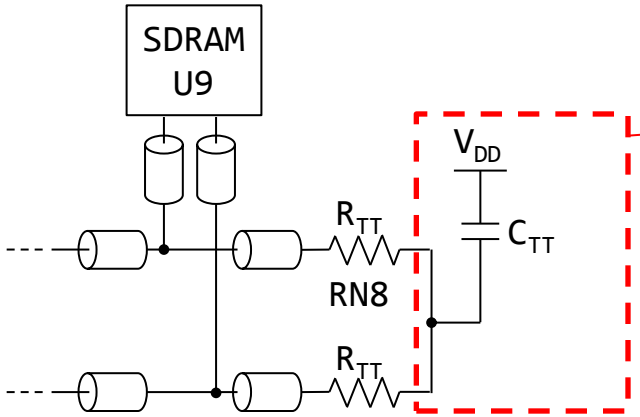
C is connected to GND as 4.4pF




```
[Path Description] 184
Pin 184
Len=0.02910 L=xxx C=xxx R=xxx /
Fork
  Len=0.08063 L=xxx C=xxx R=xxx /
  Len=0 C=4.4e-12 /
Endfork
Len=0.02910 L=xxx C=xxx R=xxx /
Fork
  Len=0.20980 L=xxx C=xxx R=xxx /
  Node U1.F7
Endfork
  :
Fork
  Len=0.20980 L=xxx C=xxx R=xxx /
  Node U9.F7
Endfork
Len=0.06910 L=xxx C=xxx R=xxx /
Node RN8.1

[Path Description] 185
Pin 185
Len=0.14930 L=xxx C=xxx R=xxx/
  :
  :
```

  - Incomplete differential termination



Dotted line area is not described in the EBD

※The EBD said in the comment part that the terminator must be added externally

➡ But how ?

Problem case of differential termination (Cont'd)

- Background of the problem
  - Until IBIS 5.0, a series component can not connect two separate [Path Description]s

Quoted from IBIS 5.0 specification

```
Connecting two separate [Path Description]s with a series
component is not allowed.
```

- It was allowed later IBIS 5.1
  - The problem will be solved in the future
  - However, check IBIS Version your EDA tool can use

Quoted from IBIS 5.1 specification

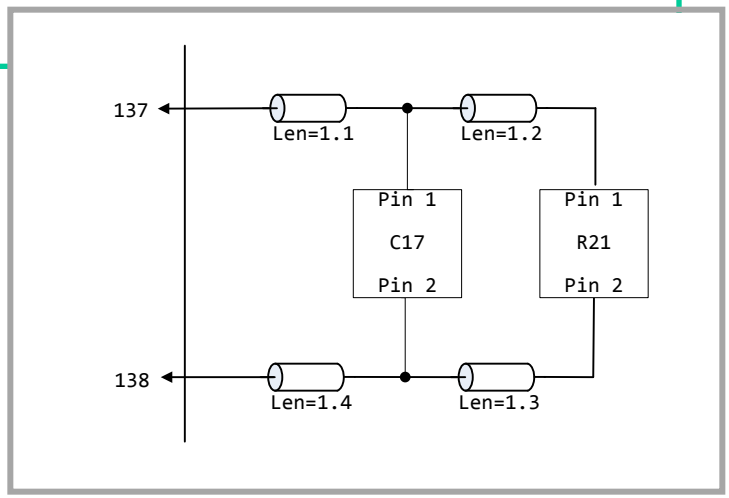
```
It is also allowed to insert a series component between
two branches of a single [Path Description], or even
between two separate [Path Description]s (see the
examples below).
```

Example described in IBIS specification

- Example of A [Path Description] including a differential pair nets (Quoted from IBIS 5.1 specification)

A path including series passive components (C17, R21) between branches forming a differential termination:

```
[Path Description]   CLK
Pin 137
Len=1.1 L=1n C=0.4p /
Node C17.1                  | Pin 1 of Series C17
Len=1.2 L=1n C=0.4p /
Node R21.1                  | Series R21 Pin 1 and 2 connections
Node R21.2
Len=1.3 L=1n C=0.4p /
Node C17.2                  | Pin 2 of Series C17
Len=1.4 L=1n C=0.4p
Pin 138
```



Example described in IBIS specification (Cont'd)

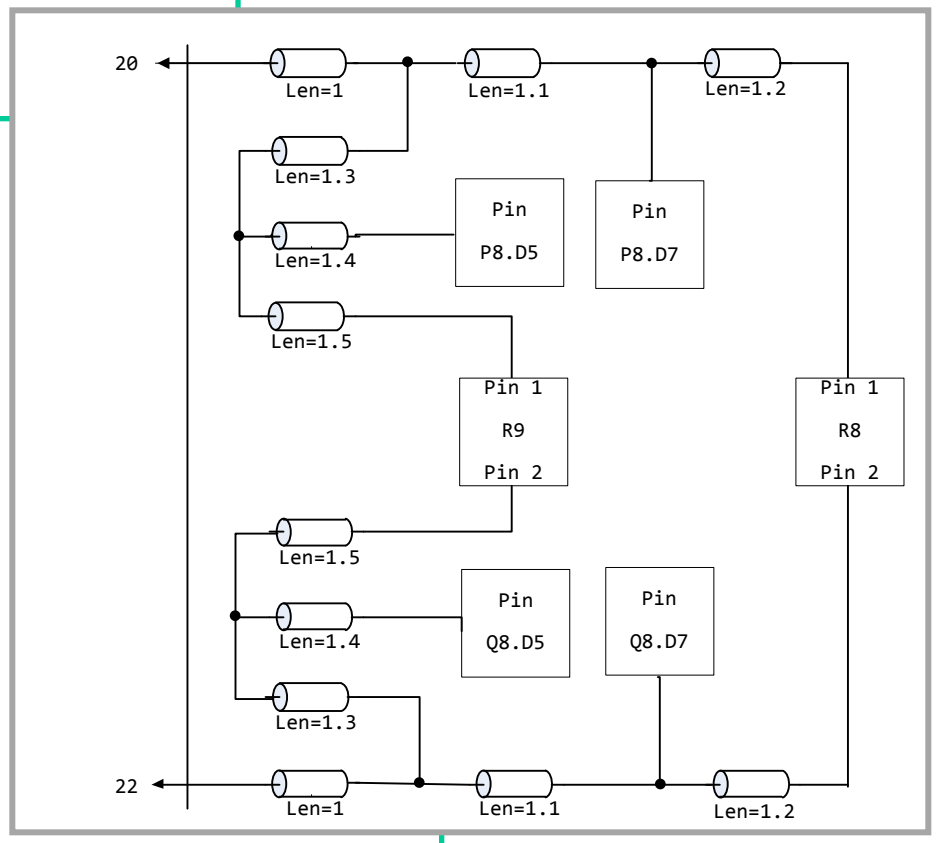
- Example of two separate [Path Description]s connected by series component (Quoted from IBIS 5.1 specification)

Two paths connected by series resistors (R8, R9) used as differential termination between components:

```
[Path Description] DP+
Pin 20
Len=1 L=1n C=
Fork
  Len=1.1 L=1
  Fork
    Node P8.D
  Endfork
  Len=1.2 L=1
  Node R8.1
Endfork
Len=1.3 L=1n
Fork
  Len=1.4 L=1
  Node P8.D5
Endfork
Len=1.5 L=1n
Node R9.1
```

Other path(s):

```
[Path Description] DP-
Pin 22
Len=1 L=1n C=0.4p   /
Fork
  Len=1.1 L=1n C=0.4p /
  Fork
    Node Q8.D7
  Endfork
  Len=1.2 L=1n C=0.4p /
  Node R8.2
Endfork
Len=1.3 L=1n C=0.4p   /
Fork
  Len=1.4 L=1n C=0.4p /
  Node Q8.D5
Endfork
Len=1.5 L=1n C=0.4p   /
Node R9.2
```



| Pin 2 of Series R9

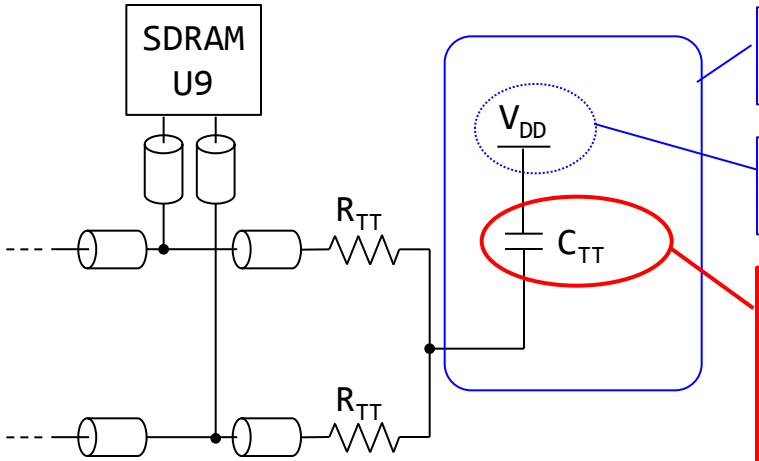
2.2 AC termination

- Problem case of AC termination
  - The capacitor is interpreted as 100nΩ resistance

```
[Model]      OSP_100n_1.5
Model_type   Terminator

|                          typ          min          max
C_comp                     0.00F        NA           NA
[Pullup Reference]         1.5V         NA           NA
[Pulldown Reference]       0.00V        NA           NA
[POWER Clamp Reference]    1.5V         NA           NA
[GND Clamp Reference]      0.00V        NA           NA

|                    C(typ)     C(min)     C(max)
[Rpower]             100nF      NA         NA
```



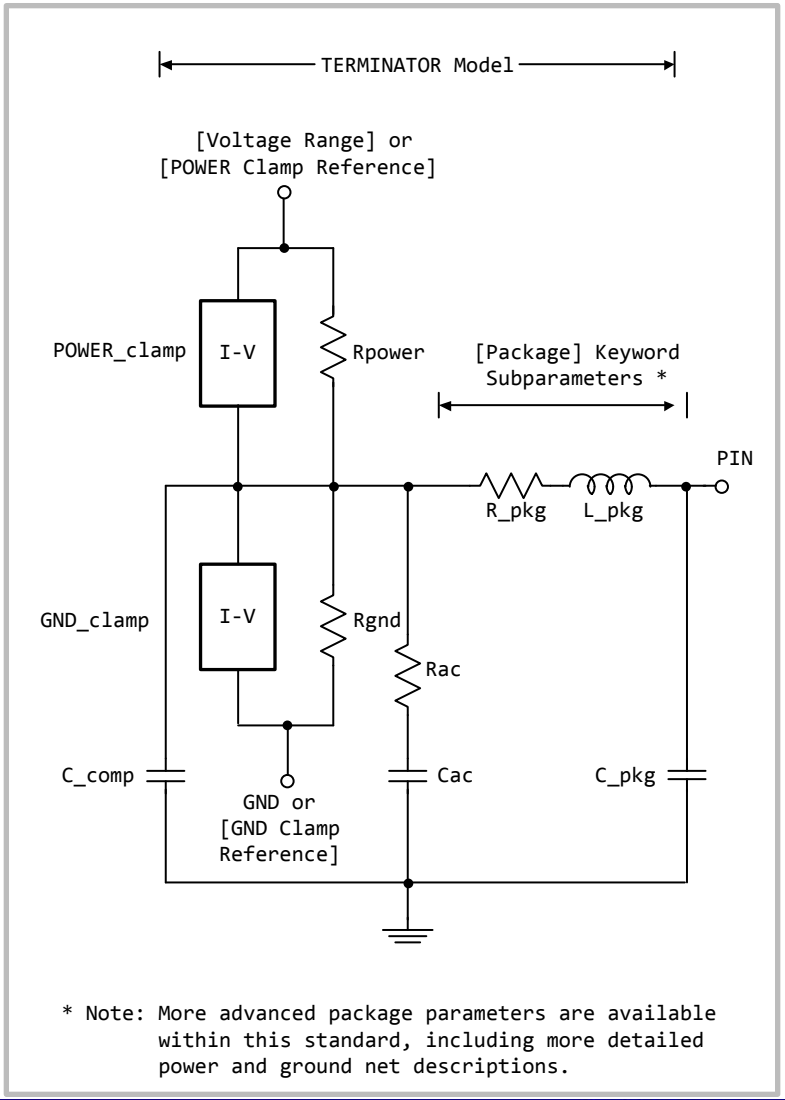
AC termination (C_{TT}+V_{DD}) is defined by the terminator model

V_{DD} is defined 1.5V by the [POWER Clamp Reference]

Though C_{TT} is defined 100nF by the [Rpower], simulators interpret as 100nΩ resistance because [Rpower] is the keyword to define the resistance connected to the POWER

2.2 AC termination (Cont'd)

- Background of the problem
  - IBIS Terminator Model can not define AC termination connected to the POWER



Quoted from IBIS specification

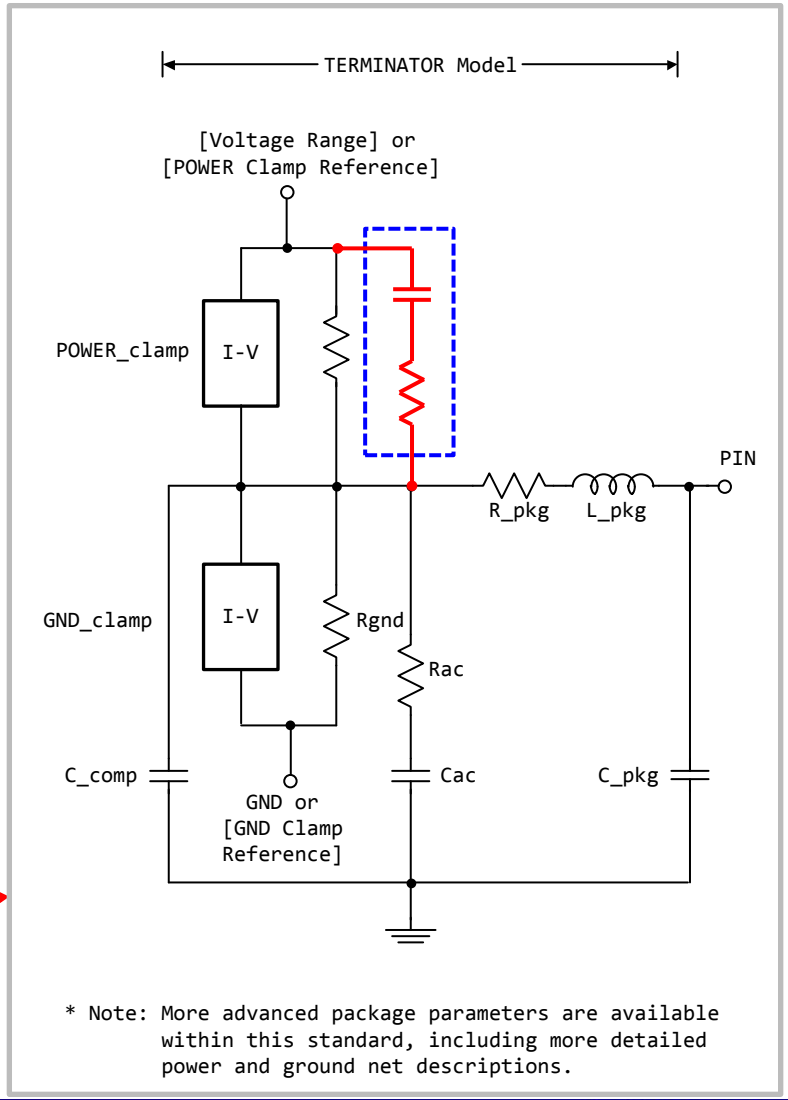
3. Proposal

- Adding a keyword to connect to the POWER to EBD or Terminator model
  - Adding a "Power" keyword to EBD model

e.g. Connected to 1.5V ideal voltage source

```
   :
Fork
   Len=2.100402 L=xxx C=xxx R=xxx/
   Node U1.F7
Endfork
Len=88.011076 L=xxx C=xxx R=xxx/
Node CTT.2
Node CTT.1
Power 1.5
```

  - Adding a keyword of AC termination connected to the POWER to Terminator model



4. Summary

- There are several problems of EBD model to use DDR3 DIMM Simulation
  - Check details of the IBIS EBD model you got
  - Edit simulation models if necessary
  - Check IBIS Version your EDA tool can use
- Proposal and Expecting for IBIS
  - Adding a keyword to connect the AC termination to the POWER
  - Adding the EBD section to IBIS Cookbook

- IBIS Promotion Working Group provide any IBIS related information, and proposal to the IBIS specification

Reference

- “IBIS (I/O Buffer Information Specification) Version 6.0”, IBIS Open Forum 2013
- “IBIS (I/O Buffer Information Specification) Version 5.1”, IBIS Open Forum 2012
- “IBIS (I/O Buffer Information Specification) Version 5.0”, IBIS Open Forum 2008
- “IBIS EBD for DDR2/DDR3 Module Board”, Lance Wang (IO Methodology), 2009 IBIS Summit, DesignCon