Introduction of IBIS Promotion Working Group

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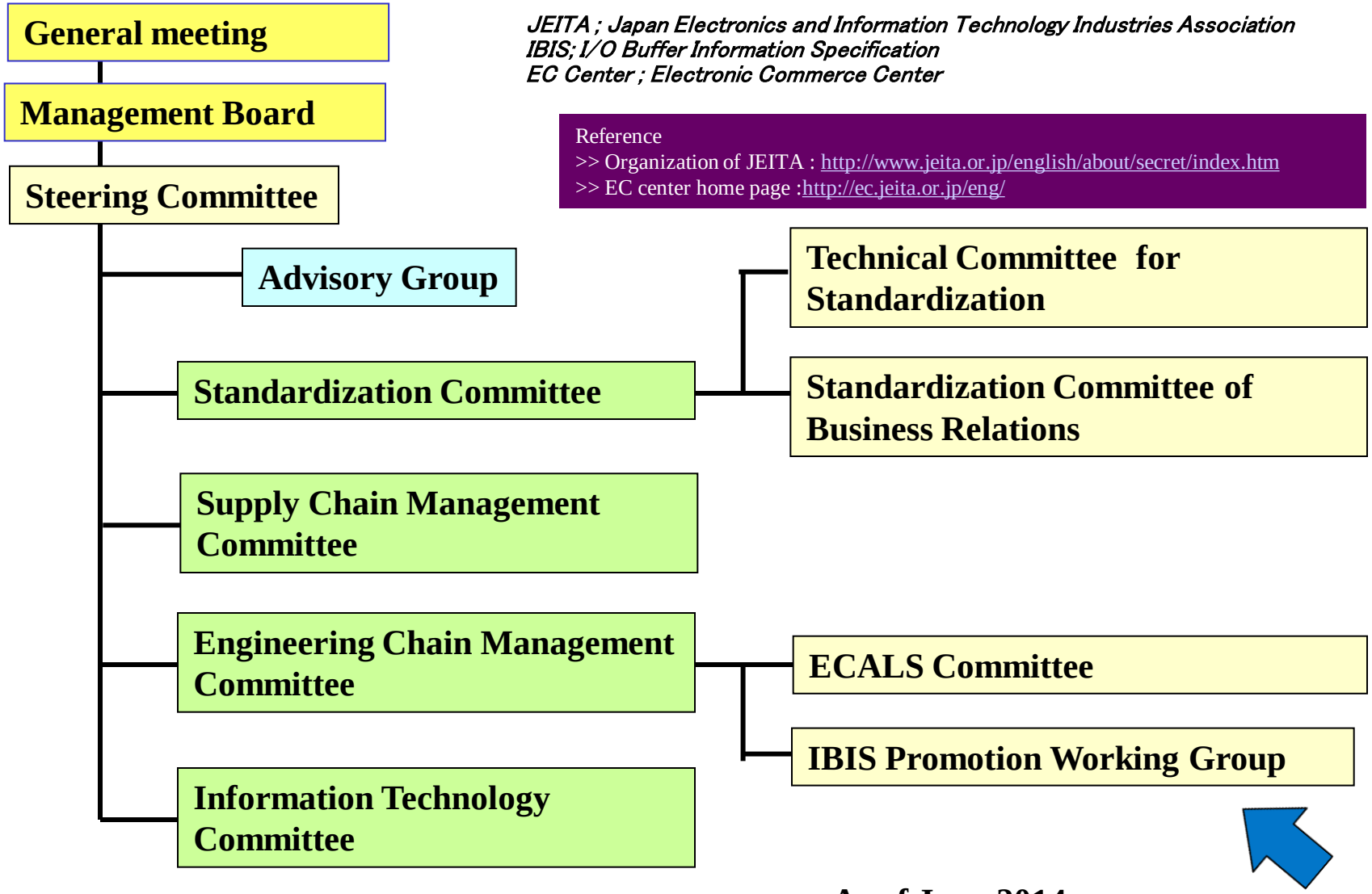
― Agenda ―

1. JEITA/EC Center Committee Organization
2. IBIS Quality Working Group Review
   - 2007 ～ 2014 June
3. IBIS Promotion Working Group (New)
   - Objective
   - Action Plan
   - Please Join Us !!

1. JEITA/EC Center Committee Organization



JEITA ; Japan Electronics and Information Technology Industries Association
IBIS; I/O Buffer Information Specification
EC Center ; Electronic Commerce Center

Reference
>> Organization of JEITA : http://www.jeita.or.jp/english/about/secret/index.htm
>> EC center home page :http://ec.jeita.or.jp/eng/

As of June 2014

2. IBIS Quality Working Group Review

- 2007 ～ 2014 June

IBIS Quality SWG 2007 – June 2013

Design Challenges and Solution with EDA Simulation

Back ground

Digital equipment company
Shorten Design TAT

Deliver High quality product in Timely Manner
EDA Simulation Must Be Utilized
Bottle neck !

Technical reason

- Short Production Cycle
- Increase Digital Circuit Frequency
- EMC Compliance
- Low Power

EDA Simulation is MUST

EMC, SI, PI, Thermal, Assemble, Stress

Business reason

- Design & Manufacturing
- Worldwide Same Time Launch
- Meet Delivery Schedule
- Supplier Management

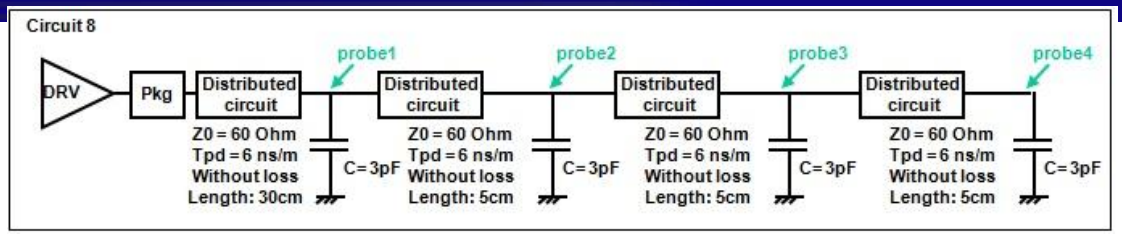
EDA Model Availability is Key

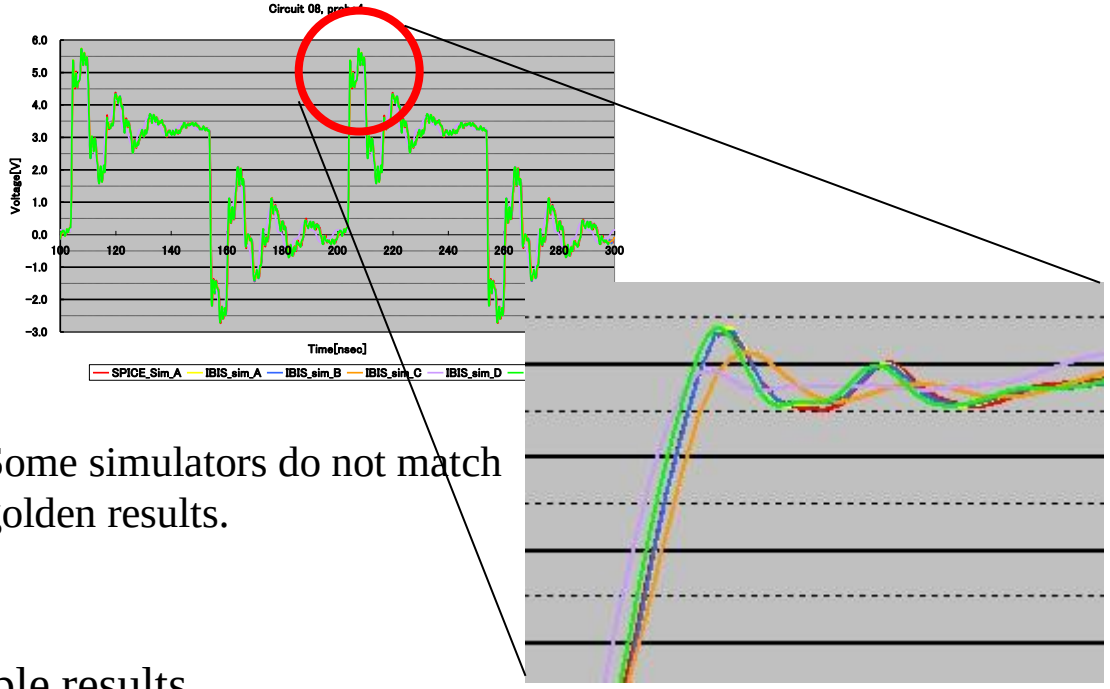
IBIS Simulation Trial Result

Simulator

Company

	A	B	C	D	E	F
U	○					
V	○					
W		X				
X			X	X		○
Y					X	
Z						○





Some simulators do not match golden results.

Multiple simulators shows multiple results.
No one can judge which is good.

Need to investigate:
Model, Simulation Setup, Simulator and Skill

JEITA provided guideline for solving this problem.

The basic concept for distribution of good IBIS models

JEITA

Golden IBIS

Test circuit group

Golden results

Upload

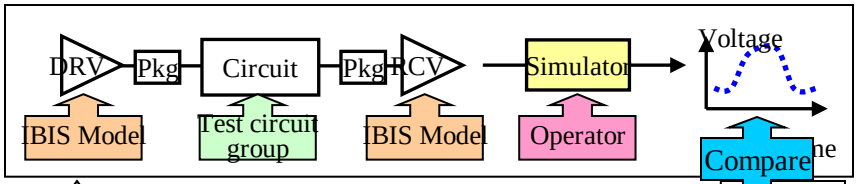
Open to the public of below data
(1)golden IBIS data
(2)Test circuit group
(3)golden results of waveforms (EXCEL data)

Web (open site)

Download

Set-Makers

Getting better IBIS from chip-vendors
Improve user's simulation skills



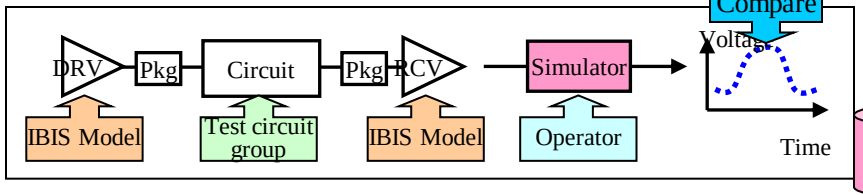
Golden IBIS

Test circuit group

Input data of test cir

better IBIS

Download

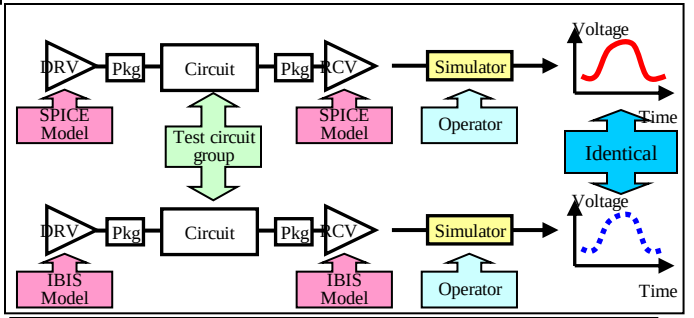


Compare

Upload

Input data of test cir

Download



EDA-Vendors

Improve the accuracy of simulator

Chip-Vendors

- offer the better IBIS model to their customers
- reduce the complaint from their customers

3. IBIS Promotion Working Group (New)

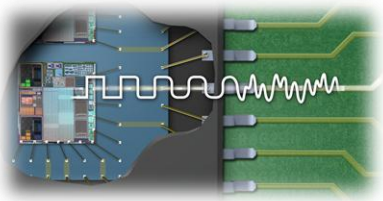
- Objective
- Action Plan
- Please Join Us !!

(Draft Idea)

Objective: Let's Use IBIS Simulation

SI/PI
IBIS 3.2
I-V Table
IBIS 5.1
IBIS 6.0
ISS
ISO
V-T Curve

Semiconductor Company



System Company

Give me IBIS 5.1 !

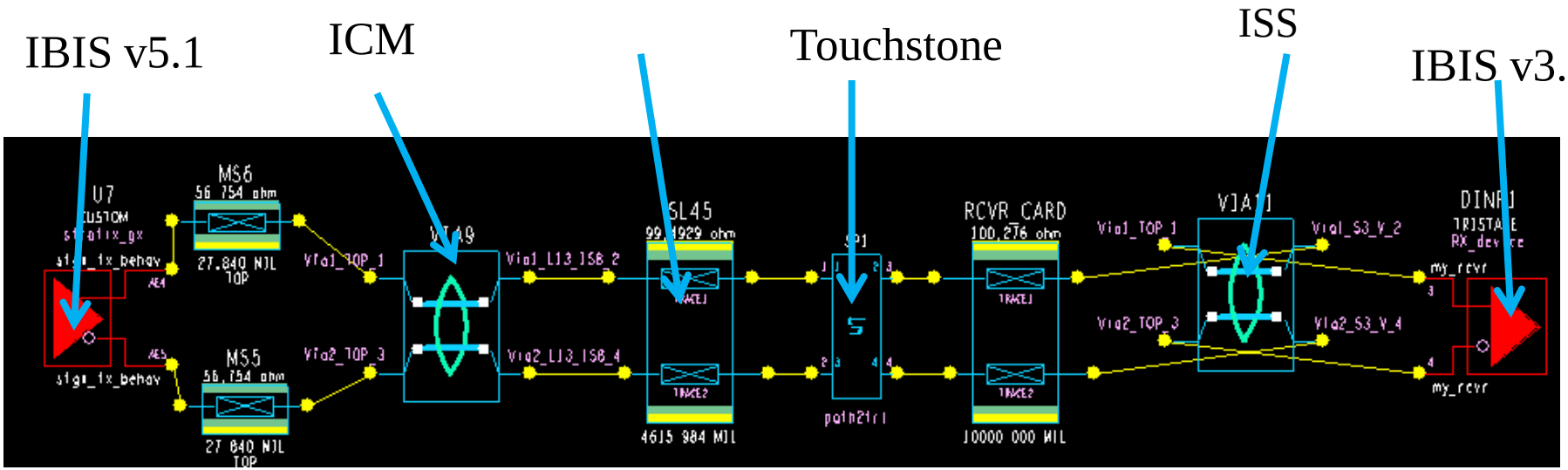
Do you need Power model ?
AMI Model ?
Do you use Linux ?
IBIS 3.2 is not enough ??

I don't know …..

IBIS Modeling
- How to develop IBIS 5.1
- AMI models

IBIS simulation
- Use PSpice ?
- V-T ?, AMI ?
- I have EBD model for memory

Action Plan 1: IBIS Spec Review



- Driver/Receiver: IBIS Version
  - Power Plane model, AMI Model, T-V table, External Model
- Interconnect Model
  - Connector : IBIS Interconnect Modeling (ICM)
  - Via model : IBIS Interconnect SPICE Subcircuit (IBIS-ISS)
- EBD
  - Electrical Board Description

Action Plan 2 : Keyword Summary

- Which keyword should be used for target application

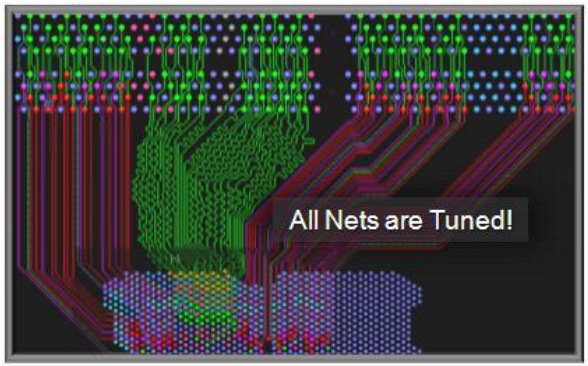
[Model] Parameter	
Model_type	Yes
Polarity	No
Enable	No
Vinl, Vinh	No
C_comp	Yes
Vmeas, Cref, Rref, Vref	No

Keyword	Required?	Description
[Pulldown]	No	Data representing the output I-V behavior of a buffer in the logic low state. This keyword is not used for input or open-source buffers. Depending on Model_type, the data may or may not include clamping effects. The data for this keyword is assumed ground-relative or relative to [Pulldown Reference], if present.
[Pullup]	No	Data representing the output I-V behavior of a buffer in the logic high state. This keyword is not used for input buffers or open-sink buffers. Depending on Model_type, the data may or may not include clamping effects. The data for this keyword is assumed Vcc-relative or relative to [Pullup Reference], if present.
[GND Clamp]	No	I-V table when the input or output of a buffer is in a high-impedance state. The voltage sweep is assumed ground-relative or relative to [GND Clamp Reference], if present.
[POWER Clamp]	No	I-V table when the input or output of a buffer is in a high-impedance state. The voltage sweep is assumed Vcc-relative or relative to [POWER Clamp Reference], if present.
		C_comp_power_clamp, C_comp_gnd_clamp are optional.
		Provides the simulator with this buffer's Tco measurement conditions

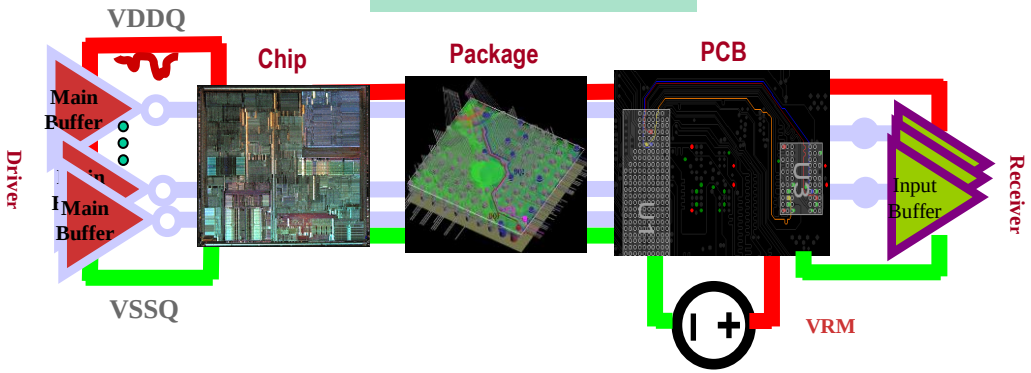
Action Plan 3: IBIS Version Summary

Which Version of IBIS Model should be used for each of cases

DDR3 Bus Crosstalk

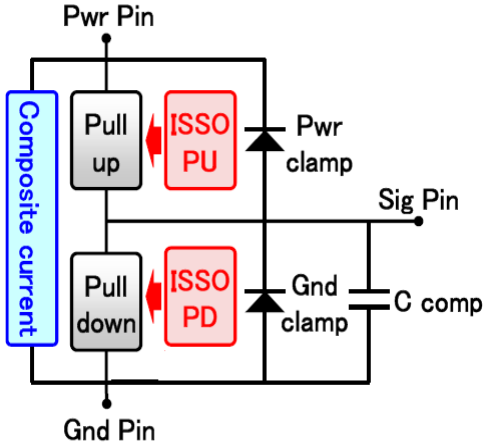


IC-PKG-PCB SSO



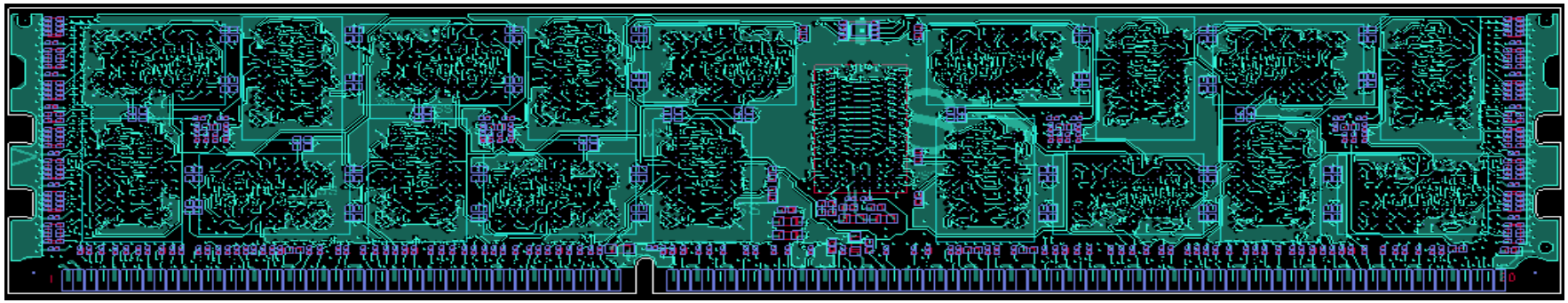
Custom SerDes (10Gbps)

Power Aware IO



Action Plan 4: IBIS Model Inconsistency

See Next Presentation for EBD sample



Proposed Activity Summary

1. IBIS Summit Japan
   - Support IBIS Open Forum for all logistics
     - Place, Program, Japan Presenters
     - Interpreting, Co-Sponsors
2. IBIS promotion of utilization
   - Provide any IBIS related information
     - Simulation Guidance
     - IBIS Version Summary
     - Keyword Summary
     - etc.

Activity Summary (cont')

3. Define IBIS simulation step guideline
   - Simulation Guideline for target topologies
   - Model Selection Guideline
4. Maintain IBIS Quality WG results
   - IBIS Quality Framework Home Page
   - JEITA Book:「SI Simulation Model」

Please Join US !

-Set Maker:	to define optimal signal performance
-Semiconductor Company:	to provide accurate IBIS model
-PCB Design Bureau:	to provide best signal performance