True Differential IBIS model for SerDes Analog Buffer

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Agenda

- Overview of Differential IBIS
- Description of test-case
- Flow used to create differential IBIS model
- Comparison: Pseudo-differential vs. True-Differential IBIS Serial-Link
- Conclusion

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Overview of Differential IBIS
- Current approaches

- Traditionally, differential buffer have been modeled as
  - Pseudo Differential buffer using two Single-ended IBIS models
    - Accuracy can suffer if there is substantial differential current which is the case with Serial Link analog buffers that has series elements between PADP and PADN
  - External Model approach: Call to buffer netlist
    - Netlist (IP) needs to be revealed
  - External Model approach: Call to S-parameter model
    - Rx buffer needs to be characterized as S-parameters

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Overview of Differential IBIS
- Alternate approach

- While S-parameter approach is best suited for analog buffers in serial links, we provide an alternate way to model it through standard IBIS tabular format with use of series elements to model differential current.
- This extends the approach suggested in IBIS cookbook that suggests modeling of differential current using series Resistance.
  - Here we propose use of reactive elements (R/L/C) to model differential current.

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Description of test-case
- IBIS modeling of Serial Link RX IO

- 10Gbps Serial link
- 28nm technology node
- Typical process node
- Rx analog buffer had additional blocks for equalization that were modeled as AMI code
  - Frontend attenuation
  - VGA
  - CTLE
  - DFE
  - CDR

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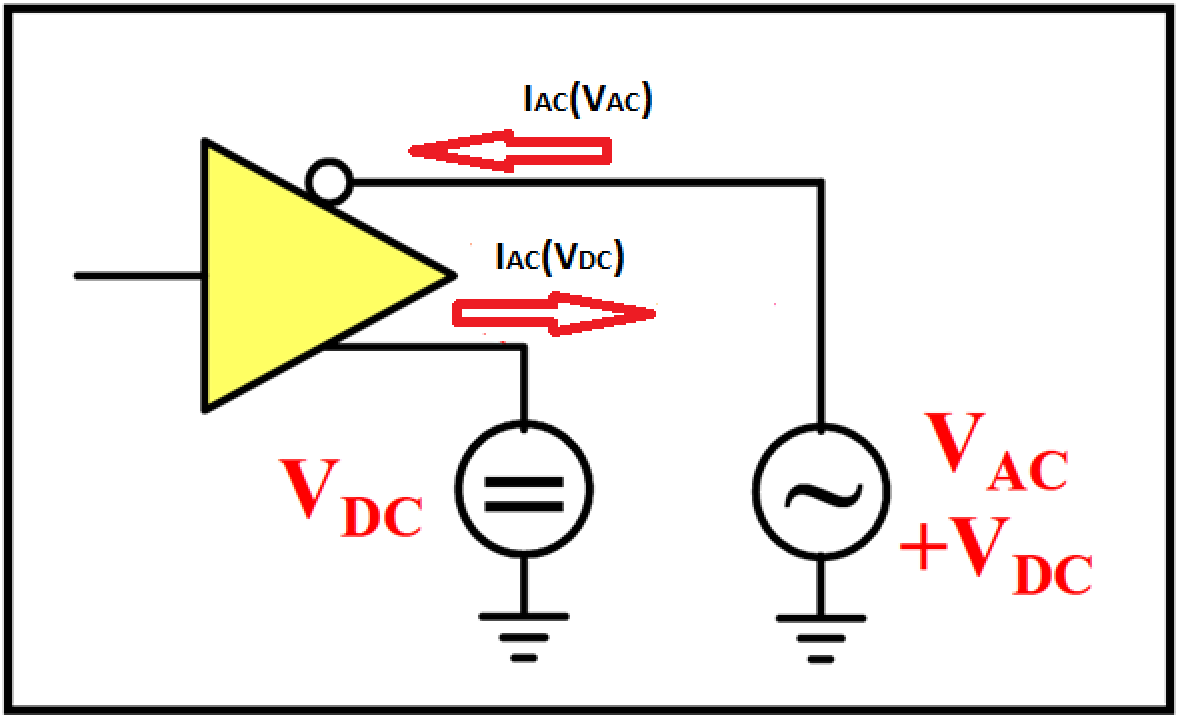
Flow used to create differential IBIS model - True differential

- Setup for common mode and differential mode currents extraction



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Flow used to create differential IBIS model - True differential

$$I\_Diff = I_{AC}(V_{DC})$$

$$I\_Comm = I_{AC}(V_{AC}) - I_{AC}(V_{DC})$$

-I_Diff flows through series element between inverting and non-inverting pins

-I_Comm flows only through common mode impedance

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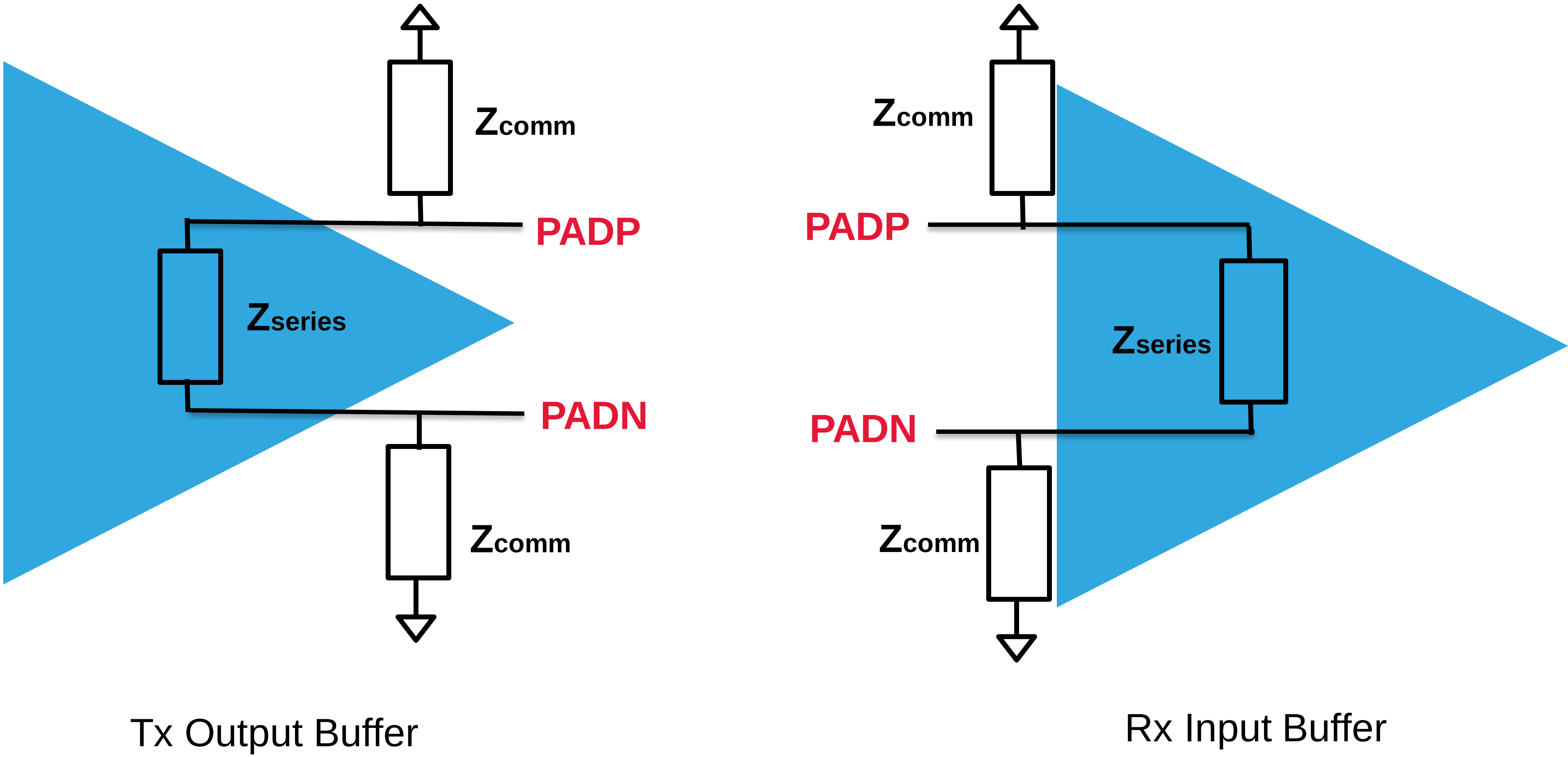
Flow used to create differential IBIS model

- True differential buffer with series element Z_{series}



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Flow used to create differential IBIS model
- True differential buffer with series element Zseries

- Zseries and Zcomm calculated at most likely operating frequency of buffer

- Assuming, at the most likely operating frequency of buffer, there could be
  – effective parallel RL circuit or effective parallel RC circuit between PADP and PADN (Z_{series})
  – Effective L or C decided depending on sign of imaginary part of I_Diff

- Always effective parallel RC between any pad and ground (Z_{comm})

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Flow used to create differential IBIS model
- Differential and common mode impedance calculations

- Effective Series Reactance = $X_{series} = \dfrac{V_{AC}}{\mathrm{Im}(I\_Diff)}$
- Effective Series Resistance= $R_{series} = \dfrac{V_{AC}}{\mathrm{Re}(I\_Diff)}$
- Effective Common mode Resistance= $R_a = \dfrac{V_{AC}}{\mathrm{Re}(I\_Comm)}$
- Effective Common mode Reactance= $X_a = \dfrac{V_{AC}}{\mathrm{Im}(I\_Comm)}$

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Flow used to create differential IBIS model
- Differential and common mode impedance calculations

- For 10G serial link testcase

Rx Series Model	R=220ohms	L=9.8nH
Rx Common mode Model	R=80ohms	C=0.223pF
Tx Common mode Model	R=50 ohms	C=0.500pF
Tx Series Model	Assume no series model	

- I_Diff and I_Comm plots for the testcase are shown next

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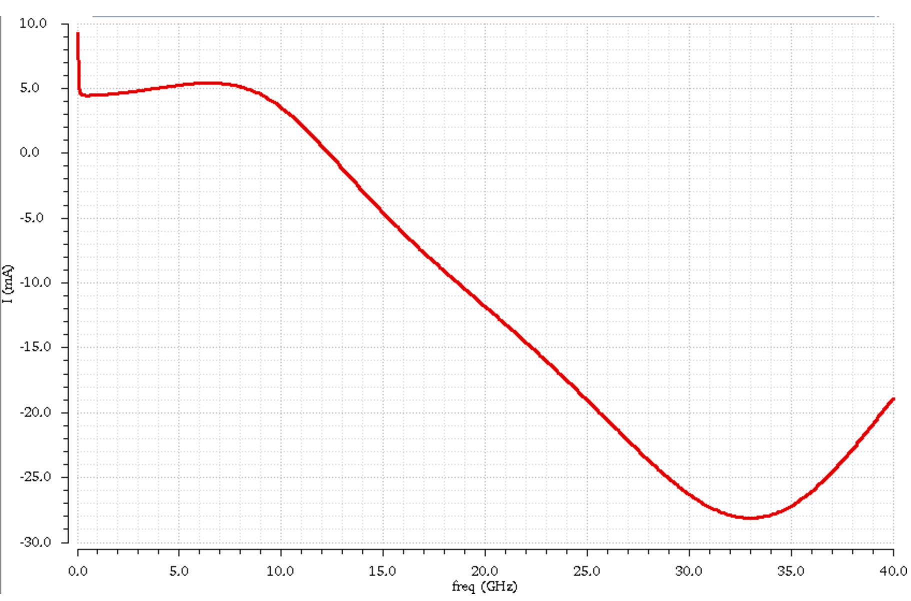
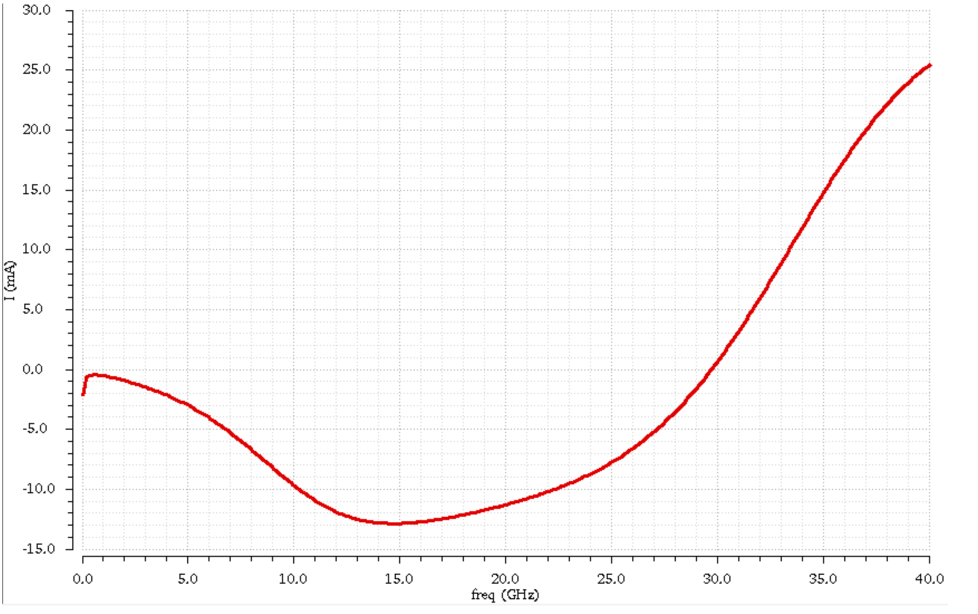
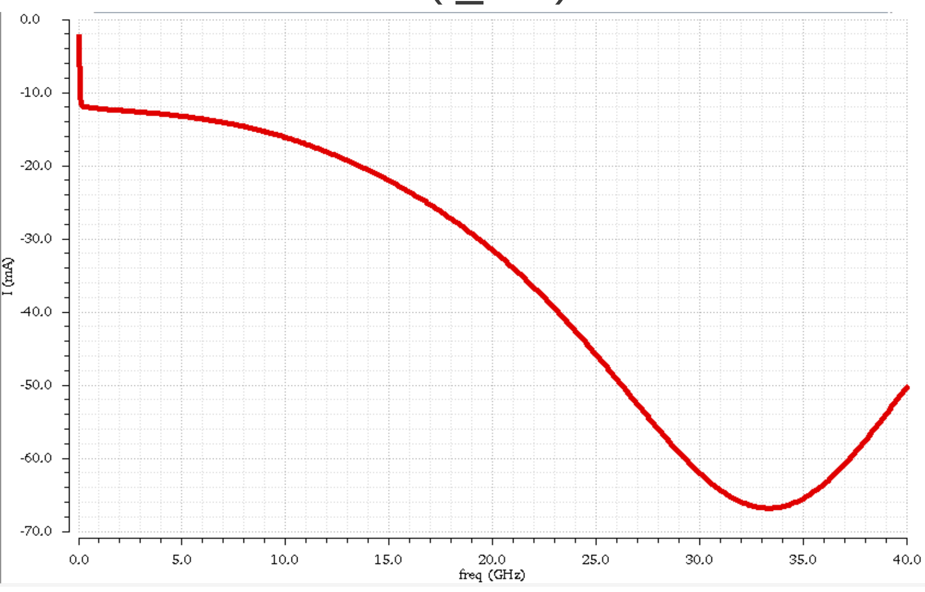
Common mode and differential currents



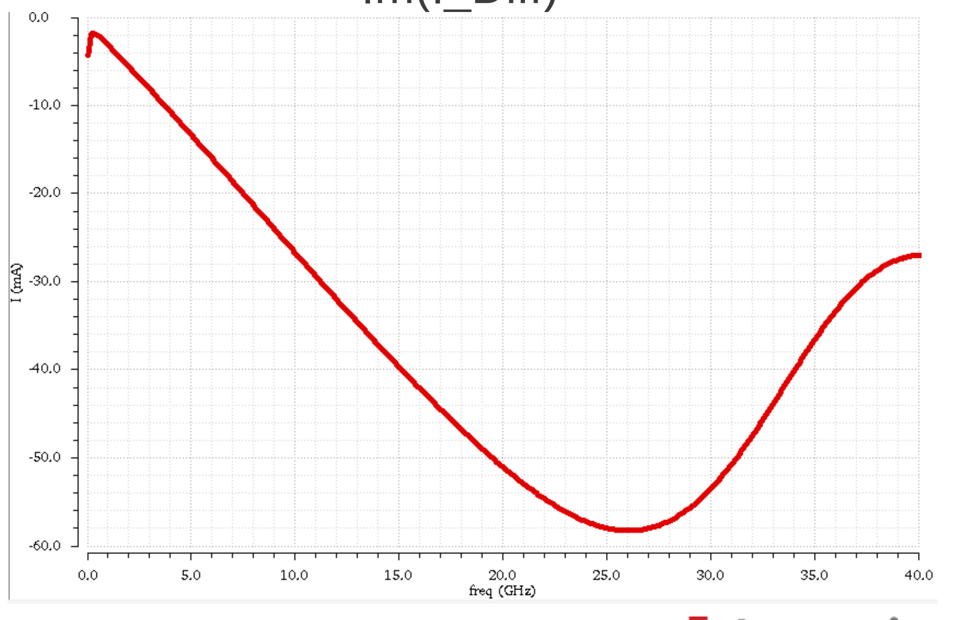
Re(I_Diff)



Im(I_Diff)



Re(I_Comm)



Im(I_comm)

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Flow used to create true-differential Rx IBIS model
- Rx IBIS model

```
|********************************************************************
***********
[Series Pin Mapping]    pin_2    model_name   function_table_group
4                        5         Rpath
4                        5         Lpath

|********************************************************************
```

```
**********
[Model] Rpath
Model_type Series
Polarity Non-Inverting
Enable Active-High
|
|                typ   min   max
 C_comp          0.0pF 0.0pF 0.0pF
|
|                typ    min    max
[Voltage Range] 1.0    NA     NA
|*****************************************************************
|            R(typ)   R(min)  R(max)
[R Series]  220       NA     NA

|
|*****************************************************************
**********
[Model] Lpath
Model_type Series
Polarity Non-Inverting
Enable Active-High
|
|                typ   min   max
 C_comp          0.0pF 0.0pF 0.0pF
|
|                typ    min    max
[Voltage Range] 1.0    NA     NA
|

|*****************************************************************
***********

|            R(typ)   R(min)  R(max)
[L Series]  9.8nH      NA     NA
|
```

- Effective Parallel RL network present as Zseries, modeled using “Model_type Series”

Flow used to create true-differential Rx IBIS model

- Rx IBIS model

- Effective Parallel RC network present as Zcomm, modeled using clamp I-V table and C_comp

```
[Model]      Rx_in
Model_type   Input
Vinl=1.5
Vinh=2.5
|
| variable                              typ          min          max
C_comp                                  0.223pF      NA           NA
[Temperature Range]                      70          NA           NA
[Voltage range]                         3.3          NA           NA
|
|*****************************************************************
**************
[POWER Clamp]
|
|  Voltage             I(typ)       I(min)       I(max)
|
  -3.3000e+00          20.6250e-03    NA          NA
   0.0000e-00          00.0000e-00    NA          NA
   3.3000e-00         -20.6250e-03    NA          NA

|*****************************************************************
**************
[GND Clamp]

|  Voltage             I(typ)       I(min)       I(max)

 -3.3000e+00         -20.6250e-03    NA            NA
  0.0000e-00          00.0000e-00    NA            NA
  3.3000e-00          20.6250e-03    NA            NA
|
|*****************************************************************
**************
```


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Flow used to create Tx IBIS model

- Tx IBIS model

- Effective Parallel RC network present as Zcomm, modeled using Pulldown and Pullup I-V tables and C_comp
- Assume no series element Zseries present

```
|
|
| variable                            typ     min      max
C_comp                              0.5pF     NA        NA
[Temperature Range]                  70       NA        NA
[Voltage range]                     1.0V      NA        NA
|
|***************************************************************
*****************
[Pulldown]
|
|  Voltage               I(typ)      I(min)       I(max)
|
  -1.000e+00          -2.00e-02     NA             NA
   0.0000e-00          0.00e-0      NA              NA
   1.000e+00           2.00e-02     NA             NA
|
|***************************************************************
*****************
[Pullup]
|
|  Voltage               I(typ)       I(min)       I(max)
|
  -1.000e+00          2.00e-02       NA            NA
   0.0000e-00         0.0000e-00     NA             NA
   1.000e+00         -2.00e-02       NA             NA
|***************************************************************
*****************
[Ramp]
|
| variable       typ                min                max
dV/dt_r     0.600/0.024E-09          NA                 NA
dV/dt_f     0.600/0.024E-09          NA                 NA
R_load = 50
```

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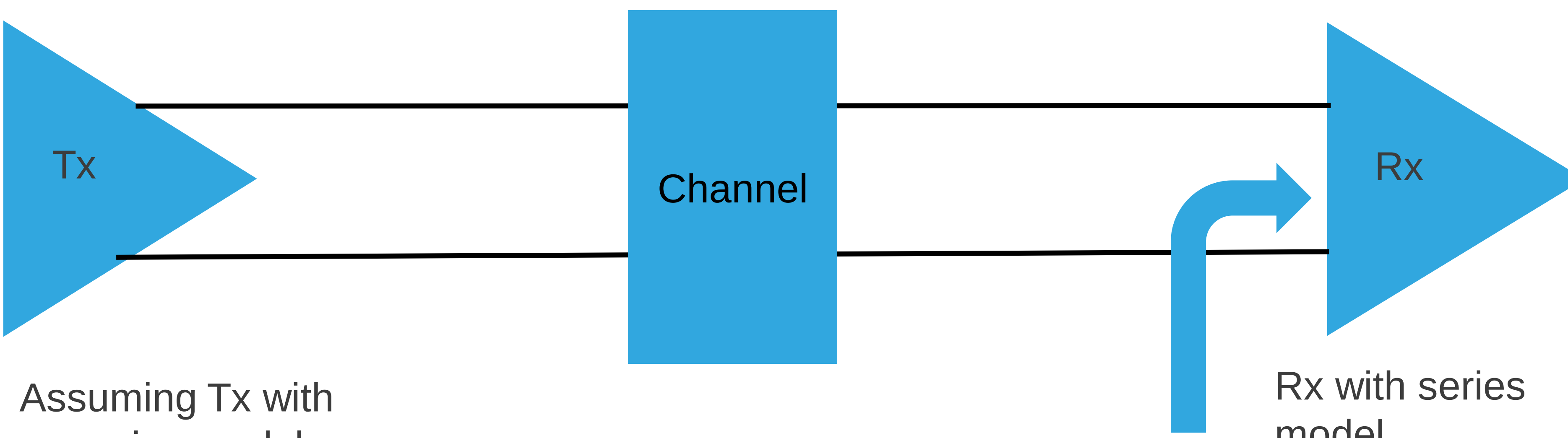
Comparison: Pseudo-differential vs. True-Differential IBIS simulations

- Serial Link Simulation Test-bench
  - 10Gbps
  - No Equalization
  - PRBS23
  - Tested on different channels



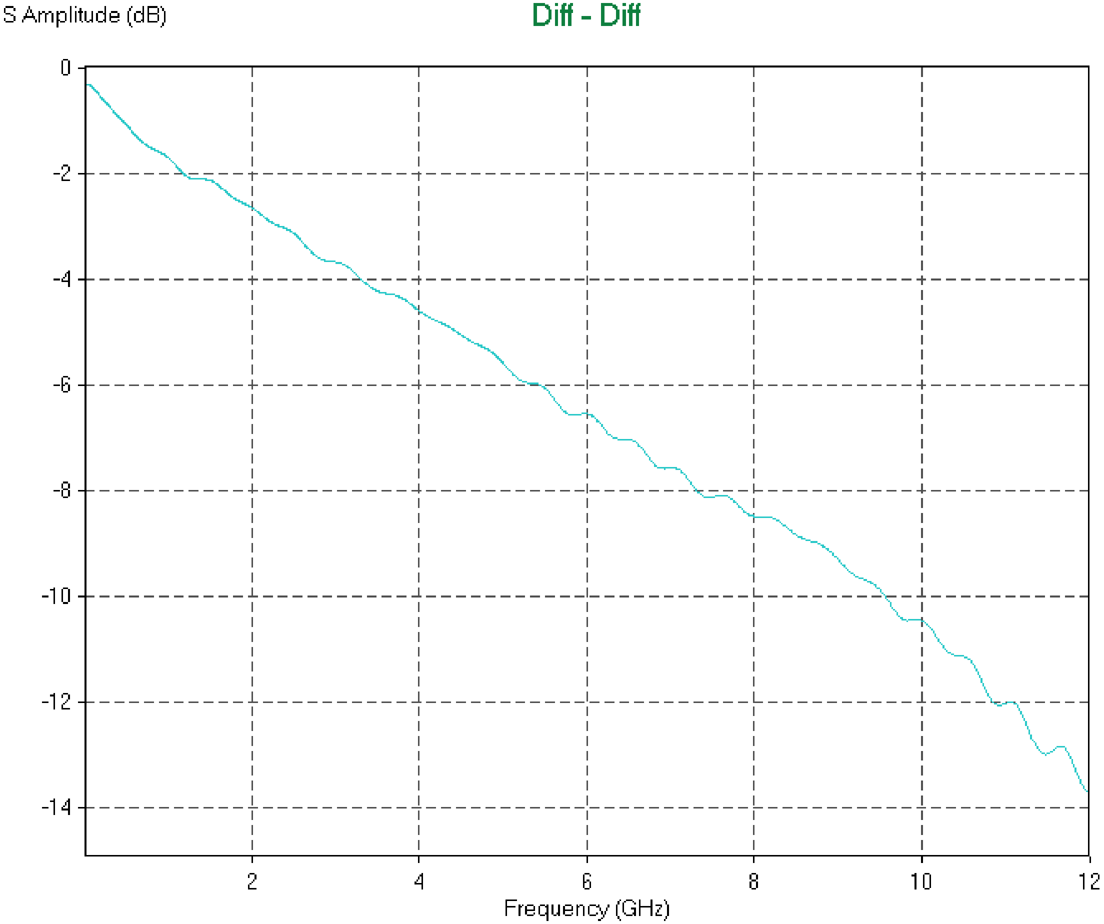
Assuming Tx with no series model

Rx with series model

Eye is seen here

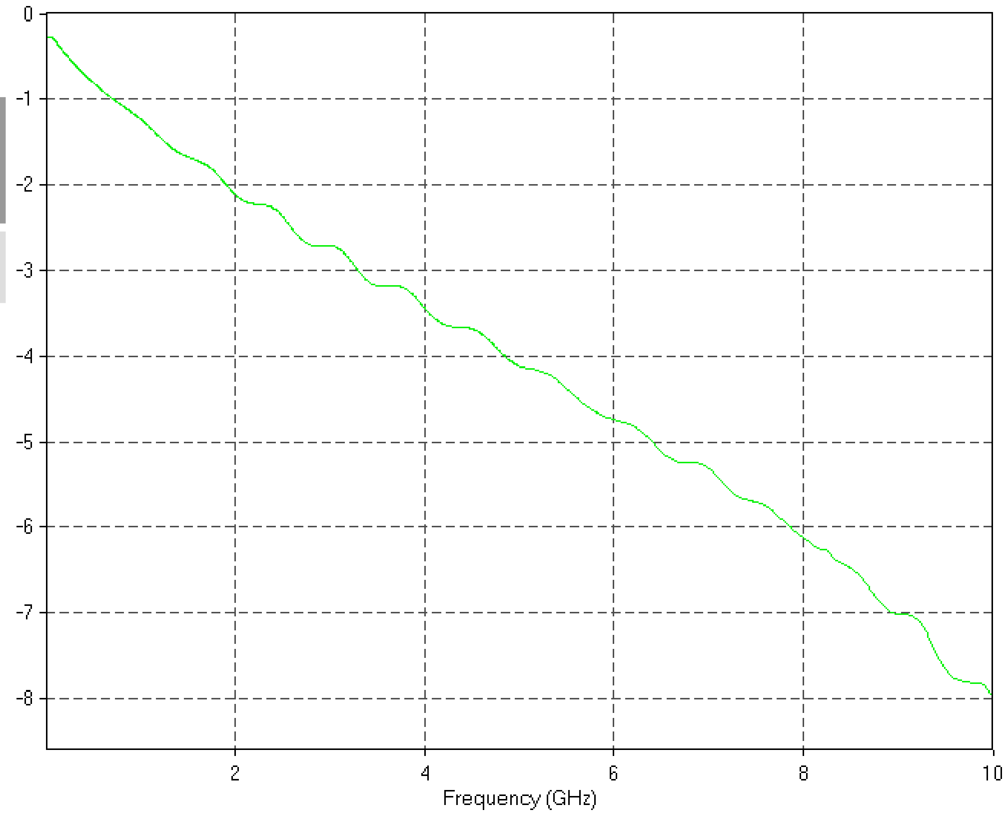
Channel 1

Frequency	Insertion Loss
5.15GHz	-5.861dB



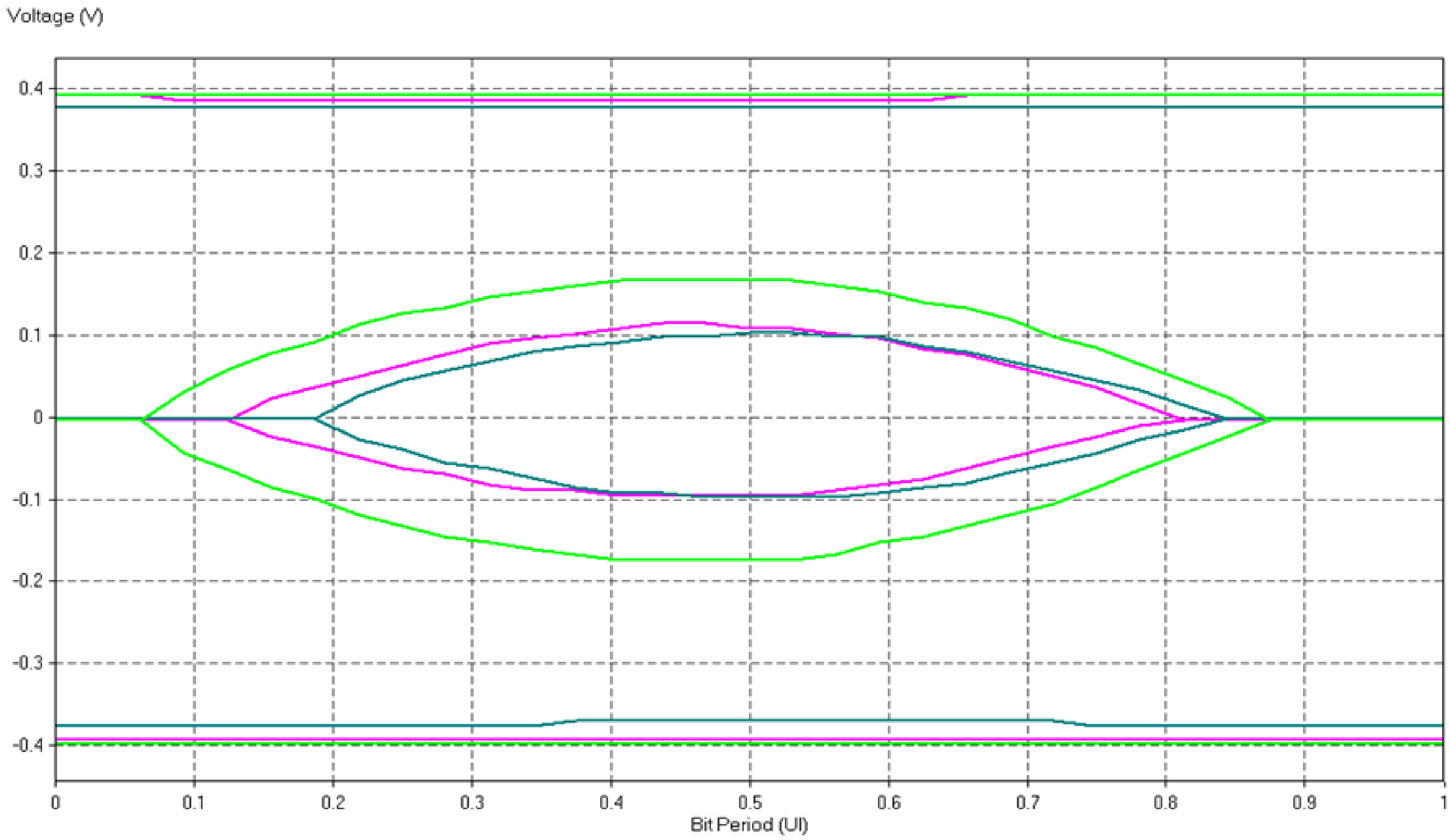
Channel 2

Frequency	Insertion Loss
5.1GHz	-4.14dB



Comparison: Pseudo-differential IBIS vs. True-Differential IBIS vs. Circuit simulations

- Channel 1



Circuit Simulation
Psuedo-differential buffer IBIS simulation
True-differential buffer IBIS simulation

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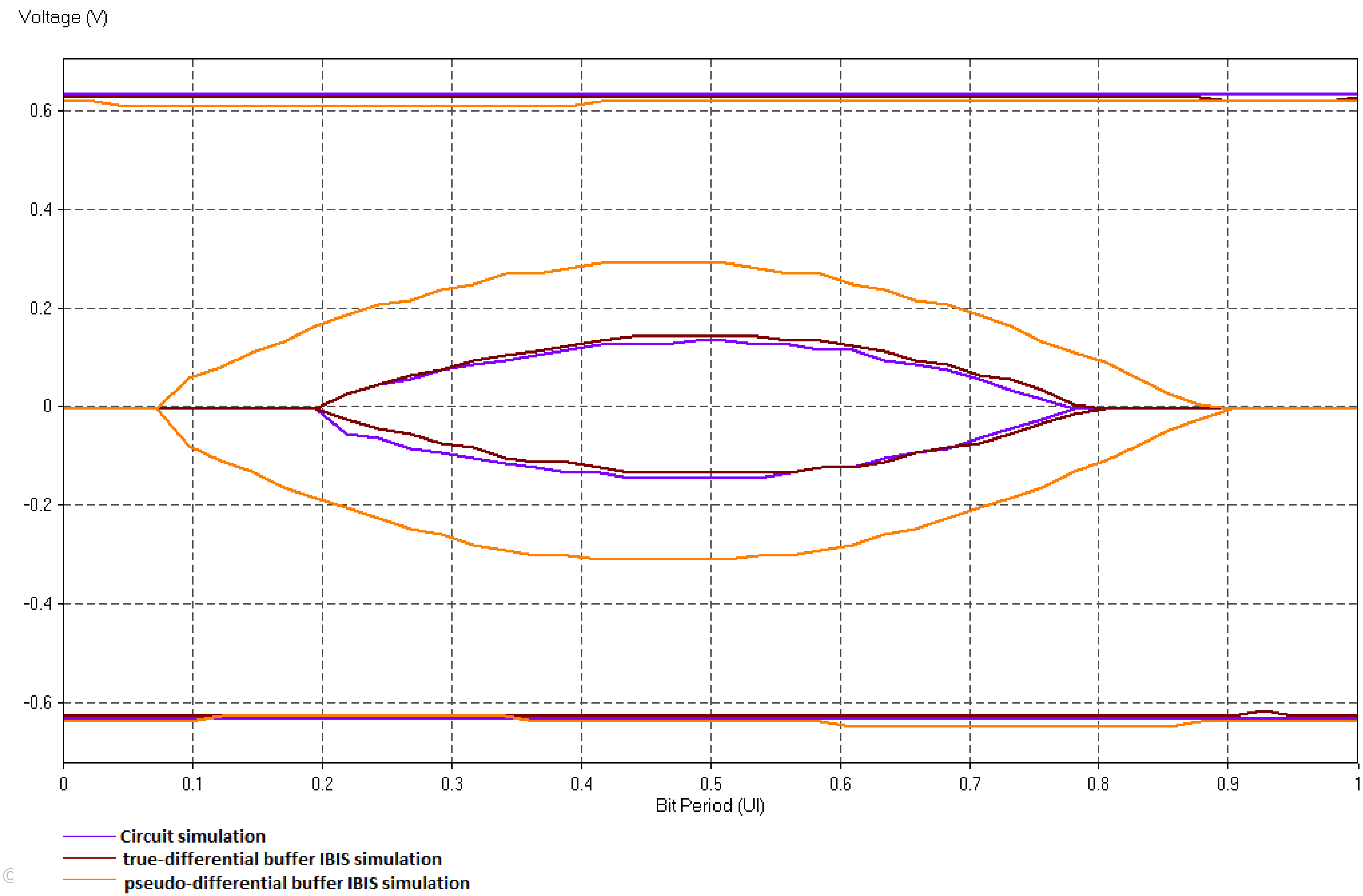
Comparison: Pseudo-differential IBIS vs. True-Differential IBIS vs. Circuit simulations

- Channel 2



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Conclusion

- Extended “Series Model Approach” in Cookbook for IBIS Version 4.0 to model differential and common-mode impedances for SERDES analog buffer.
- True differential model provides much better accuracy than pseudo differential IBIS for channel simulations in terms of
  - Jitter and eye opening
  - Reflection losses

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