Signing IBIS model against DDR4 spec

Tushar Malik, Taranjit Kukal

IBIS Asia Summit
Taipei, Taiwan
Nov. 17, 2014

cadence®

Agenda

- Problem Statement
- Overview of DDR compliance checks
- Methodology to check DDR compliance
  - Impedance
  - Slew rate
  - Pulse-width variation
- Conclusion

Agenda

- Problem Statement
- Overview of DDR compliance checks
- Methodology to check DDR compliance
  - Impedance
  - Slew rate
  - Pulse-width variation
- Conclusion

Problem Statement
- Certify Controller IBIS models before system simulations

- DDR compliance needs to be done on a system interconnect starting from Controller to Memory IO
- If DDR IBIS models do not adhere to DDR JEDEC standards, designer may wrongly associate performance issues with interconnect elements like board, connector, DIMMs, package.
- It is important that we decouple the testing into
  - Testing of IBIS models to make sure they comply with JEDEC standards
  - Testing of interconnect elements with above certified IBIS models

Problem Statement
- Do exhaustive checks on IO netlist performance

- Simulating IO-netlists for all corners to verify compliance against JEDEC specs is time-consuming.

- Since IBIS modeling is an automated process, the generated IBIS model can quickly provide results that can be verified against JEDEC requirements (for all corners and impedance settings) like
  - Impedance variation
  - Slew rates
  - Pulse-width variation
  - ZQ calibration based on process corners

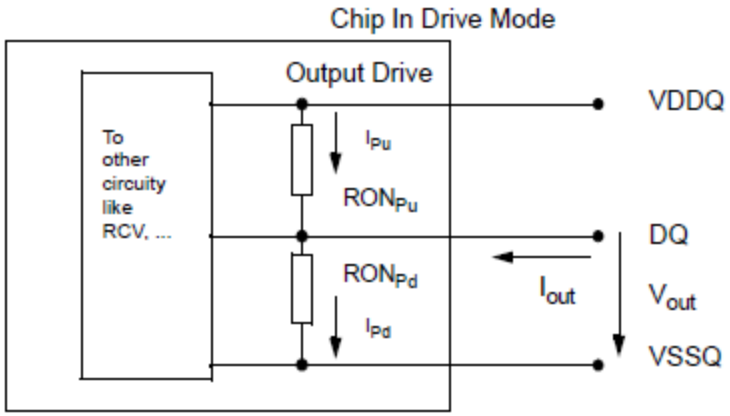
Agenda

- Problem Statement
- Overview of DDR compliance checks
- Methodology to check DDR compliance
  - Impedance
  - Slew rate
  - Pulse-width variation
- Conclusion

Overview of DDR compliance checks - JEDEC DDR4 spec (output impedance)

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\,out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\,out|}$$ under the condition that RON_{Pu} is off



RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	34Ω	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	34Ω	1,2
		VOHdc= 1.1* VDDQ	0.9	1	1.25	34Ω	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	34Ω	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	34Ω	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	34Ω	1,2

Spec indicates impedance measurement to be done at different Vout levels and that they should be within +/- 10%

Overview of DDR compliance checks - Single-ended slew rate

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$V_{OL}(AC)$	$V_{OH}(AC)$	$[V_{OH}(AC)-V_{OL}(AC)]$ / Delta TRse
Single ended output slew rate for falling edge	$V_{OH}(AC)$	$V_{OL}(AC)$	$[V_{OH}(AC)-V_{OL}(AC)]$ / Delta TFse

NOTE :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

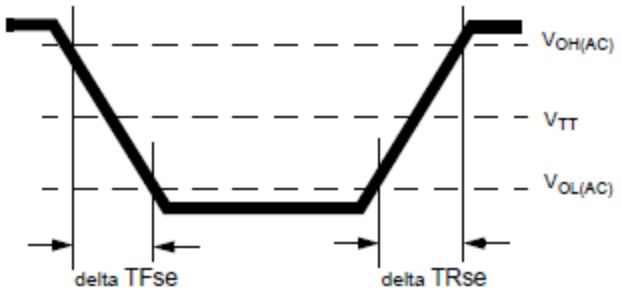


Figure 182 — Single-ended Output Slew Rate Definition

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	TBD	TBD	TBD	TBD	V/ns

Spec indicates that DQ slew rate should be within Min and Max values

cadence

Overview of DDR compliance checks - Differential slew rate

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TRdiff
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TFdiff

NOTE :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

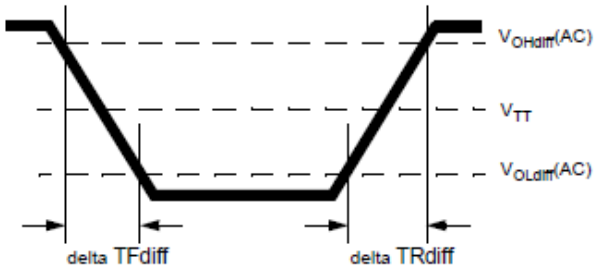


Figure 183 — Differential Output Slew Rate Definition

Table 79 — Differential output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	TBD	TBD	TBD	TBD	V/ns

Spec indicates that DQS slew rate should be within Min and Max values

Overview of DDR compliance checks - Pulse-Width@data-rate

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	
Clock Timing								
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	8	-	ns
Average Clock Period	tCK(avg)	tbd –(Definition tbd)						ps
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)

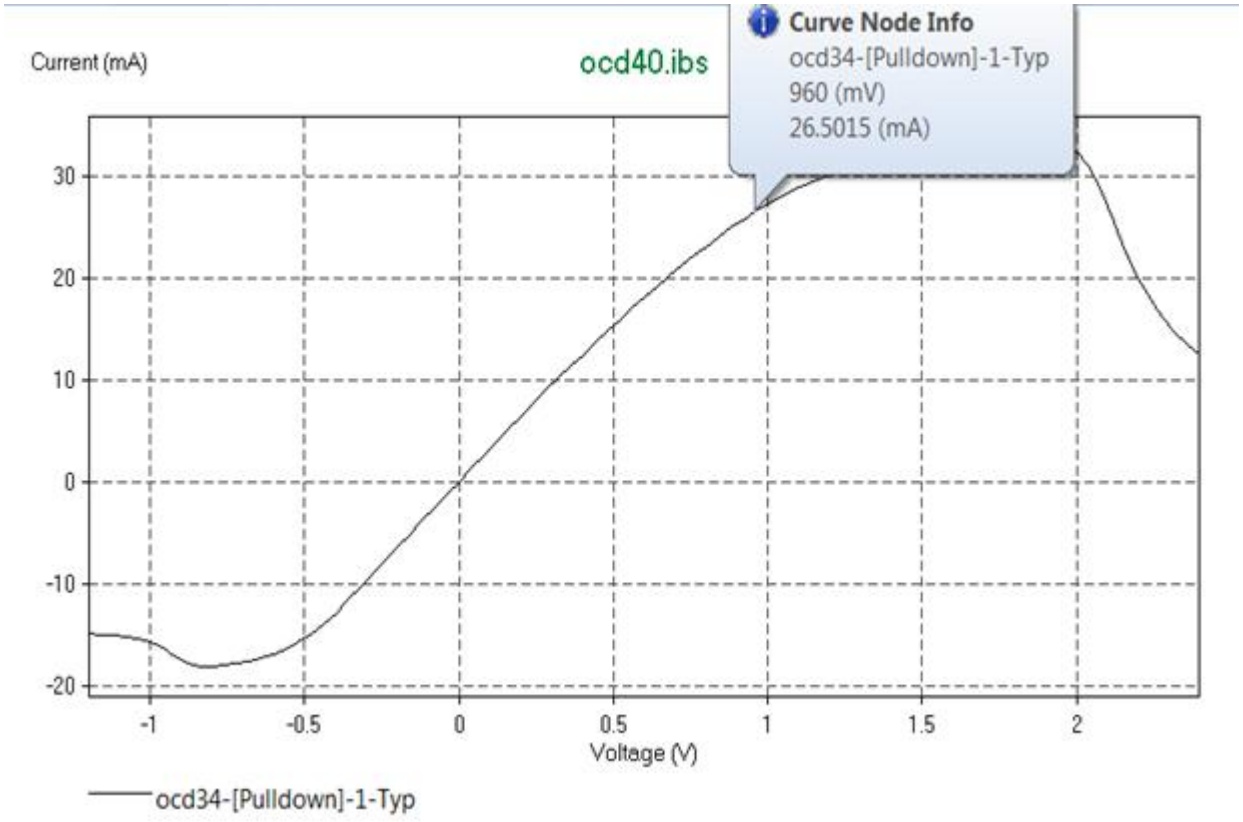
Spec indicates that the duty cycle should be greater than .45UI

Agenda

- Problem Statement
- Overview of DDR compliance checks
- Methodology to check DDR compliance
  - Impedance
  - Slew rate
  - Pulse-width variation
- Conclusion

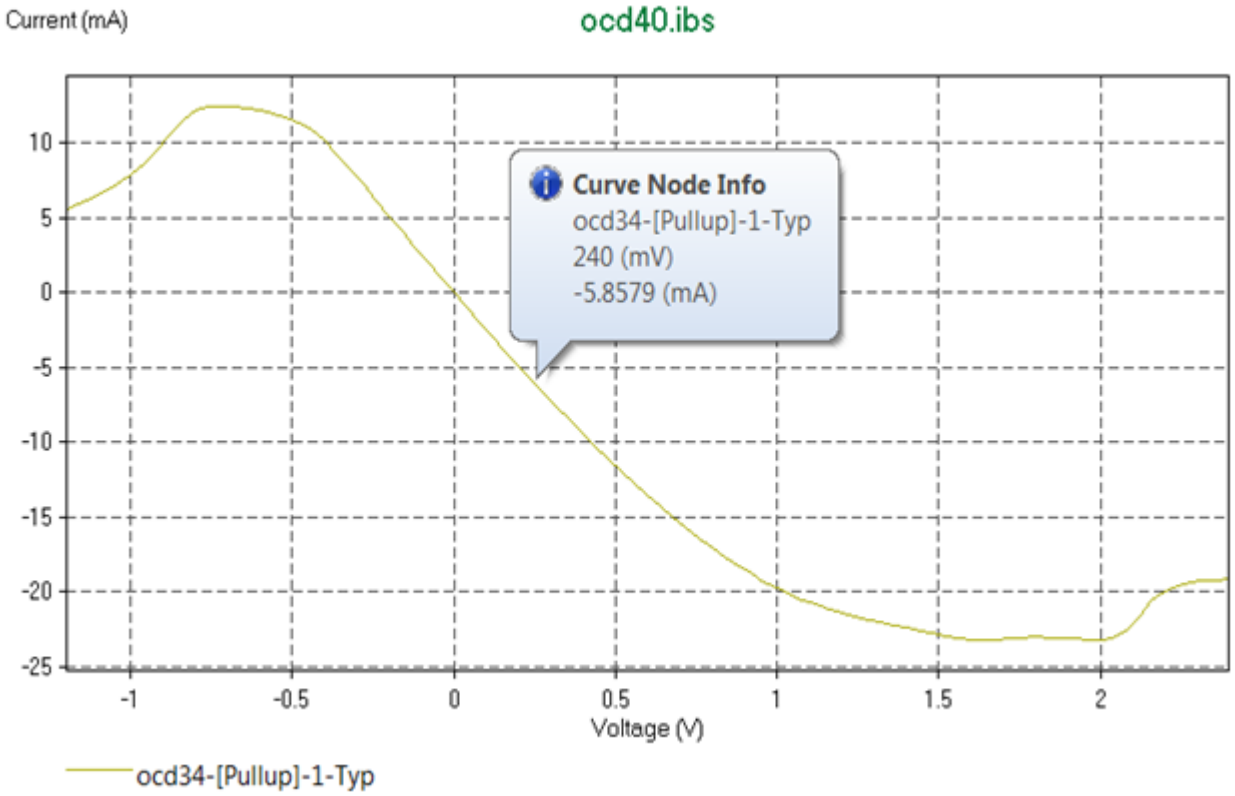
Methodology to check DDR compliance - IBIS impedance measurement (pulldown)

- IV curves of IBIS can be plotted to ensure that they fall within +/- 10% tolerance



Methodology to check DDR compliance - pullup

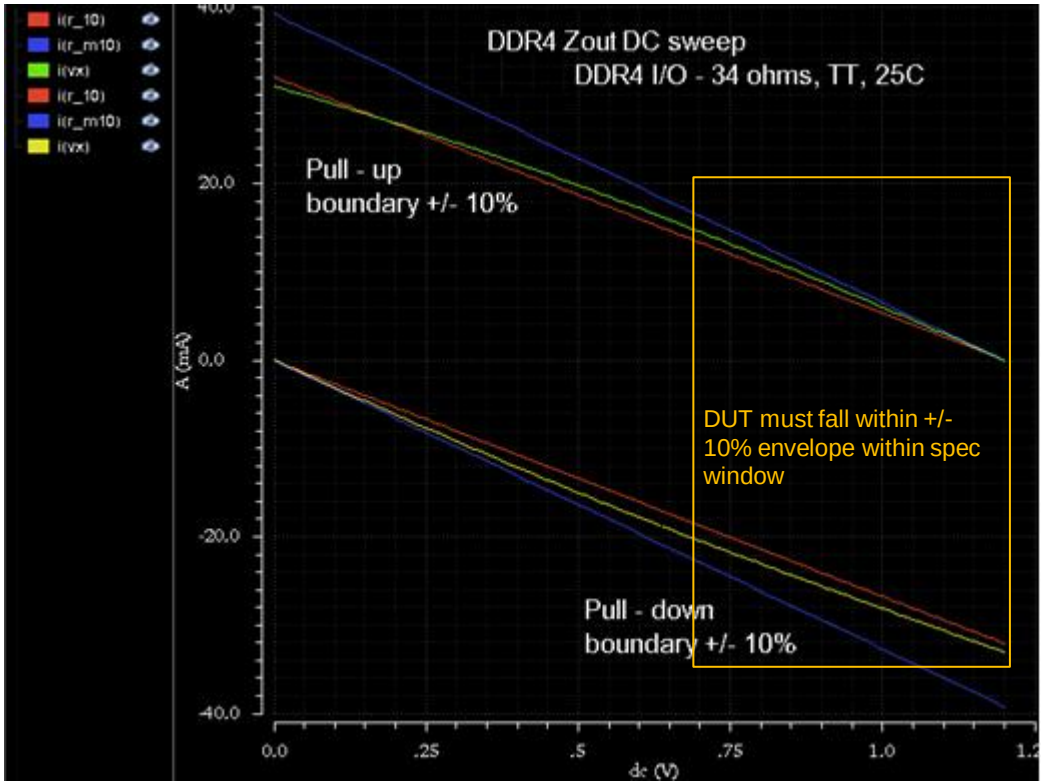
- IV curves of IBIS can be plotted to ensure that they fall within +/- 10% tolerance

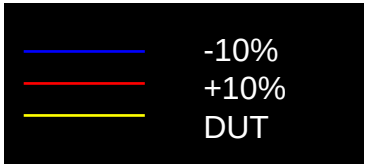


cadence

Methodology to check DDR compliance - Impedance check

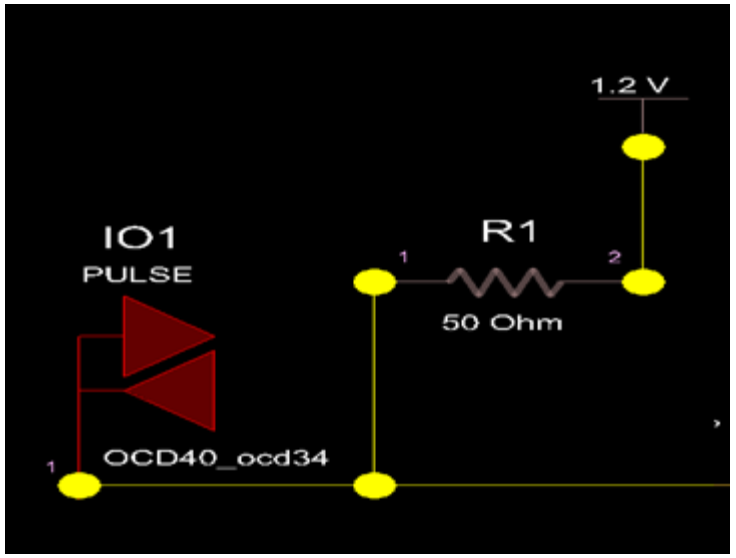
- IV plots from IBIS being compared against 10% limits



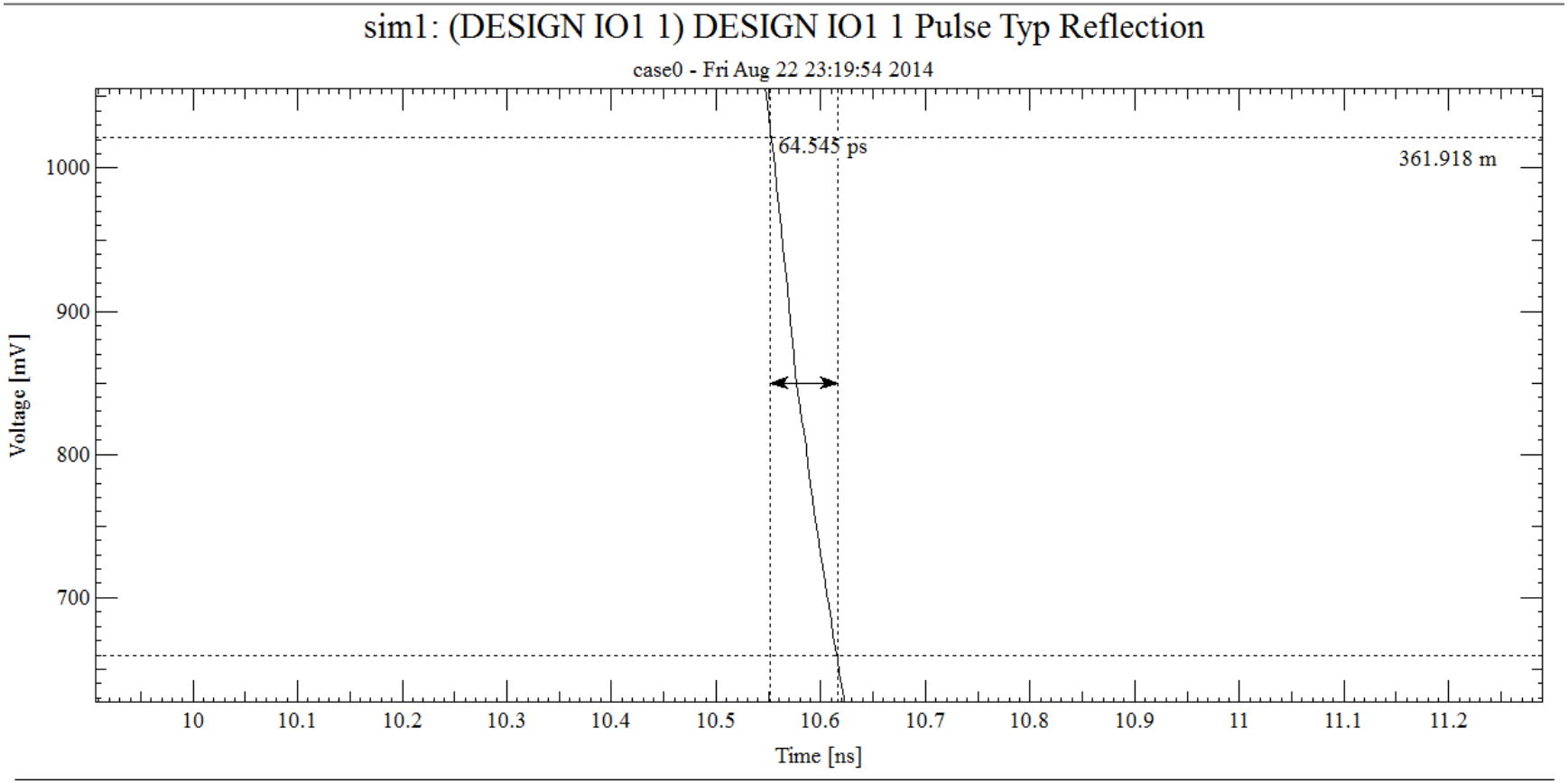


Methodology to check DDR compliance
- Single ended slew rate measurement test-bench

- Figure shows simple drive of IO buffer with 50ohms pull-up to capture the rise time.

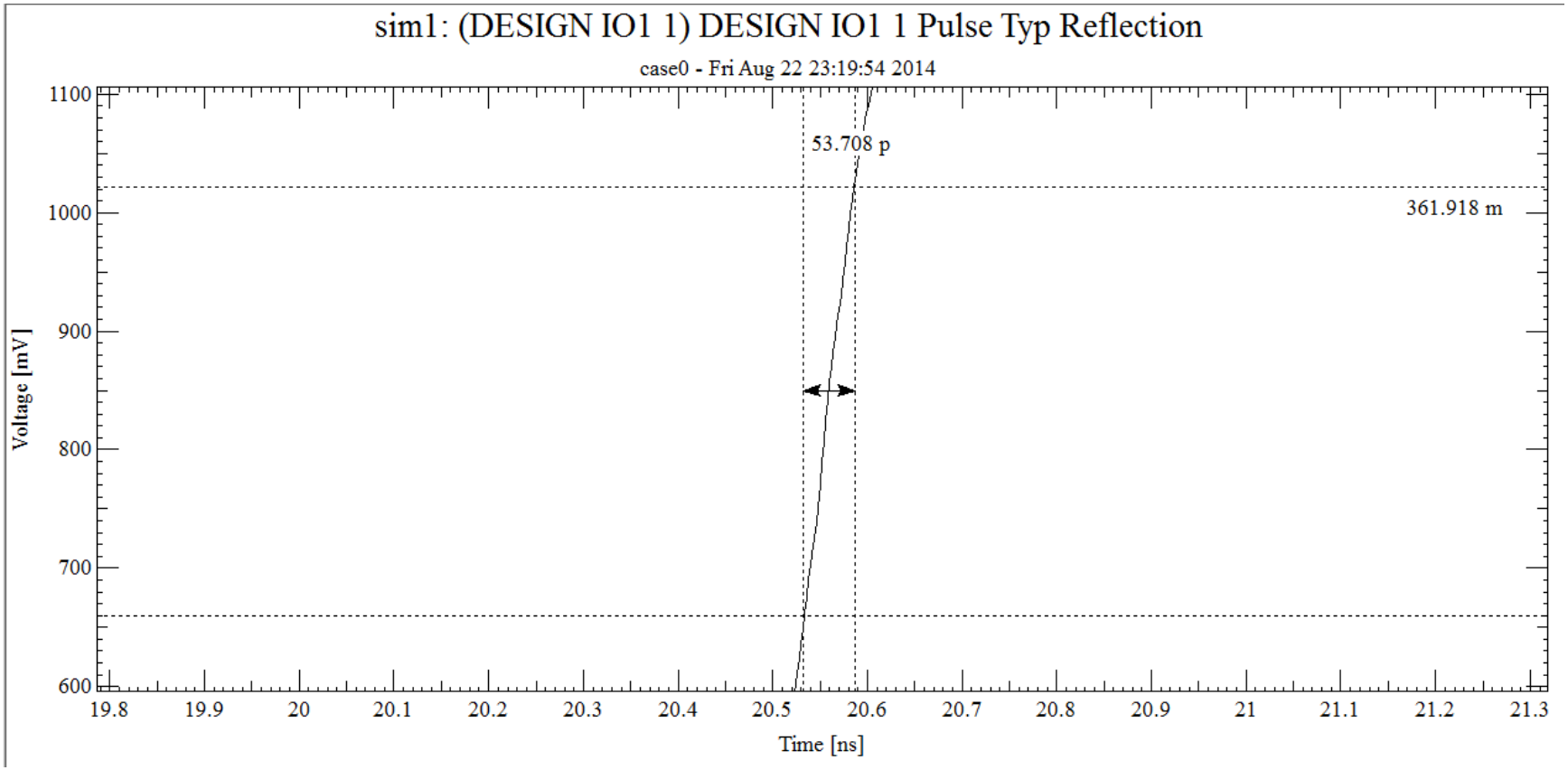


Falling slew rate dv/dt



Here dv/dt = 360mV/65pS = 5.6 V/ns which is within spec of 4 to 9 V/ns

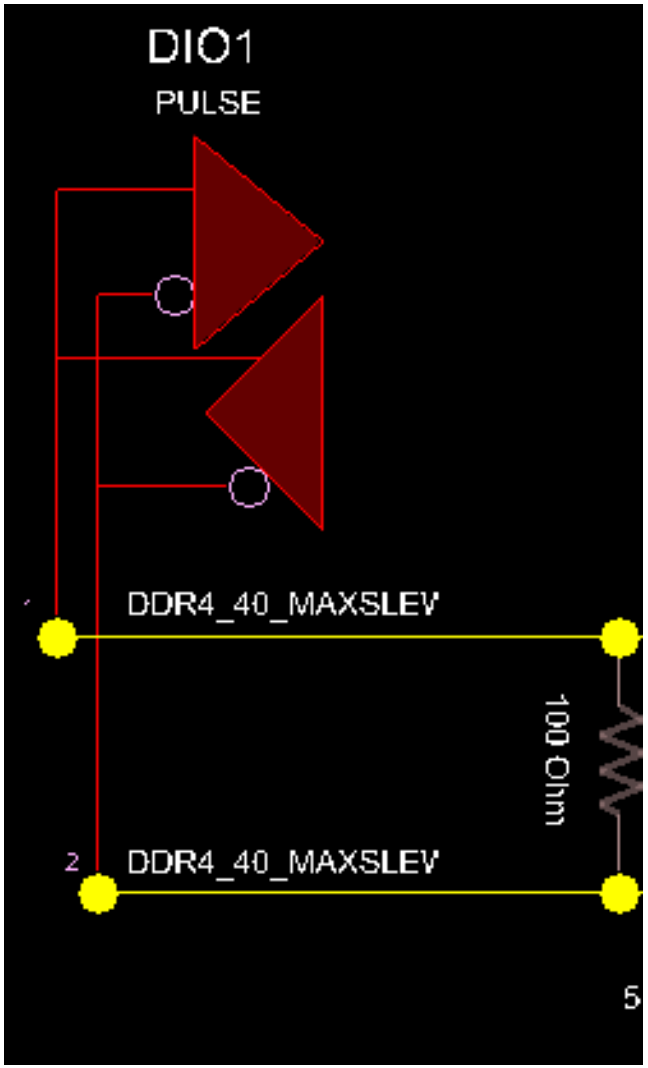
Rising slew rate



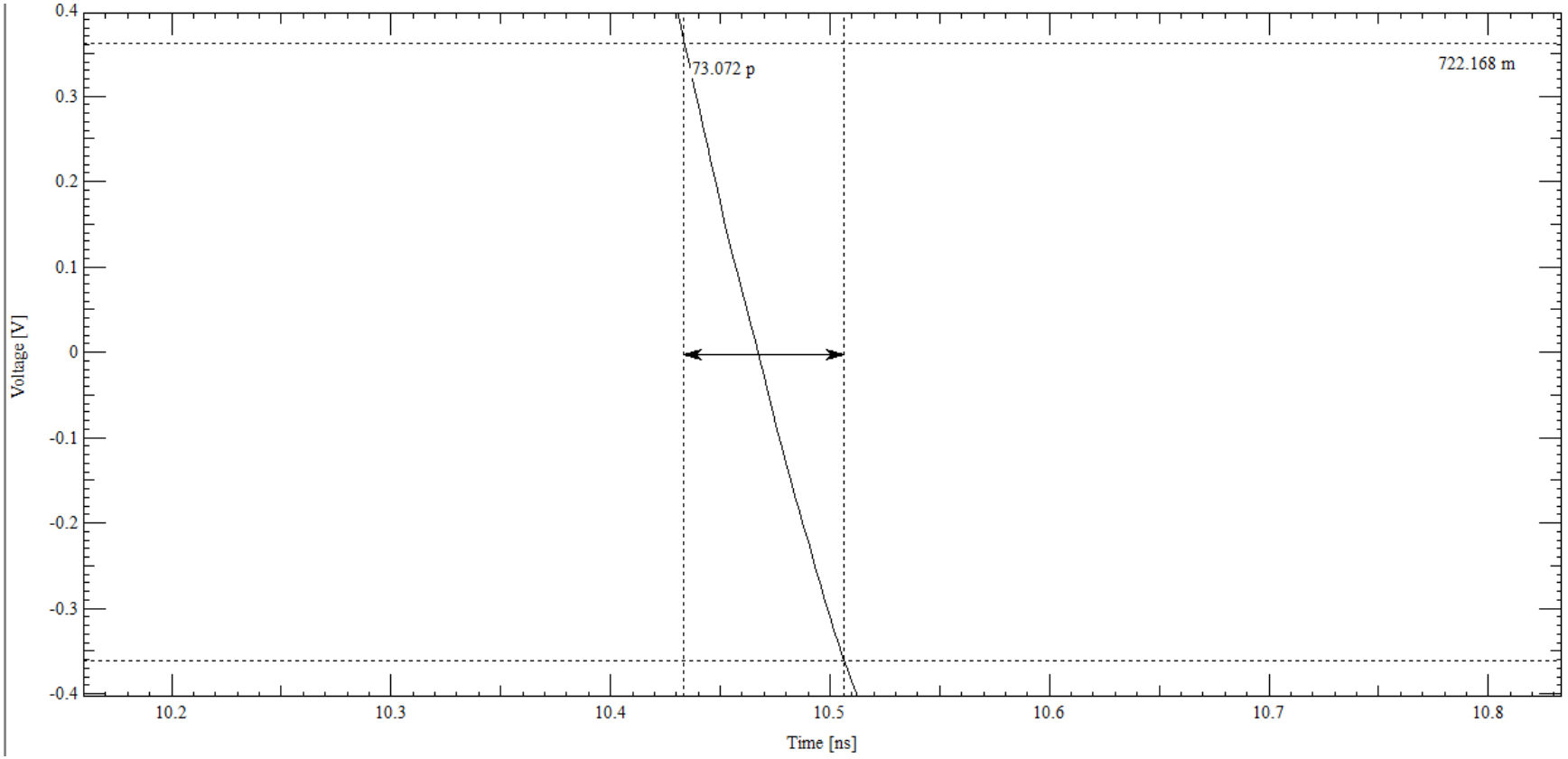
Here dv/dt = 360mV/54pS = 6.6 V/ns which is within spec of 4 to 9 V/ns

Methodology to check DDR compliance - Differential test-bench (DDR4)

- Figure shows simple drive of differential IO buffer with 100 ohms termination to capture the rise and fall time.

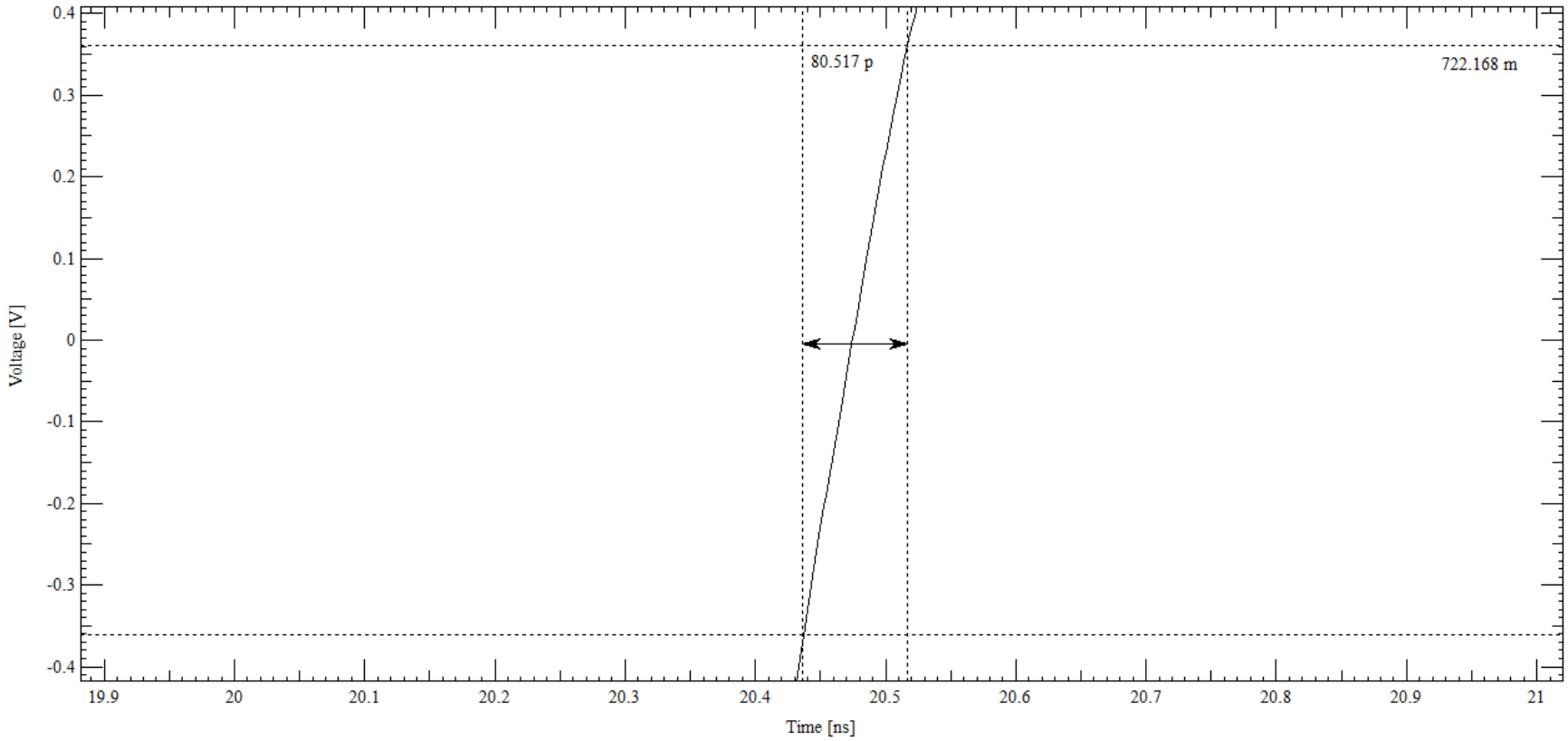


Falling Slew Rate



Here dv/dt = 722mV/73pS = 9.9 V/ns which is within spec of 8 to 18 V/ns

Rising Slew Rate

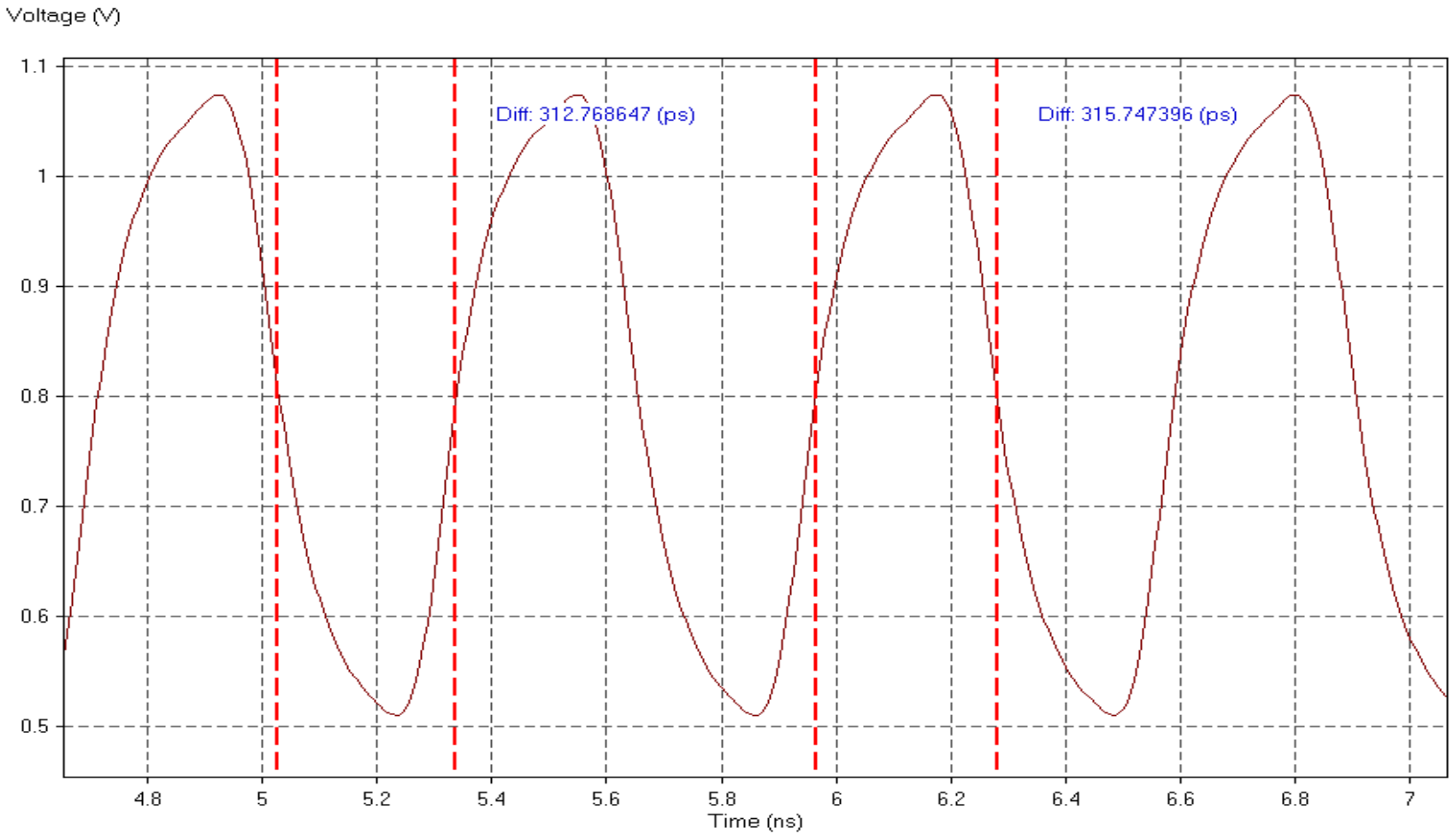


Here dv/dt = 722mV/80pS = 9.0 V/ns which is within spec of 8 to 18 V/ns

Methodology to check DDR compliance - Timing Checks

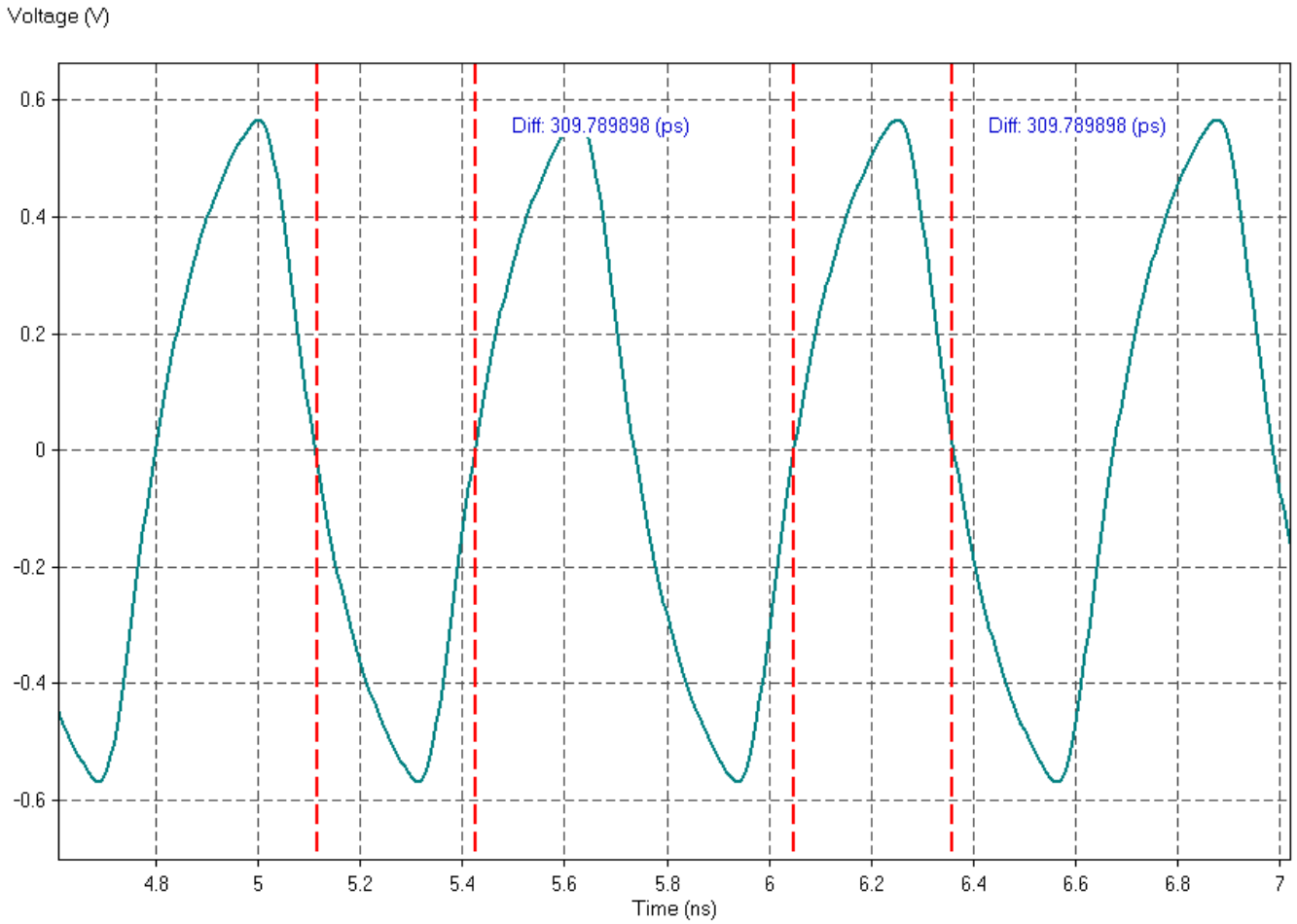
- Average High Pulse
- Average Low Pulse
- Average Clock Period

Data Pulse variation @ 3.2G (slow corner)



Here min duty cycle is 312pS/625pS = .499UI > .45UI

Clock Pulse variation



Here min duty cycle is 309pS/625pS = .494UI > .45UI

Agenda

- Problem Statement
- Overview of DDR compliance checks
- Methodology to check DDR compliance
  - Impedance
  - Slew rate
  - Pulse-width variation
- Conclusion

Conclusion

- It is important to verify DDR controller IBIS separately before doing system simulations
- IBIS verification against JEDEC requirements can help in
  - Quickly verifying PHY netlist for compliance
  - Ensuring that IBIS models have been correctly made with proper netlist settings, especially when ZQ calibration needs to be properly done to obtain proper impedance values at corners.