WELCOME FROM MICHAEL MIRMAK, INTEL CORPORATION

On behalf of the I/O Buffer Information Specification (IBIS) Committee, I would like to welcome you to this Asian IBIS Summit, our fifth in Taiwan. We are delighted to see continued interest in our IBIS summits, and hope that these events have now become an autumn "tradition" for the IBIS community here.

IBIS itself recently celebrated the 15th year of being an international standard under the International Electrotechnical Commission (IEC). Our growth worldwide and our long history present us with challenges and opportunities. We are challenged daily in maintaining the stability of IBIS across versions while offering new features and supporting the latest technologies. You can see this most clearly in recent IBIS-AMI updates for advanced buffer designs as well as our work in improving IBIS support of modern interconnects.

Our greatest opportunity is the ability to hear from you, the IBIS community. Through these Summits and our online conversations, we are able to understand your needs and work together to ensure IBIS meets them. We encourage you to provide feedback both on our specifications and on how we can interact with you better.

We are especially grateful to our sponsors ANSYS, Cadence Design Systems, Intel Corporation, IO Methodology, and Synopsys for making this Summit possible.. We encourage you to express your thanks to them for their support of IBIS.

As always, we wish you success and hope that you will find the presentations and discussions beneficial and enjoyable.

Sincerely,

Michael Mirmak
Chair, IBIS Committee

WELCOME FROM MICHAEL MIRMAK, INTEL CORPORATION

首先我僅代表 IBIS 委員會，歡迎您來到這次亞洲 IBIS 峰會，今年是我們在台灣的第五次會議。我們很高興看到我們的 IBIS 峰會被持續關注，並希望這個會議現在能成為一個秋天的“傳統”節目。

IBIS 標準本身成為國際電子技術委員會（IEC ）的國際標準已有的 15 個年頭了。我們在全球的增長和我們悠久的歷史為我們提供了機遇和挑戰。在維持 IBIS 跨版本的穩定性，同時提供新的功能，並支持最新的技術方面我們每天都面臨著挑戰。您可以從最近為先進的緩衝設計的 IBIS-AMI 更新，以及我們在改善 IBIS 支持現代互連器件的工作可以清楚地看到這一點。

我們最大的機遇是您對 IBIS 社區的支持。通過這些峰會和我們的在線交談，我們能夠理解您的需求，我們要共同努力，確保 IBIS 滿足需求。我們鼓勵您對我們的規范以及如何更好的互動給予反饋。

我們要特別感謝我們的贊助商 ANSYS， Cadence，英特爾公司， IO Methodology 和 Synopsys 使這次峰會可能。我們感謝他們對 IBIS 支持。

一如以往，我們祝你成功，並希望你能發現演講和討論對您有益。

此致
馬夢寬
IBIS 委員會主席

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

8:15 SIGN IN
- Vendor Tables Open at 8:30

9:00 **Welcome**
- Michael Mirmak
  (Chair IBIS Open Forum, Intel Corporation, USA)

9:10 **Activities and Direction of IBIS 5**
Michael Mirmak (Intel Corporation, USA)

9:35 **Handling of Overclocking Caused by Delay in Waveform Tables 12**
Radek Biernacki*, Ming Yan*, Randy Wolff**
Justin Butterfield**
(*Keysight Technologies, **Micron Technology, USA)

10:05 **Differential Buffer Using IBIS Models for PDN Simulations 20**
Lance Wang (IO Methodology, USA)

10:35 BREAK (Refreshments and Vendor Tables)

10:55 **True Differential IBIS Model for SerDes Analog Buffer 29**
Shivani Sharma, Tushar Malik, Taranjit Kukal
(Cadence Design Systems, India)

11:30 **IBIS AMI Validation 42**
Zilwan Mahmod, Anders Ekholm (Ericsson, Sweden)

12:00 FREE BUFFET LUNCH (Hosted by Sponsors)
- Vendor Tables

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

Activities and Direction of IBIS

Michael Mirmak
Intel Corp.
Chair, IBIS Open Forum

Asian IBIS Summit
Taipei, Taiwan
Nov. 17, 2014

http://www.eda.org/ibis/

Agenda

- IBIS Today
  - Documents and Support Services
- Upcoming Changes in IBIS
  - Major Approved BIRDs
- Work for the Future

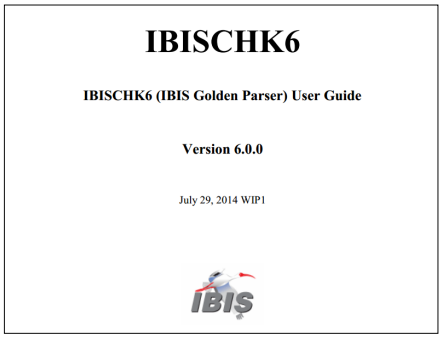
IBIS TODAY

IBIS Today

- IBIS 6.0 was approved Sept. 2013
  - http://www.eda.org/ibis/ver6.0/
  - Expands IBIS-AMI jitter support
  - Adds IBIS-AMI repeater support
- IBISCHK6 parser released June 2014
  - Available free: http://www.eda.org/ibis/ibischk6
  - Source code available for licensed purchase
  - Current “bugs” listed at http://www.eda.org/ibis/bugs/ibischk/

New Support Features

- IBISCHK6 Parser User's Guide
  - From the IBIS Quality Task Group
  - http://www.eda.org/ibis/ibischk6/ibischk_6.0.0_UserGuide_wip1.pdf
  - Lists usage, plus every Note, Caution, Error and Warning message
  - Explains the extent of the parser's checks


IBISCHK6

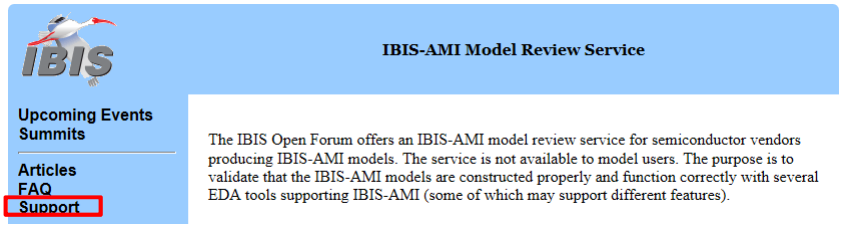
IBISCHK6 (IBIS Golden Parser) User Guide

Version 6.0.0

July 29, 2014 WIP1

Model Review Service

- The IBIS Open Forum has supported review of IBIS models for many years
  - Independent review by volunteer EDA experts, with separate reports provided individually to the submitter
- Recently expanded to cover IBIS-AMI
- Visit http://www.eda.org/ibis/support/ for details


IBIS-AMI Model Review Service

Upcoming Events
Summits

Articles
FAQ
Support

The IBIS Open Forum offers an IBIS-AMI model review service for semiconductor vendors producing IBIS-AMI models. The service is not available to model users. The purpose is to validate that the IBIS-AMI models are constructed properly and function correctly with several EDA tools supporting IBIS-AMI (some of which may support different features).

UPCOMING CHANGES

Changes After IBIS 6.0

- BIRD: Buffer Issue Resolution Document
  - A change to the IBIS specification that is not yet part of an IBIS version
- Up to today, three approved BIRDs make major changes
- Five other approved BIRDs make clarifications or corrections
- See http://www.eda.org/ibis/birds/

Major Approved BIRDs

- BIRD155.2: AMI Dependent Parameters
  - Allows AMI parameters to depend on the state of other parameters
- BIRD168.1: …Overclocking Caused by Delay in Waveform Tables
  - Unifies amount of delay that can be removed from V-t and I-t tables
- BIRD173: Package RLC Matrix Diagonals
  - Increases package model data checking

WORK FOR THE FUTURE

BIRDs Under Development

- 11 BIRDs have been proposed but not approved
- Major areas covered include
  - Backchannel Adaptation for Equalization
  - Expanded Package Capabilities
  - Touchstone for AMI Analog Buffer Models
  - Parameter Passing for External Circuits
- The Advanced Technology Task Group and the Interconnect Task Group are discussing these

Visit http://www.eda.org/ibis/subcommittee/
to review BIRD development progress and contribute

Organizational Changes

- A major revision of the IBIS Open Forum basic policies and procedures is underway
- Changes to the IBIS Open Forum “Charter” will allow for greater involvement in votes and officer elections by Membership Companies worldwide

The IBIS Open Forum would like to encourage more international participation and involvement, including those elected to IBIS Board offices

Request for Feedback

- How can IBIS standards be more useful?
  - What features would help you most?
- How can the IBIS Open Forum keep you better informed?
  - More frequent web updates?
  - More frequent e-mail information?
  - Increased use of social media?
  - More Summits?

Your feedback is critical to the development and improvement of IBIS standards!

Q/A

KEYSIGHT TECHNOLOGIES

Unlocking Measurement Insights for 75 Years

Micron

Handling of Overclocking Caused by Delay in Waveform Tables

Radek Biernacki and Ming Yan, Keysight Technologies

Randy Wolff and Justin Butterfield, Micron Technology

IBIS Summit

Taipei, Taiwan, November 17, 2014

(presented by Lance Wang, IO Methodology)

Originally presented at
IBIS Summit, Shanghai, PRC
November 14, 2014

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KEYSIGHT TECHNOLOGIES

Micron

What is Overclocking

- A trigger event happens during transition from the low/high state to the high/low state
- The trigger event initiates transition in the opposite direction
- Interrupted transitions are **NOT** the intended operation
- The IBIS specification does not provide any means to determine buffer behavior upon interrupted transitions

KEYSIGHT TECHNOLOGIES

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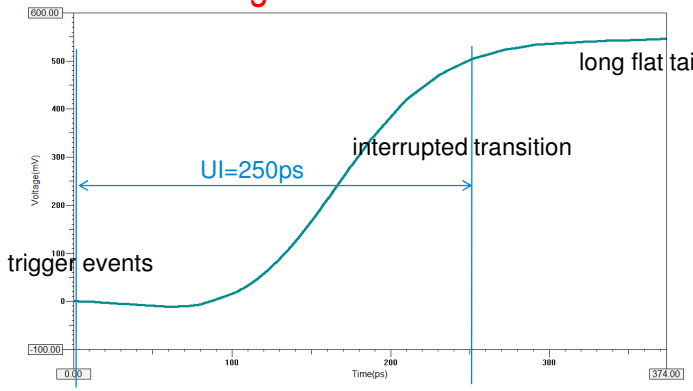
True Overclocking



- Not discussed here – we are not trying to impose any restrictions or interpretation of true overclocking

KEYSIGHT TECHNOLOGIES

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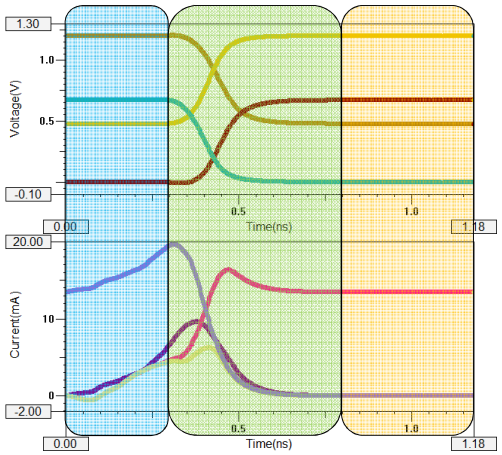
Power Aware IBIS Models

- Two types of waveform tables are used: the classic voltage tables and the (composite) current tables
- The driver voltage transition may be significantly delayed with respect to the pre-driver current
- The two waveform tables need to be recorded in the IBIS file using the same absolute time scale and be time aligned
- The driver voltage transition may be valid for faster bit rates than those corresponding to the overall time span of the combined waveform tables

KEYSIGHT TECHNOLOGIES

Micron

Typical Combined Waveform Data



Pre-driver current 300ps

Driver switching 500ps

Dead time 370ps

KEYSIGHT TECHNOLOGIES

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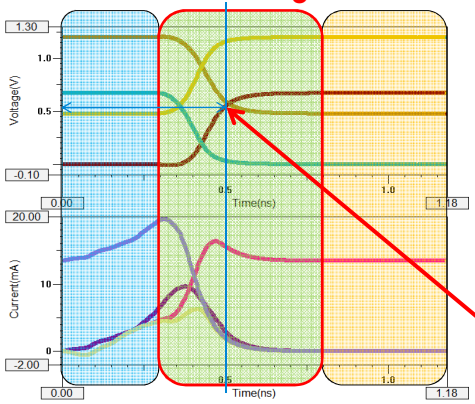
Fictitious Overclocking in Power Aware Models



Pre-driver current 300ps

Driver switching 500ps

Dead time 370ps

- For these waveforms:
  - The Driver switching occurs within a 500ps window.
  - Thus, a bit time of 500ps or greater should not cause true overclocking problems.
  - Fictitious overclocking if delay is not properly handled.

KEYSIGHT TECHNOLOGIES

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What EDA Platforms Do About It

- Several ways to address it
  - The user can specify the amount of initial delay to ignore
  - Automatically detect the amount of initial delay to ignore
  - Do nothing (no special “windowing” applied)
- Neither of the approaches is correct nor desired
  - Potentially inconsistent simulation results, or
  - Declared “overclocked” operation

KEYSIGHT TECHNOLOGIES

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Who the Decision Belongs To

ONLY THE MODEL MAKER
KNOWS THE EXACT
AMOUNT OF DELAY TO REMOVE

KEYSIGHT TECHNOLOGIES

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IBIS BIRD 168.1 – "Handling of Overclocking Caused by Delay in Waveform Data"

- Approved for the next version of the IBIS spec (after 6.0)
- Proposes a new keyword under the [Model] keyword

  [Initial_Delay]
- The new keyword is optional
- One or two sub-parameters can be specified

  V-T and/or I-T

http://www.eda-stds.org/ibis/birds/bird168.1.docx

KEYSIGHT TECHNOLOGIES

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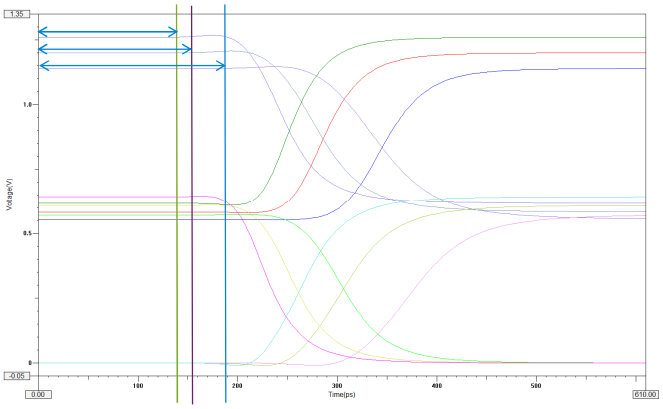
Example of V-T Sub-parameter Data



Max corner initial delay = 140ps

Typ corner initial delay = 155ps

Min corner initial delay = 190ps

- The same value of the initial delay specified for V-T sub-parameter applies to all voltage tables in the [Model]

KEYSIGHT TECHNOLOGIES

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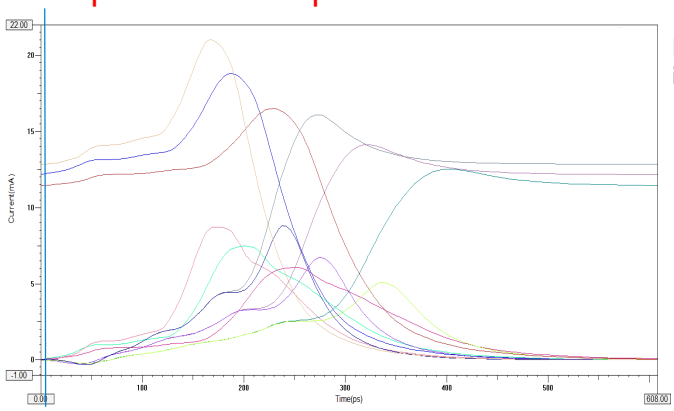
Example of I-T Sub-parameter Data



Min/Typ/Max corner
initial delay = 5ps

- The same value specified for I-T sub-parameter applies to all current tables in the [Model]

KEYSIGHT TECHNOLOGIES

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How the Initial_Delay Values are Applied

- The initial delay value is first removed (subtracted) from the time values in the first column of the corresponding tables
- The same value is used to delay the trigger events which activate any of the corresponding tables
- This shortens the transition times accordingly, allowing higher bit rate signals to be properly simulated
- Following the specified initial delay values will make the simulation results consistent across all EDA platforms

KEYSIGHT TECHNOLOGIES

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Example of Specifying Initial Delay in an IBIS File

```
[Model]

   [Initial Delay] | This keyword specifies removable delay(s)
   | time table       typ            min            max
     V-T              0.20e-9        0.22e-9        0.18e-9
     I-T              0.05e-9        NA             NA
```

- Up to three columns with three IBIS corner values

KEYSIGHT TECHNOLOGIES

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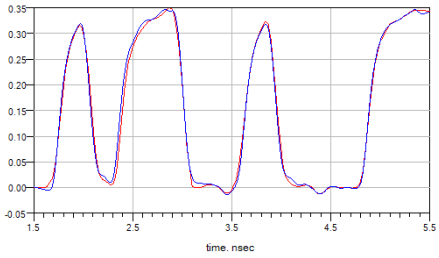
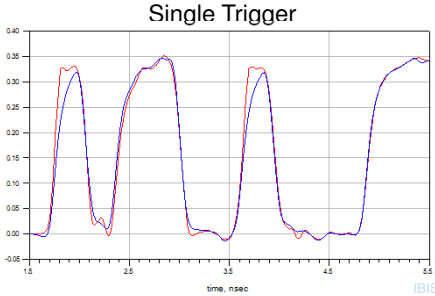
Example: LPDDR4 3200Mbps

- UI = 312.5ps
- Duration of the waveform tables = 920ps

Multiple Triggers



Single Trigger



IBIS
Spice

KEYSIGHT TECHNOLOGIES

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Summary

- A new keyword will be added to the next version of the IBIS spec
- It will unify the way the initial delay is handled, making the simulation results consistent across different EDA tools
- It adds complexity to the triggering algorithms inside of the EDA simulator tools for the benefit of the IBIS model users

Differential buffer using IBIS models for PDN simulations

Lance Wang
Asian IBIS Summit – Taipei
Nov. 17th, 2014

Outline

This is a case study for differential pair buffers in Power Delivery Network (PDN) simulations

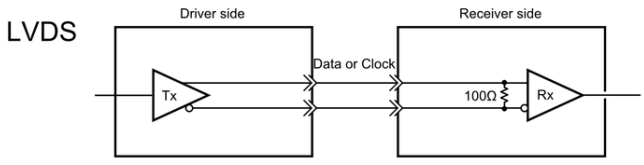
- Motivation
- Review IBIS PDN feature for single-end buffer
- Power currents using non-PDN IBIS model and IBIS with PDN feature for differential pair buffer in simulation
- Average-Out approach for differential buffer PDN simulation
- Summary

Motivation

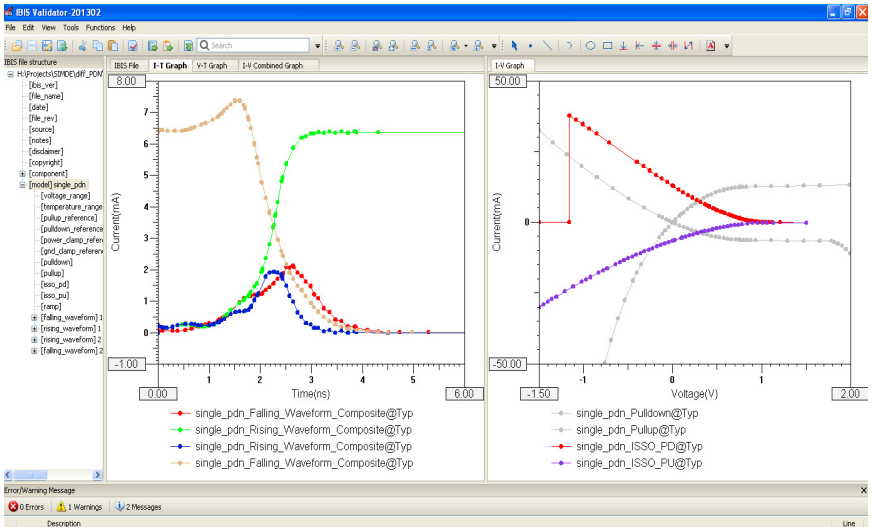
- Many times we need to do a PDN simulation with differential pair buffers in the network using IBIS models
- IBIS Spec doesn't include how to make IBIS PDN model for differential pair buffers
- Seeking a reasonable solution for differential buffer PDN simulation using existing IBIS modeling specification

The test case

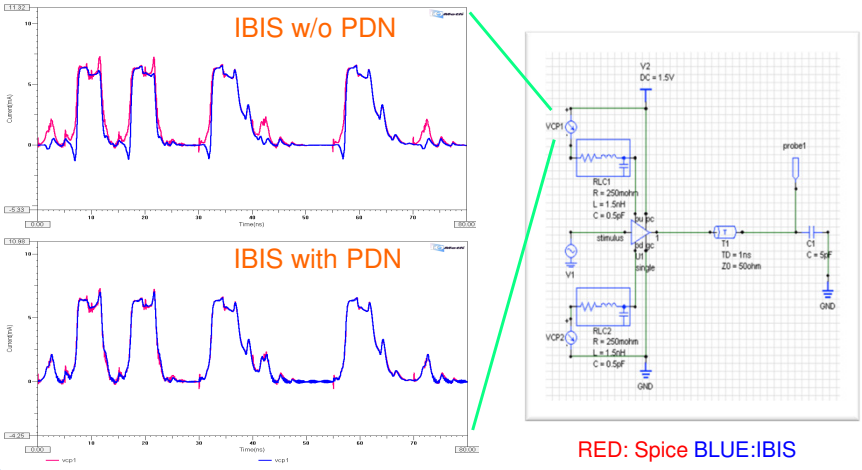
- LVDS 1.5v true-differential buffer
- We have access to each pin/buffer power supply
- Positive and negative pin buffer are identical
- Push-up and Pull-down are almost even
- We are checking on Driver side only



Review of IBIS PDN Feature

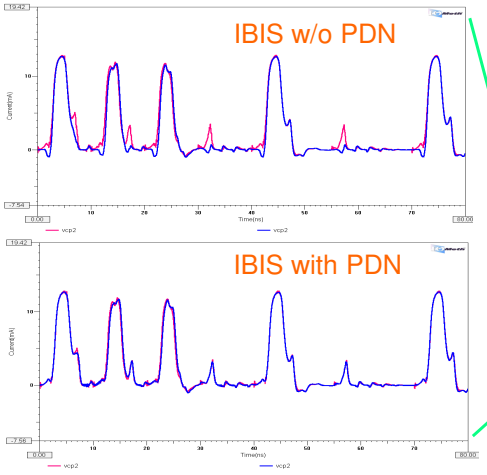


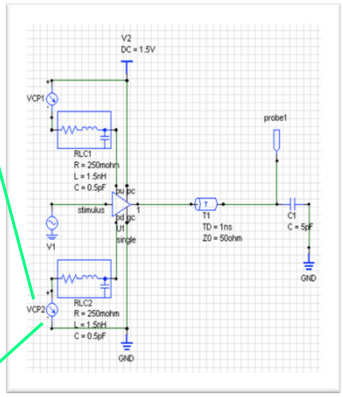
Test circuit and results (Power)



RED: Spice BLUE:IBIS

Test circuit and results (Ground)



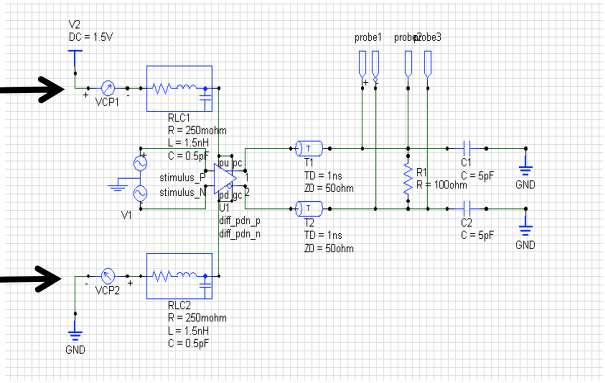


RED: Spice BLUE:IBIS

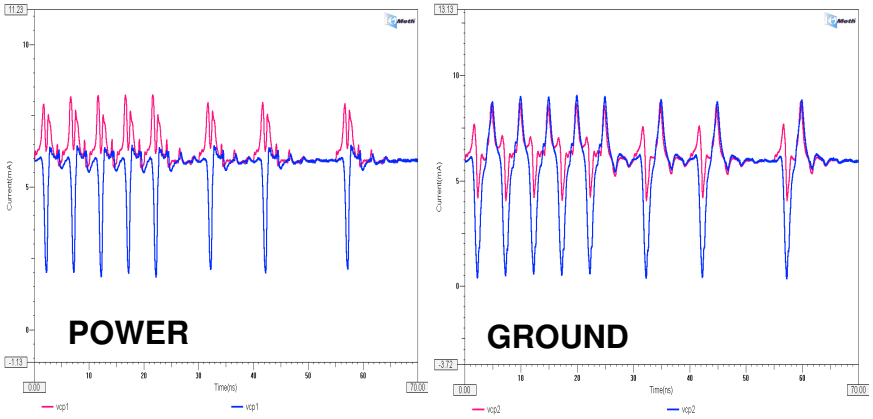
Differential pair buffer test circuit

POWER →

GROUND →

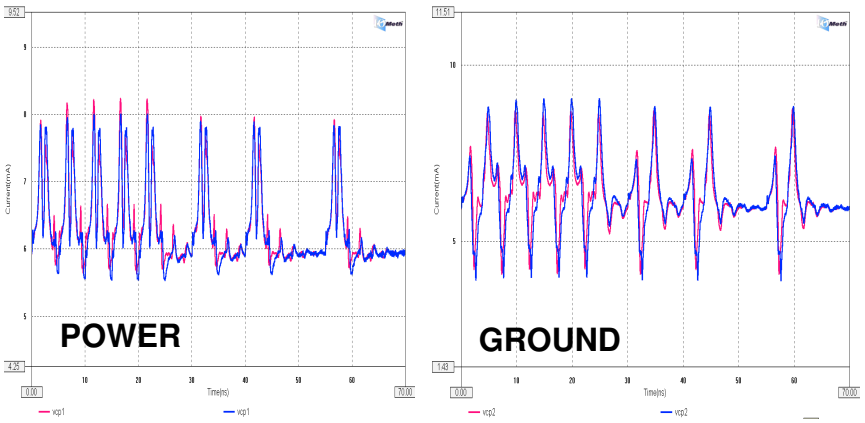


Differential pair buffer result (IBIS without PDN feature)



RED: Spice BLUE:IBIS

Differential pair buffer result (IBIS with PDN feature) – Extracted from single pins



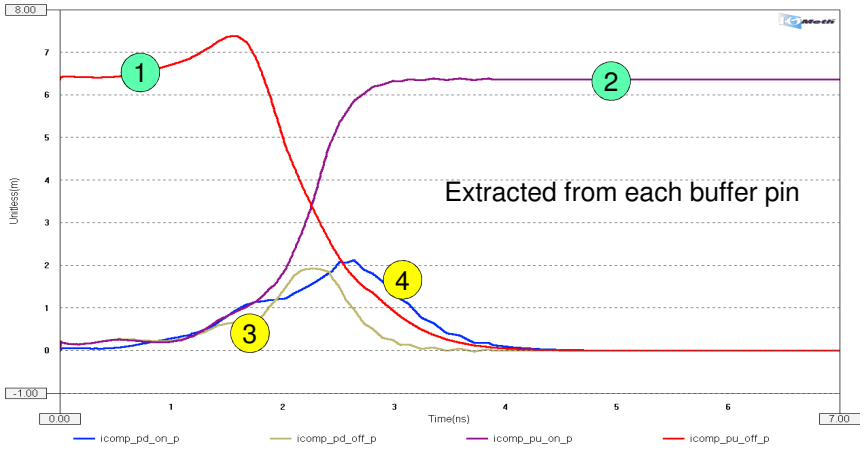
RED: Spice BLUE:IBIS

Differential pair PDN simulation analysis

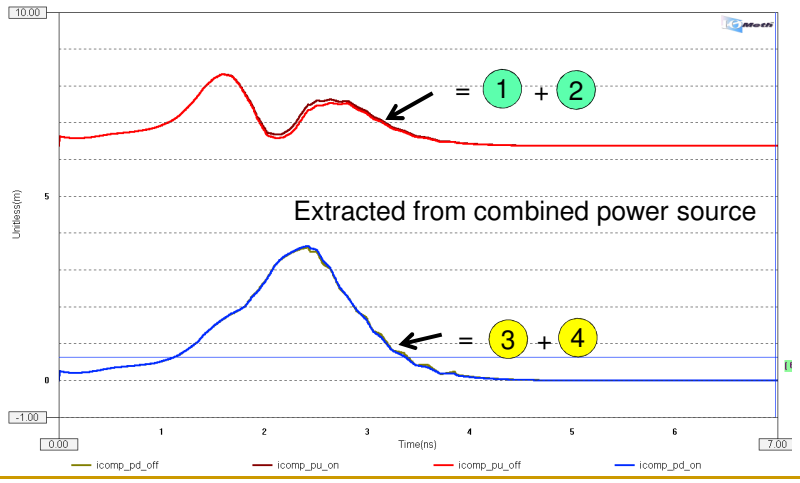
- Result using IBIS model without PDN features is not acceptable
- Result using IBIS model with PDN features is GOOD!
  - This result is using the IBIS model extracted from separate power source for each P/N pins

What if we don't have the access to each buffers power pins?

Look into the [Composite Current] curve



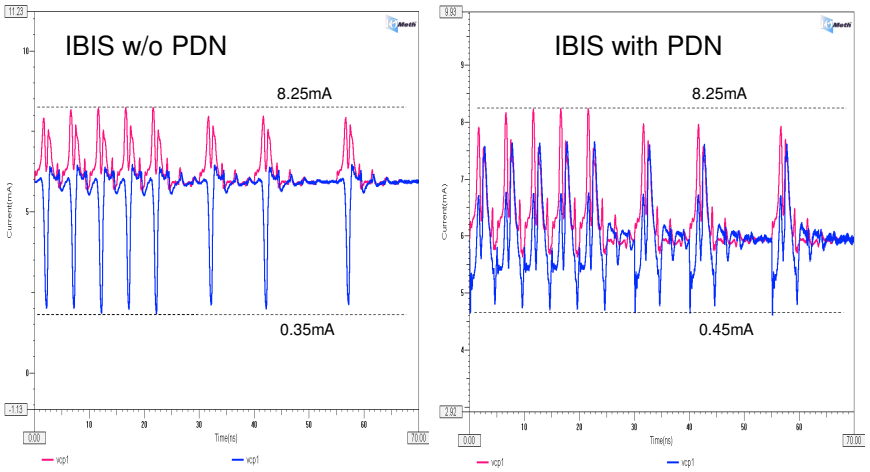
Look into the [Composite Current] curve



ISSO* and Composite Current curves for combined power source

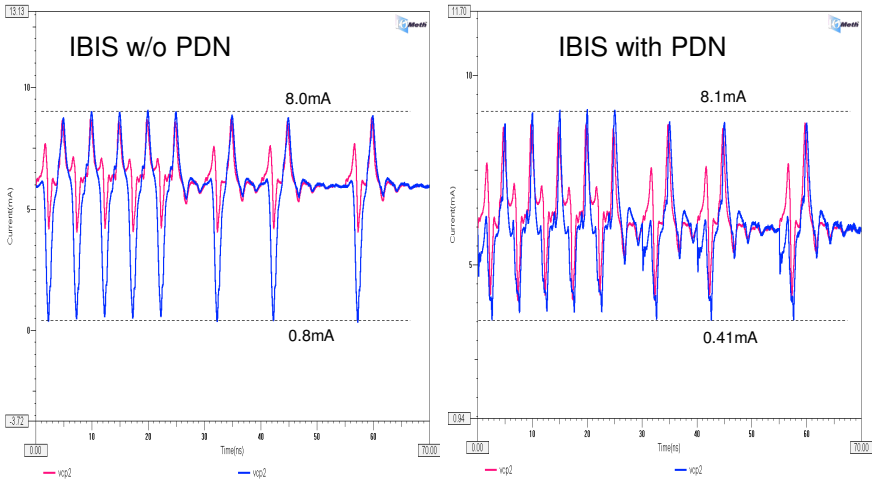
- We can get combined ISSO* by setting up both Pullup or Pulldown then take the average for each buffer
- Due to actual P/N pins take one pullup and one pulldown at the same time for differential pair, Composite Current we get is (1)+(2) and (3)+(4)
  - We can also do an average-out to see if it would close to the Spice simulation results

Result for combined POWER pin



RED: Spice BLUE:IBIS

Result for combined GROUND pin

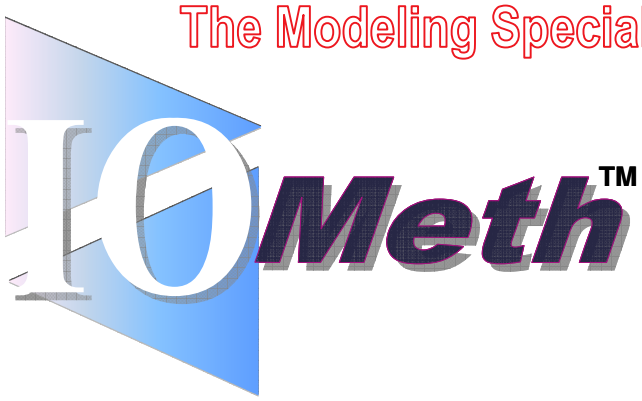


RED: Spice BLUE:IBIS

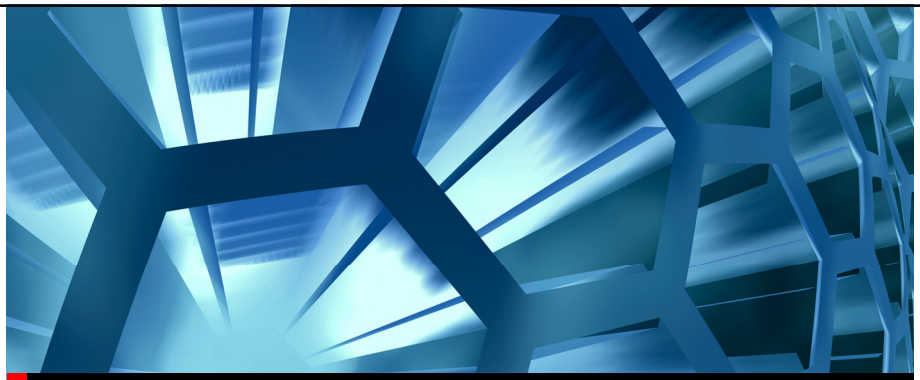
Summary

- IBIS PDN feature helps to have more accurate result for single-end buffer PDN simulation
- IBIS model without PDN features is not acceptable for differential pair PDN simulations
- If we can access to each P/N pin power source separately, the IBIS model with PDN feature can be used in differential pair PDN simulations accurately
- If we only can access to combined power source pins, the average-out method could be workaround to use in IBIS differential pair PDN simulations

The Modeling Specialist



http://www.iometh.com



True Differential IBIS model for SerDes Analog Buffer

Shivani Sharma, Tushar Malik, Taranjit Kukal

IBIS Asia Summit
Taipei, Taiwan
Nov. 17, 2014

cadence

Agenda

- Overview of Differential IBIS
- Description of test-case
- Flow used to create differential IBIS model
- Comparison: Pseudo-differential vs. True-Differential IBIS Serial-Link
- Conclusion

cadence

Agenda

- Overview of Differential IBIS
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  cadence

Overview of Differential IBIS - Current approaches

- Traditionally, differential buffer have been modeled as
  - Pseudo Differential buffer using two Single-ended IBIS models
    - Accuracy can suffer if there is substantial differential current which is the case with Serial Link analog buffers that has series elements between PADP and PADN
  - External Model approach: Call to buffer netlist
    - Netlist (IP) needs to be revealed
  - External Model approach: Call to S-parameter model
    - Rx buffer needs to be characterized as S-parameters

  cadence

Overview of Differential IBIS - Alternate approach

- While S-parameter approach is best suited for analog buffers in serial links, we provide an alternate way to model it through standard IBIS tabular format with use of series elements to model differential current.
- This extends the approach suggested in IBIS cookbook that suggests modeling of differential current using series Resistance.
  - Here we propose use of reactive elements (R/L/C) to model differential current.

cadence

Agenda

- Overview of Differential IBIS
- Description of test-case
- Flow used to create differential IBIS model
- Comparison: Pseudo-differential vs. True-Differential IBIS Serial-Link
- Conclusion

cadence

Description of test-case
- IBIS modeling of Serial Link RX IO

- 10Gbps Serial link
- 28nm technology node
- Typical process node
- Rx analog buffer had additional blocks for equalization that were modeled as AMI code
  - Frontend attenuation
  - VGA
  - CTLE
  - DFE
  - CDR

cadence

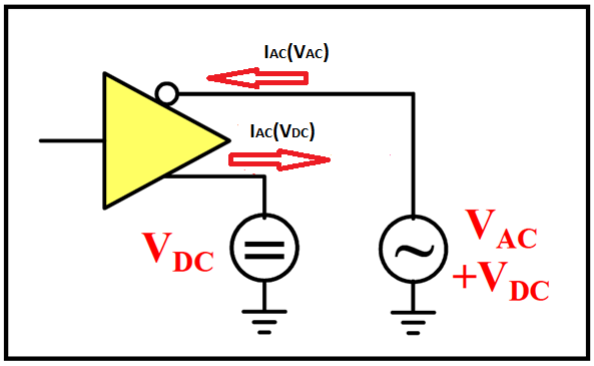
Agenda

- Overview of Differential IBIS
- Description of test-case
- Flow used to create differential IBIS model
- Comparison: Pseudo-differential vs. True-Differential IBIS Serial-Link
- Conclusion

cadence

Flow used to create differential IBIS model - True differential

- Setup for common mode and differential mode impedance extraction



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Flow used to create differential IBIS model - True differential

$$I\_Diff = I_{AC}(V_{DC})$$
$$I\_Comm = I_{AC}(V_{AC}) - I_{AC}(V_{DC})$$

-I_Diff flows through series element between inverting and non-inverting pins

-I_Comm flows only through common mode impedance

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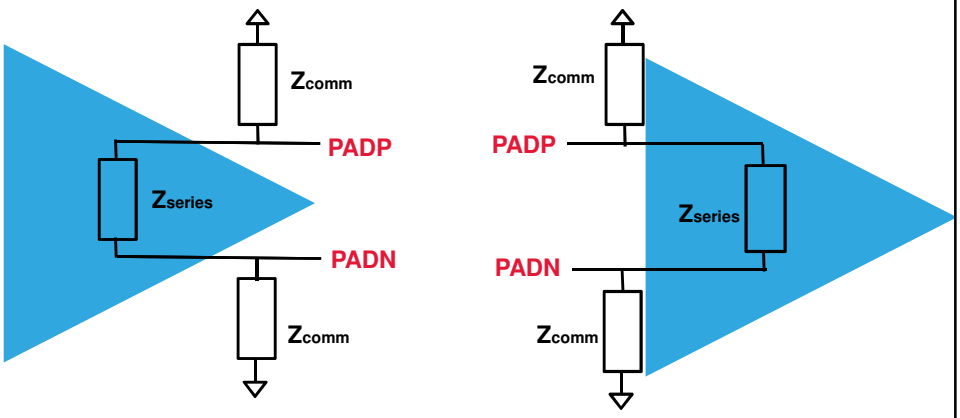
Flow used to create differential IBIS model

- True differential buffer with series element Z_{series}



Output Buffer

Input Buffer

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Flow used to create differential IBIS model

- Differential and common mode impedance calculations

- Series Reactance = $X_{series} = \frac{V_{AC}}{\mathrm{Im}(I\_Diff)}$
- Series Resistance= $R_{series} = \frac{V_{AC}}{\mathrm{Re}(I\_Diff)}$
- Common mode Resistance= $R_a = \frac{V_{AC}}{\mathrm{Re}(I\_Comm)}$
- Common mode Reactance= $X_a = \frac{V_{AC}}{\mathrm{Im}(I\_Comm)}$

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Flow used to create differential IBIS model

- Differential and common mode impedance calculations

- Depending on sign, reactance could be inductive or capacitive
- Impedance to be calculated at most likely operating frequency of buffer
- For 10G serial link Rx buffer testcase

Series Model	R=220ohms	L=9.8nH
Common mode Model	R=80ohms	C=0.223pF

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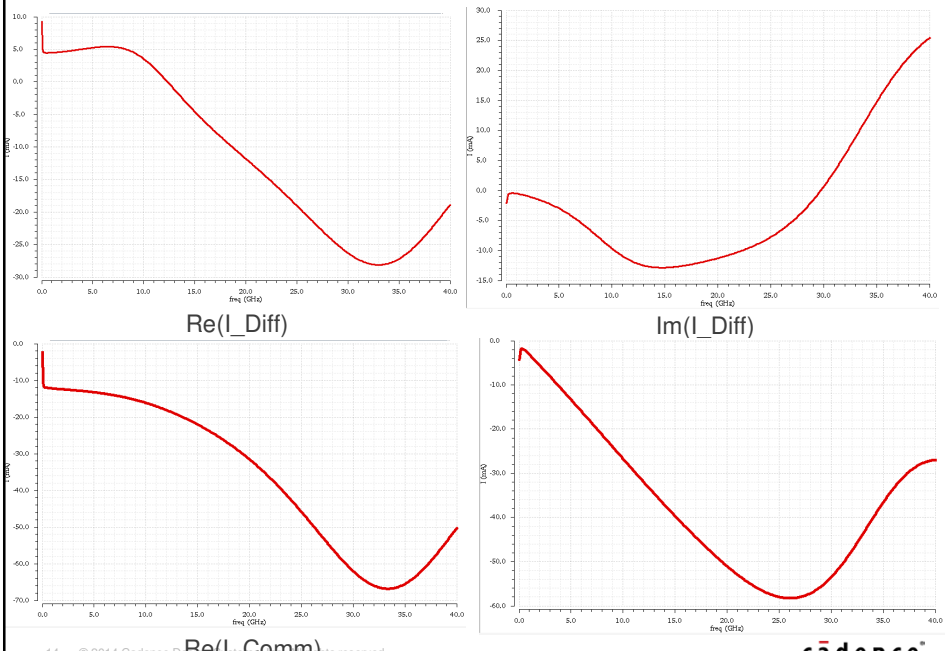
Common mode and differential currents



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Flow used to create differential IBIS model
- IBIS model

- Parallel RL network present as Zseries, modeled using “Model_type Series”

```
|*****************************************************************
***********
[Series Pin Mapping]   pin_2   model_name  function_table_group
4                       5        Rpath
4                       5        Lpath

|*****************************************************************

                **********
                [Model] Rpath
                Model_type Series
                Polarity Non-Inverting
                Enable Active-High
                |
                |              typ   min   max
                 C_comp        0.0pF 0.0pF 0.0pF
                |
                |              typ    min   max
                [Voltage Range] 1.0    NA    NA
                |***************************************************************
                |          R(typ)   R(min)  R(max)
                [R Series]  220       NA    NA

                |
                |*************************************************************
                **********
                [Model] Lpath
                Model_type Series
                Polarity Non-Inverting
                Enable Active-High
                |
                |              typ   min   max
                 C_comp        0.0pF 0.0pF 0.0pF
                |
                |              typ    min   max
                [Voltage Range] 1.0    NA    NA
                |

                |*************************************************************
                ***********

                |          R(typ)   R(min)  R(max)
                [L Series]  9.8nH       NA    NA
                |
```


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Flow used to create differential IBIS model
- IBIS model

- Parallel RC network present as Zcomm, modeled using clamp I-V table and C_comp

```
[Model]     Rx_in
Model_type  Input
Vinl=1.5
Vinh=2.5
|
| variable                      typ         min         max
C_comp                          0.223pF     NA          NA
[Temperature Range]              70         NA          NA
[Voltage range]                 3.3         NA          NA
|
|*****************************************************************
**************
[POWER Clamp]
|
|  Voltage              I(typ)       I(min)       I(max)
|
  -3.3000e+00          20.6250e-03    NA          NA
   0.0000e-00          00.0000e-00    NA          NA
   3.3000e-00         -20.6250e-03    NA          NA

|*****************************************************************
**************
[GND Clamp]

|  Voltage              I(typ)       I(min)       I(max)

 -3.3000e+00         -20.6250e-03    NA           NA
  0.0000e-00          00.0000e-00    NA           NA
  3.3000e-00          20.6250e-03    NA           NA
|
|*****************************************************************
**************
```


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Agenda

- Overview of True Differential IBIS
- Description of test-case
- Flow used to create differential IBIS model
- Comparison: Pseudo-differential vs. True-Differential IBIS Serial-Link
- Conclusion

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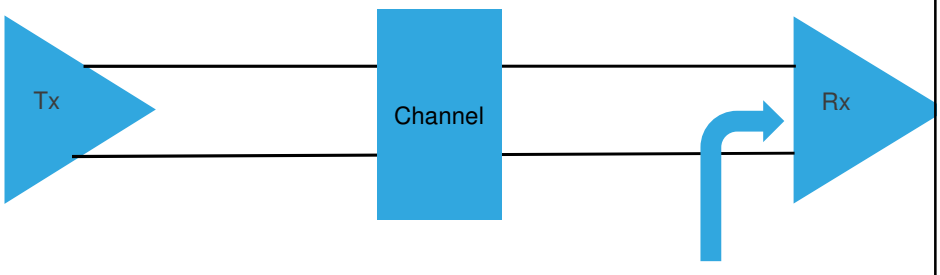
Comparison: Pseudo-differential vs. True-Differential IBIS simulations

- Serial Link Simulation Test-bench
  - 10Gbps
  - No Equalization
  - PRBS23
  - Tested on different channels



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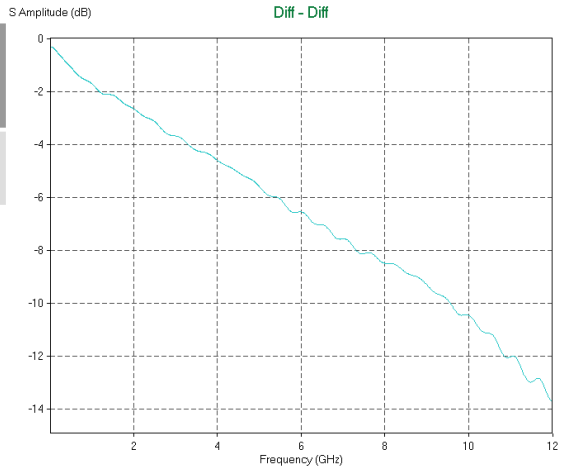
Channel 1

Frequency	Insertion Loss
5.15GHz	-5.861dB



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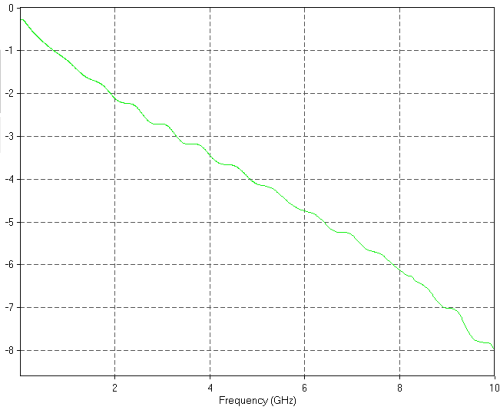
Channel 2

Frequency	Insertion Loss
5.1GHz	-4.14dB



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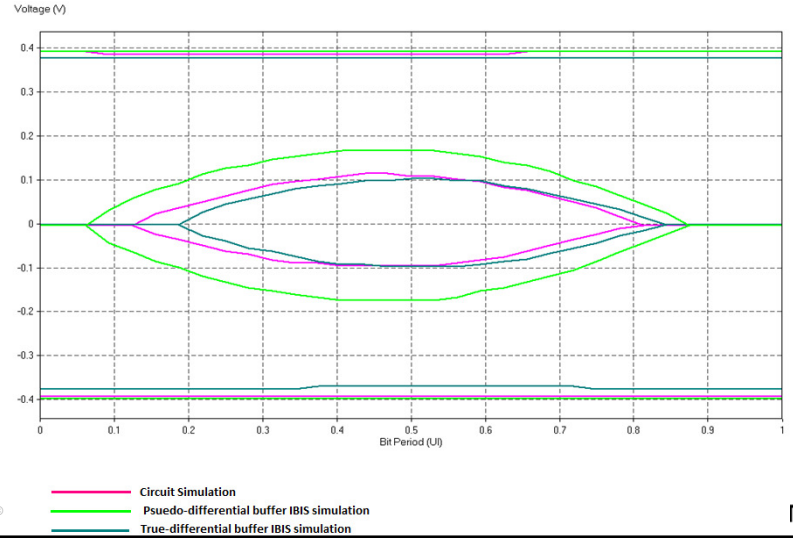
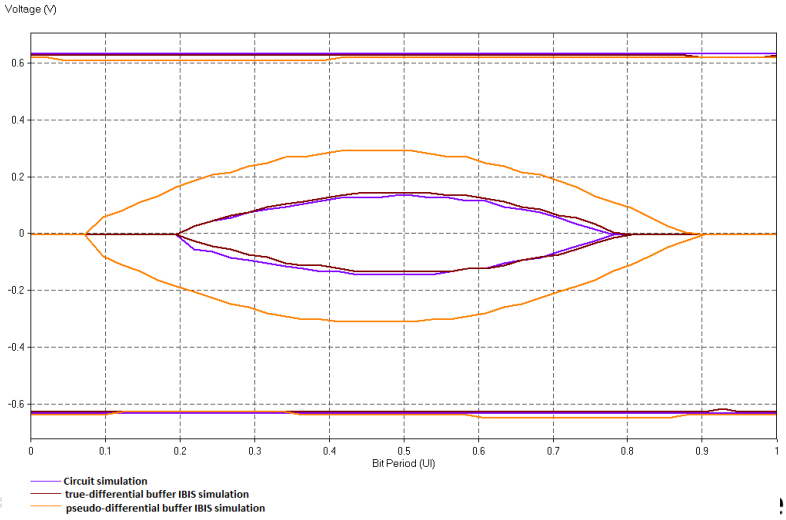
Comparison: Pseudo-differential IBIS vs. True-Differential IBIS vs. Circuit simulations

- Channel 1



Comparison: Pseudo-differential IBIS vs. True-Differential IBIS vs. Circuit simulations

- Channel 2



Agenda

- Overview of Differential IBIS
- Description of test-case
- Flow used to create differential IBIS model
- Comparison: Pseudo-differential vs. True-Differential IBIS Serial-Link
- Conclusion

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Conclusion

- Extended “Series Model Approach” in Cookbook for IBIS Version 4.0 to model differential and common-mode impedances for SERDES analog buffer.
- True differential model provides much better accuracy than pseudo differential IBIS for channel simulations in terms of
  - Jitter and eye opening
  - Reflection losses

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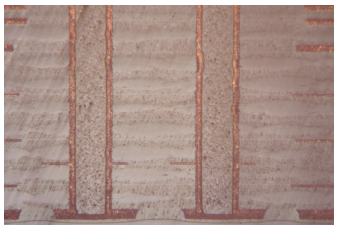
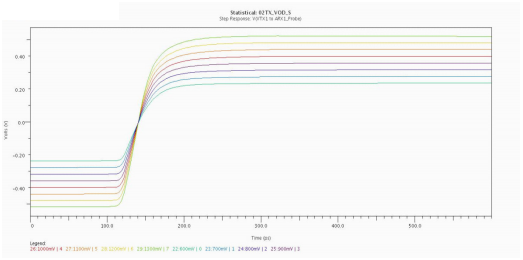
IBIS AMI VALIDATION

ASIAN IBIS SUMMIT
TAIPEI, TAIWAN, NOVEMBER 17, 2014





Taipei, Taiwan, November 17, 2014
Zilwan Mahmod, Anders Ekholm

AGENDA

- Design goals
- IBIS AMI Validation
  - IBIS AMI Certification
  - PCB Passive correlation
  - TX Active correlation
  - RX Active correlation
- Experiences

DESIGN GOALS

- What design goal do we have with IBIS AMI analysis?
  - To verify a robust design over manufacturing variations.
  - To verify a given design criteria like BER, Eye mask.
  - To optimize the design eye to the given criteria.
  - To verify the design with a high fault coverage.
  - To verify the design in a short predictable timeframe.
  - To minimize design iterations.

IBIS AMI VALIDATION

To achieve the design goals we need correct and accurate models with high performance.

- How do we validate IBIS AMI models?
  - IBIS Checker
  - Certification
  - Active correlation
    - TX correlation
    - RX correlation

IBIS AMI CERTIFICATION

Certification is the first step an IBIS AMI model needs to go through, this is to check that the model behavior is reasonable.

- Certification needs to check the following:
  - Is the model delivery complete, all files included.
  - Does this model describe enough variation, process corners.
  - Does this model describe all possible configuration parameters.
  - And only the possible configuration parameters.
  - Is it compliant with IBIS AMI standard (IBIS 6.0 specification)
  - Is it compliant with Ericsson requirements outside of IBIS AMI standard?
  - Is the model describing the buffer's electrical behavior accurately.

IBIS AMI CERTIFICATION

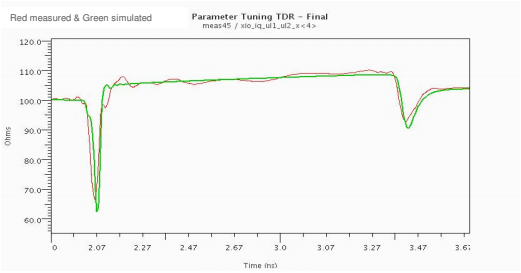
- Certification needs to check the following cont.:
  - Are the necessary jitter parameters included (for both TX and RX)?
  - Is documentation complete enough to use the model?
  - Is the model performance fast enough?
  - Are the configuration parameters the same as the real IC uses?
  - If not are there information on how to translate parameters from the model to the physical IC settings?
  - Are the settings reasonable and in correct order?
  - Is it compatible with the used simulation environment?
  - If model is interoperable with other vendors models?
- Output is a certification report

PCB PASSIVE VALIDATION

To be able to do active correlation we need to make sure our simulation environment are predicting our passive interconnect accurately enough.

›We achieve this by doing passive correlation, or simulator calibration (similar to measurement instrument calibration).

- Produce a PCB using the material and stackup selected for the design.
- Use TDR or VNA measurements to get a representation of the used trace structures in you design.

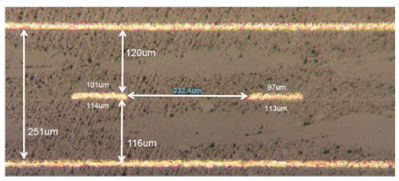


›Adjust PCB Physical Parameters

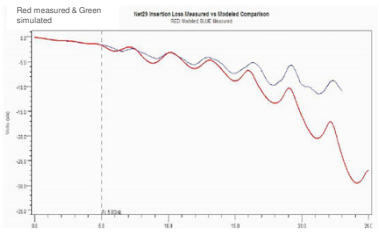
- propagation delay error – adjust ε_r
- impedance error - adjust cross-section
- attenuation error - adjust tan δ, roughness

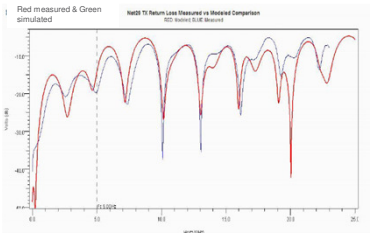
PCB PASSIVE VALIDATION

- Perform cross section cuts of all relevant structures in the PCB to get physical properties of geometries in the used simulation tool.



- Create the same data set in your simulation environment.
- Adjust/tweak the simulation model parameters to achieve an accurate enough result. So the passive model will predict your system performance.



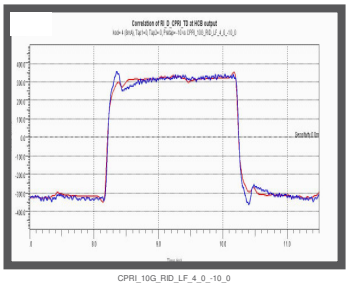


TX ACTIVE VALIDATION
MEASUREMENT ENVIRONMENT

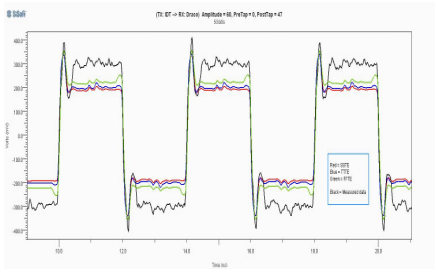
- Select suitable trace loads for correlation.
- Run a set of cases of IC configuration settings.
  - Run a slow clock from TX and measure waveforms.
  - Run a PRBS (eg. PRBS7) and measure waveforms.
  - Transfer waveform data to simulation environment.
- “deembed” measurement or “embed” simulation.
- Make sure to use the same measurement point.

TX ACTIVE VALIDATION
SIMULATION ENVIRONMENT

- Simulate the same traces with the same probe point
- Simulate for the same stimuli cases
- Make an overlay correlation of the waveforms



CPRI_10G_RID_LF_4_0_-10_0



RX ACTIVE VALIDATION

RX correlation methods is still being determined.

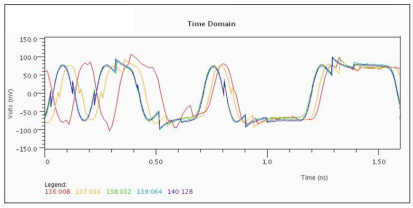
- –How can we correlate at Decision Point?
- –Standard waveform overlay correlation will not be possible.
- –Maybe a Feature Selective Validation (FSV) is possible?
- –Which Features should be Selected for correlation?

IC internal meas. features are not standardized. ☹

- –Makes the FSV correlation harder.
- –Can IBIS Open Forum standardize this ? ☺

EXPERIENCES

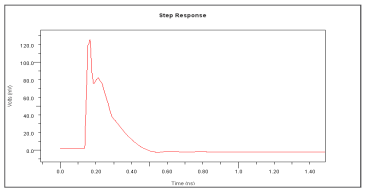
- ›Many models fails during certification
  - –A.AMI controls incomplete
    - ›H/W has more settings than AMI model.
    - ›AMI model has more settings than H/W.
    - ›AMI file has fixed values for all settings.
    - ›Misses dependency tables.
  - –Algorithmic models don't run
    - ›Compiled for wrong O/S.
    - ›External runtime libraries required.
  - –Model controls don't work
    - ›Changing settings has no effect.



Changing samples/bit affects results

EXPERIENCES

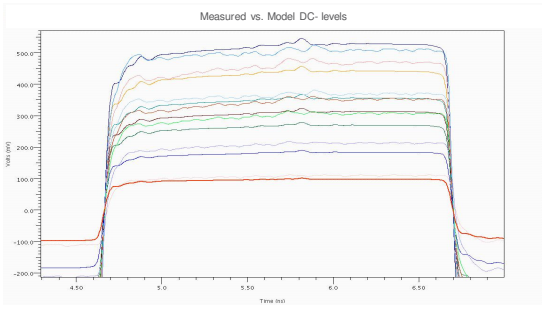
- Models don't meet spec requirements
  - Models crash with some samples/bit settings.
- Syntax (IBIS Parser) errors
- Analog Models
  - Incomplete or missing data in A.ibs file.
  - Improbable analog models.
    - Improbable voltage, impedance or behavior.
    - "Idealized" analog models.



This is supposed to be a step response

EXPERIENCES

- Some models fail during TX correlation
  - Some of the simulated DC levels don't match the measured DC levels.



EXPERIENCES

- RX correlation process is still being worked on
  - Should be considered as not trustable until proven by active correlation!

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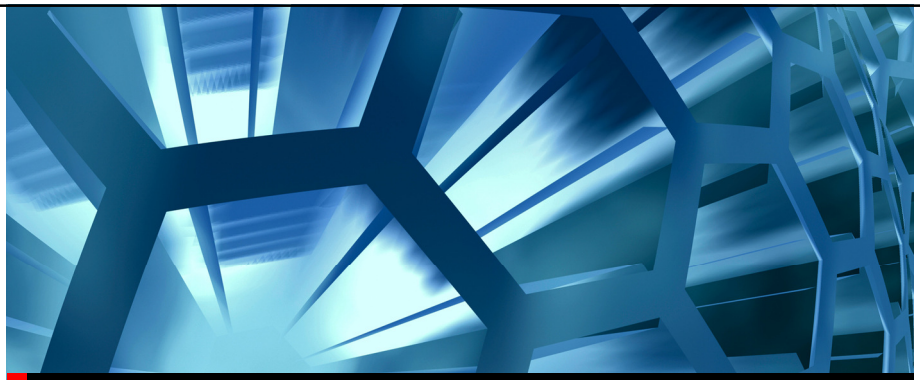

Signing IBIS model against DDR4 spec

Tushar Malik, Taranjit Kukal

IBIS Asia Summit
Taipei, Taiwan
Nov. 17, 2014

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Agenda

- Problem Statement
- Overview of DDR compliance checks
- Methodology to check DDR compliance
  - Impedance
  - Slew rate
  - Pulse-width variation
- Conclusion

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Agenda

- Problem Statement
- Overview of DDR compliance checks
- Methodology to check DDR compliance
  - Impedance
  - Slew rate
  - Pulse-width variation
- Conclusion

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Problem Statement
- Certify Controller IBIS models before system simulations

- DDR compliance needs to be done on a system interconnect starting from Controller to Memory IO
- If DDR IBIS models do not adhere to DDR JEDEC standards, designer may wrongly associate performance issues with interconnect elements like board, connector, DIMMs, package.
- It is important that we decouple the testing into
  - Testing of IBIS models to make sure they comply with JEDEC standards
  - Testing of interconnect elements with above certified IBIS models

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Problem Statement
- Do exhaustive checks on IO netlist performance

- Simulating IO-netlists for all corners to verify compliance against JEDEC specs is time-consuming.
- Since IBIS modeling is an automated process, the generated IBIS model can quickly provide results that can be verified against JEDEC requirements (for all corners and impedance settings) like
  - Impedance variation
  - Slew rates
  - Pulse-width variation
  - ZQ calibration based on process corners

5

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Agenda

- Problem Statement
- Overview of DDR compliance checks
- Methodology to check DDR compliance
  - Impedance
  - Slew rate
  - Pulse-width variation
- Conclusion

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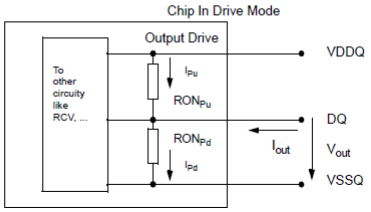
Overview of DDR compliance checks - JEDEC DDR4 spec (output impedance)

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that RON_{Pu} is off



RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	34Ω	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	34Ω	1,2
		VOHdc= 1.1* VDDQ	0.9	1	1.25	34Ω	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	34Ω	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	34Ω	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	34Ω	1,2

Spec indicates impedance measurement to be done at different Vout levels and that they should be within +/- 10%

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Overview of DDR compliance checks - Single-ended slew rate

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$V_{OL}(AC)$	$V_{OH}(AC)$	$[V_{OH}(AC)-V_{OL}(AC)]$ / Delta TRse
Single ended output slew rate for falling edge	$V_{OH}(AC)$	$V_{OL}(AC)$	$[V_{OH}(AC)-V_{OL}(AC)]$ / Delta TFse

NOTE :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

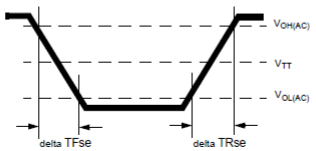

Figure 182 — Single-ended Output Slew Rate Definition

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	TBD	TBD	TBD	TBD	V/ns

Spec indicates that DQ slew rate should be within Min and Max values

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Overview of DDR compliance checks - Differential slew rate

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TRdiff
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TFdiff

NOTE :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

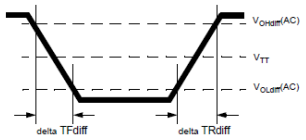

Figure 183 — Differential Output Slew Rate Definition

Table 79 — Differential output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	TBD	TBD	TBD	TBD	V/ns

Spec indicates that DQS slew rate should be within Min and Max values

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Overview of DDR compliance checks - Pulse-Width@data-rate

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	
Clock Timing								
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	8	-	ns
Average Clock Period	tCK(avg)	tbd –(Definition tbd)						ps
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)

Spec indicates that the duty cycle should be greater than .45UI

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Agenda

- Problem Statement
- Overview of DDR compliance checks
- Methodology to check DDR compliance
  - Impedance
  - Slew rate
  - Pulse-width variation
- Conclusion

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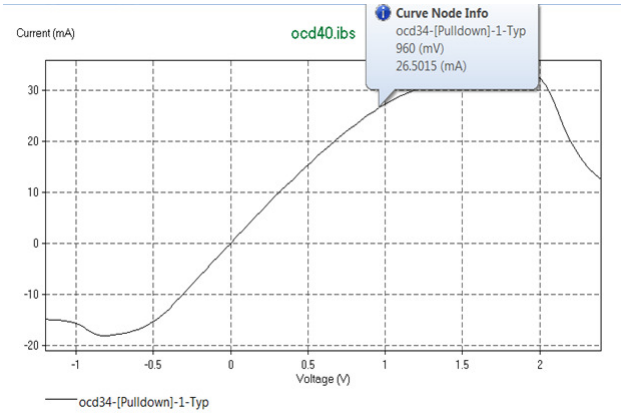
Methodology to check DDR compliance - IBIS impedance measurement (pulldown)

- IV curves of IBIS can be plotted to ensure that they fall within +/- 10% tolerance



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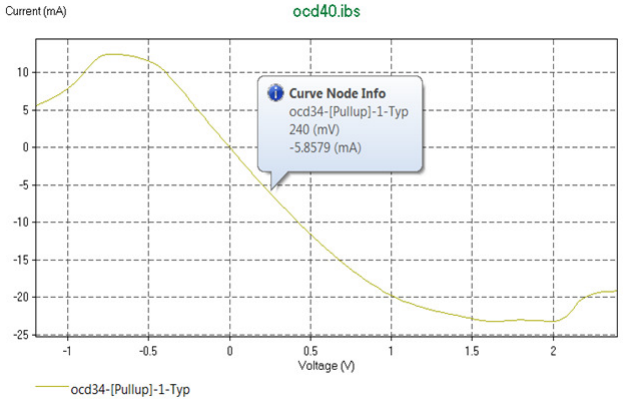
Methodology to check DDR compliance - pullup

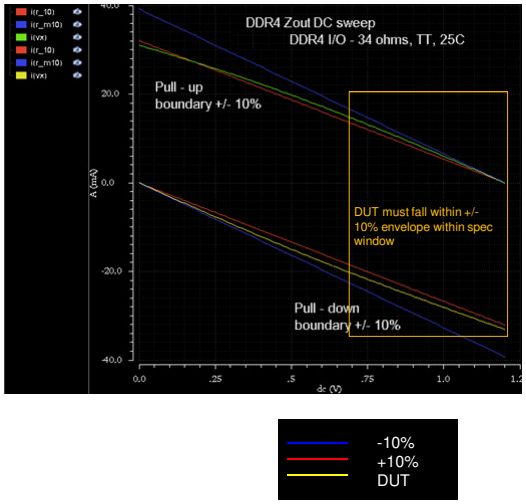
- IV curves of IBIS can be plotted to ensure that they fall within +/- 10% tolerance



cadence

Methodology to check DDR compliance - Impedance check

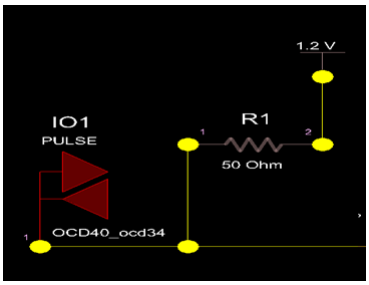
- IV plots from IBIS being compared against 10% limits



cadence

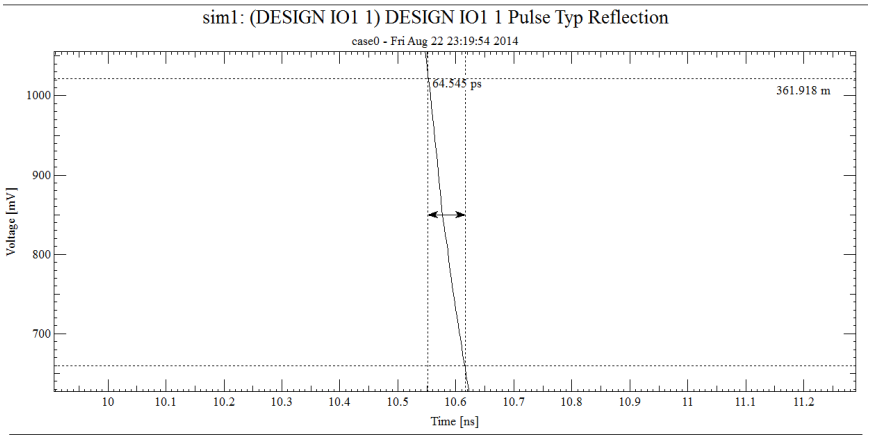
Methodology to check DDR compliance - Single ended slew rate measurement test-bench

- Figure shows simple drive of IO buffer with 50ohms pull-up to capture the rise time.



cadence

Falling slew rate dv/dt



Here dv/dt = 360mV/65pS = 5.6 V/ns which is within spec of 4 to 9 V/ns

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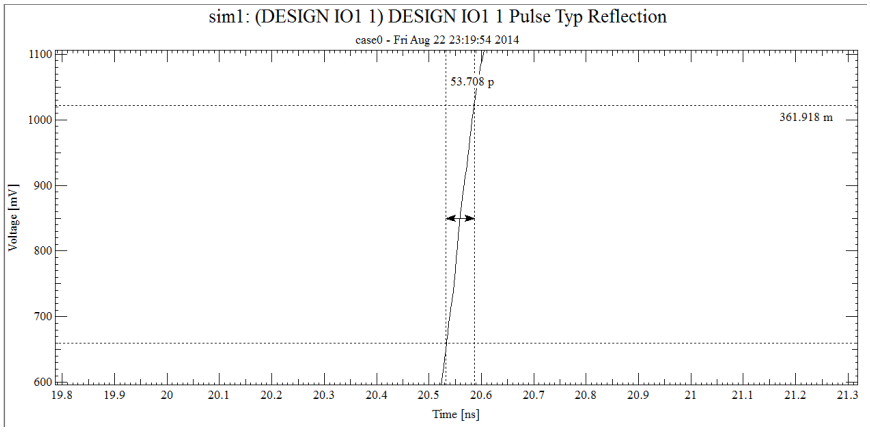
Rising slew rate



Here dv/dt = 360mV/54pS = 6.6 V/ns which is within spec of 4 to 9 V/ns

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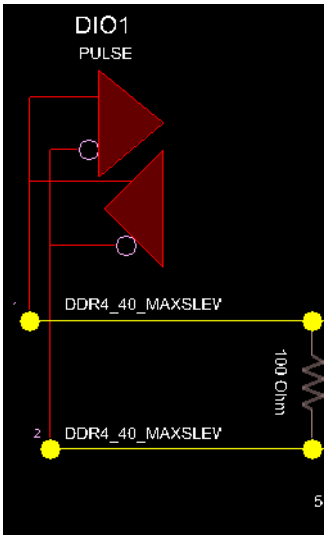
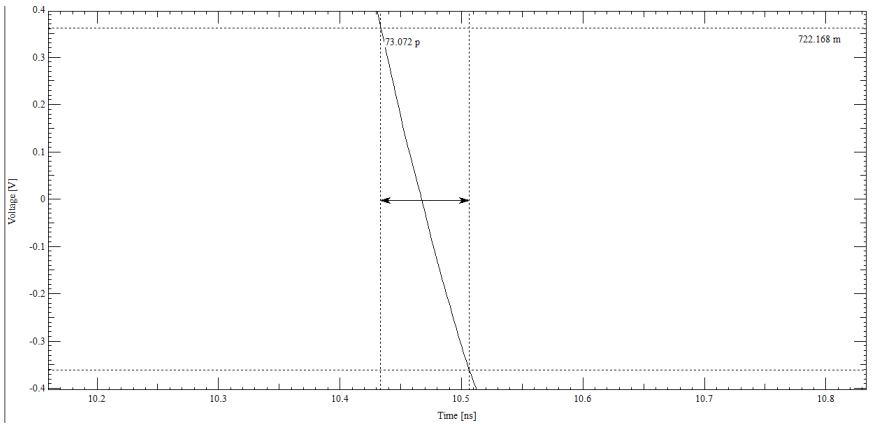
Methodology to check DDR compliance - Differential test-bench (DDR4)

- Figure shows simple drive of differential IO buffer with 100 ohms termination to capture the rise and fall time.



cadence

Falling Slew Rate



Here dv/dt = 722mV/73pS = 9.9 V/ns which is within spec of 8 to 18 V/ns

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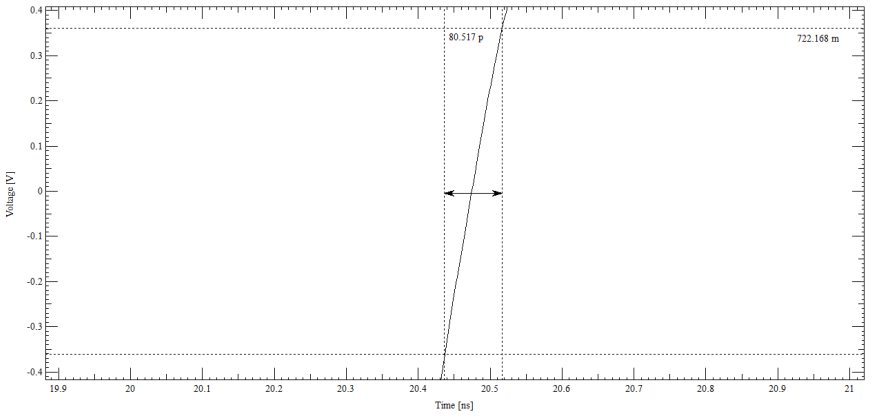
Rising Slew Rate



Here dv/dt = 722mV/80pS = 9.0 V/ns which is within spec of 8 to 18 V/ns

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Methodology to check DDR compliance - Timing Checks

- Average High Pulse
- Average Low Pulse
- Average Clock Period

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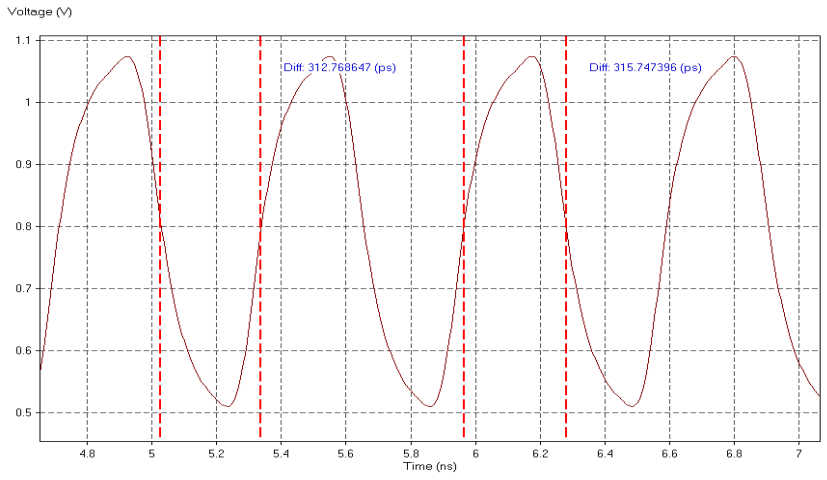
Data Pulse variation @ 3.2G (slow corner)



Here min duty cycle is 312pS/625pS = .499UI > .45UI

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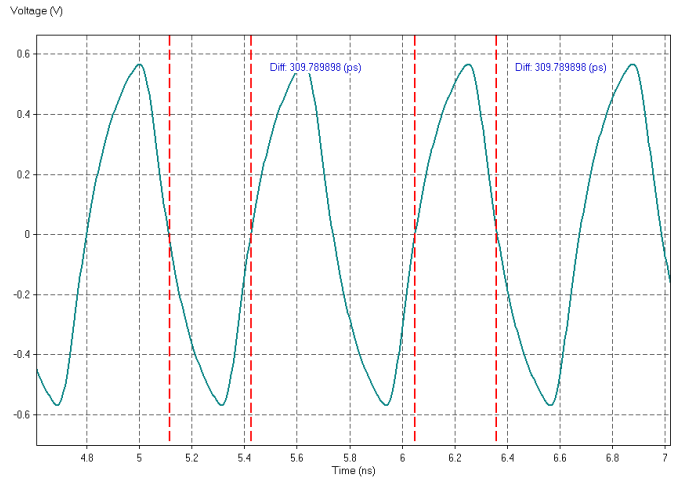
Clock Pulse variation



Here min duty cycle is 309pS/625pS = .494UI > .45UI

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Agenda

- Problem Statement
- Overview of DDR compliance checks
- Methodology to check DDR compliance
  - Impedance
  - Slew rate
  - Pulse-width variation
- Conclusion

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Conclusion

- It is important to verify DDR controller IBIS separately before doing system simulations
- IBIS verification against JEDEC requirements can help in
  - Quickly verifying PHY netlist for compliance
  - Ensuring that IBIS models have been correctly made with proper netlist settings, especially when ZQ calibration needs to be properly done to obtain proper impedance values at corners.

  cadence

cadence®

  cadence

Corner Considerations

Bob Ross, Teraspeed Labs
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Asian IBIS Summit
Taipei, Taiwan
November 17, 2014

(Given by Anders Ekholm, Ericsson)

Outline

- **Overview**
- **Corner Review**
- **Parameter Passing Corners in IBIS Version 6.0**
- **Upcoming Interconnect Modeling Corners**
- **Td, Zo to/from L, C Conversions**
- **Concluding Comments**

Overview

- Corners in this presentation mean the assignment of Typ, Min, Max (or Typ, Slow, Fast) entries
- Different areas of IBIS have different corner definitions
- IBIS supports passing parameter values into IBIS-ISS (an HSPICE subset) sub-circuits
- The parameter descriptions can also contain corners
- Purpose of this presentation is to show different methods and provide some advice

Corner Review

- [Model] Corners
- [External Model] Corners
- [External Circuit] Corners
- [Package] Corners
- IBIS-AMI Corners

[Model] Corners

- Typ: Typical process and conditions
- Min: Slow, Weak process and conditions (low voltage and high temperature for CMOS)
- Max: Fast, Strong process and conditions (high voltage and low temperature for CMOS)
- [Model Spec] corners are aligned with [Model]
- C_comp corners are by magnitude and represent the range of values
- [External Model] Corner lines track [Model] corners (shown next)

[External Model] Corners

```
[External Model] Buffer
Language IBIS-ISS
|
| Corner corner_name file_name     .subckt_name
Corner   Typ         buffer.iss    typ_typ
Corner   Min         buffer.iss    slow_min
Corner   Max         buffer.iss    fast_max
```

- [External Model] is under [Model]
- [Model] corner selection determines which Corner line to use

[External Circuit] Corners

```
[External Circuit] Circuit
Language IBIS-ISS
|
| Corner corner_name file_name     .subckt_name
Corner   Typ         circuit.iss   typ_typ
Corner   Min         circuit.iss   slow_min
Corner   Max         circuit.iss   fast_max
```

- User or EDA tool selects Corner line:
  - For buffer, set same as [Model] setting
  - For on-die interconnect, Corner can be used for range of values or aligned with connected [External Circuit] buffer

[Package] Corners

- Default corners show range of values:

```
[Package] | Corners by magnitude value give range
L_pkg  <Typ_val>  <Min_val>  <Max_val>
C_pkg  <Typ_val>  <Min_val>  <Max_val>
R_pkg  <Typ_val>  <Min_val>  <Max_val>
```

- Most IBIS models have pin-specific detail that overrides [Package] setting:
  - L_pin, C_pin, R_pin
  - [Package Model] with [Define Package Model]

IBIS-AMI Corners

- **AMI File, For example:**

```
(<parameter_name> (Usage Info) (Type Float)
                  (Corner <Typ_val> <slow_val> <fast_val>))
```

- **Typ, Slow, Fast entries**
- **Slow, Fast entries not clear for some parameters such as Zo for reference impedance**
- **(Beyond Corners, IBIS-AMI allows these choices: List, Range, Steps, Increment, Value)**
- **User or EDA tool makes Corner selection**
- **Corners used for speed entry or range of values**

Parameter Passing Corners in IBIS Version 6.0

- **Note, "parameter" used in several ways**
  - **"parameter" name variable in IBIS-AMI**
  - **"Parameter definition file" (an AMI file)**
  - **"Parameters" line assignment for [External Model] or [External Circuit]**
  - **"parameter" value passed into IBIS-ISS sub-circuit**
  - **"Parameter file (a non-AMI file for storing parameter names and assignments)**

Parameter Passing Corners in IBIS V6.0

- Used with [External Model] or [External Circuit]
- Actual corner selections stored in an IBIS-AMI file or a separate parameter file with any extension
- Parameter values passed into IBIS-ISS sub-circuits
- User selects which Parameter line corner to use
- Example shown next with transmission line Td (delay), Zo (reference impedance) parameters

[External Circuit] with Parameters Corner

```
Parameters Td=<name>.ami(<root>(Model_Specific(Td)))
Parameters Zo=<name>.ami(<root>(Model_Specific(Zo)))
....
[External Circuit] Interconnect-ISS
Language IBIS-ISS
|
| Corner corner_name file_name     .subckt_name
Corner   Typ         t-line.iss    typ_typ
Corner   Min         t-line.iss    slow_min
Corner   Max         t-line.iss    fast_max
```

- Assume Parameters corners used in ALL Corner lines
- Td, Zo parameter values passed into the typ_min, slow_min, fast_max sub-circuits

[External Circuit] Parameters Using IBIS-AMI Example

- **Parameters to pass into IBIS-ISS:**

```
Parameters Td=<name>.ami(<root>(Model_Specific(Td)))
Parameters Zo=<name>.ami(<root>(Model_Specific(Zo)))
```

- **AMI File, (Model_Specific section):**

```
(Td (Usage Info) (Type Float)
                    (Corner 60e-12  66e-12  54e-12))
(Zo (Usage Info) (Type Float)     (Corner 50 55 45))
```

- **(Zo corner is ambiguous – larger value is selected as slow, (weaker) corner**

[External Circuit] Parameter Example Comments

- **Not clear whether the Parameters Lines should be aligned with the Typ, Min, Max corners or used as a range of values for each of the Corner lines**
- **Helpful solutions: use specific assignment:**
  - **Assign parameters directly in each IBIS-ISS sub-circuit**
  - **Or use separate parameter names; for example, Td_typ, Td_min, Td_max for individual range of values**
  - **Or use direct parameter Value assignment**
- **Minimize complication by minimizing user selections, where possible**

Upcoming Interconnect Modeling Corners

- Attaches IBIS-ISS or Touchstone descriptions to buffers, die interfaces or pin interfaces
- Focus here is on IBIS-ISS applications
- Syntax is similar to [External Circuit] connection syntax ("File_ISS" replaces "Corner" and "Language")

```
| file_type   corner_name file_name    .subckt name
File_ISS      Typ         net.iss      netlist_typ
File_ISS      Min         net.iss      netlist_min
File_ISS      Max         net.iss      netlist_max
```

Param Line in Upcoming Interconnect Modeling Proposal

- Supports parameter passing to IBIS-ISS ("Param" is used to be distinct from the multiple meanings of Parameter)

```
Param   <Name>   <Typ>   <Min>   <Max>
```

- Min: Slow, Weak (where possible)
- Max: Fast, Strong (where possible)
- Mixing Min, Max possible for uncorrelated ranges
- All Min, All Max should be one option

Adding Param Line Example:

```
| Param    Name      Typ       Min      Max
Param      Td        60ps      66ps     54ps
Param      Zo        50        55       45
|
| file_type  corner_name file_name    .subckt name
File_ISS     Typ          net.iss      netlist_typ
File_ISS     Min          net.iss      netlist_min
File_ISS     Max          net.iss      netlist_max
```

Interconnect Proposal Advice

- Similar to [External Circuit] advice
- Minimize or avoid parameter passing, where possible
- Be specific with parameter corner names
- Embed parameter values in sub-circuits
- Otherwise, parameters might be treated as a range of values

Td, Zo to/from L, C Conversions

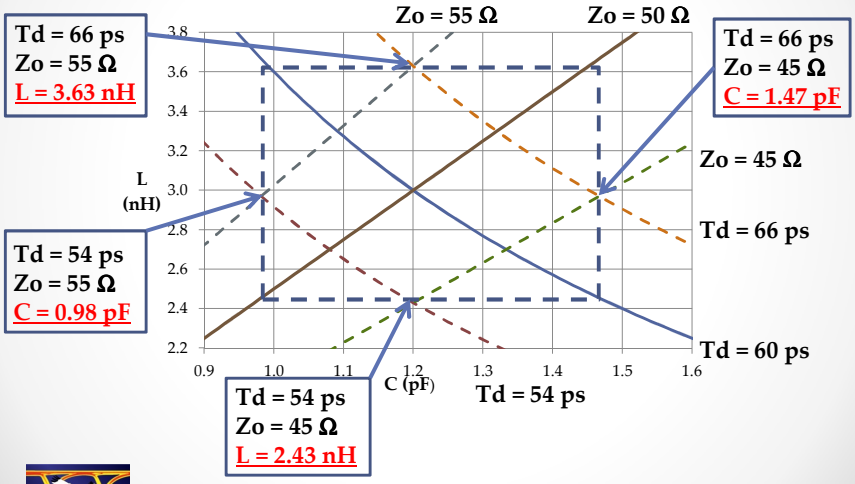
- Interconnect or package values may be extracted from TDR measurement in terms of ideal transmission line Td (delay) and Zo (reference impedance) values
- These values can be used directly, or might be converted to L, C representations for package models or for parameters in Interconnect Models
- L, C representation of corners give different 'effective" ranges than the original Td, Zo corners

Equations to Plot L versus C as a Function of Td, Zo

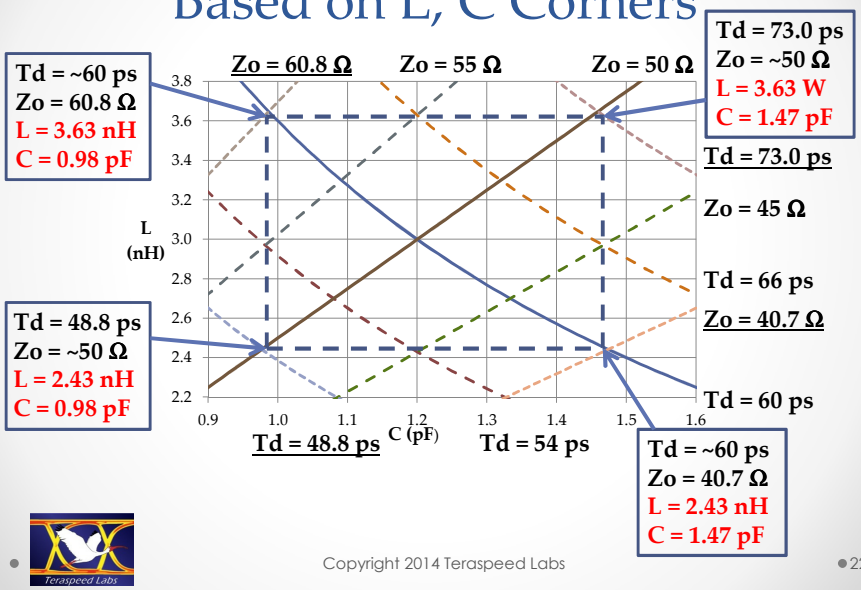
- Transmission line to/from package transformations:
  - Td = Time delay
  - Zo = Reference impedance
  - L = Inductance
  - C = Capacitance

  - Td = Sqrt(LC), Zo = Sqrt(L/C) or
  - L = TdZo, C = Td/Zo ➔ $L = Td^2/C$, $L = Zo^2C$

L, C Min/Max Values from Example Td, Zo Corners



Wider "Effective" Td, Zo Based on L, C Corners



Wider "Effective" Td, Zo Based on L, C Corner Analysis

|Param	Name	Typ	Min	Max	| Original
Param	Zo	50	55	45	
Param	Td	60ps	66ps	54ps	

|Param	Name	Typ	Min	Max	L, C
Param	L	3.00nH	3.63nH	2.43nH	parameter
Param	C	1.20pF	1.47pF	0.98pF	corners

- Combinations of L, C parameter do NOT give the Original ranges, as shown in previous slide:
  - Td range = 48.8 ps to 73.0 ps
  - Zo range = 40.7 Ω to 60.8 Ω

Concluding Comments

- IBIS contains several methods to describe corners and to assign and pass parameters
- Minimize parameter passing with corners because of different possible interpretations
- EDA tool should be capable of mixing or matching Typ, Min, Max conditions
- L, C corner values derived from Td, Zo corners can give different "effective" ranges

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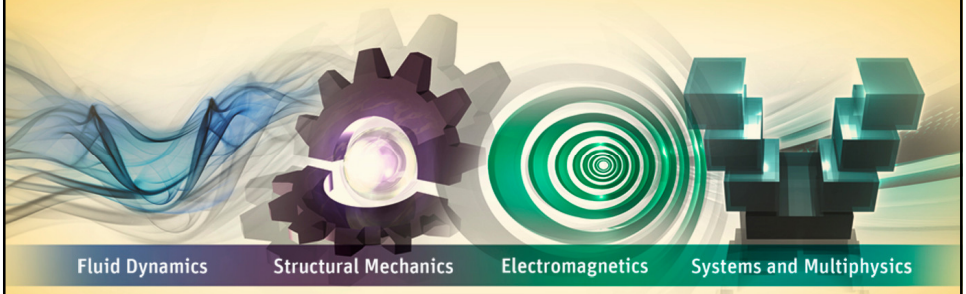
Best Practices for High-Speed Serial Link Simulation



Asian IBIS Summit
Taipei, Taiwan
November 17, 2014

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Background

- High speed serial design becoming very common
- Increased reliance on s-parameter models in circuit simulation
- S-parameters can have subtle (and often not subtle) problems in simulation
- How can we best discover or avoid these issues before circuit simulation?

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Agenda

- Bandwidth
- Sampling Rate
- Model Concatenation
- Passivity
- Causality

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Data Bandwidth

"What is the appropriate bandwidth for a given model?"

 4

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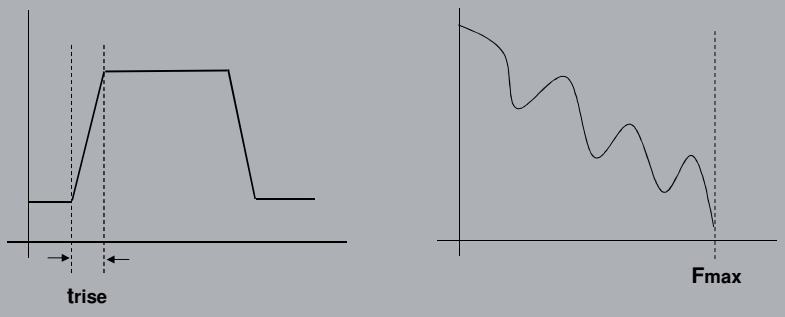
Data Bandwidth

- Always have a realistic DC point
- Maximum frequency dependent on application
- Rule of thumb
  - Fmax = .35/trise



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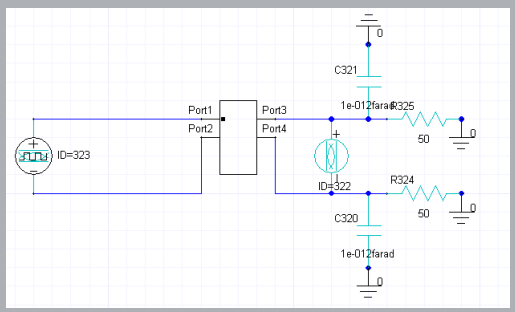
Max Frequency Study

- Set up test circuit
  - 10Gb/s data rate
  - 10ps rise/fall time
  - 750 mm stripline model
  - Sweep Fmax from 5 to 50GHz, 10MHz step



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Max Frequency Test

- QuickEye analysis
  - Convolution based fast transient
  - PRBS15 pattern
- VerifEye analysis
  - Statistical eye analysis
- Both take advantage of LTI assumption
  - Characterize linear channel with step response

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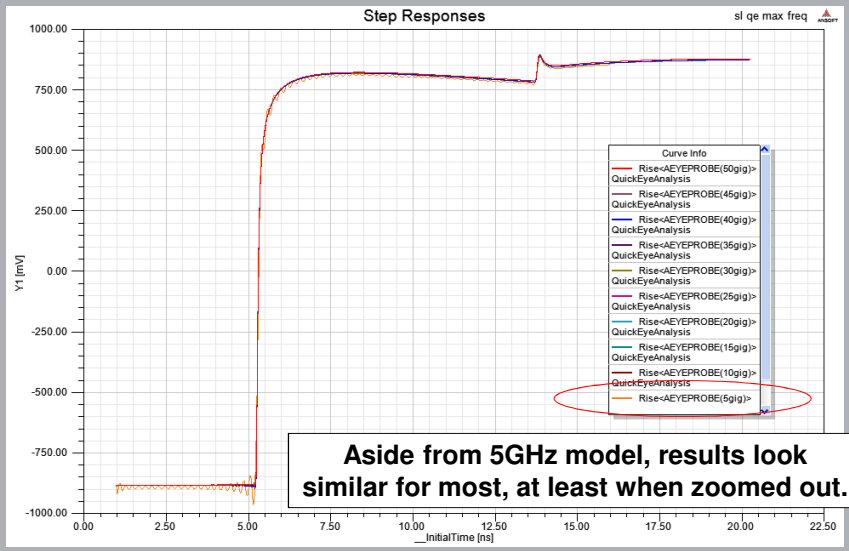
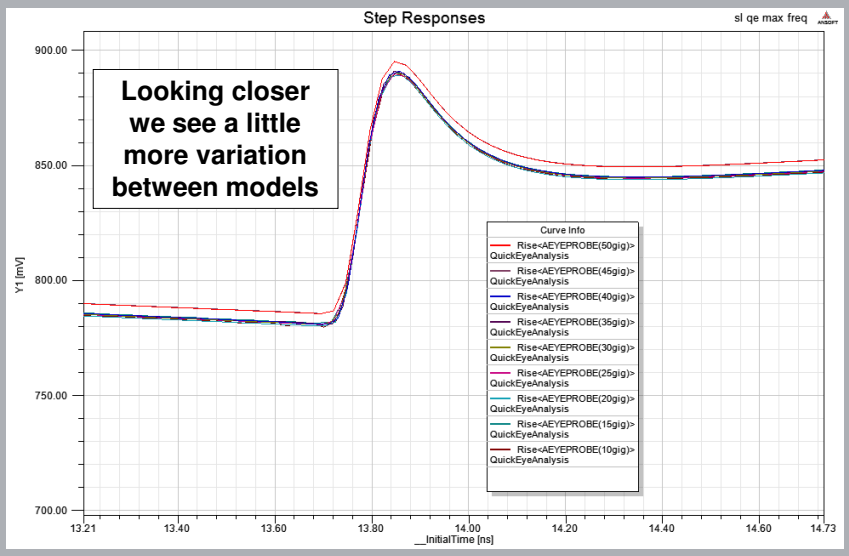
Max Frequency Sweep: Step Responses

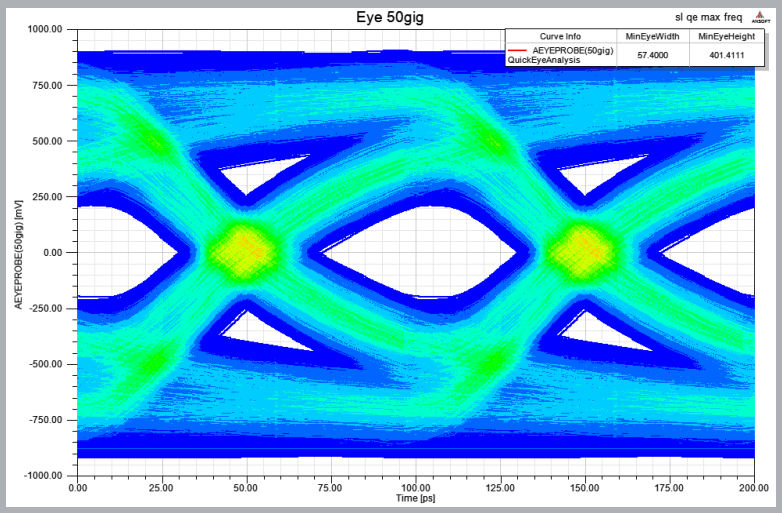


Aside from 5GHz model, results look similar for most, at least when zoomed out.

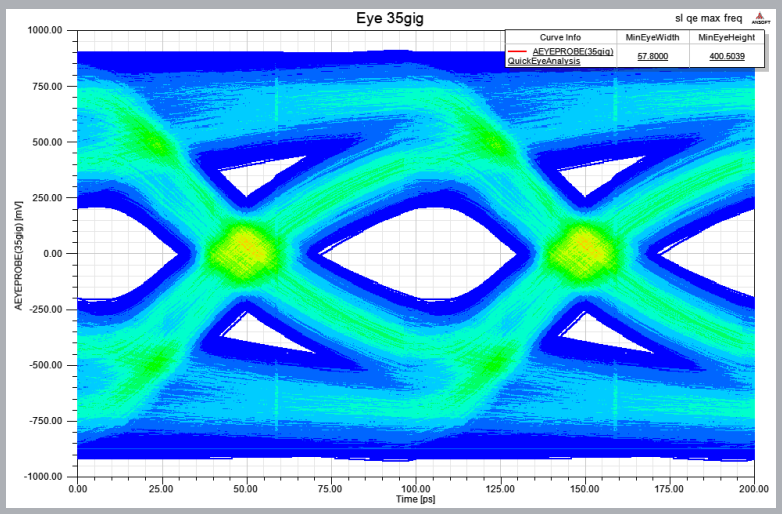
Max Frequency Sweep: Step Responses



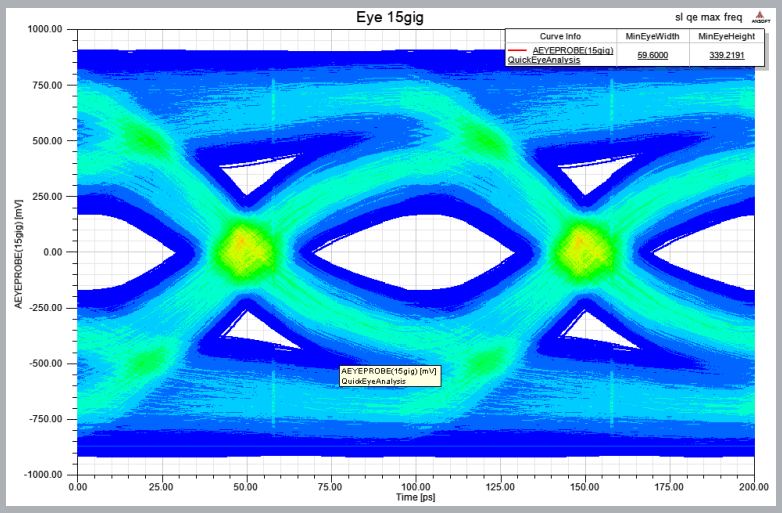
Max Frequency, QuickEye Results, 50GHz



Max Frequency, QuickEye Results, 35GHz



Max Frequency, QuickEye Results, 15GHz



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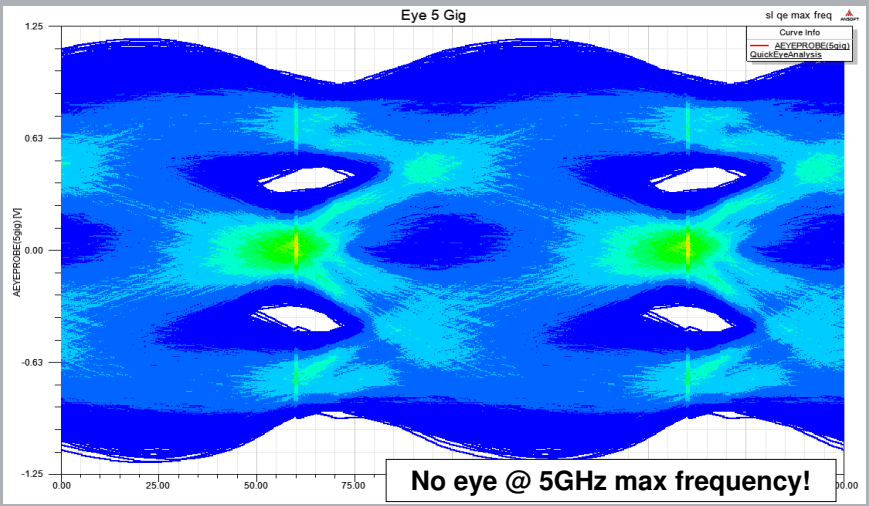
Max Frequency, QuickEye Results, 5GHz



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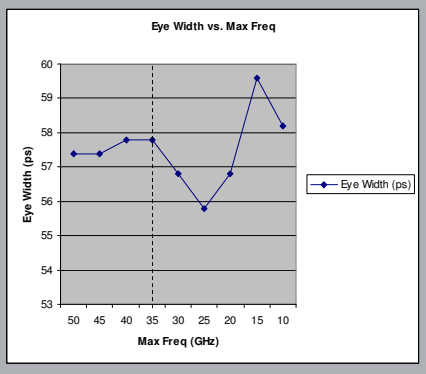
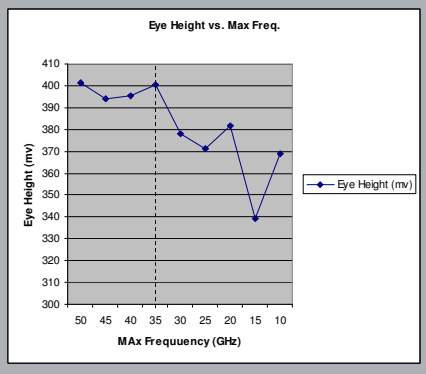
Max Frequency vs. Eye Opening

QuickEye Results





Fmax = .35/trise = .35/10ps = 35GHz

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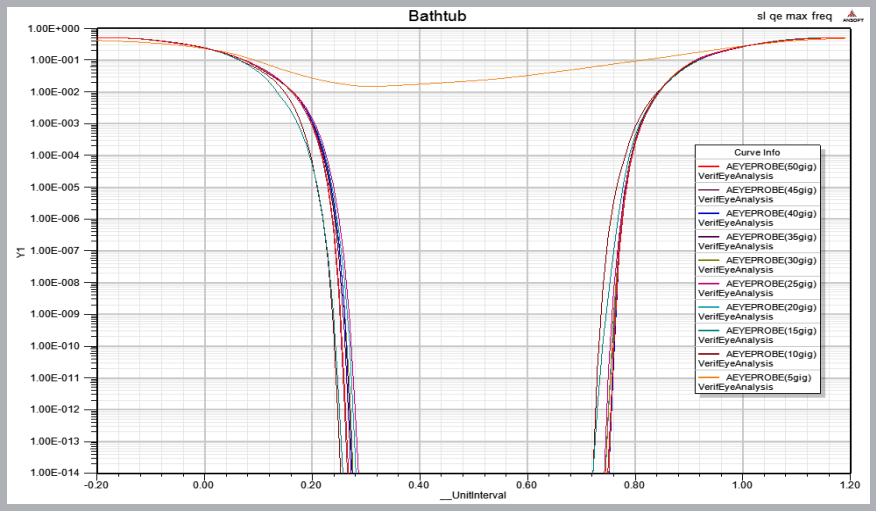
Max Frequency, VerifEye Results



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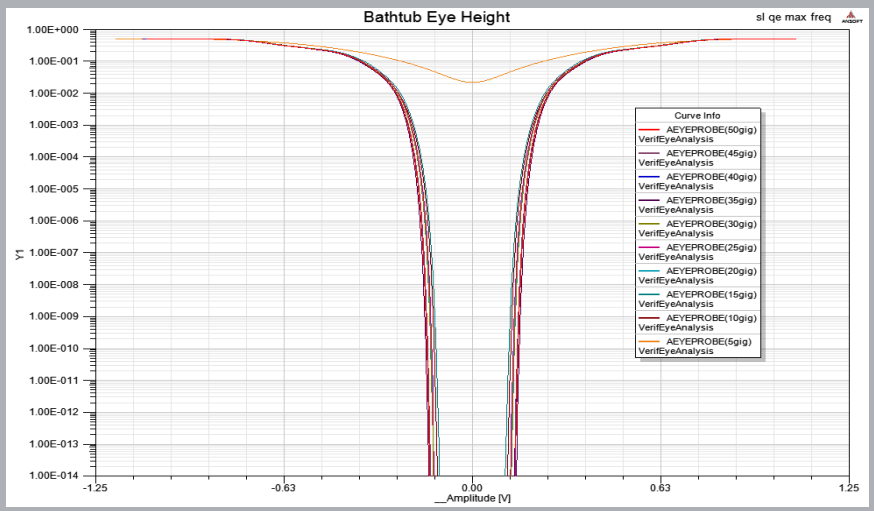
Max Frequency, VerifEye Results



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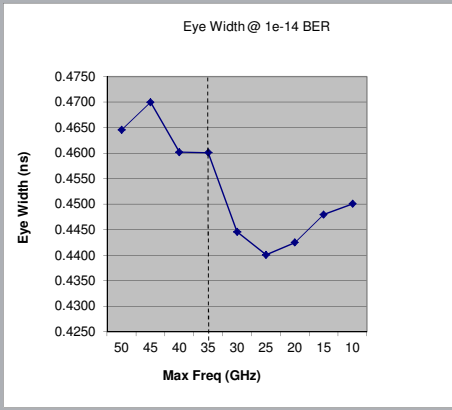
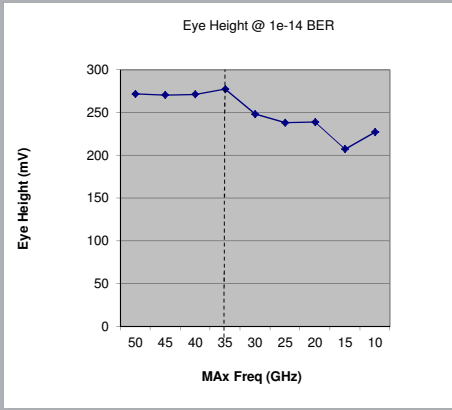
Max Frequency vs. Eye Opening

VerifEye Results





Fmax = .35/trise = .35/10ps = 35GHz

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Frequency Step

"Why do I care about low frequency data for a SERDES application? Doesn't encoding take care of that?"

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Frequency Step

- Tendency to focus on bandwidth and max frequency
- Remember to check if there is enough low frequency data in the model
  - Low frequency info required in order to reconstruct the propagation delay in the model
  - Remember Nyquist:
    - Ts = .5 / Fmax
    - Fs = .5 / Tmax

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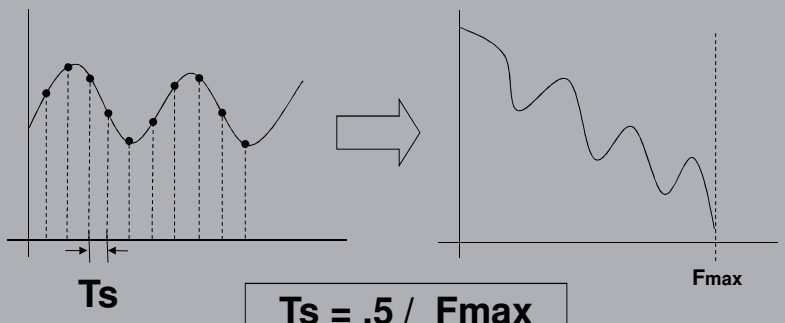
Nyquist and Sampling

- Traditionally taught as the time domain sample rate required to achieve a certain frequency domain bandwidth



Ts = .5 / Fmax

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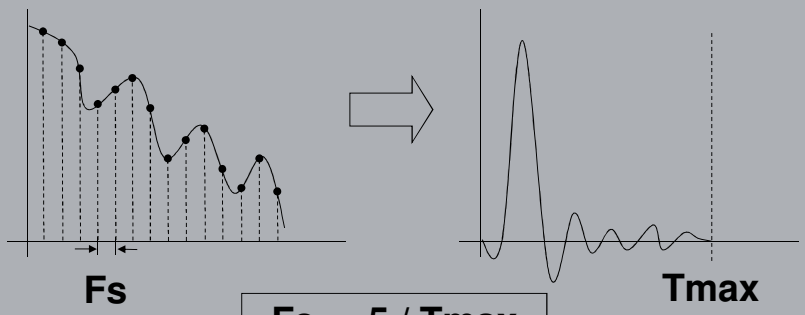
Nyquist and Sampling

- Given that frequency and time are duals of each other, there is a frequency domain sample rate requirement for reconstructing time delay



Fs = .5 / Tmax

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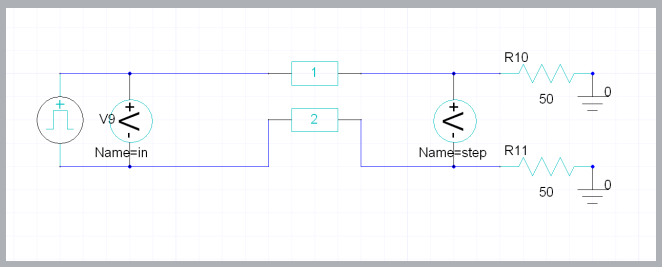
Test Channel for Sampling Experiment

- Step Source
- 750mm transmission line s-parameters
- Original data 0 to 50GHz, 10MHz step
- Resample at greater frequency step sizes



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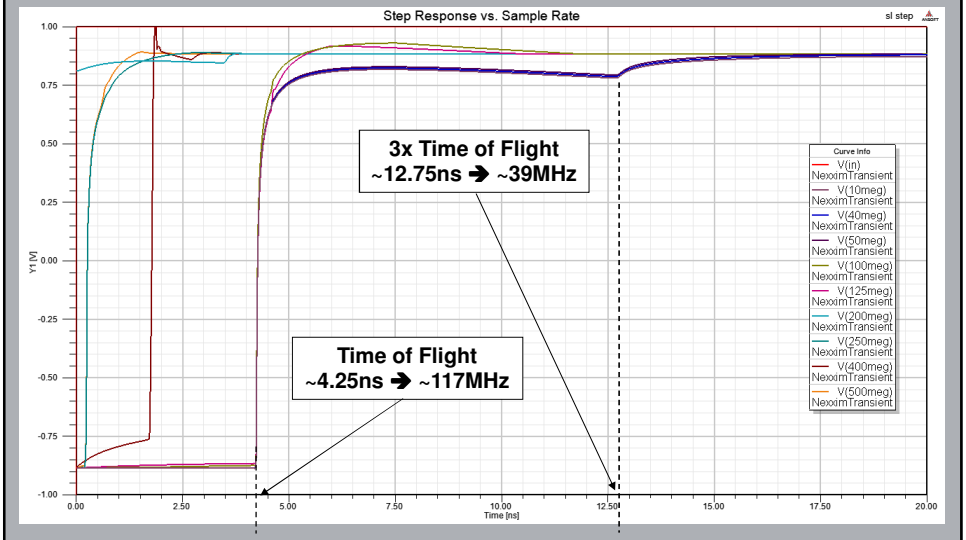
Step Responses



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Frequency Step Guidelines

- When considering your frequency step size, determine the actual delay time you need to capture
- Depending on terminations, you may need to account for multiple reflections
- Essentially the settling time for the step response of the model is the t_{max} that should dictate the sample rate

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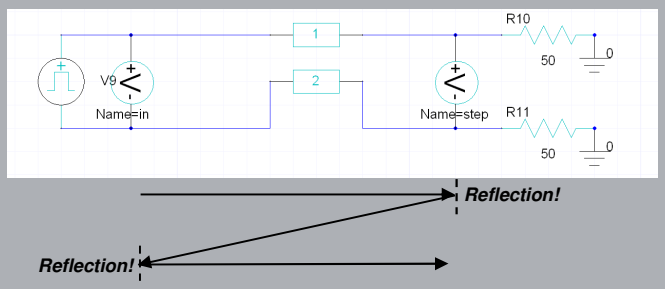
Frequency Step Guidelines

- Rule of thumb
  - 3x time of flight
  - This allows for a reflection at the far end to make an additional round trip to the near end and back



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Model Concatenation

"Do I have to do this for every single model if I need to make a single set of s-parameters for my whole channel?"

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Model Concatenation

- Sometimes there is the need to concatenate part or all of a channel into a single s-parameter model
- The step size in the new model is governed by the overall delay you need to capture
- This will require you to oversample each of the individual blocks in order to get the overall delay right

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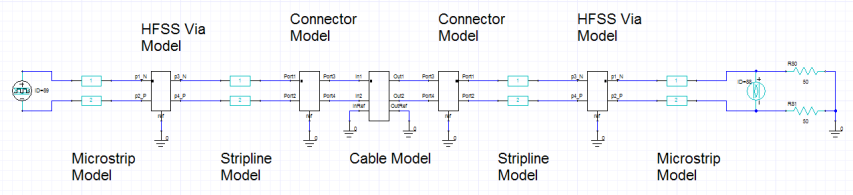
Model Concatenation



- Max frequency still dependant on rise time
- You can use the same 3x time of flight rule
- Better yet, look at the step response of the circuit for a more accurate view of the settling time

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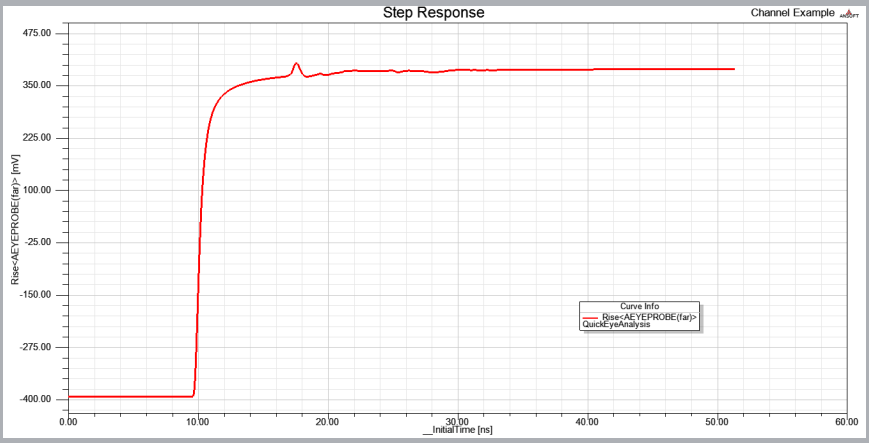
Model Concatenation



•3x t.o.f would be 30ns, ~17MHz sample rate
•Real settling time closer to 50ns, 10MHz step needed for full accuracy

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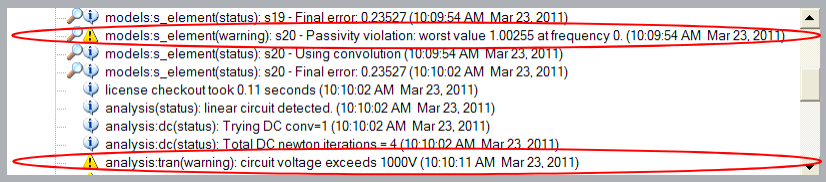
Passivity

"My simulation just failed! What do these warnings mean?"



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Passivity

- What is Passivity and why do I care?
  - Models must not create power/energy
  - Known source of inaccuracy in s-parameter models
  - Causes simulations to fail via non-convergence
  - Is a function of the entire matrix
  - Can check passivity using Singular Value Decomposition (SVD)
    - Max singular values of the s-matrix at each frequency point in the model must be <= 1

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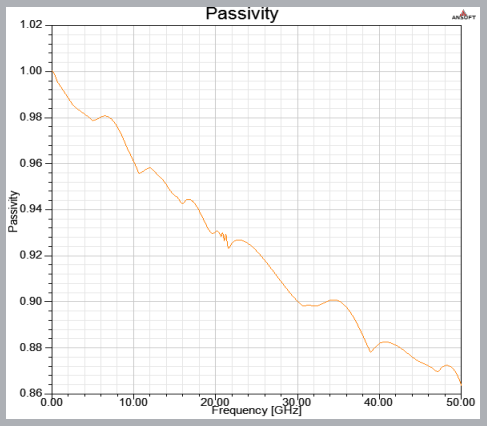
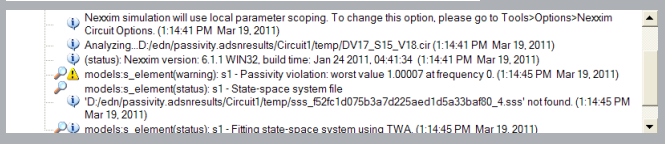
Look at Maximum Singular Value



Freq	Passivity
0.00000Hz	1.00007
0.00500GHz	1.00007
0.01000GHz	1.00007
0.01500GHz	1.00006
0.02000GHz	1.00006
0.02500GHz	1.00006
0.03000GHz	1.00006
0.03500GHz	1.00005
0.04000GHz	1.00005
0.04500GHz	1.00005
0.05000GHz	1.00004
0.05500GHz	1.00004
0.06000GHz	1.00003
0.06500GHz	1.00002
0.07000GHz	1.00002
0.07500GHz	1.00001
0.08000GHz	1.00000
0.08500GHz	0.99999
0.09000GHz	0.99998
0.09500GHz	0.99997
0.10000GHz	0.99996
0.10500GHz	0.99995
0.11000GHz	0.99994
0.11500GHz	0.99993
0.12000GHz	0.99992
0.12500GHz	0.99990
0.13000GHz	0.99989
0.13500GHz	0.99988
0.14000GHz	0.99986
0.14500GHz	0.99985
0.15000GHz	0.99983



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Passivity

- *Is it OK if my model is "a little" non-passive?*
  - Short answer: No
  - Long answer: No, but you might be lucky
    - It can be hard to say if non-passive data will stay stable long enough to get good results in simulation
    - It might just be a matter of stop time
    - Termination can mask non-passivity by absorbing the extra energy produced by the matrix

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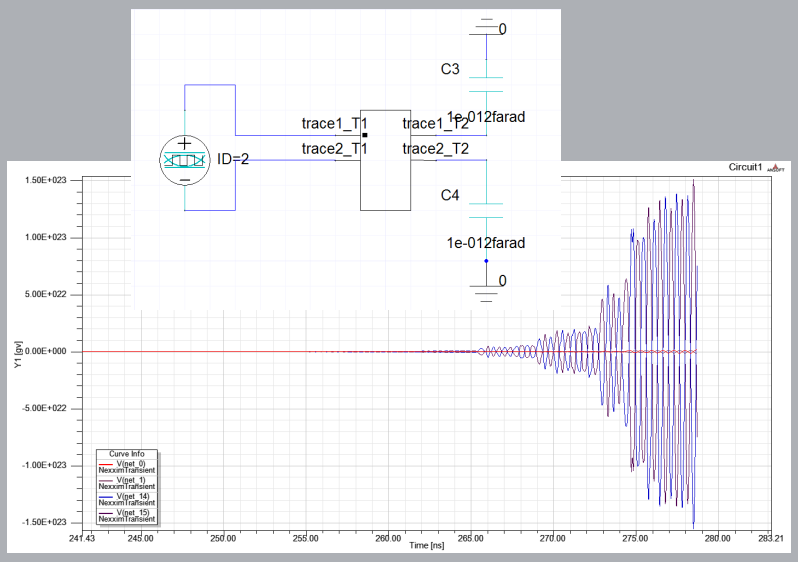
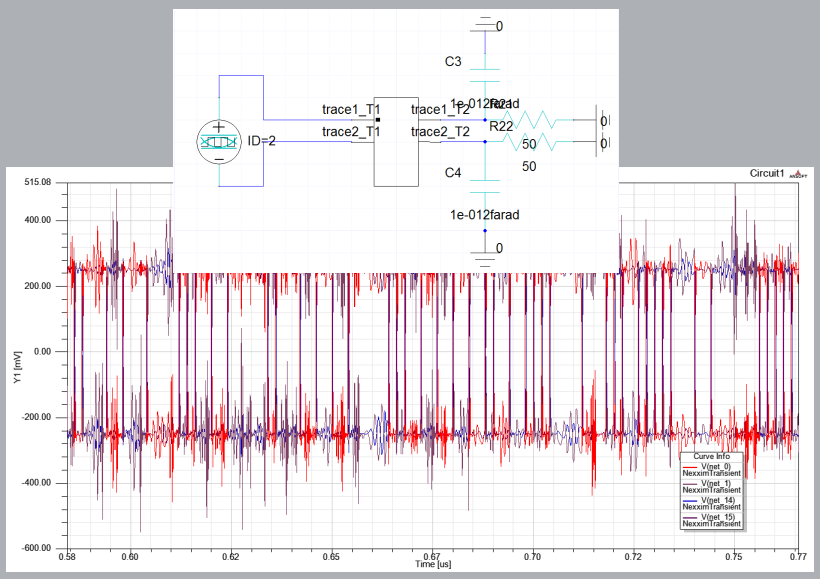
Non-Passive Data



Termination Can Absorb Extra Energy



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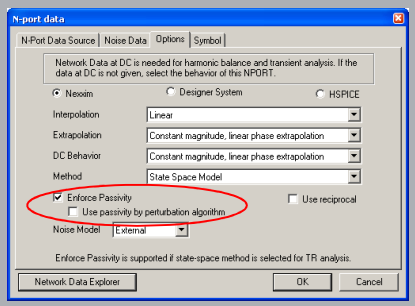
Passivity

- So what do I do?
  - Passivity Enforcement
    - Convex optimization
    - Perturbation
  - Drawbacks
    - Can result in worse fit to the data
    - Not always successful
  - For field solver models, consider tightening the error tolerance and re-simulating



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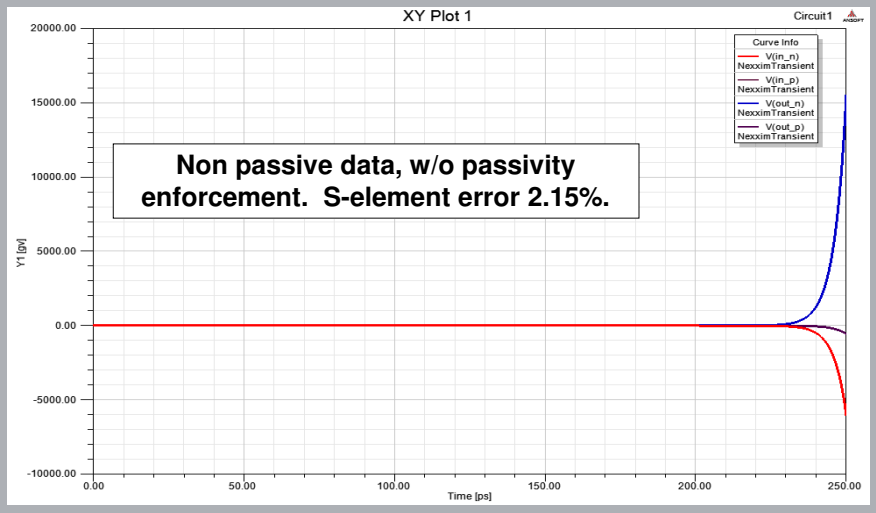
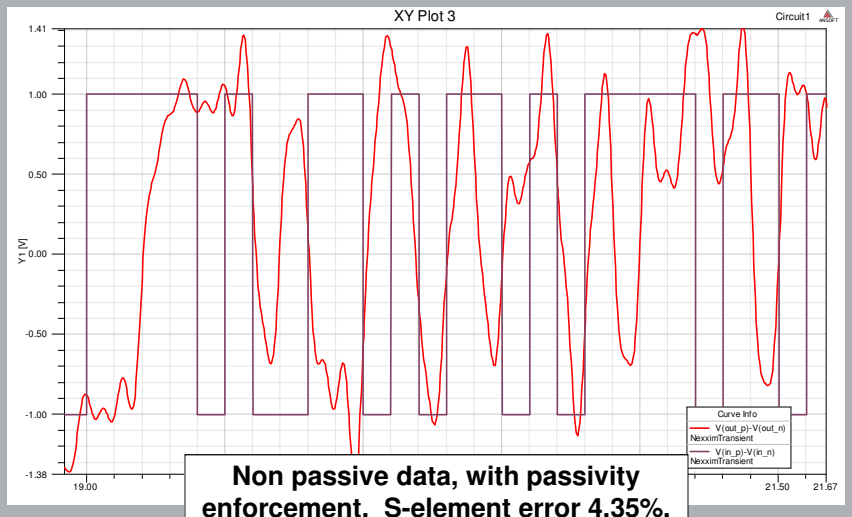
Passivity Enforcement



Passivity Enforcement



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Causality

"Why do I need to care about causality, and how do I know if I have a problem?"

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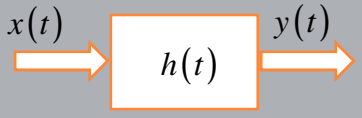
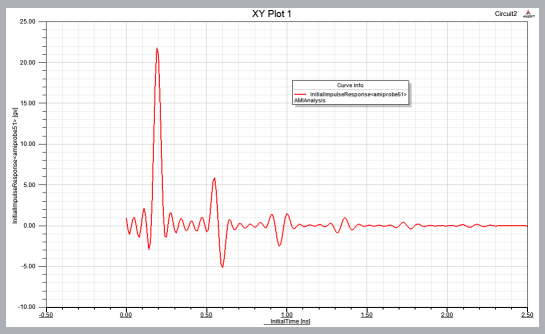
Causality

- Several definitions
  - Causes must precede effects
  - Impulse response is 0 before t=0
  - Signals cannot travel faster than the speed of light



$$h(t) = 0 \quad t < 0$$



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Causality

- What can cause non-causality in S-parameter models?
  - Bad dielectric models in fieldsolvers
  - Loose convergence criteria in fieldsolver
  - Under sampling leading to interpolation/extrapolation error
  - Measurement noise

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Causality

- Detection of non-causality is not as simple as non-passivity
  - Need to use Hilbert relationship
    - For LTI structures, the real and imaginary parts are even/odd complements in the frequency domain
    - The Hilbert transform allows the real or imaginary parts to be reconstructed from each other
    - In theory this should be straightforward, but sampled bandlimited data add significant numerical complexity

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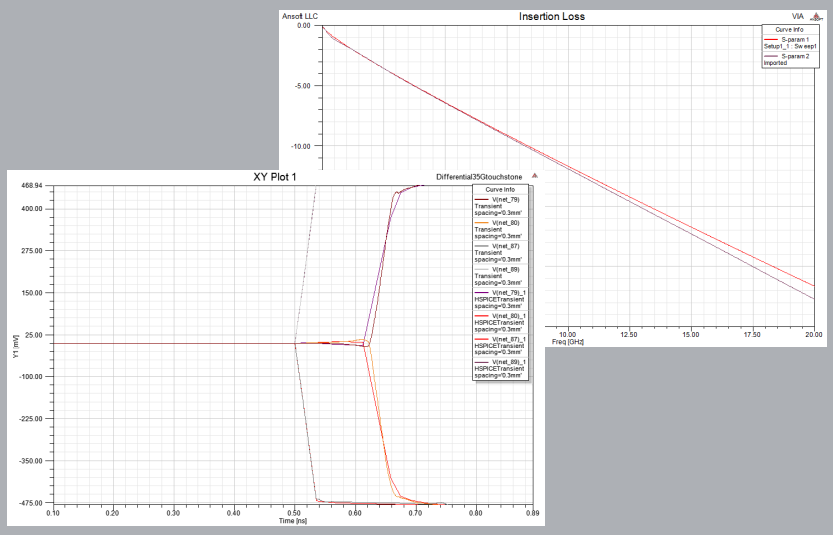
Which Model is Causal?



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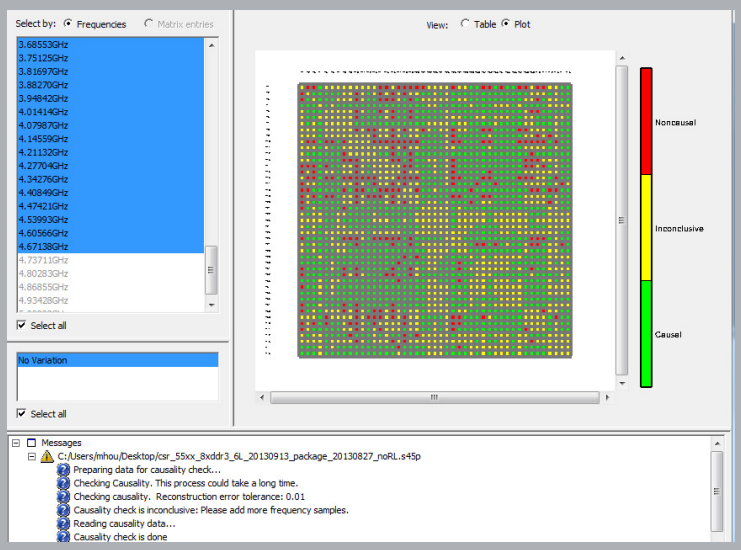
Causality Checking



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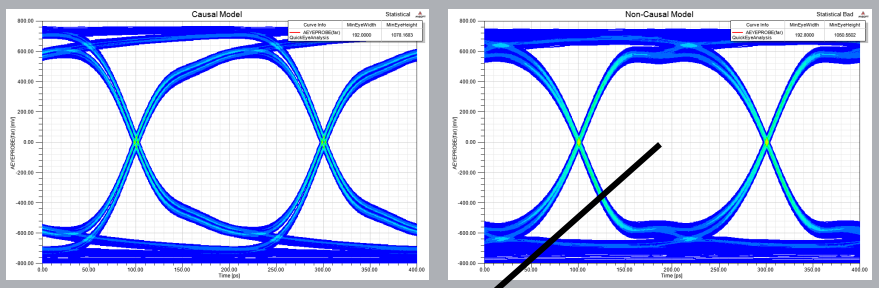
Causality Checking in State-Space



models:s_element(warning): s41 - Causality violation: Worst error relative to threshold for S(2,2) is 1.00483 percent. (12:01:09 PM Mar 23, 2011)
models:s_element(status): s41 - processing row 3 of 4 of the scattering data matrix... (12:01:09 PM Mar 23, 2011)
models:s_element(warning): s41 - Causality violation: Worst error relative to threshold for S(3,1) is 0.420155 percent. (12:08:20 PM Mar 23, 2011)
models:s_element(warning): s41 - Causality violation: Worst error relative to threshold for S(3,2) is 0.778083 percent. (12:15:31 PM Mar 23, 2011)
models:s_element(warning): s41 - Causality violation: Worst error relative to threshold for S(3,3) is 0.410643 percent. (12:22:14 PM Mar 23, 2011)
models:s_element(status): s41 - processing row 4 of 4 of the scattering data matrix... (12:22:14 PM Mar 23, 2011)
models:s_element(warning): s41 - Causality violation: Worst error relative to threshold for S(4,1) is 0.77204 percent. (12:28:37 PM Mar 23, 2011)
models:s_element(warning): s41 - Causality violation: Worst error relative to threshold for S(4,2) is 0.415145 percent. (12:35:11 PM Mar 23, 2011)
models:s_element(warning): s41 - Causality violation: Worst error relative to threshold for S(4,3) is 12.2196 percent. (12:41:52 PM Mar 23, 2011)

In general, violations greater then 0.25% are usually cause for concern.

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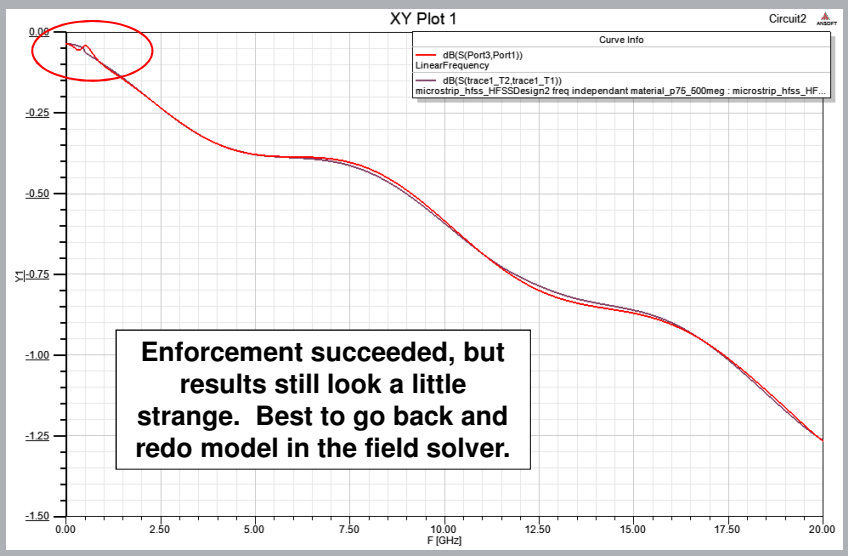
Causality Detection and Enforcement

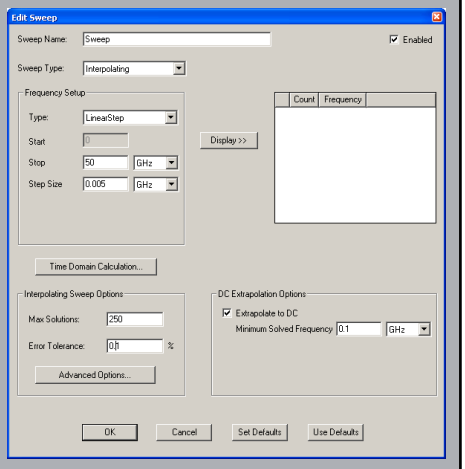
- Enforcement
  - Use causal reconstruction instead of original data
- Issues with causality enforcement
  - If a model is non-causal it is not necessarily true to assume that either the real or imaginary part is “correct”
  - Essentially throwing away half of the s-parameter data
  - If the issue can be addressed in the fieldsolver tool, that will always be a more accurate option than enforcement

Non-causal Data (purple) vs. Causal Reconstruction (red)



Going Back to the Fieldsolver

- A few things to try:
  - Causal dielectric models, e.g. Djordjevic-Sarkar
  - Tighten convergence criteria
  - Minimum solved frequency



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Causality and Passivity

- Non-causal data can lead to non-passive simulation results
  - Loss of accuracy with non-causal models
  - A bad fit to non-causal data can be the cause
  - Remember that both passivity and causality are requirements to ensure stability

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Conclusions

- Need to ensure that the model data is accurate and appropriate for simulation
  - Bandwidth
  - Frequency Sampling
  - Stability
    - Passivity
    - Causality
- Passivity and causality can be enforced, but this can affect accuracy
- S-parameter data integrity is key for good signal integrity simulations


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Thank You!
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