

# Using IBIS-AMI Model for 25Gbps Retimer Simulation

Wei Maoxiang, YinChanggang, Zhu Shunlin <u>Wei.maoxiang@zte.com.cn, yin.changgang@zte.com.cn</u> <u>Zhu.shunlin@zte.com.cn</u>

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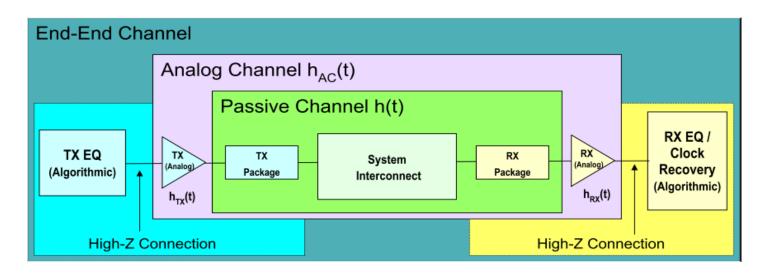
- Introduction to IBIS-AMI Model
- Repeater in SerDes System
- Lab Correlation for AMI Models
- The Application of Retimer in 25Gbps Channel
- Summary

#### Introduction to IBIS-AMI Model

- Accuracy simulation and fast run time
- IP Protection
- Supported by most EDA tools
- AMI model to provide adaptive DFE, CDR, jitter and other simulation

#### Introduction to IBIS-AMI Model

- Combination of analog & algorithmic elements
- Analog part can be considered linear and time-invariant
- Equalization and CDR can be modeled in the algorithmic part

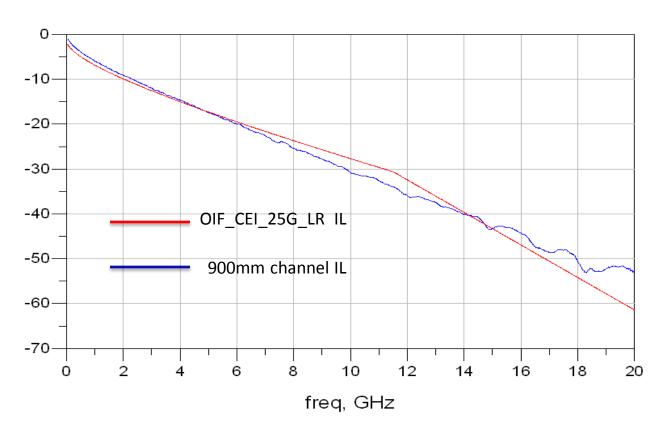


Picture reference from "IBIS-AMI Terminology Overview" at DAC 2009 IBIS Summit

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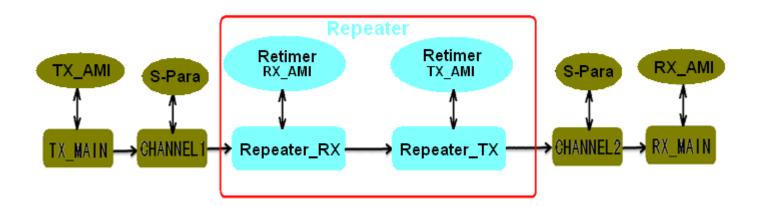
## Repeater in SerDes System

- Insertion loss increase rapidly with data rate up to 25Gbps
- When system channel is above 30inches, the IL exceed the standard of OIF/IEEE



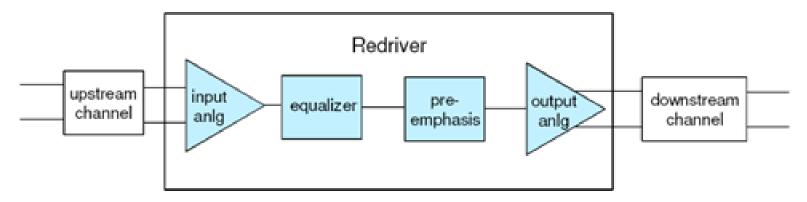
## Repeater in SerDes System

Full Channel Serdes System Including Repeater



## Repeater Device1 — Redriver

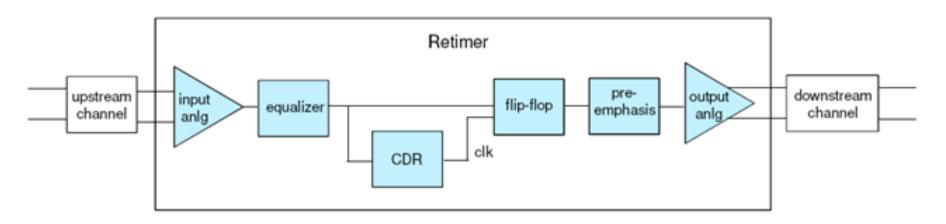
- Provide additional equalization pre-emphasis capability for highspeed transceiver system
- Recover data from the high loss and high reflection transmission medium



- Redriver output circuit is driven continuously by input signal
- No retiming is performed
- Application: 10Gbase-KR, e.g.

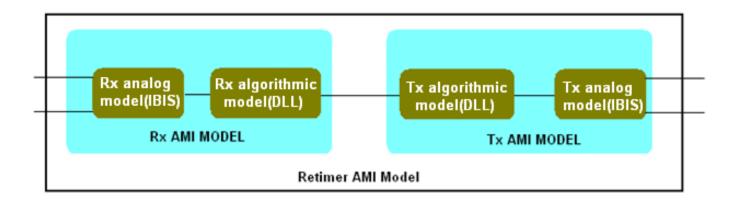
## Repeater Device2 — Retimer

 CDR: Clock Data Recovery, recover the clock from the input data, triggers a limiter and driver to optimally equalize signal



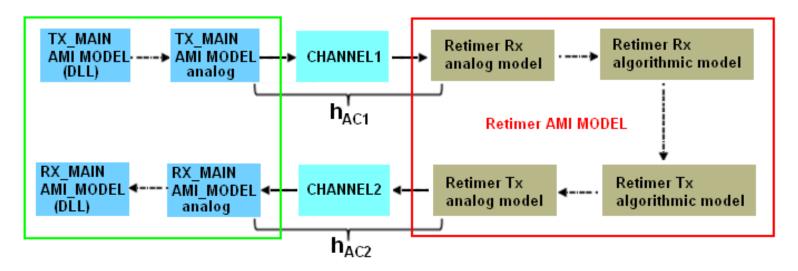
- Retimer output buffer is driven by switching events of flip-flop
- Digital data is recovered
- Jitter in clock is passed down to downstream channel
- Application: 100Gbase-KR4, e.g.

### **Retimer AMI Model**



- A retimer model includes two back-to-back AMI Rx and Tx models
- Rx and Tx analog model represents the device input termination and the output impedance respectively
- Rx and Tx algorithmic models represent equalization, CDR and preemphasis

#### **Retimer AMI Simulation**



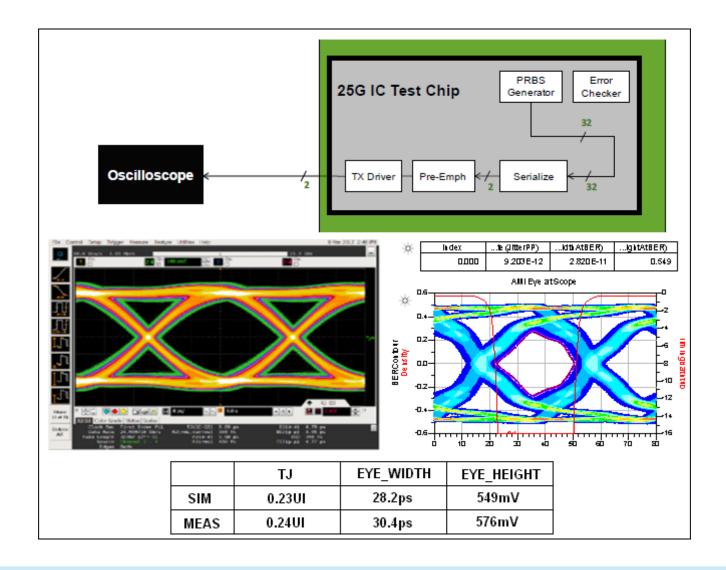
- Tx\_main analog model, channel1 and the retimer Rx analog model are linear and time-invariant, represented by combined impulse response, hac1
- The retimer Tx analog model, channel2 and Rx\_main analog model are also linear and time-invariant, represented by combined impulse response, hac2
- Tx\_main algorithmic model's output is convolved with hac1 to produce the signal to retimer Rx algorithmic model
- The retimer Tx algorithmic model's output is convolved with hac2 to produce the signal to the Rx\_main algorithmic model

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#### **Lab Correlation for AMI Models**

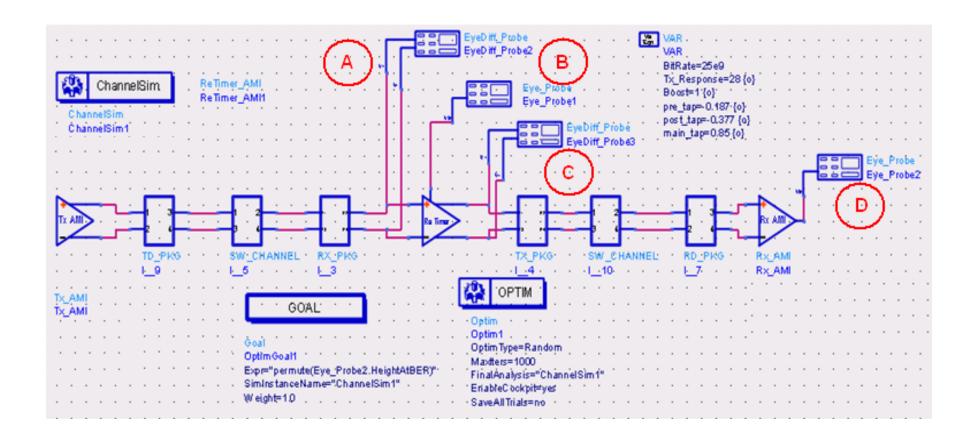
- Passive Simulation & measurement
  - Extracting S-Parameters using 2D/3D EM solver
  - Correlation based on VNA and TDR/TDT measurements
- Active Simulation
  - AMI simulation setup
  - Eye diagram analysis and design margin budget
- Correlate with laboratory measurements

#### **Lab Correlation for AMI Models**

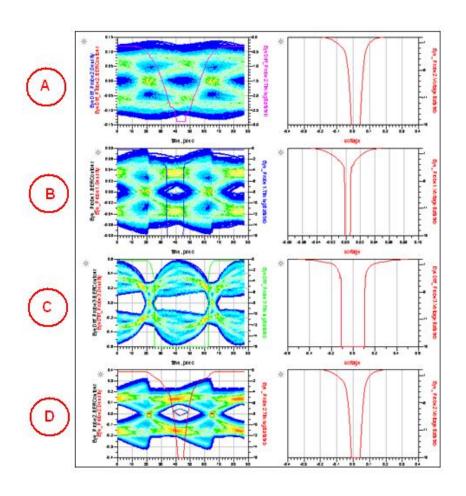


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## The Application of Retimer in 25Gbps Channel



## The Application of Retimer in 25Gbps Channel



- Five Optimizing Variables
  - Broadcom Tx:
     tap\_filter\_-1 (-0.187,0)
     tap\_filter\_0 (0.6,1)
     tap\_filter\_1 (-0.387,0)
    - Retimer
      Tx\_Response:(1-42)Boost:(1-8)
- PRBS15 1Mbit 20-30 minutes

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## **Summary**

- IBIS-AMI model can be used to provide adaptive DFE, CDR, jitter and other simulation
- Retimer is a good solution for long channels of highspeed SerDes system (>30 inches)
- As data rate increases, system design margin decreases;
   Need more accurate simulation model; AMI model accuracy need to be verified
- Retimer AMI model help us to estimate channel margin, pre-emphasis and equalization parameter in 25Gbps serial link simulation



