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Handling of Overclocking Caused by Delay in Waveform Tables

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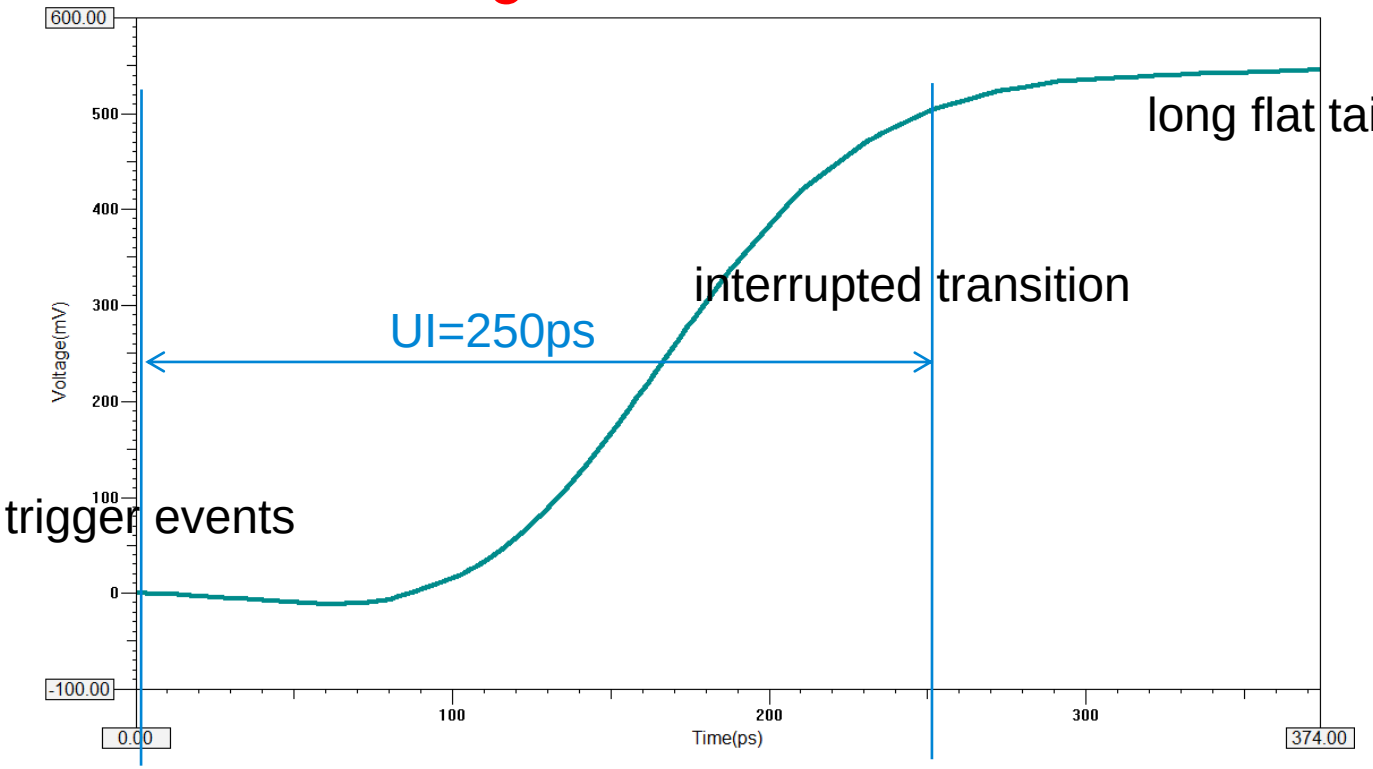
(presented by Tao Zhang, Keysight Technologies)

What is Overclocking

- A trigger event happens during transition from the low/high state to the high/low state
- The trigger event initiates transition in the opposite direction
- Interrupted transitions are **NOT** the intended operation
- The IBIS specification does not provide any means to determine buffer behavior upon interrupted transitions

True Overclocking

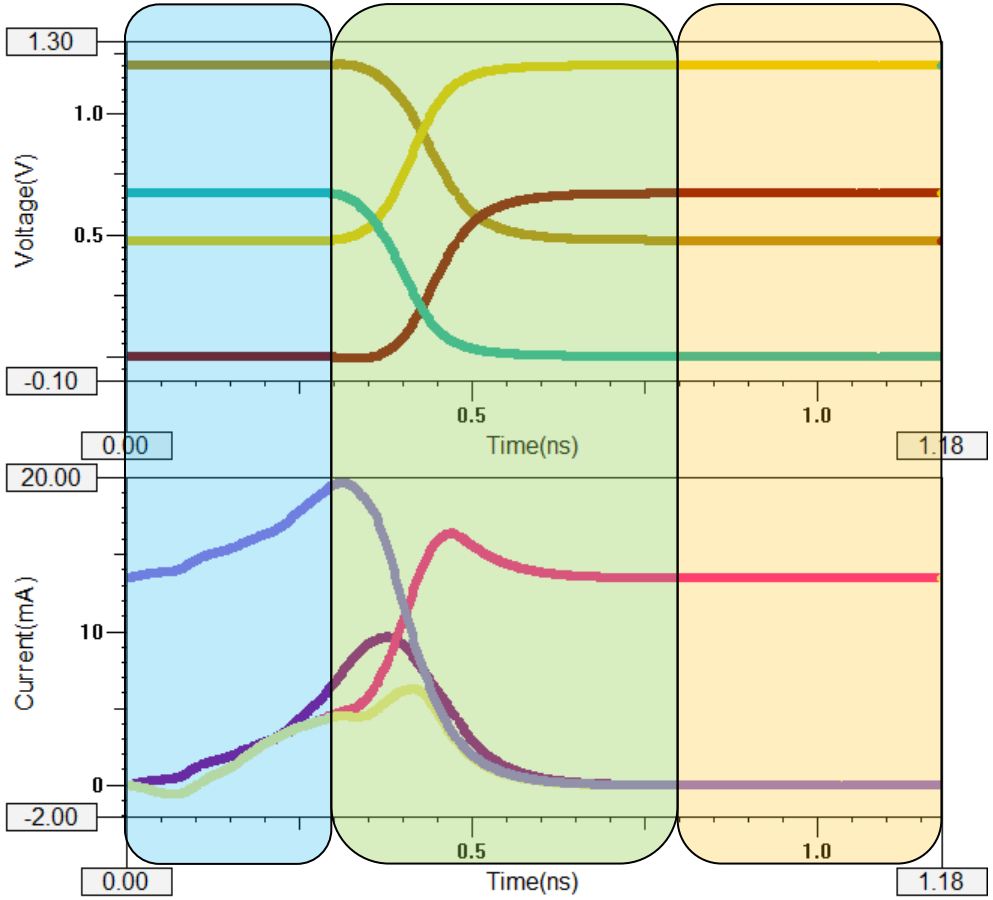


- Not discussed here – we are not trying to impose any restrictions or interpretation of true overclocking

Power Aware IBIS Models

- Two types of waveform tables are used: the classic voltage tables and the (composite) current tables
- The driver voltage transition may be significantly delayed with respect to the pre-driver current
- The two waveform tables need to be recorded in the IBIS file using the same absolute time scale and be time aligned
- The driver voltage transition may be valid for faster bit rates than those corresponding to the overall time span of the combined waveform tables

Typical Combined Waveform Data

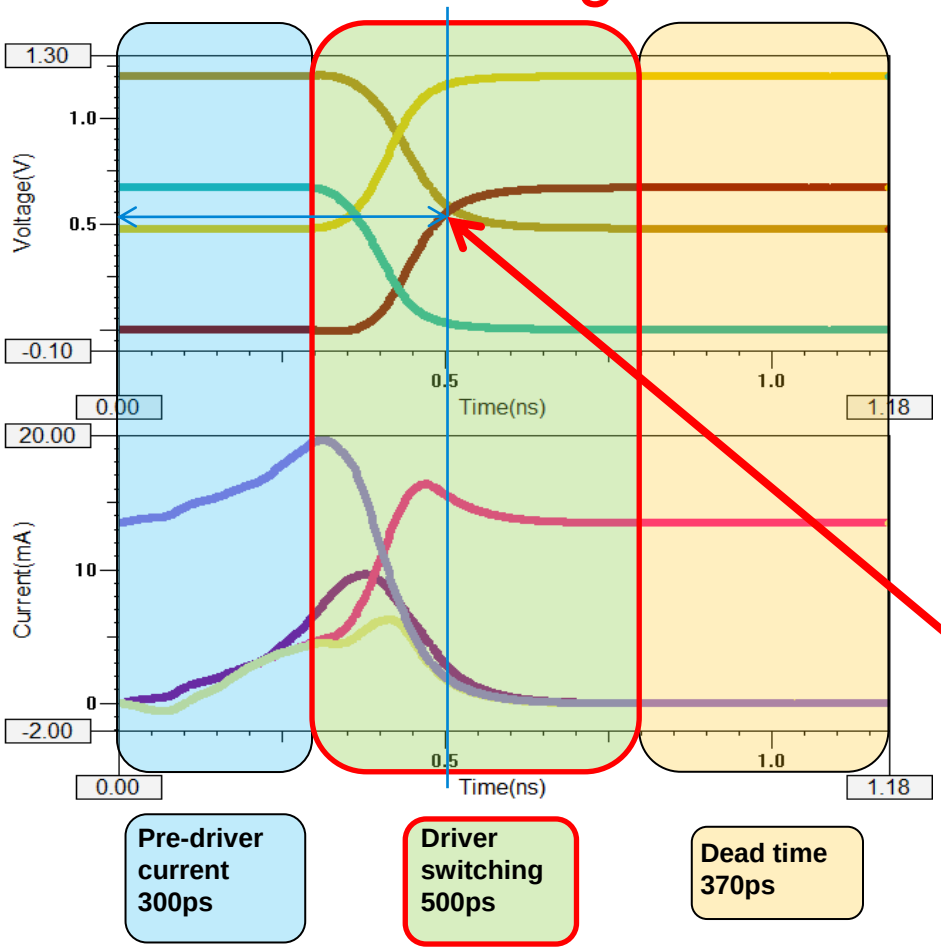


Pre-driver current 300ps

Driver switching 500ps

Dead time 370ps

Fictitious Overclocking in Power Aware Models



- For these waveforms:
  - The Driver switching occurs within a 500ps window.
  - Thus, a bit time of 500ps or greater should not cause true overclocking problems.
  - Fictitious overclocking if delay is not properly handled.

What EDA Platforms Do About It

- Several ways to address it
  - The user can specify the amount of initial delay to ignore
  - Automatically detect the amount of initial delay to ignore
  - Do nothing (no special “windowing” applied)
- Neither of the approaches is correct nor desired
  - Potentially inconsistent simulation results, or
  - Declared “overclocked” operation

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Who the Decision Belongs To

ONLY THE MODEL MAKER KNOWS THE EXACT AMOUNT OF DELAY TO REMOVE

IBIS BIRD 168.1 – “Handling of Overclocking Caused by Delay in Waveform Data”

- Approved for the next version of the IBIS spec (after 6.0)
- Proposes a new keyword under the [Model] keyword

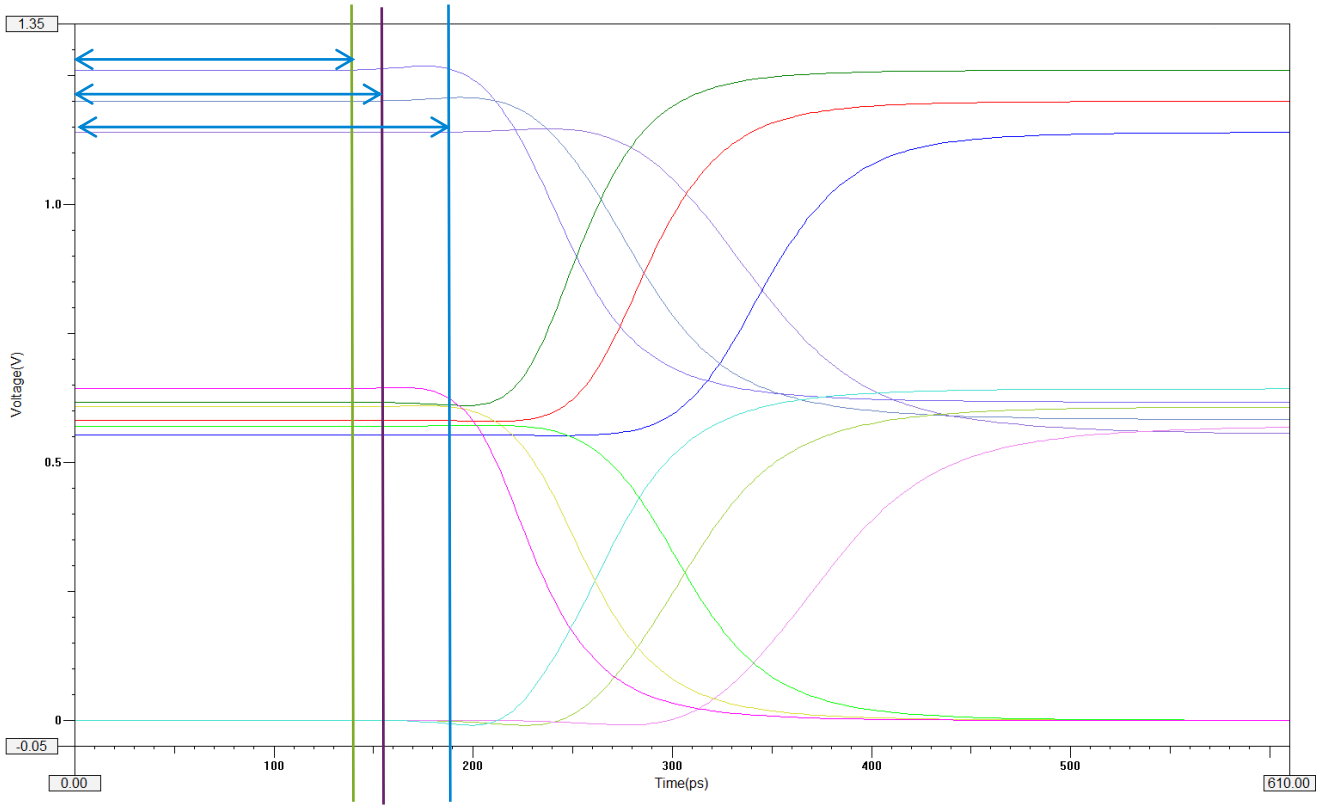
  [Initial_Delay]

- The new keyword is optional
- One or two sub-parameters can be specified

  V-T and/or I-T

http://www.eda-stds.org/ibis/birds/bird168.1.docx

Example of V-T Sub-parameter Data



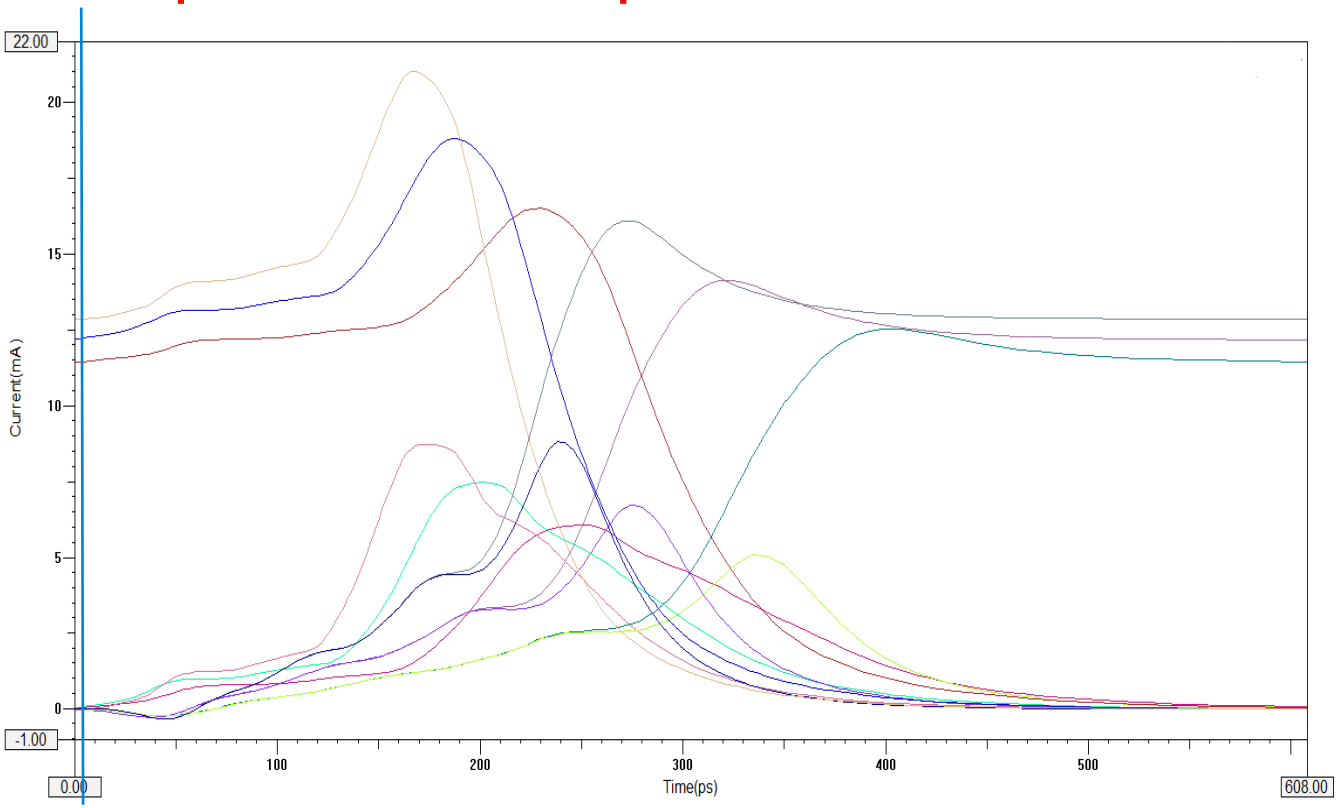
Max corner initial delay = 140ps

Typ corner initial delay = 155ps

Min corner initial delay = 190ps

- The same value of the initial delay specified for V-T sub-parameter applies to all voltage tables in the [Model]

Example of I-T Sub-parameter Data



Min/Typ/Max corner
initial delay = 5ps

- The same value specified for I-T sub-parameter applies to all current tables in the [Model]

How the Initial_Delay Values are Applied

- The initial delay value is first removed (subtracted) from the time values in the first column of the corresponding tables
- The same value is used to delay the trigger events which activate any of the corresponding tables
- This shortens the transition times accordingly, allowing higher bit rate signals to be properly simulated
- Following the specified initial delay values will make the simulation results consistent across all EDA platforms

Example of Specifying Initial Delay in an IBIS File

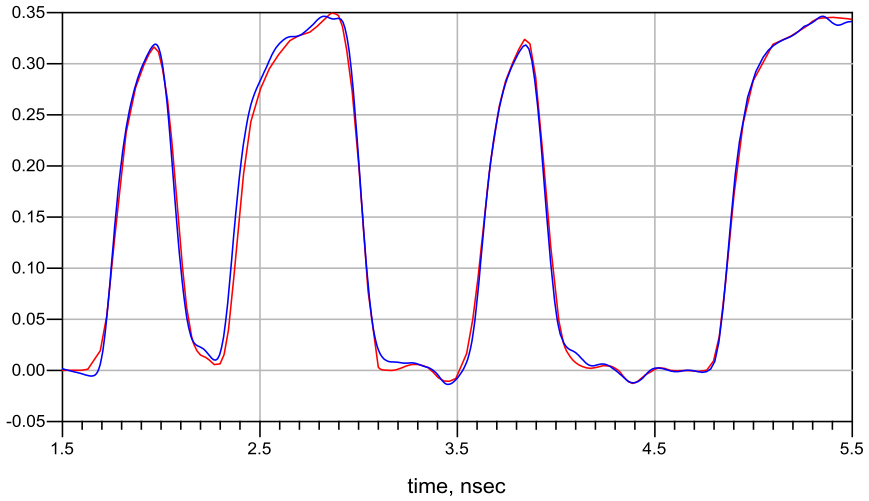
```
[Model]

   [Initial Delay] | This keyword specifies removable delay(s)
   | time table       typ             min             max
     V-T             0.20e-9         0.22e-9         0.18e-9
     I-T             0.05e-9         NA              NA
```

- Up to three columns with three IBIS corner values

Example: LPDDR4 3200Mbps

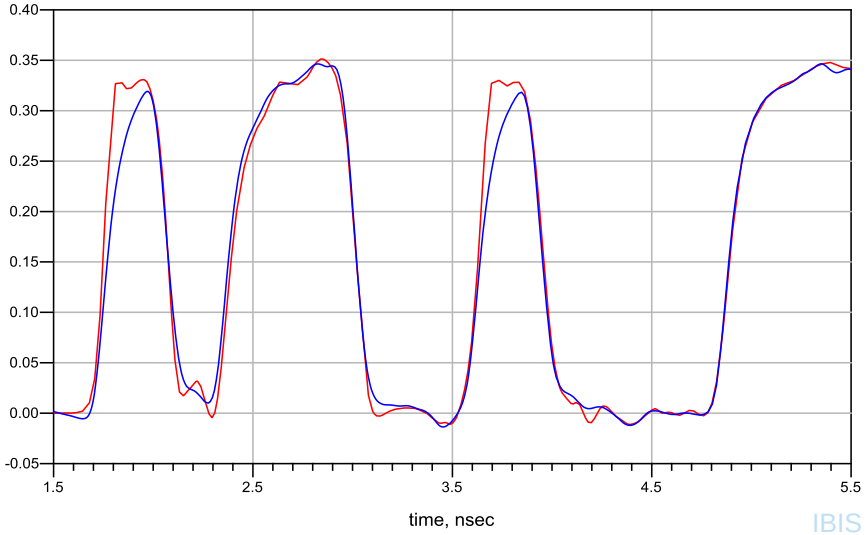
- UI = 312.5ps
- Duration of the waveform tables = 920ps

Multiple Triggers



IBIS
Spice

Single Trigger



Summary

- A new keyword will be added to the next version of the IBIS spec
- It will unify the way the initial delay is handled, making the simulation results consistent across different EDA tools
- It adds complexity to the triggering algorithms inside of the EDA simulator tools for the benefit of the IBIS model users