Correlation between IBIS5.x and SPICE
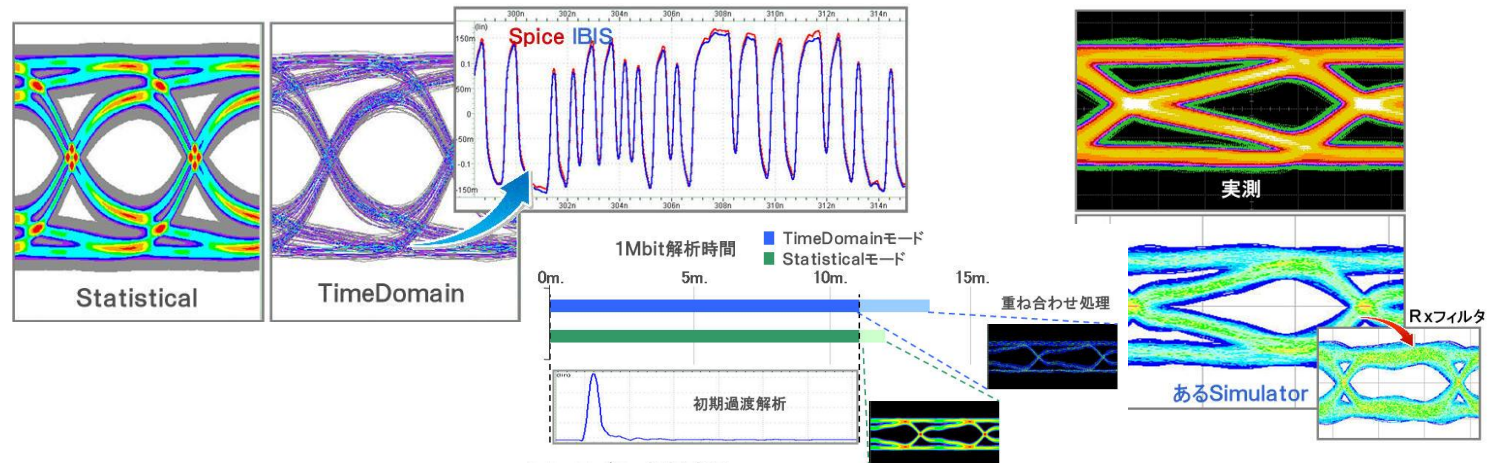
Asian IBIS Summit
Yokohama, JAPAN
November 22,2013
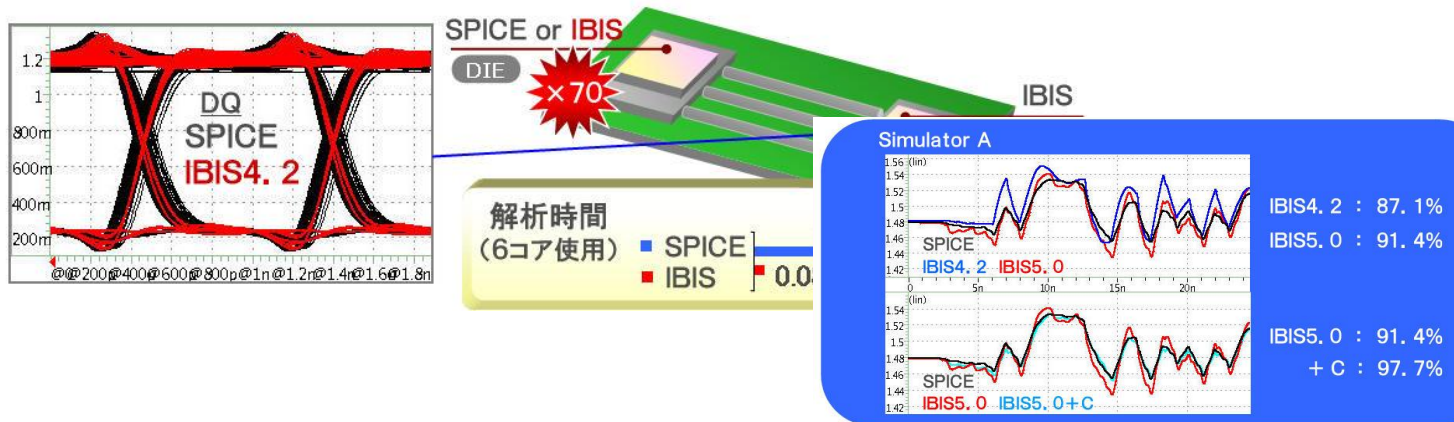
Ricoh Company, Ltd.

MDS Development Section

MIM Technology Development Department

ICM Development Center

R&D Group

Kazuki Murata

2013/11/22
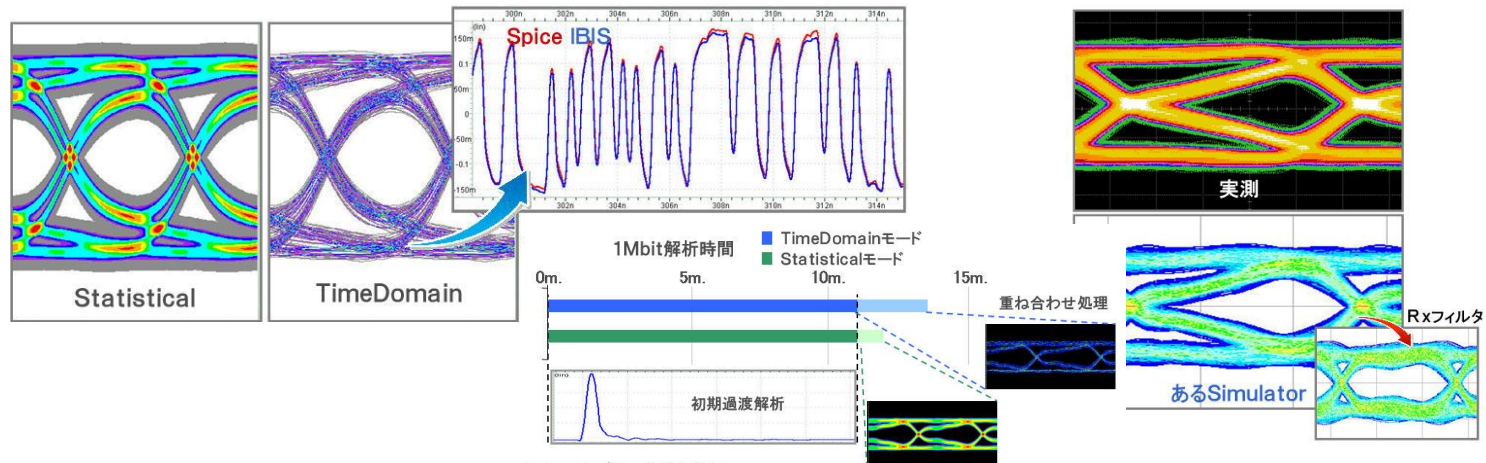
Contents

RICOH
imagine. change.

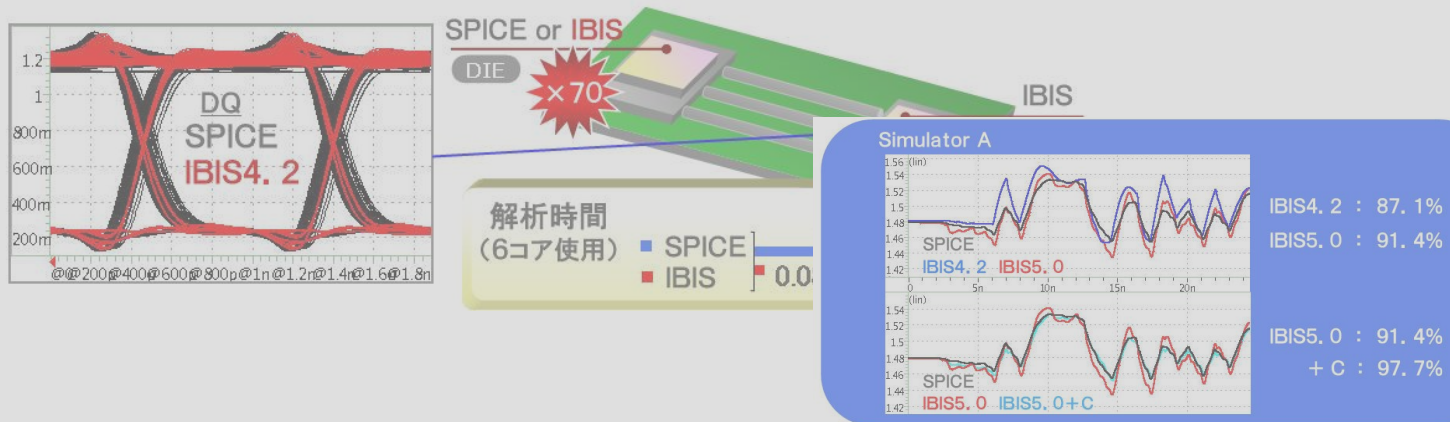## 1. Correlation between IBIS-AMI and SPICE

2. Accuracy of SSO analysis using IBIS5.1

Contents

1. Correlation between IBIS-AMI and SPICE

2. Accuracy of SSO analysis using IBIS5.1

Current trends of SI simulation

RICOH
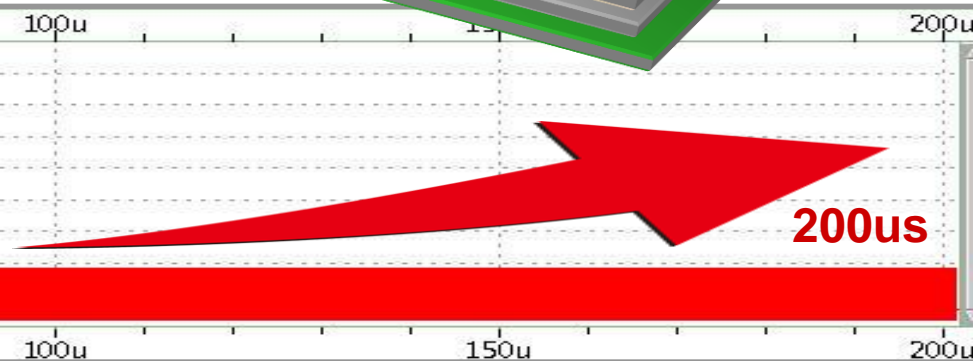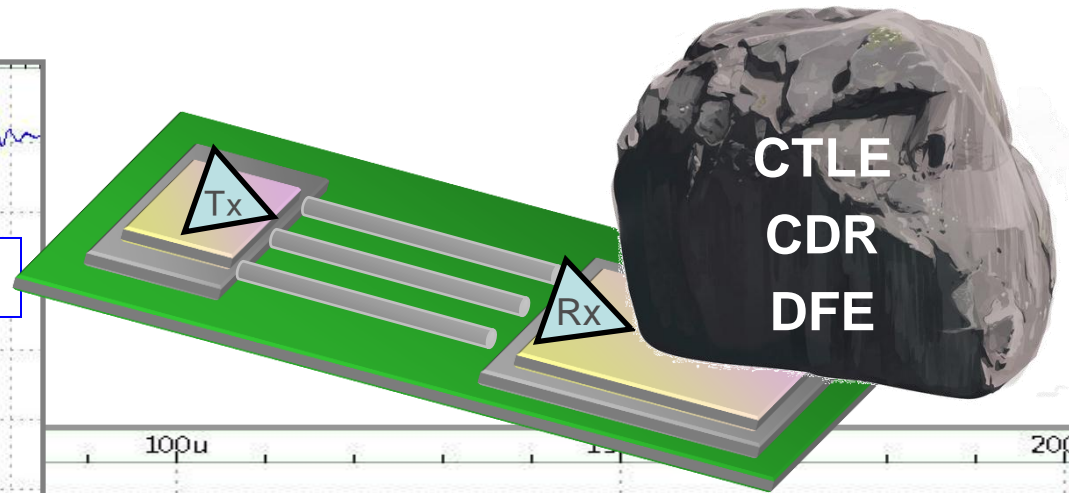imagine. change.
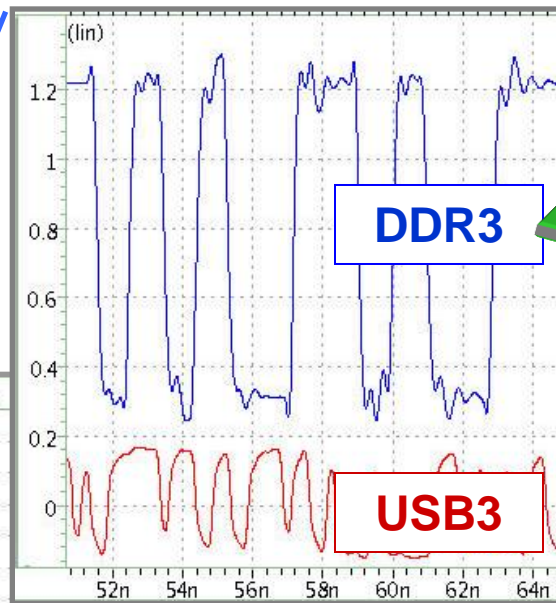
SI simulation time

DDR3_1066 : 400bit (200tCK) = 200**n**sec

USB3.0 : 1,000,000bit = 200**u**sec x1k

Simulation models

To perform SERDES simulation, CDR and EQ models are also required.

DDR3

USB3

CTLE
CDR
DFE

Tx

Rx

200ns

200us

4

IBIS-AMI and simulation method

RICOH
imagine. change.

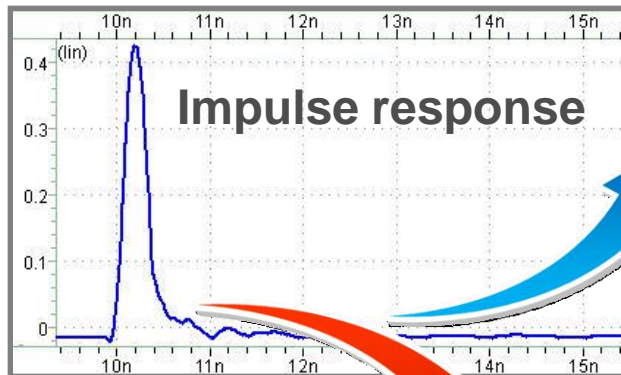**IBIS-AMI 'Algorithmic Modeling Interface'**

Can increase in simulation speed by convolution.

Can implement characteristic of CDR and EQ.
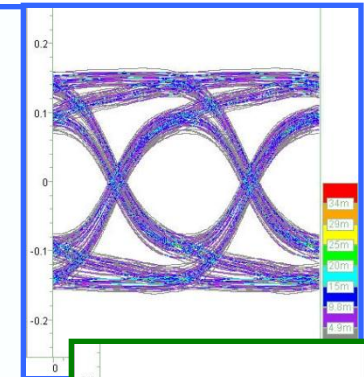
Simulation method

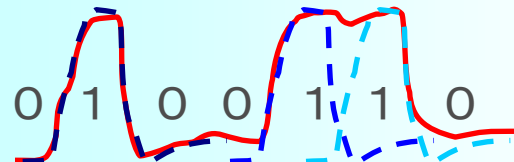Various EDA tools can support IBIS-AMI now.

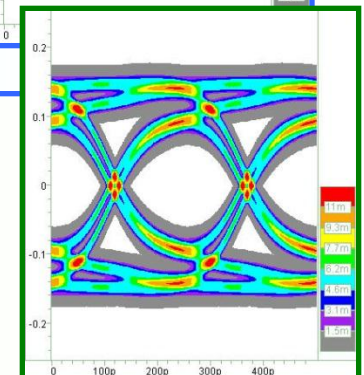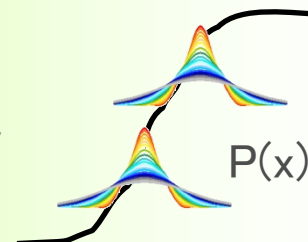Make any number of bits Eye diagram from impulse response.

Impulse response

Time domain mode

Using Superposition technique.

0 1 0 0 1 1 0

Statistical mode

Using probability density function.

P(x)

5

Subject

RICOH
imagine. change.

Correlation between IBIS-AMI model and SPICE model.

'De-facto standard SPICE simulator + SPICE model' gives golden result.

Good correlation between legacy IBIS and golden result is well known.

Then, how about IBIS-AMI model ?

The results with several EDA tools are equal to one another ?

Interpretation of IBIS depends on EDA tools.

Four simulators show the same result ?

(Using latest version as of 2013.08)

Actually, IBIS-AMI can be useful ?

Application examples of IBIS-AMI simulation.

Can we apply IBIS-AMI simulation to practice ?

How long Simulation time we can reduce?

Method of Correlation
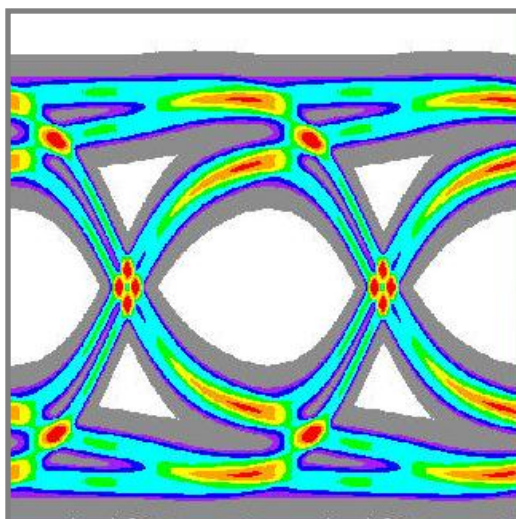
RICOH
imagine. change.

Simulation model

Ricoh's SERDES Tx SPICE model.

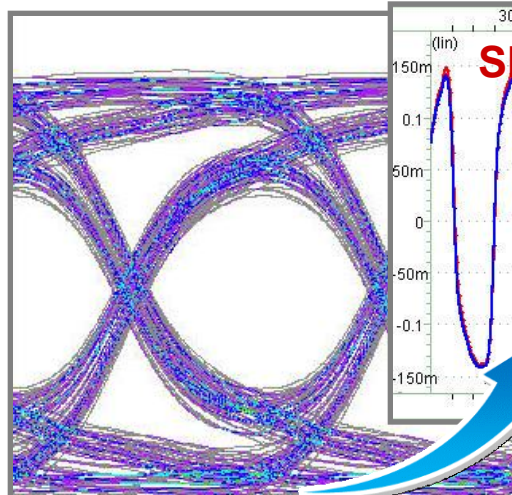IBIS-AMI is modeled on the SPICE.

Curve Overlay Metric (FOM)

IBIS Open Forum I/O Buffer Accuracy Handbook p.13

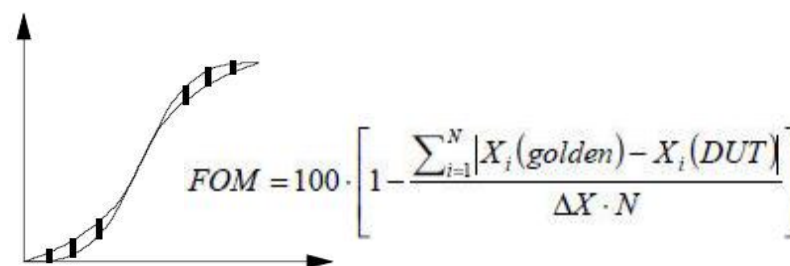Obtain continuous time domain waveforms in time domain mode.

Statistical mode

Time domain mode

(w/o continuous time domain waveforms)

$$FOM = 100 \cdot \left[1 - \frac{\sum_{i=1}^{N} |X_i(golden) - X_i(DUT)|}{\Delta X \cdot N} \right]$$

   7
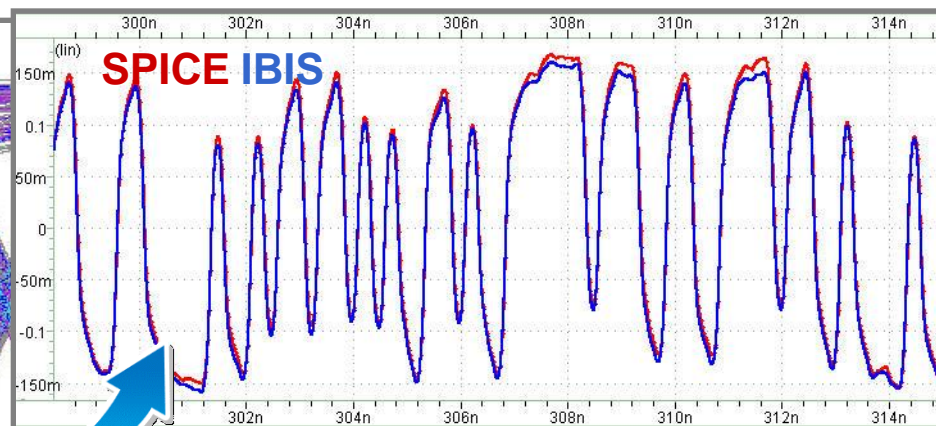
Results 'Tx Waveforms'

Simulator A 99.0%

SPICE

AMI

Simulator B 98.8%

SPICE

AMI
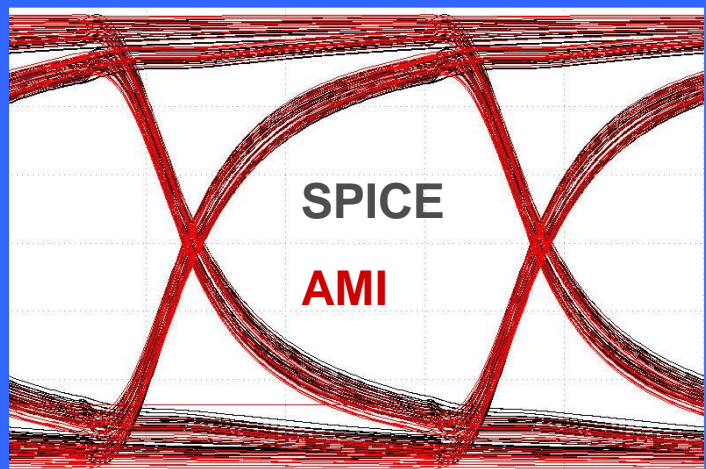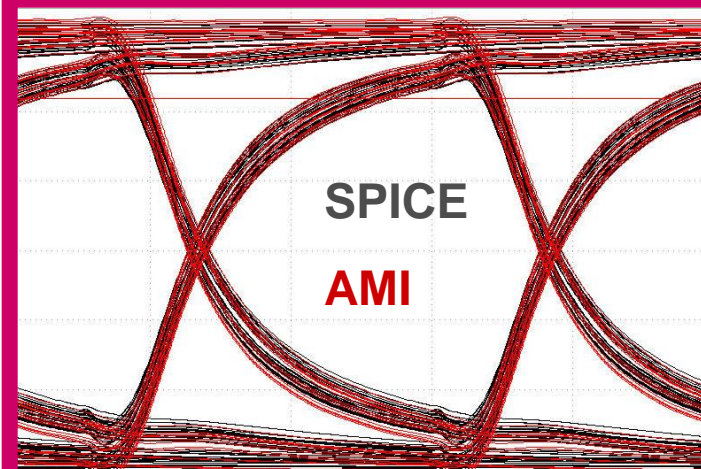
Simulator C can not generate transient waveforms.

SPICE

AMI

Simulator C N/A

SPICE

AMI

Simulator D 98.6%

Correlation between IBIS5.x and SPICE

Application examples
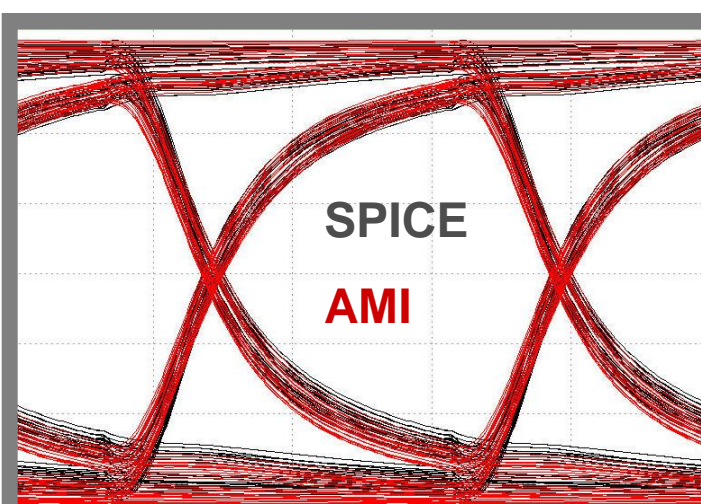
RICOH
imagine. change.

Summary

Transmission lines including PKGs, PCBs, connectors and cables were modeled.

Run 1M bits simulation using these models and SERDES IBIS-AMI on various Tx emphasis level.

Probe point : Rx Chip's Pin vs. measurement.

Ricoh's Chip in MFP
Giga bits SERDES
Emphasis, Equalizer

Probe point : Rx CTLE output
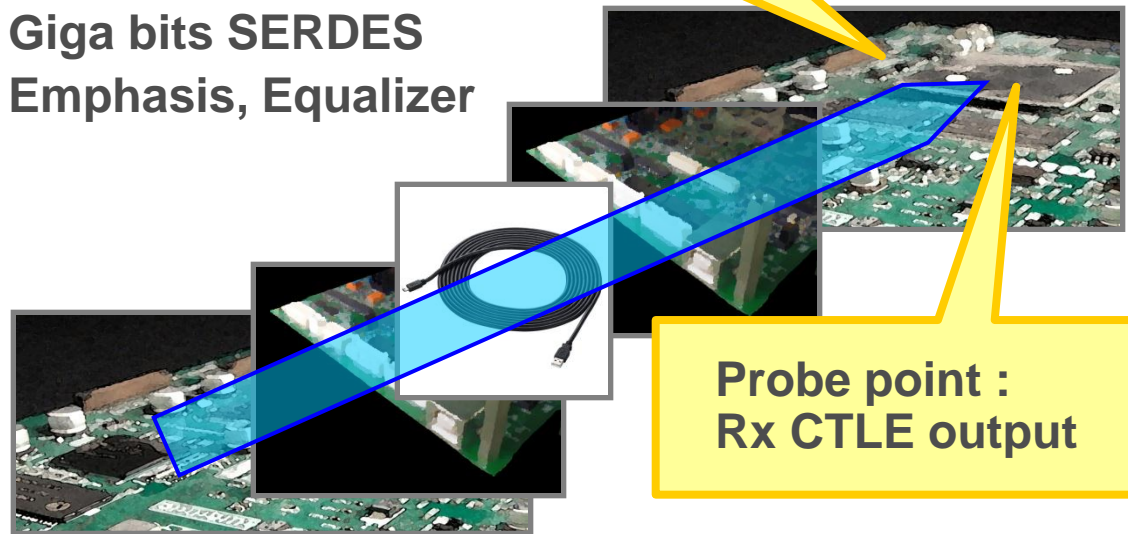
Measurement correlation

Measurement correlation

w/o Emphasis

Measurement

Simulation

Rx Filter

w/ Emphasis

Measurement

Simulation
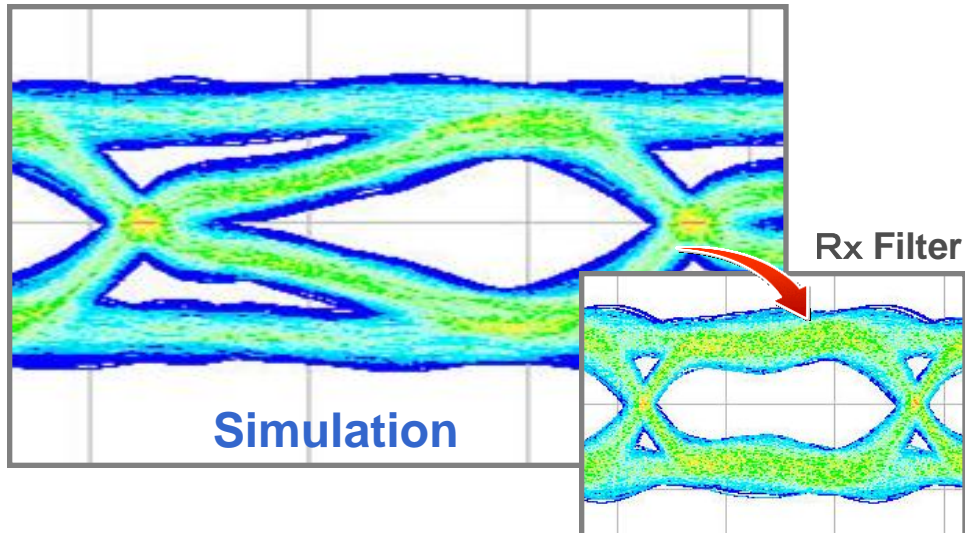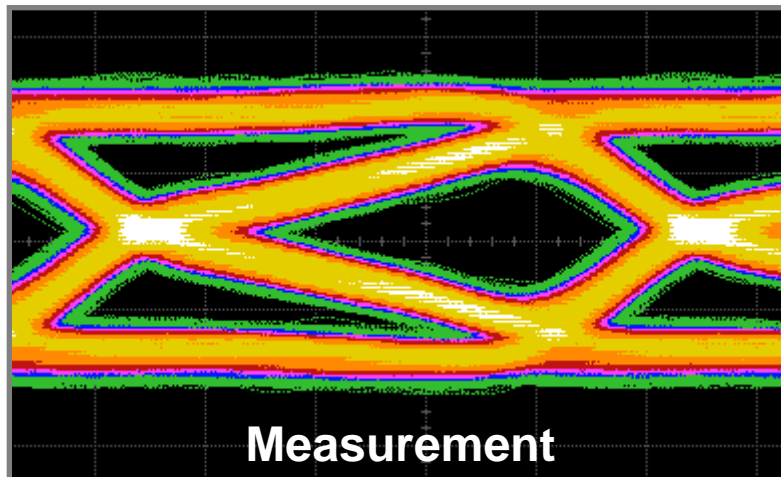
Simulation time
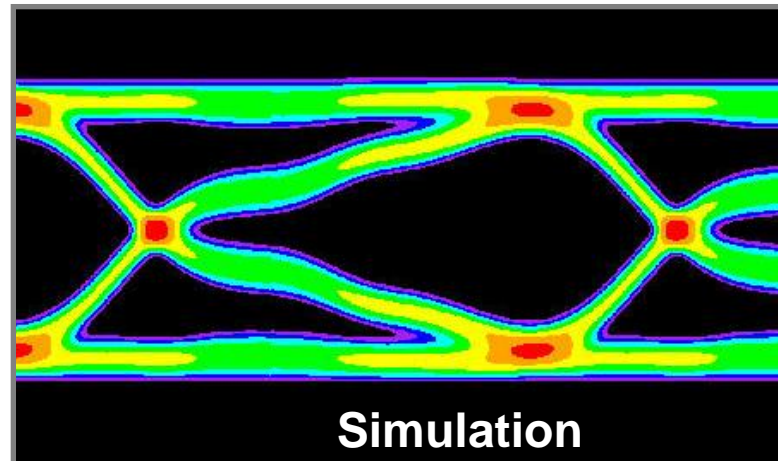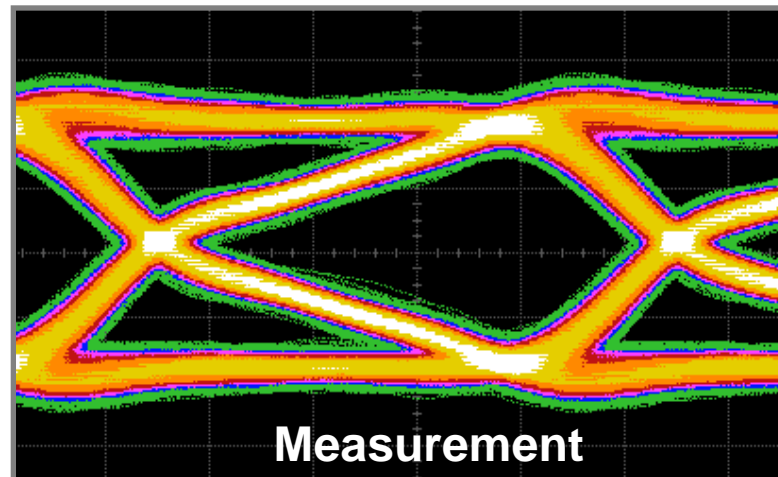
RICOH
imagine. change.

Simulation with IBIS-AMI in simulator A

Much shorter than typical transient simulation.

It took several min to perform 1M bits simulation.

Statistical mode is faster since superposition technique is unnecessary.

Similar result in any simulator

■ **Time domain mode**
■ **Statistical mode**

1M bits simulation Time

0m.   5m.   10m.   15m.

Superposition technique

Impulse response
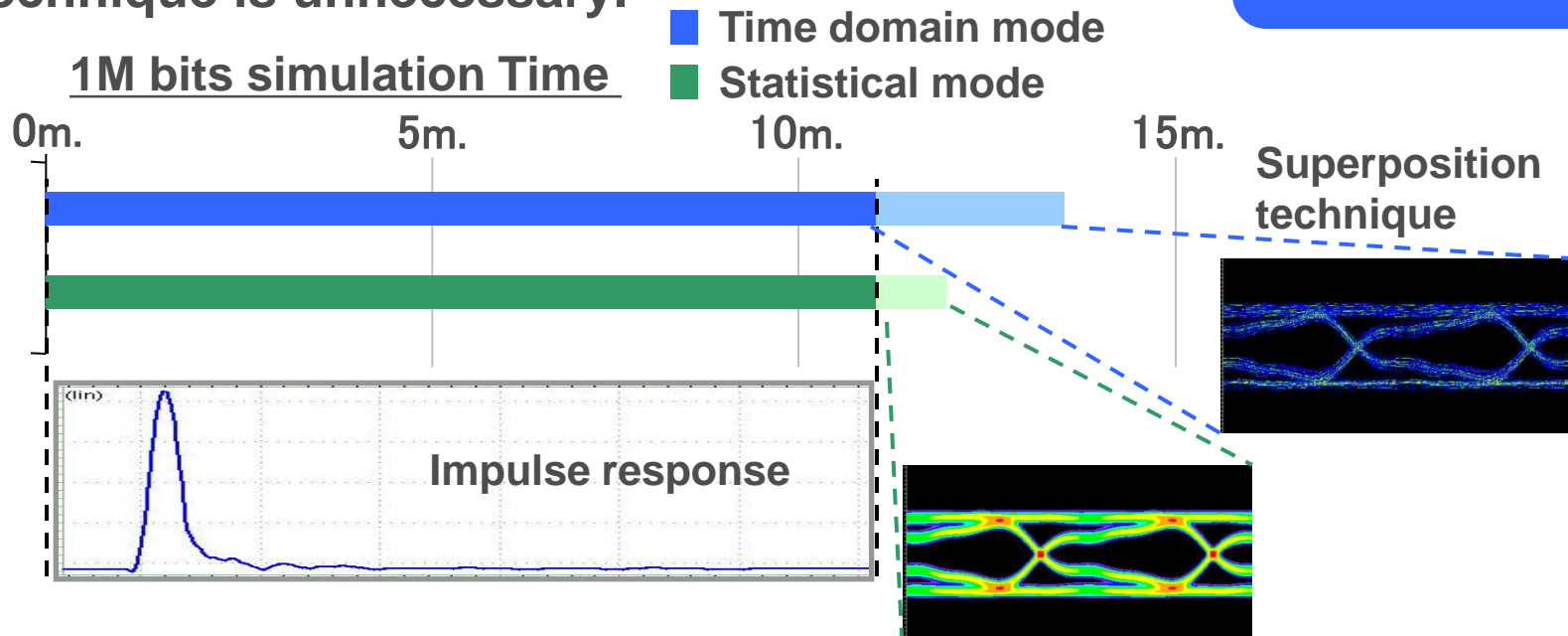
Simulation with SPICE model

Haven't finished after 60 hours.

It will finish in 2.8 years.

Conclusion

RICOH
imagine. change.

IBIS-AMI vs. SPICE

IBIS-AMI model is highly correlative with SPICE model.

Difference between simulators

According to this result, difference between simulators is not recognized.
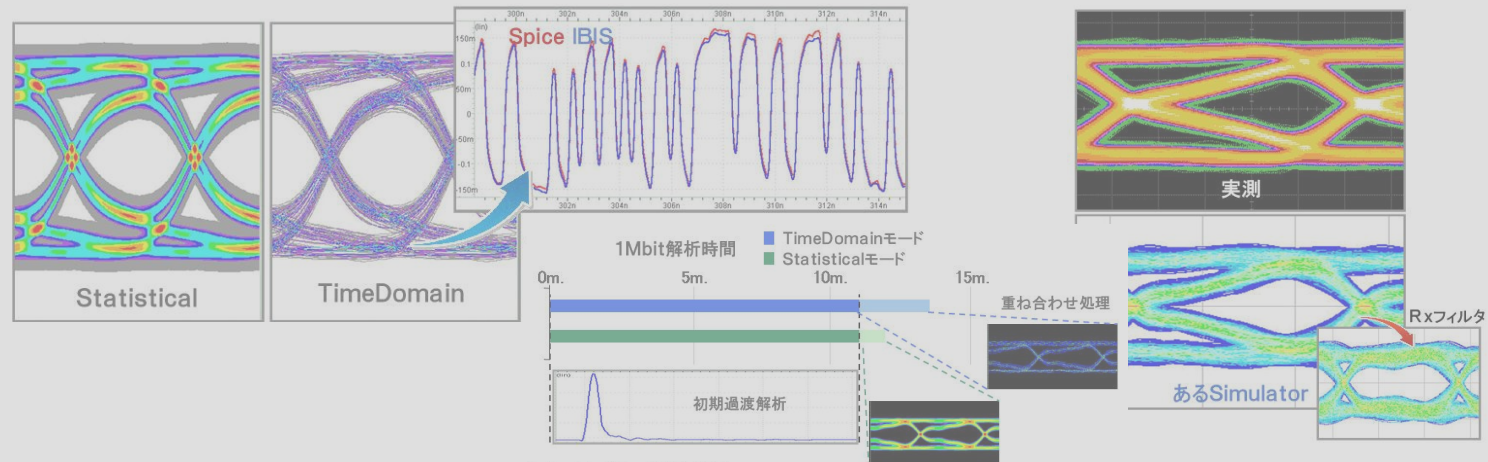
Application examples

Simulation result using IBIS-AMI is highly correlative with measurement.

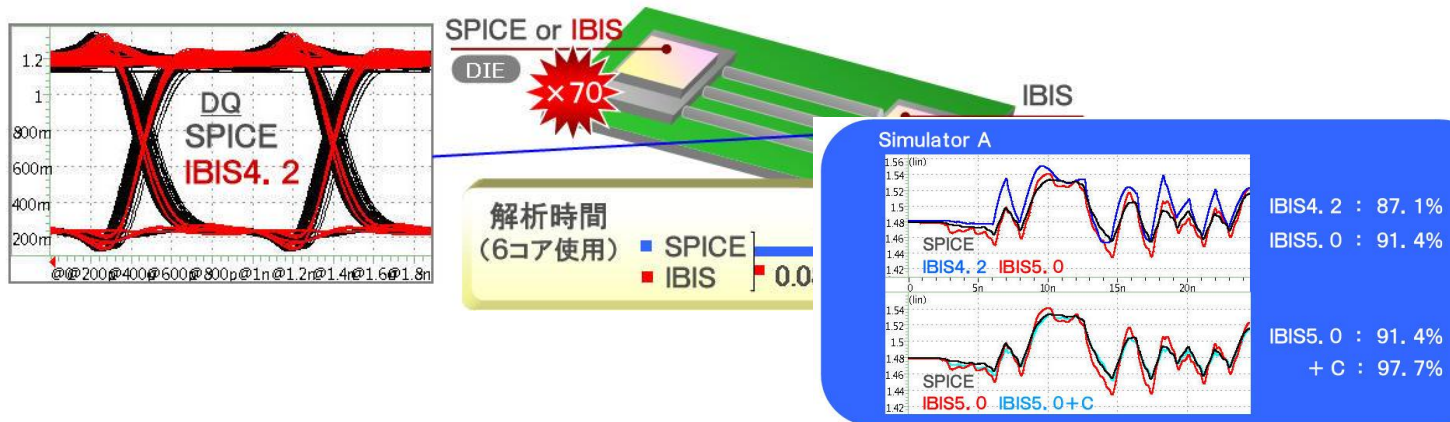Simulation time using IBIS-AMI is much shorter than typical transient simulation time.

Contents

RICOH
imagine. change.

1. Correlation between IBIS-AMI and SPICE

2. Accuracy of SSO analysis using IBIS5.1

13

Actual condition of SSO sim.

RICOH
imagine. change.

Examples of DDR3 SI simulation with SPICE

To simulate SSO noise, use 70 SPICE models.

SPICE **x70**
DIE

S-parameter
PKG

IBIS
DRAM

W-element
Bord

Simulation time

	0h.	12h.	24h.
4cores			
6cores			
8cores			

1day

Sim.

Measurement
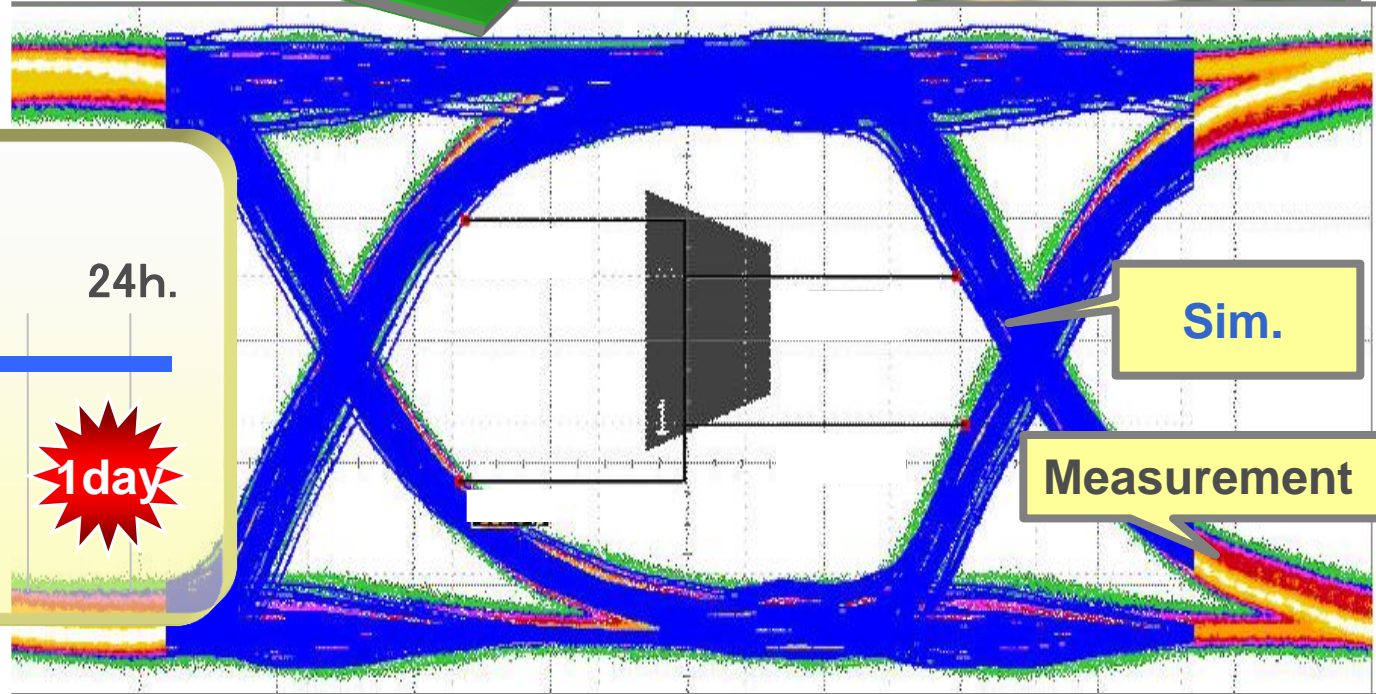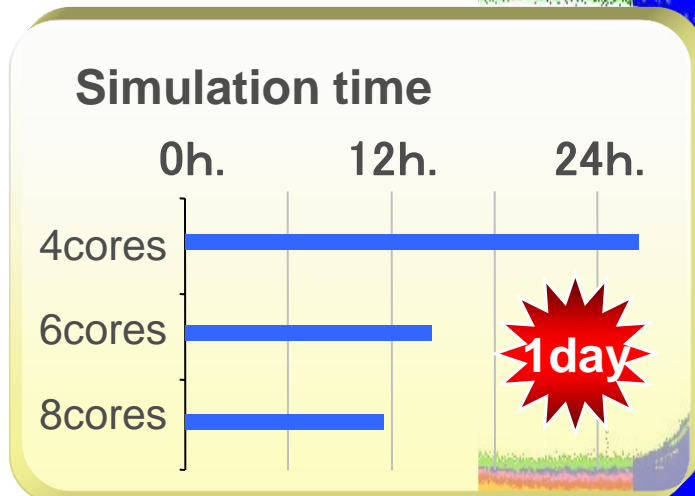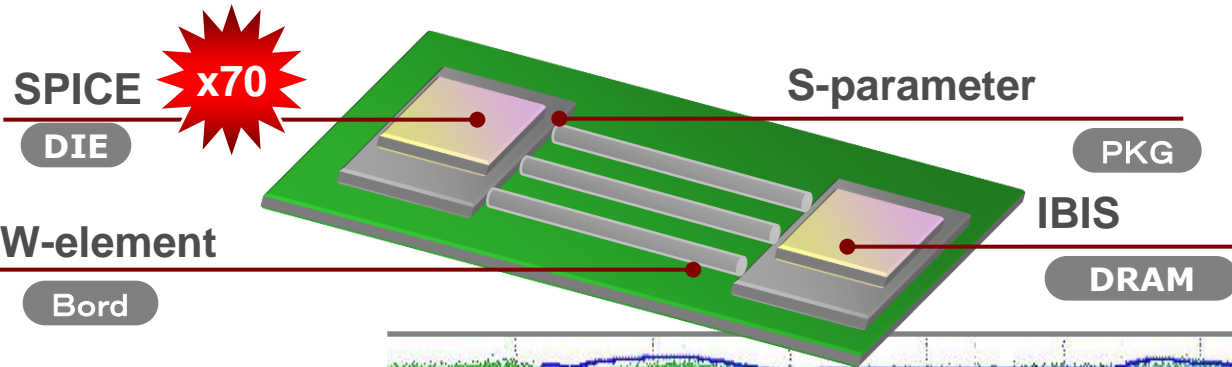
[ISSO] [Composite Current]

RICOH
imagine. change.

IBIS4.2

Simulation speed is over ten times faster than SPICE, but SSO noise can't be represented.

SPICE or **IBIS**

DIE

×70

IBIS

DRAM

Simulation time
- SPICE
- IBIS   0.08

0.5   1

×12
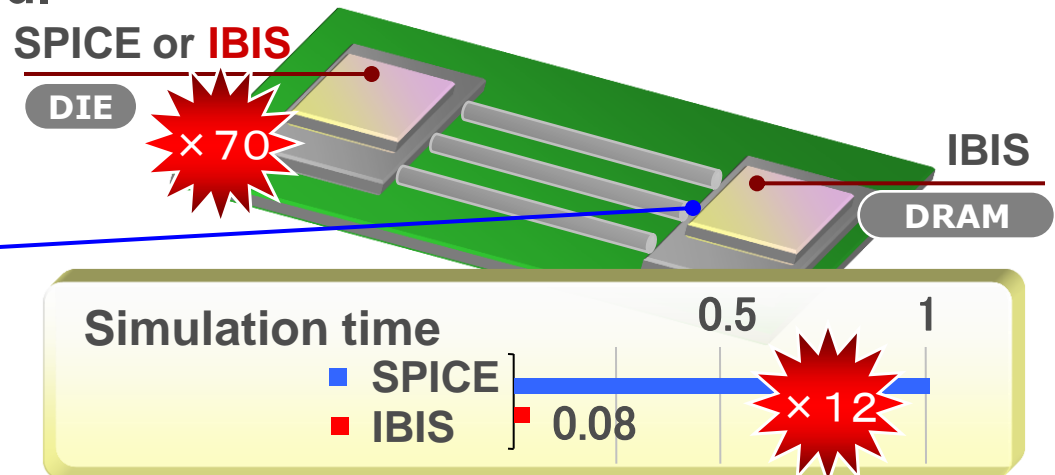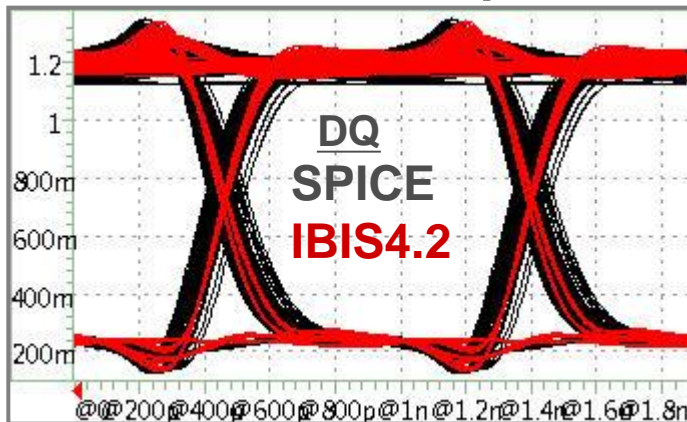
IBIS5.x

Added current waveforms and influence of SSO noise on drivability.

IBIS5.x

[ISSO_PU]

i [Composite Current]

IBIS4.2   [Pullup]   [POWER Clamp]   [Waveform]

[Pulldown]   [GND Clamp]

[ISSO_PD]

Subject

RICOH
imagine. change.
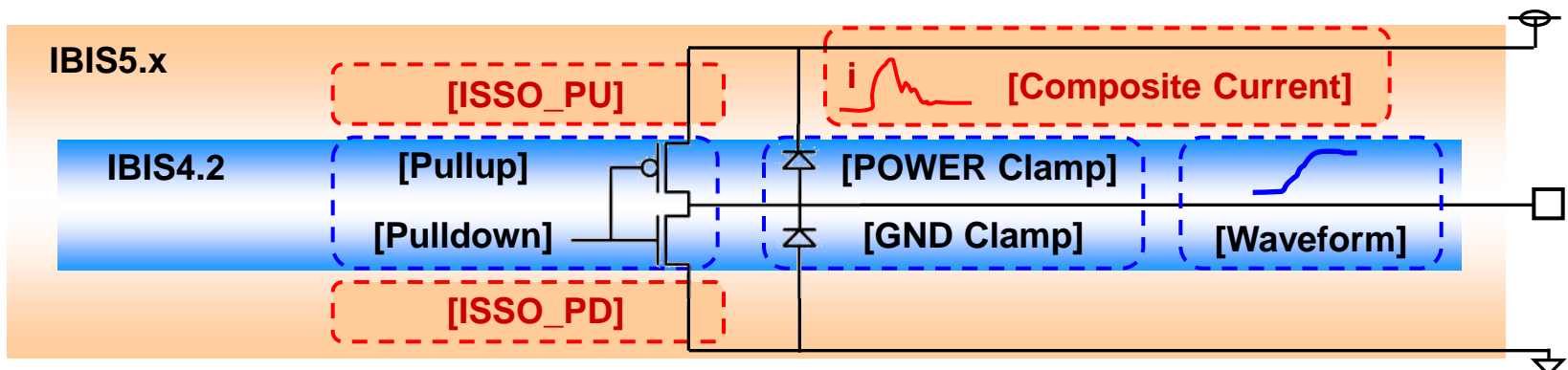
SSO noise can be represented by IBIS simulation ?

'De-facto standard SPICE simulator + SPICE model' gives golden result.

Current waveform is equal to golden results ?

SSO noise is equal to golden result ?

SSO noise can affect IBIS waveforms ?

It is difficult to simulate SSO noise with IBIS4.2.

Added keywords [ISSO_PU] [ISSO_PD] from IBIS5.0.

IBIS waveform under an influence of SSO noise is equal to golden result ?

Actually, IBIS5.x can be useful ?

 16

Method of Correration

RICOH
imagine. change.
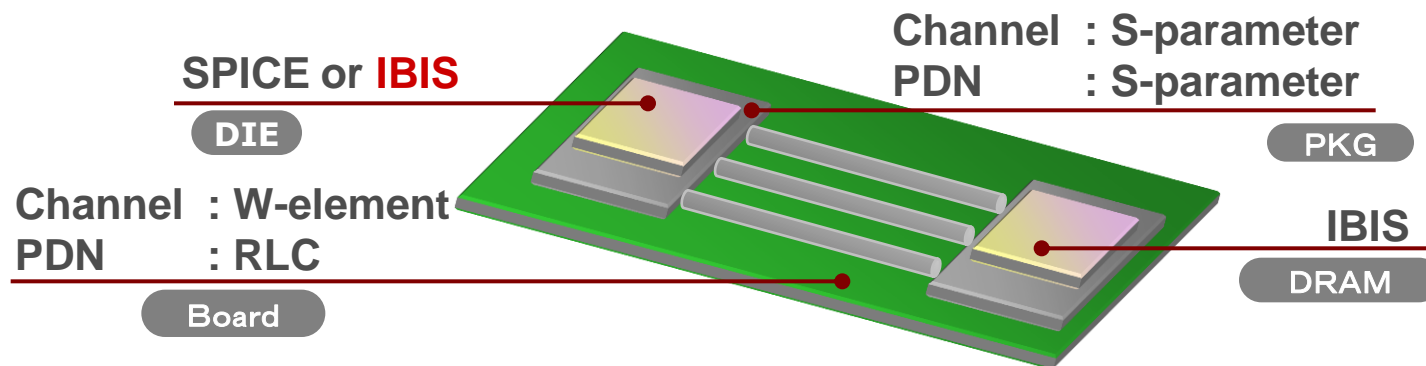
Simulation model

SPICE model : DDR3_SSTLIO

IBIS5.1 is modeled on the SPICE.

 (0 Error & Warnings in IBISCHK5.1.4)

Extract S-parameter for PKG model by 2.5D field solver.

PCB transmission lines are W-element.

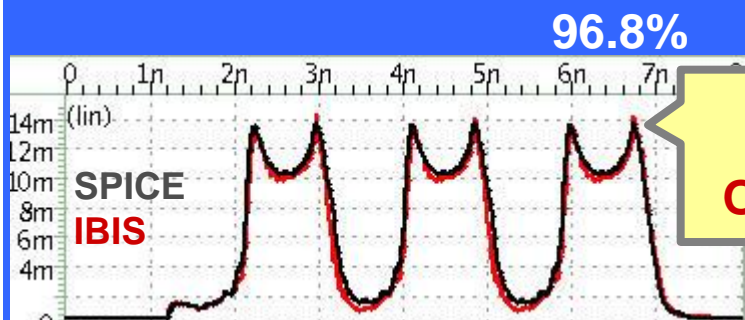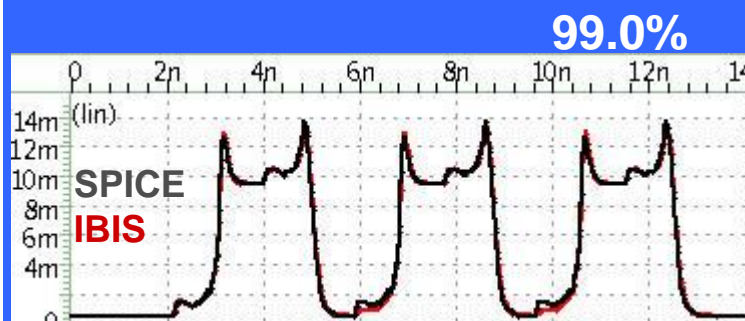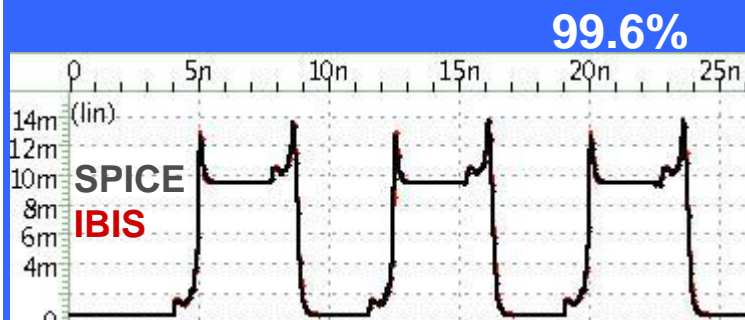Extract RLC for PCB's PDN model.

Channel : S-parameter
PDN   : S-parameter

SPICE or IBIS

DIE

PKG

Channel : W-element
PDN   : RLC

IBIS

Board

DRAM

Curve Overlay Metric (FOM)

IBIS Open Forum I/O Buffer Accuracy Handbook p.13

Result 'Current waveforms'

RICOH
imagine. change.

Simulator A

Ideal power

Simulator B

99.6%

97.8%

99.0%

98.0%

96.8%

81.6%
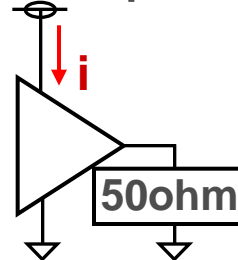
133MHz

266MHz

533MHz

50ohm
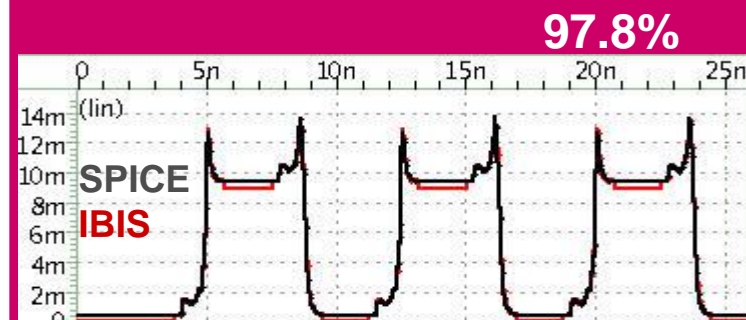
Low accuracy.

Over Clocking ?

(C)2013 Ricoh Company, Ltd. All Rights Reserved.

18

Problems

RICOH
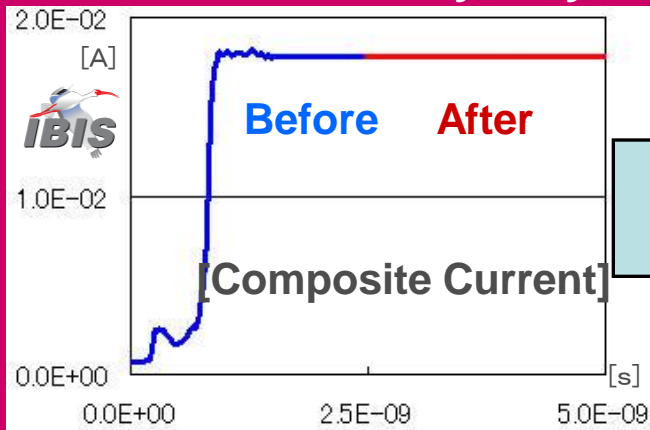imagine. change.

Accuracy of current waveforms and Over Clocking problem

Accuracy of supply current depends on simulators and conditions.

DC discontinuity only occurs in simulator B.

IBIS

Before   After

[Composite Current]

After

Before
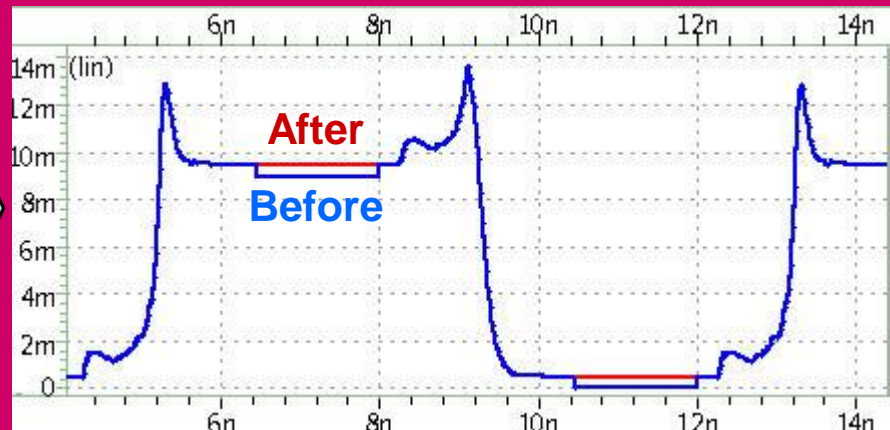
Over clocking occurs notably in simulator B.

[Composite Current]

IBIS

Short delay   Long delay

1Gbps

Long delay   0.5Gbps   1Gbps

Short delay

Result 'SSO noise'
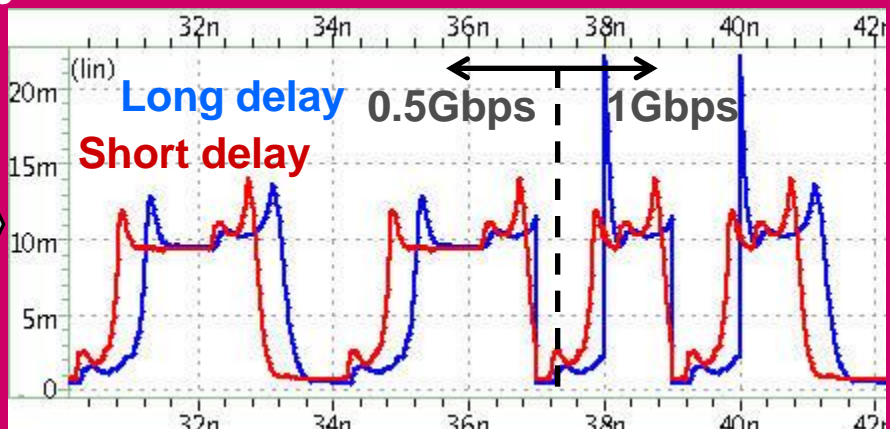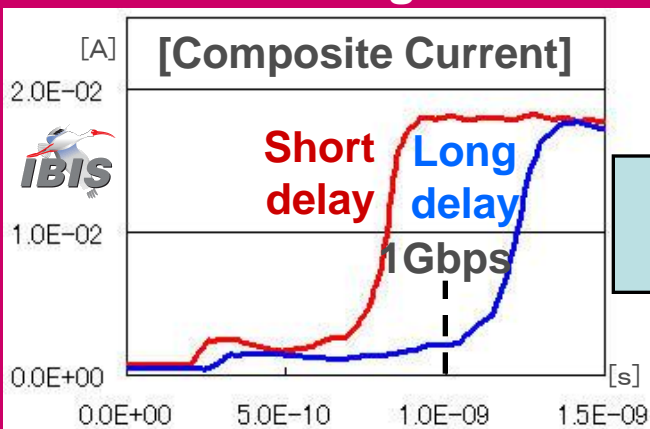
RICOH
imagine. change.
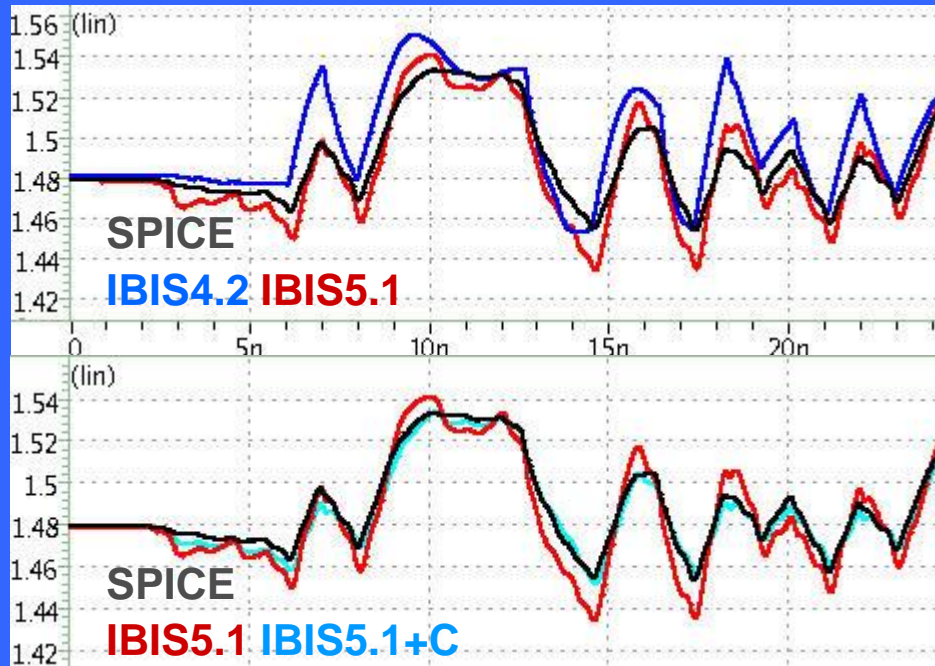
Simulator A

IBIS4.2 : 87.1%

IBIS5.1 : 91.4%

IBIS5.1 : 91.4%

+ C : 97.7%

Voltage controlled capacitor
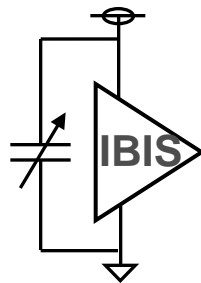
IBIS

SPICE or IBIS

DIE

x70

Power

IBIS

DRAM

Result 'Output voltage waveforms'

RICOH
imagine. change.

Simulator A   CLK

Low score.

SPICE
IBIS4.2 : 97.9%
IBIS5.1 : 97.9%

Simulator A   CLK   tJit(per)

SPICE
IBIS4.2
IBIS5.1

Trigger

1.00
0.15
0.18

Problems

RICOH
imagine. change.
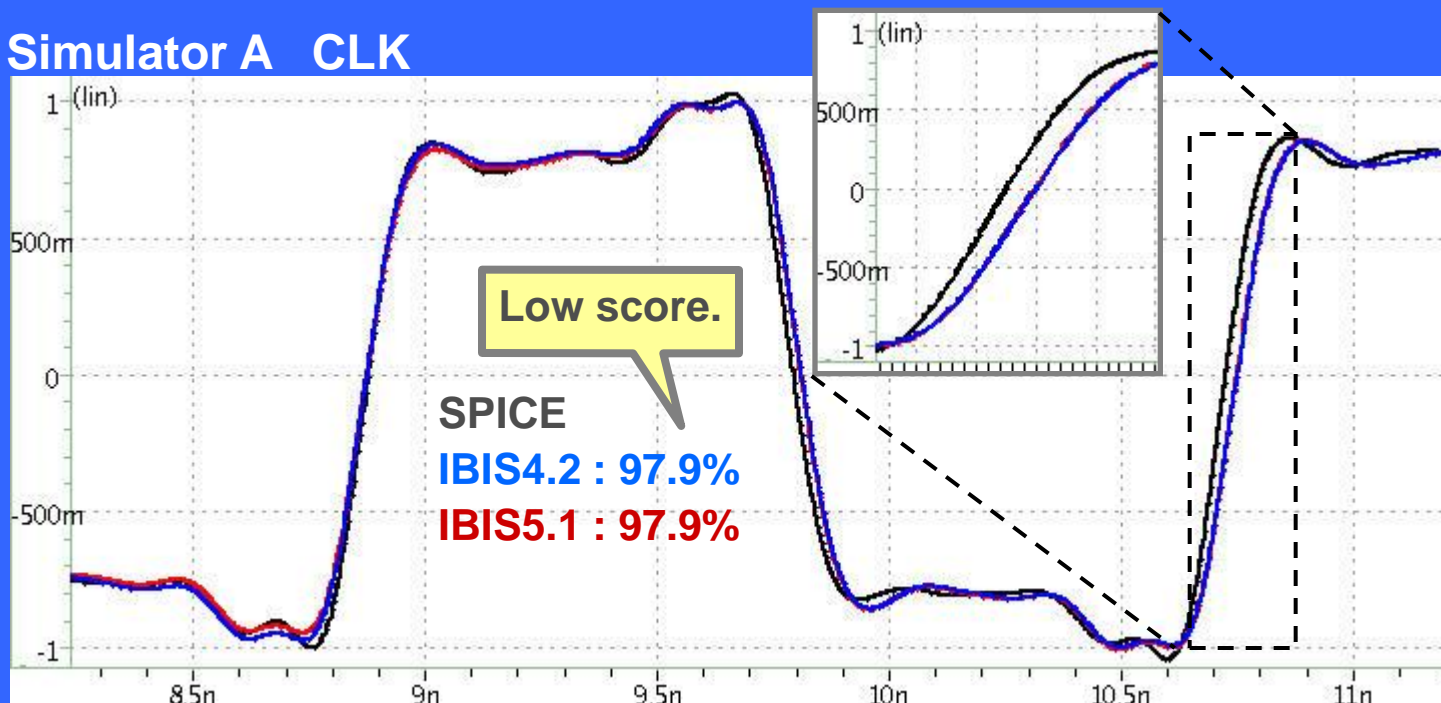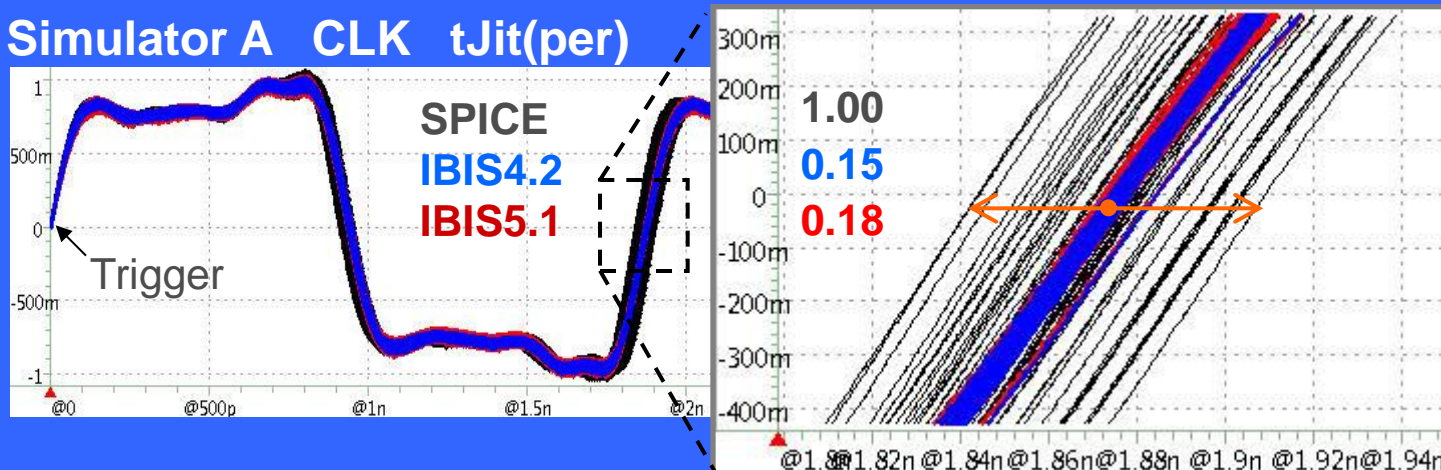
Representation of 'Jitter'

Both IBIS4.2 and IBIS5.x can not represent jitter due to SSO.

There is no IBIS keyword associates output waveforms with SSO noise in time domain. (the modeling is very hard.)

But, CLK jitter of DDR3 is mainly due to SSO noise, and therefore SSO noise cannot be ignored in simulation.

I hope to overcome this difficulty with IBIS

Jitter due to SSO

Conclusion

RICOH
imagine. change.

Accuracy of SSO noise

IBIS Keywords added from IBIS5.0 provide accuracy improvement of SSO noise.

Voltage controlled capacitor makes further improvement, and SSO analysis with IBIS model is equivalent with SPICE model.

Accuracy of output waveforms

SSO noise does not affect IBIS output waveforms.

In particular, IBIS model can not represent jitter, therefore FOM became low score.

Problems

Current waveforms in a certain simulator is low accuracy. Further improvement is desired.

SSO analysis with IBIS model has accuracy problems.

RICOH
imagine. change.

Thank you.