An Advanced Behavioral Buffer Model With Over-Clocking Solution

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Agenda

1. SPICE Model and Behavioral Buffer Model
2. Over-Clocking Problem in IBIS
3. Proposed Solution and Results

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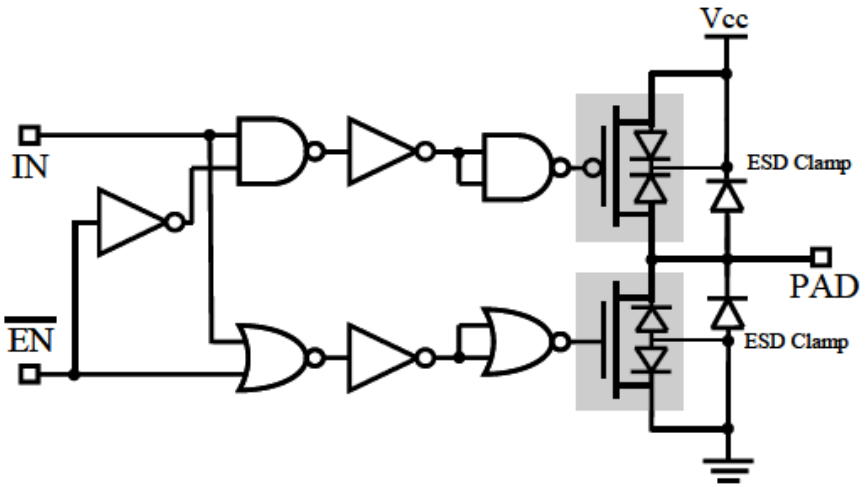
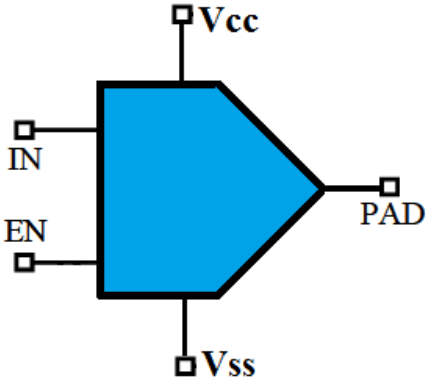
SPICE Model and Behavioral Buffer Model

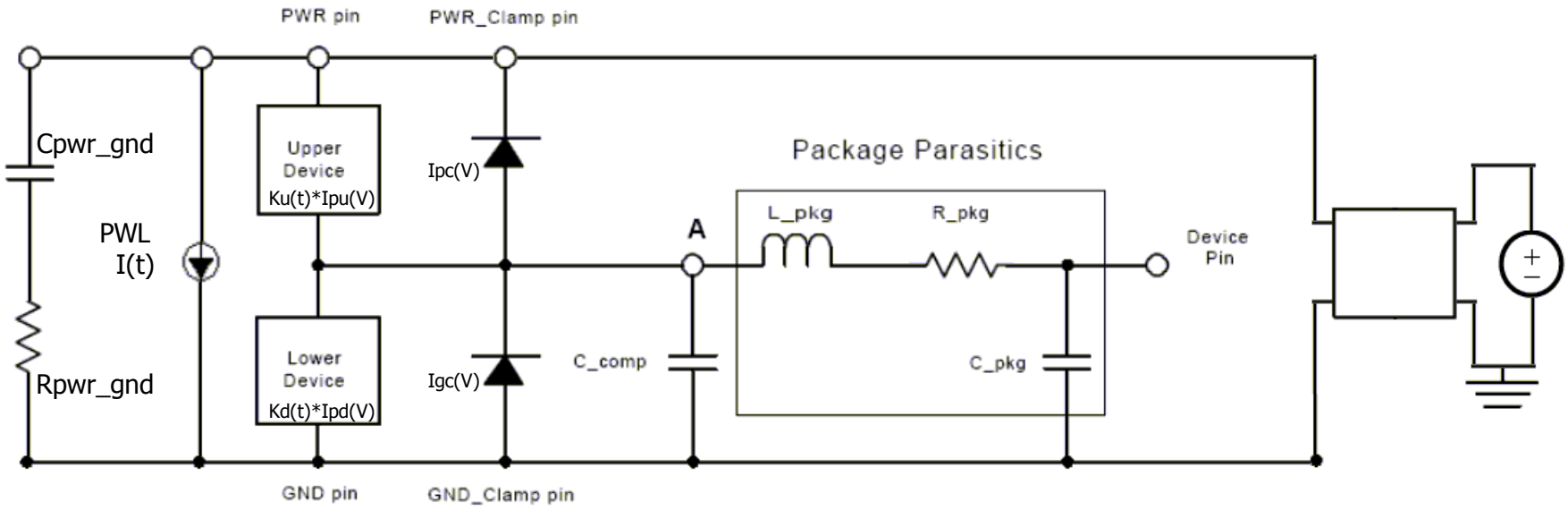
- SPICE model is a circuit netlist at transistor level, it contains detailed information about the circuit design and process parameters.
- Behavioral model is a black box model with certain terminal information, which is obtained from measurement or extracted from SPICE model. IBIS is a widely adopted standard behavioral model.





A Simple Schematic for IBIS Model

- The non-linear behavior of pullup, pulldown and clamps are described by I/V tables, and modeled as voltage controlled current sources.
- The transition behavior is described by the V/T table of the rising/falling waveforms under specified loading condition. And they are used to derive/scale instantaneous value of the I/V curves.
- Other important parasitic elements
- IBIS, as a behavioral model, does not contain transistor equation, some of the physics and detailed response may not exist in a simple model, hence the issue that will be discussed next.



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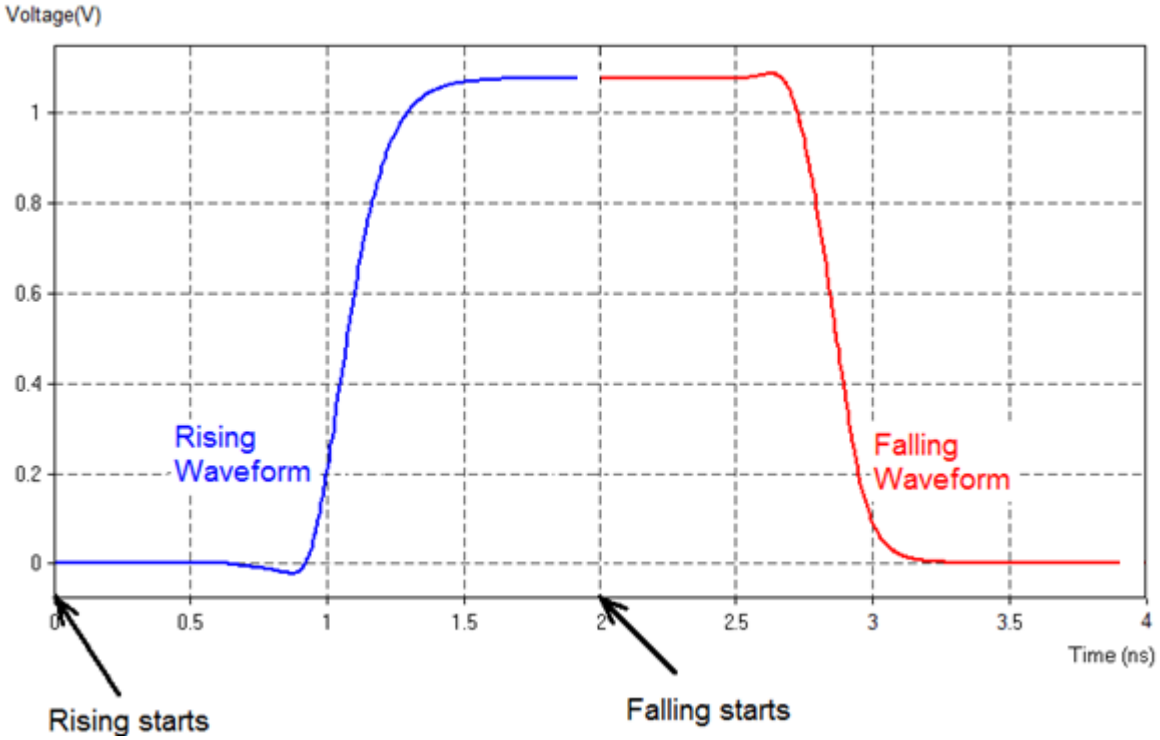
Understand the Over-Clocking

- Normal operating, the input data bit width > the time range of the IBIS rising and falling waveform.

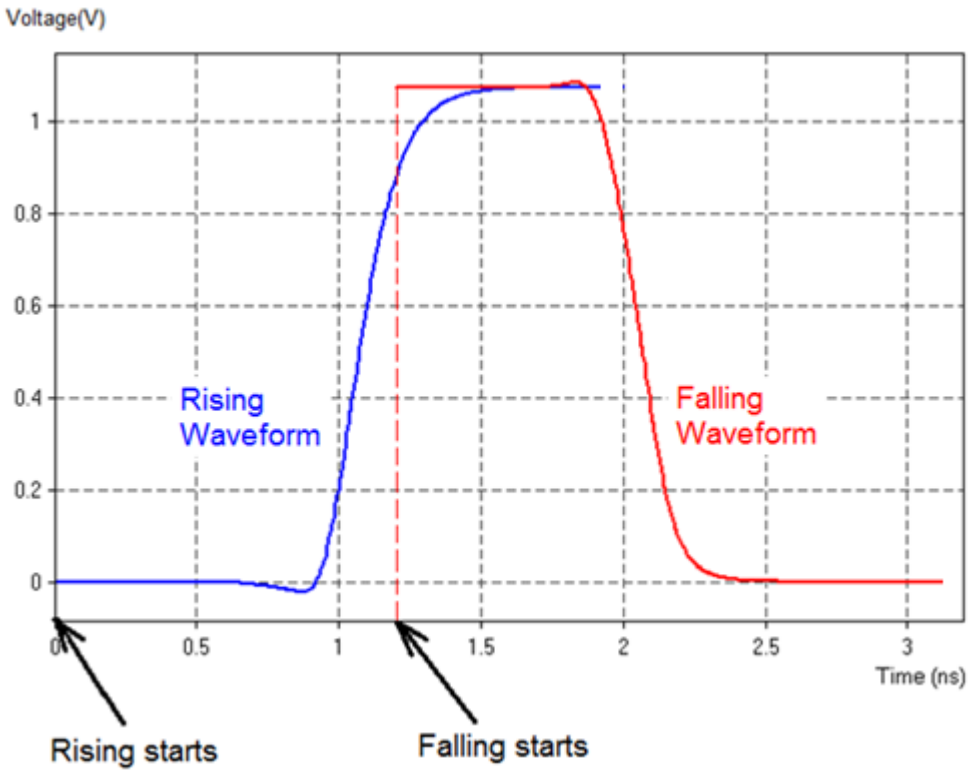


Normal operation

Understand the Over-Clocking (cont.)

- If the input signal bit width is smaller than the time range of the IBIS waveforms, the next transition is triggered before this transition is finished.
- The behavior of the IBIS simulator may be unpredictable.

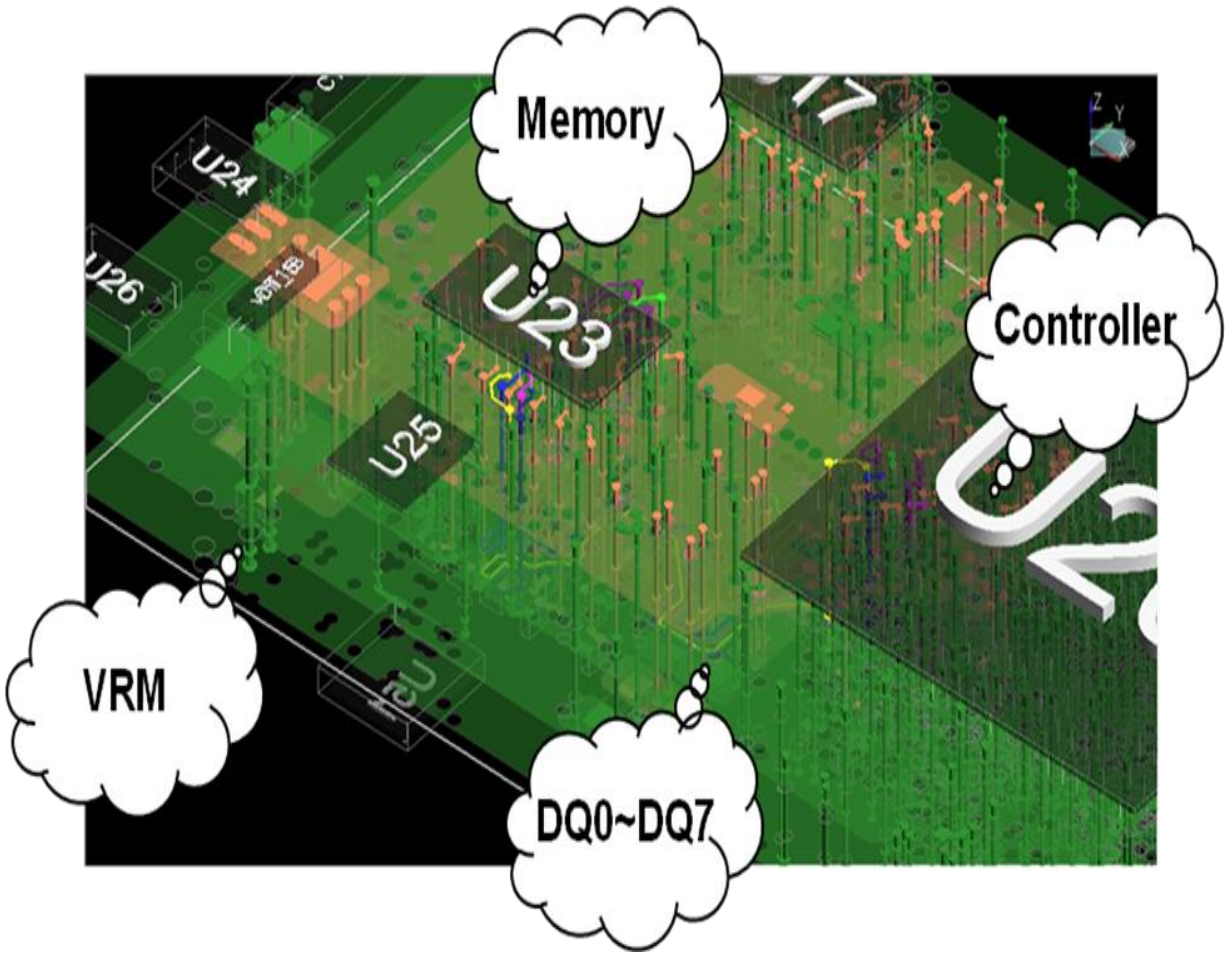
- Google “IBIS Overclocking” to find out more about this issue discussion since 2002



Over-clocking operation

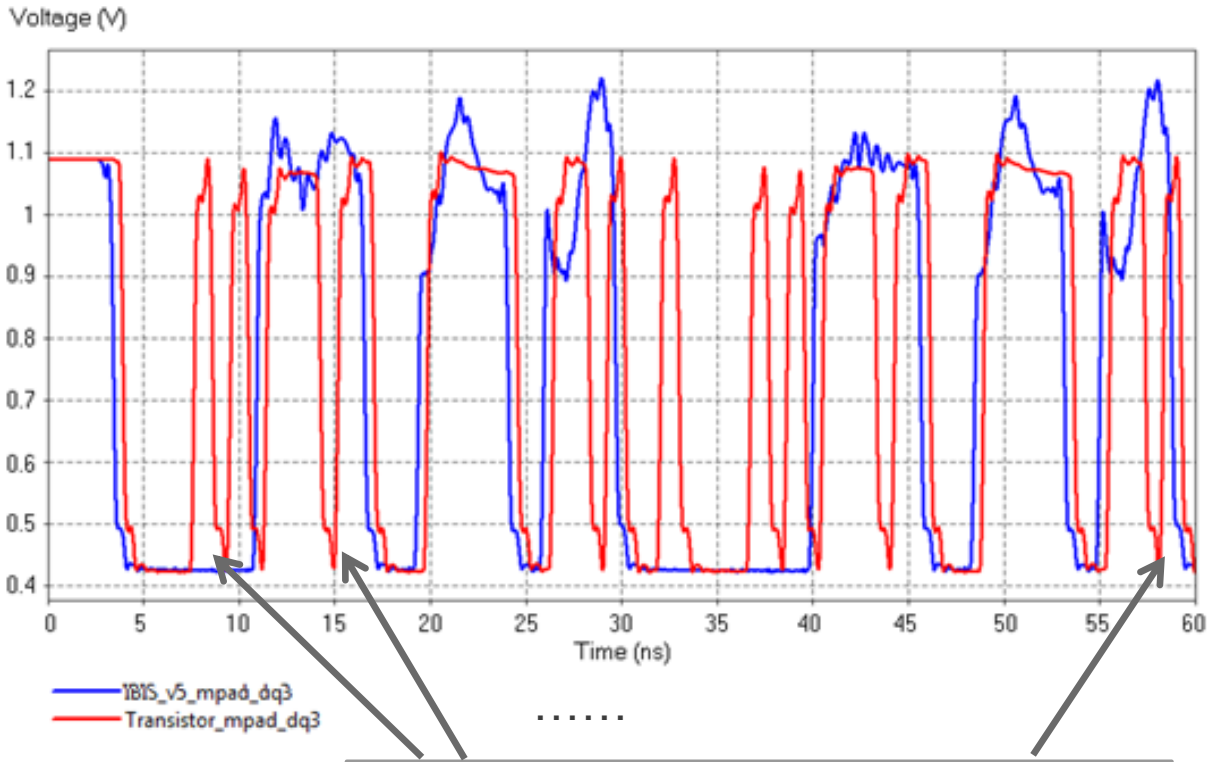
Simulation Problem Is Shown with A DDR3 SSO Test Case

8 signal nets + 1 power nets + 1 ground net from a real PCB design. Bit width is 1ns, the pattern is 00010101110110011111001101001O



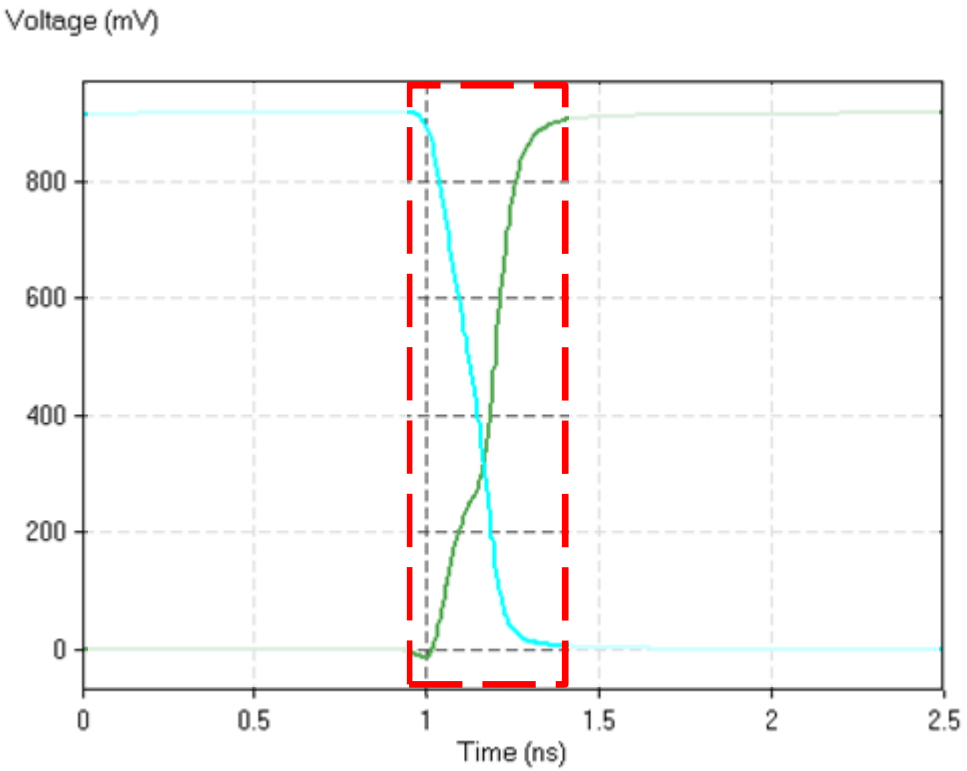
Problematic Results from Over-Clocking

- A test case operating over-clocking
- Simulation results show missing bits



Existing Solution to Solve Over-Clocking Problem

- V/T curve windowing by cutting the initial delay and the flat tail of the rising/falling waveforms of IBIS model to make the time range shorter
- The windowing can be done either in IBIS model creation or simulation tools



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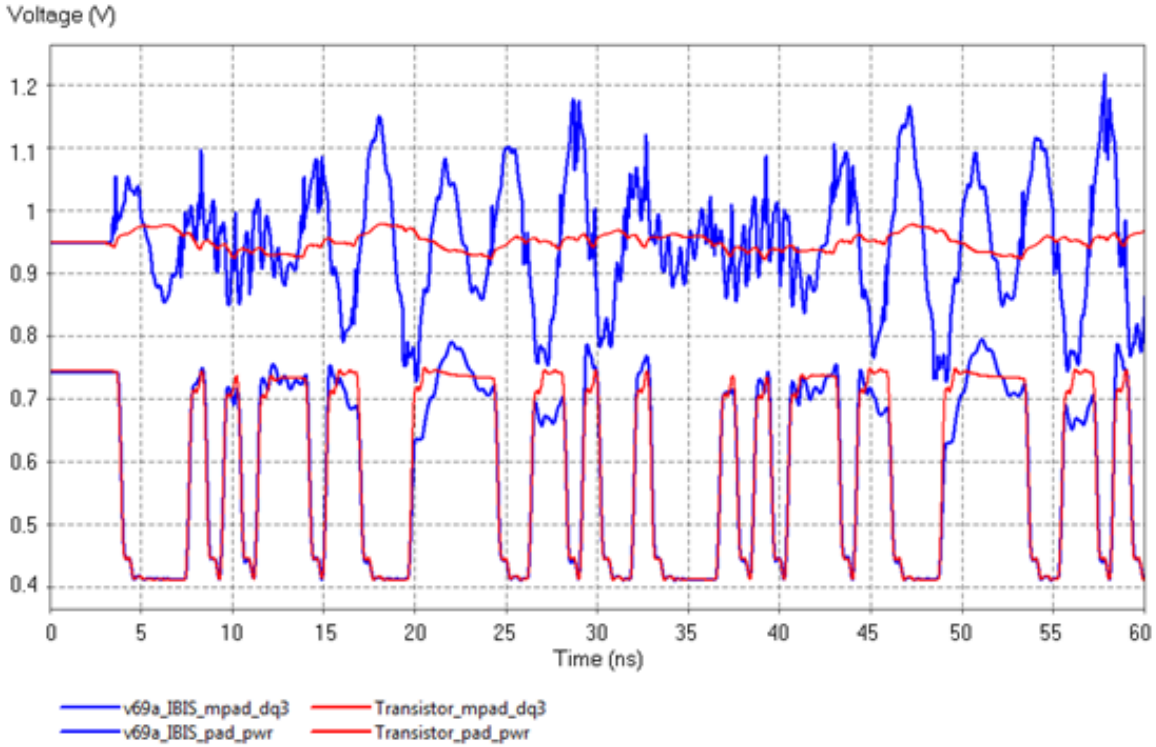
Simulation Results with V/T Windowing

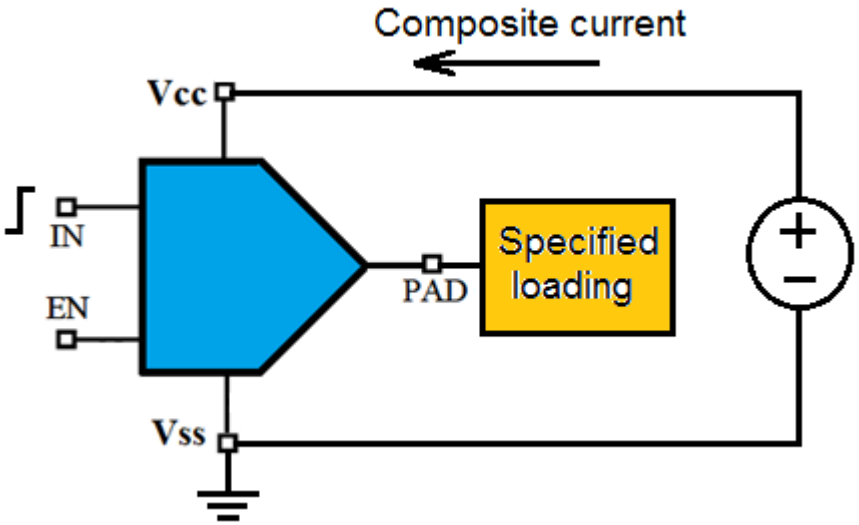
- The missing bits resolved
- Therefore, simulator with proper V/T windowing scheme should automatically handle overclocking issue in IBIS 4.2 model



- However, voltage on power net mismatches between transistor model and IBIS model due to the dynamic power noise not modeled.

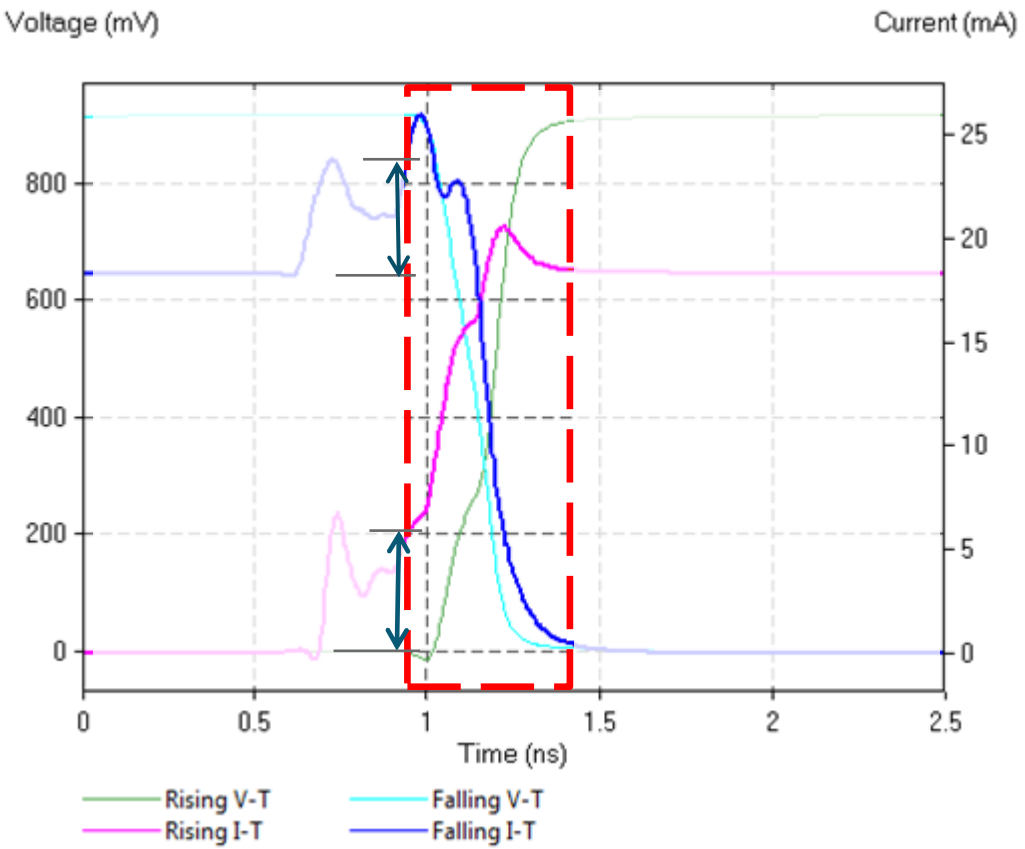
New Challenge of Over-Clocking with Composite Current

- To accurate model the power-aware buffer model, the composite currents (I/T) are introduced in IBIS V5.0 to give the current waveforms on power pin.
- The I/T data must be time correlated with the waveform V/T data which are extracted from pad pin.
- The composite current includes the contribution of the pre-driver and all the other on-die P/G paths. It has wider time range than V/T waveform.



Windowing with Composite Current

- Now both V/T and I/T need to be windowed.
- Choosing window based on wider I/T curve will not help, since over-clocking solution requires narrow timing window for higher frequency operation.
- Still choosing a window based on V/T will cut the composite current incomplete which will form a sharp step current.



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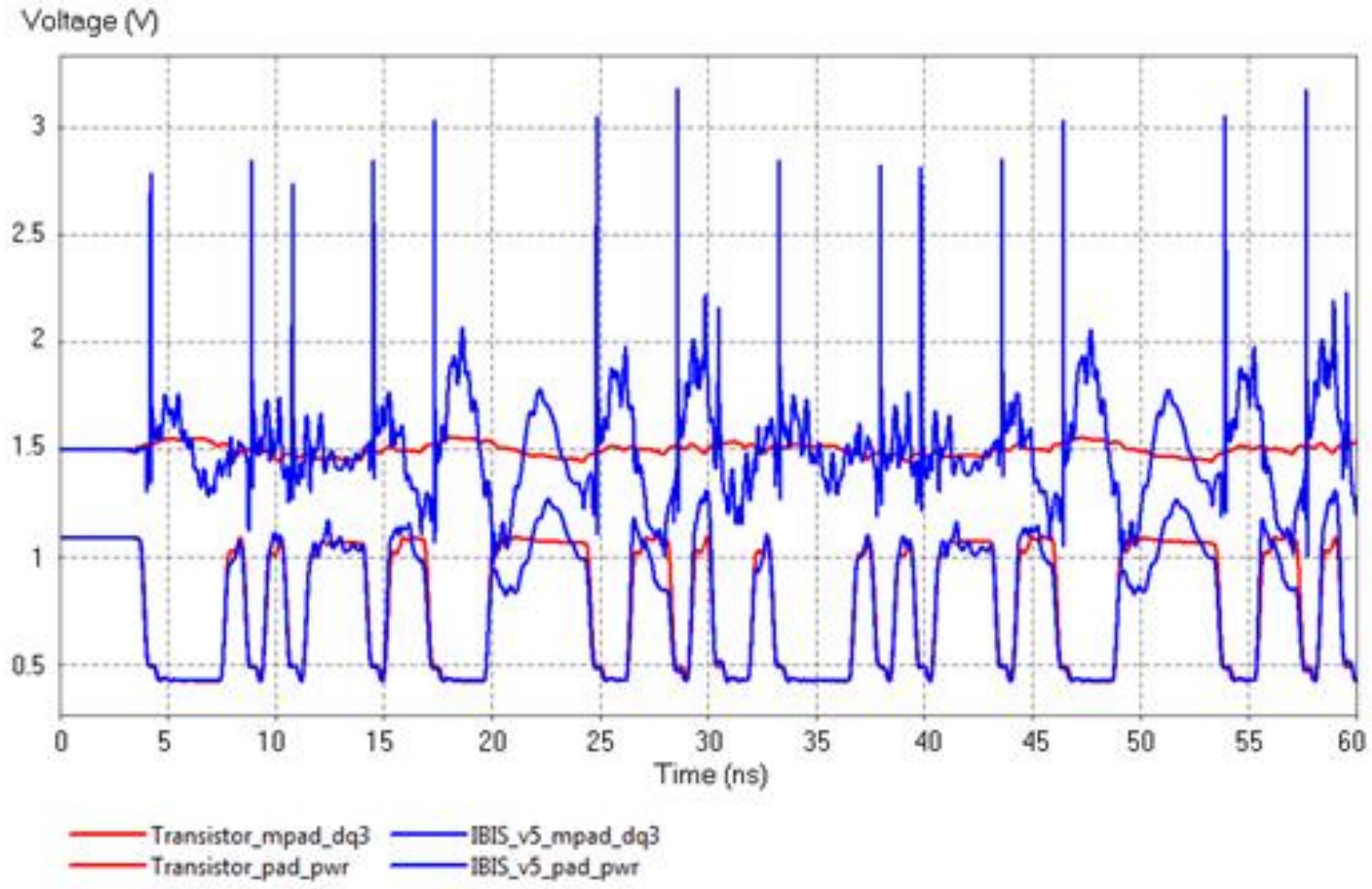
The Sharp Step of Incomplete Composite Current Causes Unreal Large Voltage Spikes



Observation of This New Challenge

- With the addition of composite current (I/T) in IBIS 5.0, old windowing technique (V/T based) in IBIS simulator need to be improved, and can't be directly applied to I/T data to solve over-clocking issue.
- With IBIS 5.0 models become increasingly popular in the last few years, there are more awareness and discussion of this issue.
- A solution was developed by us two years ago to tackle this challenge.

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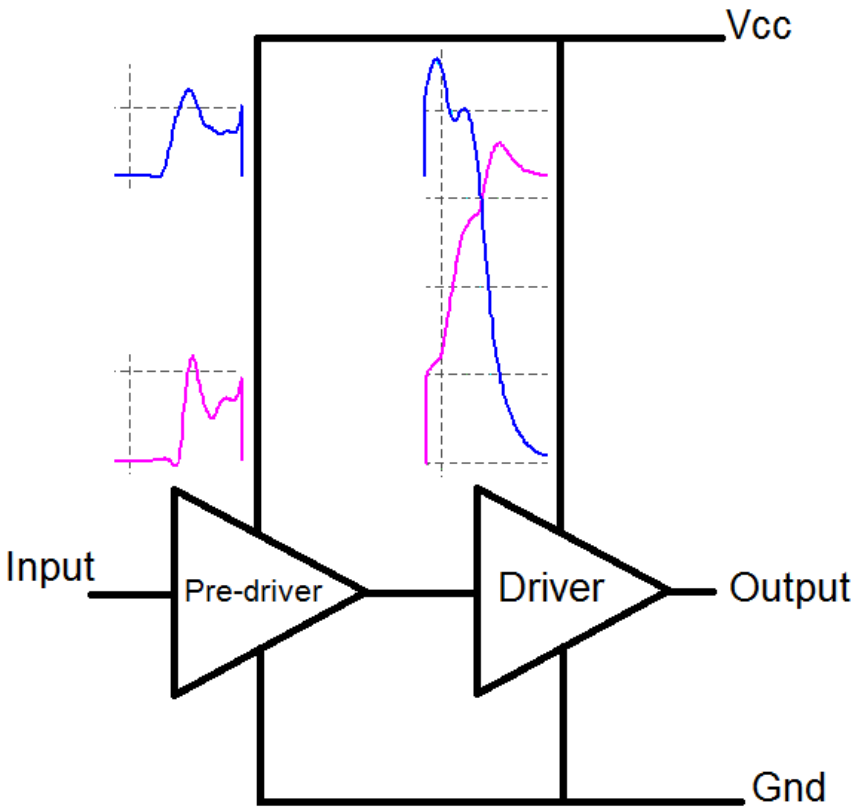
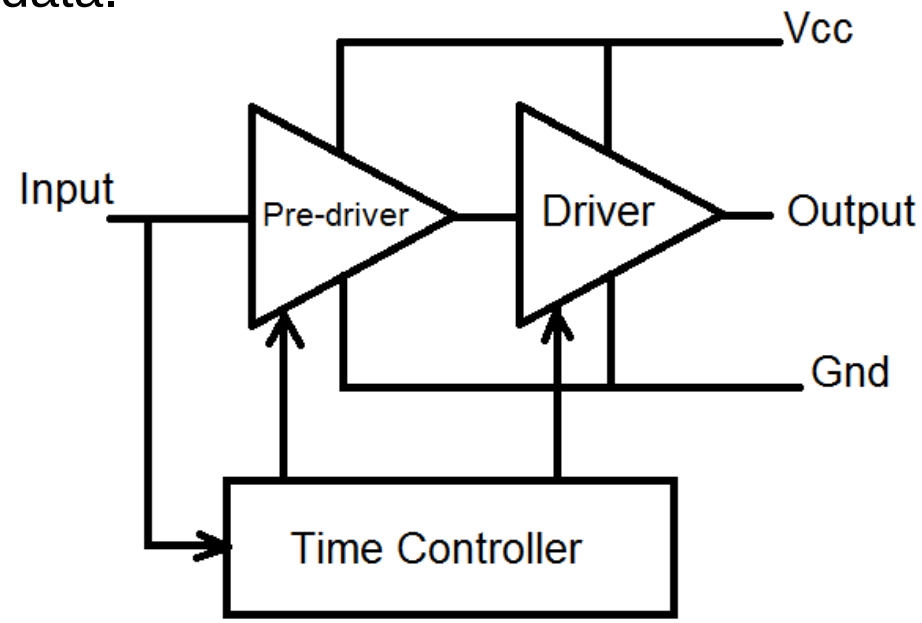
Key Point of Advanced Over-Clocking Solution

- Using the V/T waveform windowing
- Adding one stage to the existing driver to keep the pre-driver behavior for the buffer switching delay and power current
- Taking the composite current compensation into two parts:
  - Driver contribution
  - Pre-driver contribution

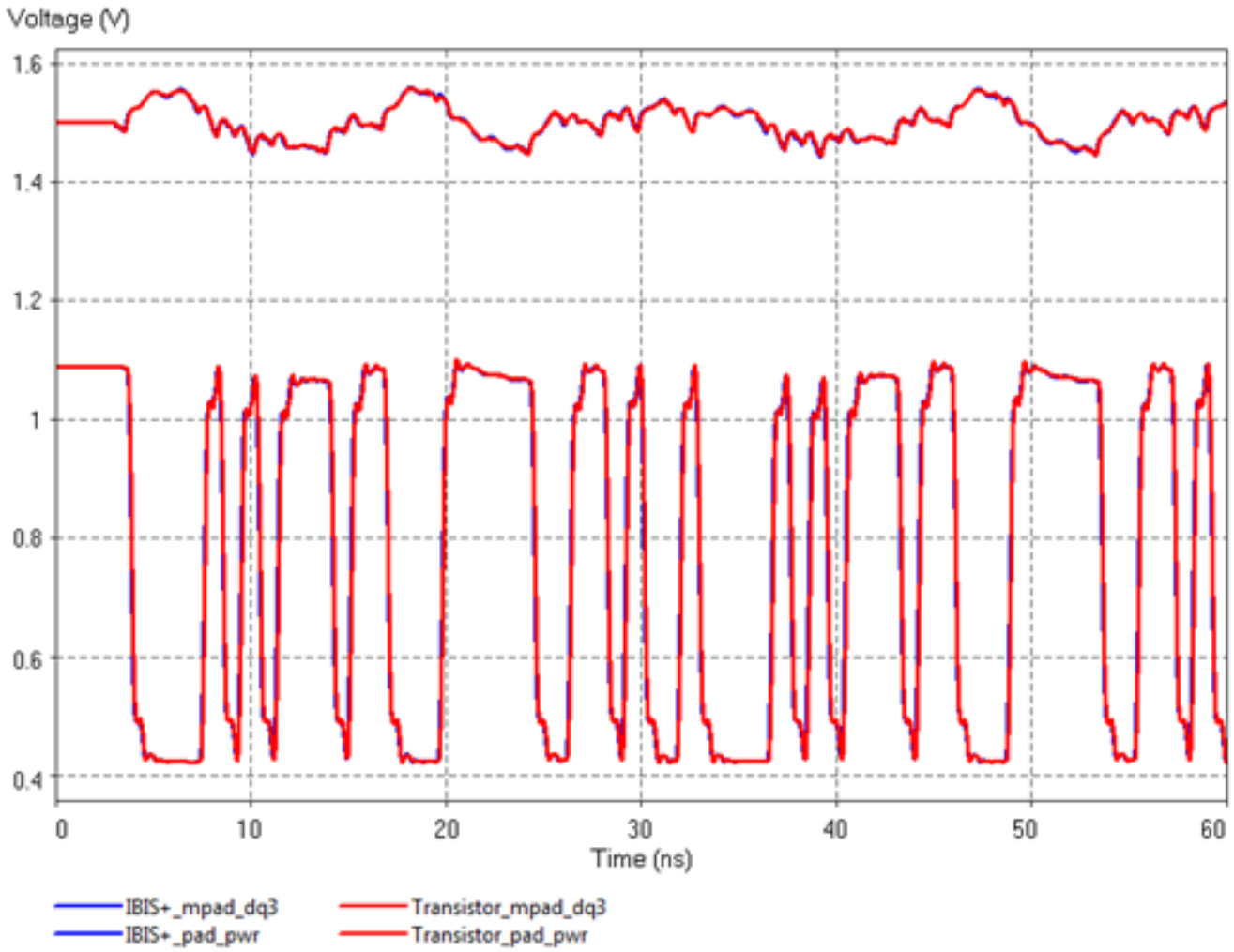


Implementing the Proposed Over-Clocking Solution

- The proposed over-clocking solution can be implemented into an advanced IBIS model, which is a SPICE netlist with integrated model data and simulation algorithm.
- The proposed over-clocking solution can also be implemented into an advanced IBIS simulator to automatically handle the windowing of both V/T and I/T data.



Simulation results with Advanced Over-Clocking Solution



Simulation Performance Summary

- Very good correlation between IBIS and the original transistor model for real SSO simulation, both signals and power/ground waveforms match very well, even under over-clocking scenario.
- The 60ns simulation time is based on 32 clock cycles of data input.
- It takes 54 minutes for original transistor level SPICE model.
- It takes 55 seconds for the behavioral model with the advanced over-clocking solution.
- Note: HSPICE is used to run the simulations for all the models, including the advanced IBIS model with over-clocking solution.

Conclusion

- Power-aware buffer model generation has been implemented for IBIS 5.0 standard. When used in high-speed power-aware SSO simulations, user often has to deal with IBIS over-clocking issues.
- With the proposed algorithm for handling composite currents under over-clocking situation, more advanced model shows significant accuracy improvement compared with traditional IBIS models, while keeping the fast simulation advantages of IBIS.
- Advances in IBIS standard, together with advances in modeling and simulation algorithms, continue to make this behavioral model technique a great and practical engineering approach for high-speed design.

References

- [1] Perivand F. Tchrani, Yuzhe Chen, Jiayuan Fang, “Extraction of Transient Behavioral Model of Digital I/O Buffers from IBIS”, 46th IEEE Electronic Components & Technology Conference, Orlando, May 28-31, 1996, pp 1009-1015.
- [2] Ying Wang and Han Ngee Tan,“The Development of Analog SPICE Behavioral Model Based on IBIS Model”, Proceedings of the Ninth Great Lakes Symposium on VLSI, March 1999.
- [3] Sam Chitwood, Raymond Y. Chen, Jiayuan Fang, “An Initial Case Study for BIRD95 - Enhancing IBIS for SSO Power Integrity Simulation”, IBIS Summit DesignCon, January 2005.
- [4] Raymond Y. Chen, “Recent Development of IBIS and Related EDA Technologies”, Sigrity Annual User Forum, May 24, 2011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