IBIS Modeling for IO-SSO Analysis

Thunder Lay and Jack W.C. Lin
IBIS Asia Summit
Taipei, Taiwan
Nov. 19, 2013

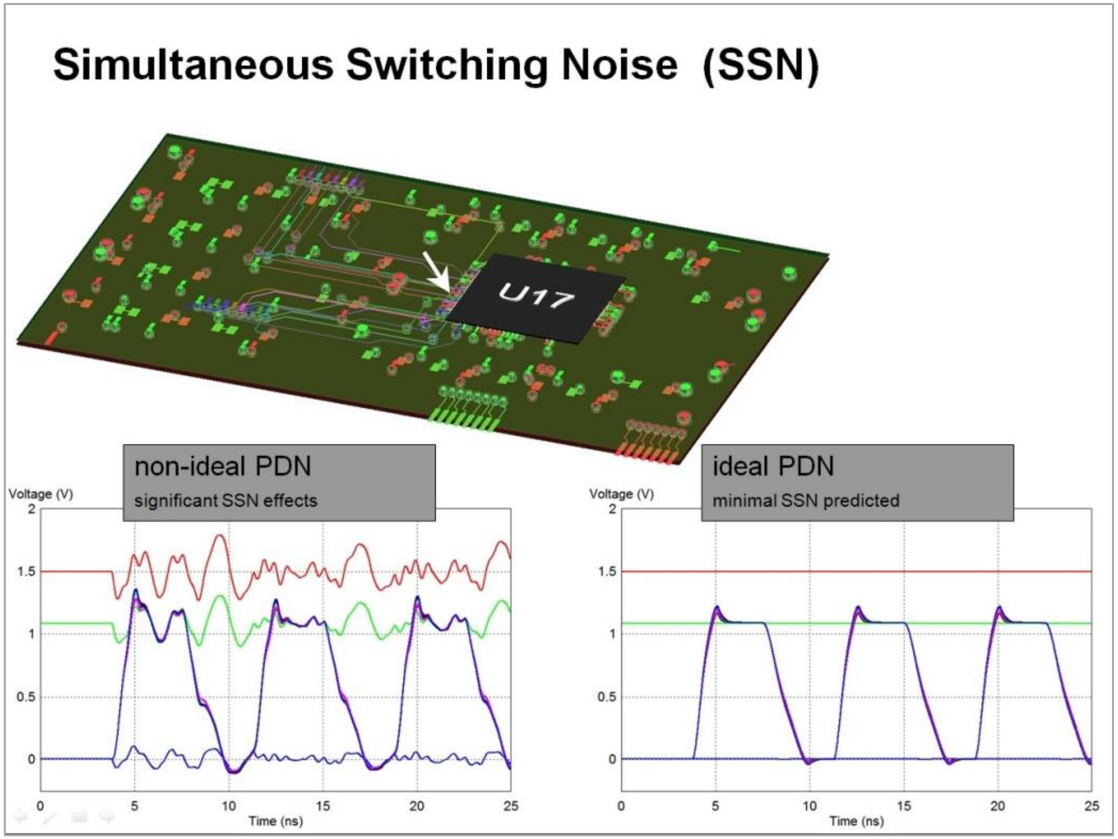
cadence®

Agenda

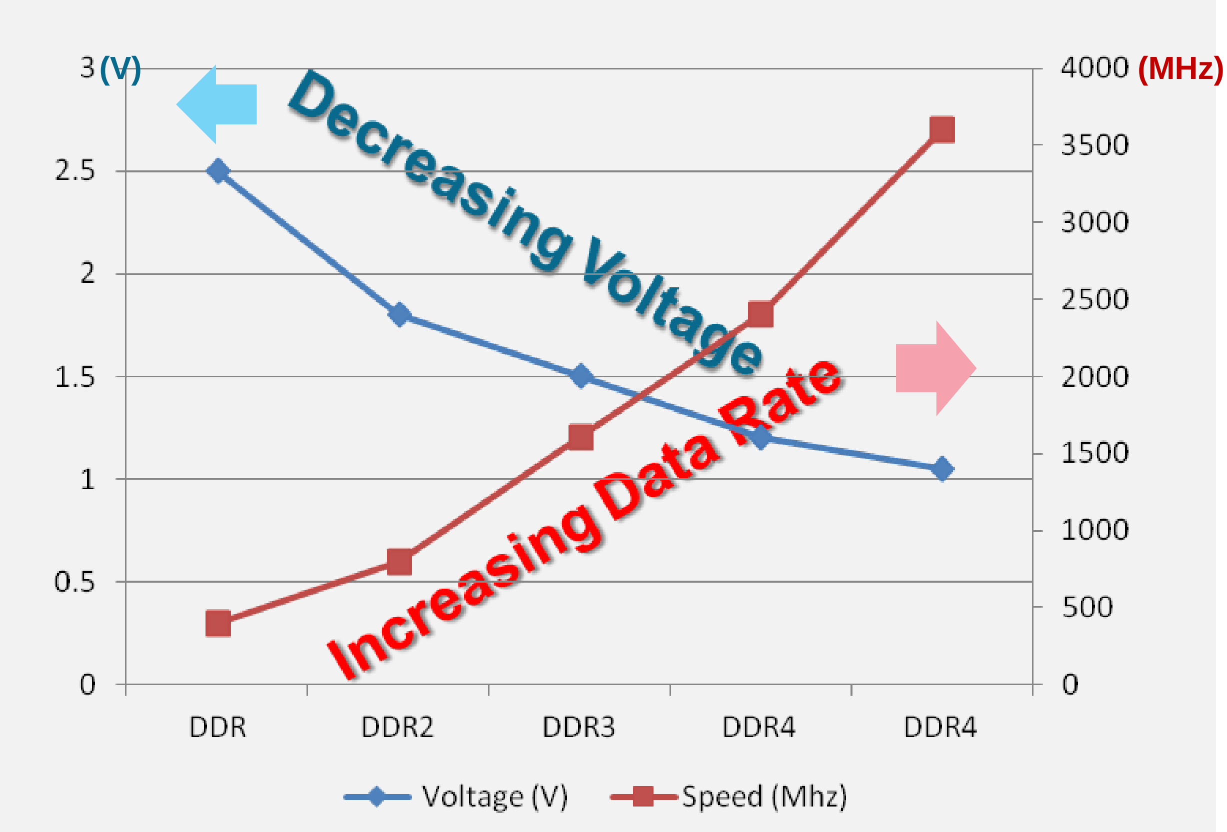
- **What is IO-SSO?**
- Missing Components in Traditional IO-SSO Analysis
- Accurate On-die and Package Effects in IBIS Models
- Creating IBIS Models with On-die Interconnect
- Case Study – IO-SSO Analysis with IBIS Models
- Summary

What is IO-SSO?

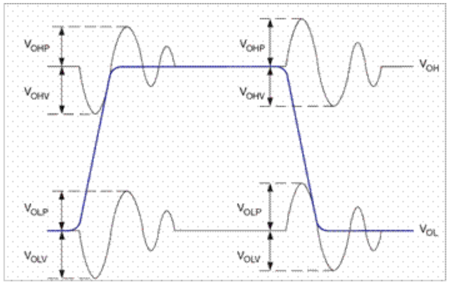
- A DDR memory interfaces is a parallel bus
  - Many signals represent a data byte/word/32-bit word/64-bit word
  - Simultaneous switching signals / outputs are referred to as SSO
  - The noise between power and ground created is referred to as simultaneous switching noise (SSN)
  - IC Designers refer to this phenomenon as IO-SSO
  - SI/PI can be verified by IO-SSO



IO-SSO Impacts Timing and Noise Margin



- Data transfers are faster and more sensitive to instability of the PDN
    - DDR runs at 2.5 V
    - DDR2 runs at 1.8 V
    - DDR3 runs at 1.5V
    - DDR4 to run at 1.2 V – 1.05V



Ground bounce Peaks and Valleys must be minimized with low signal voltages

+

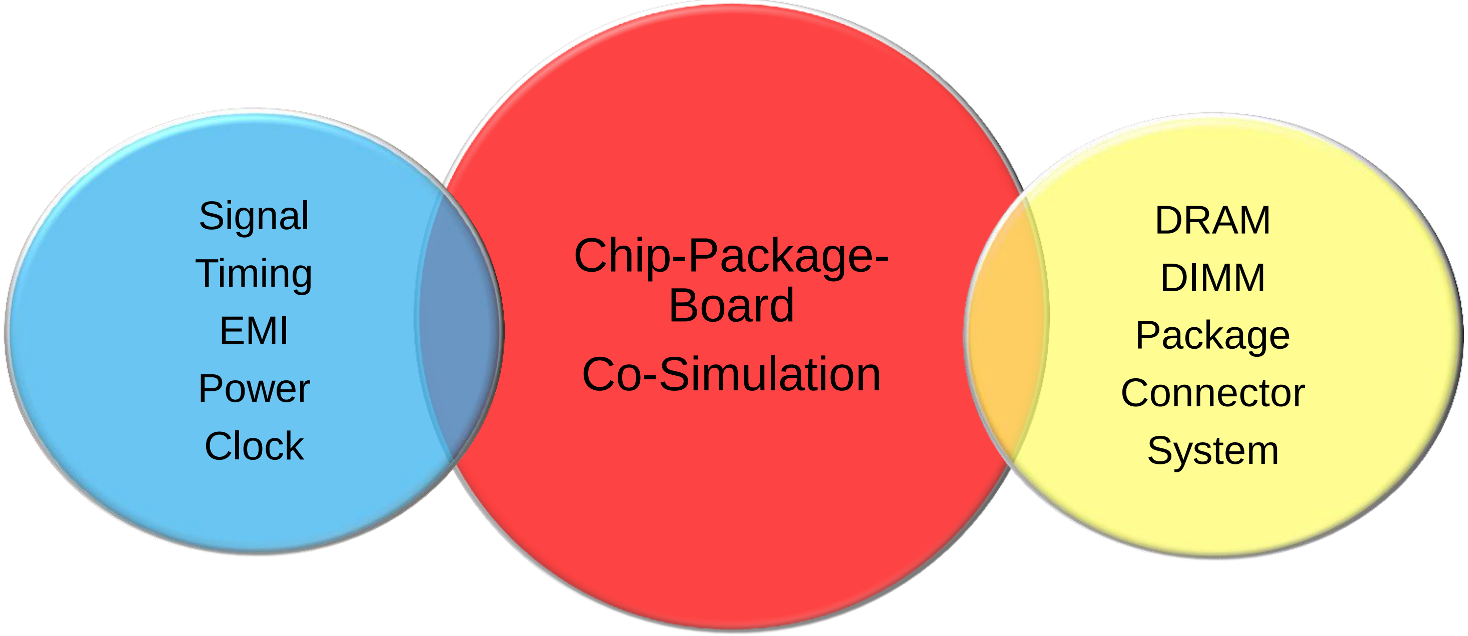
Decreasing Timing Budget

±600ps → ±300ps → ±150ps

SSN effects impact timing and noise budget

Higher Data Rate ➔ High Level Interactions

Electrical and Physical worlds collide requiring multi-fabric simulation



Signal
Timing
EMI
Power
Clock

Chip-Package-Board

Co-Simulation

DRAM
DIMM
Package
Connector
System

Increased interaction between signals

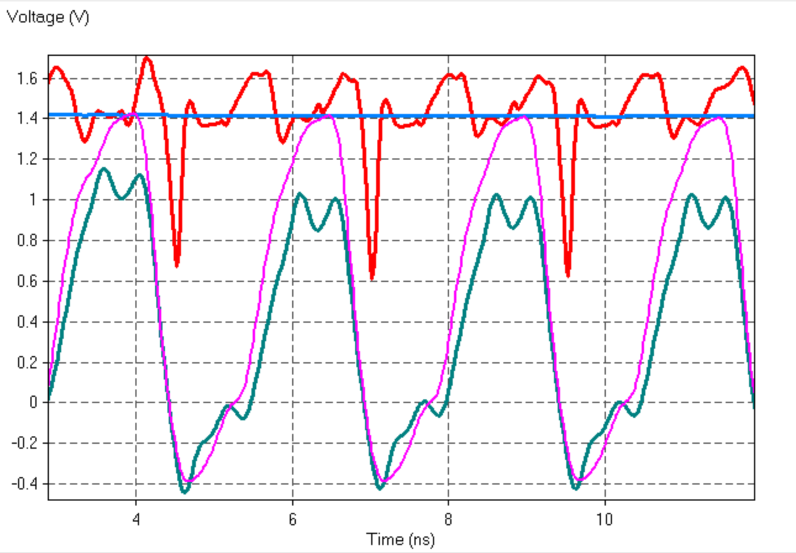
Increased interaction between system hardware components

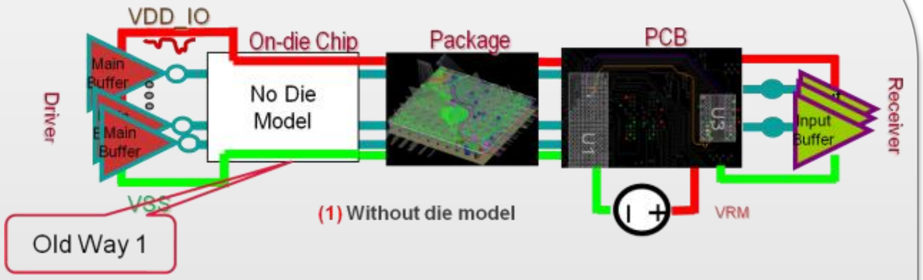
Traditional IO-SSO Simulation Scenarios

- Pessimistic result when analyzed without on-die model.
- Optimistic result when analyzed with estimated on-die model.

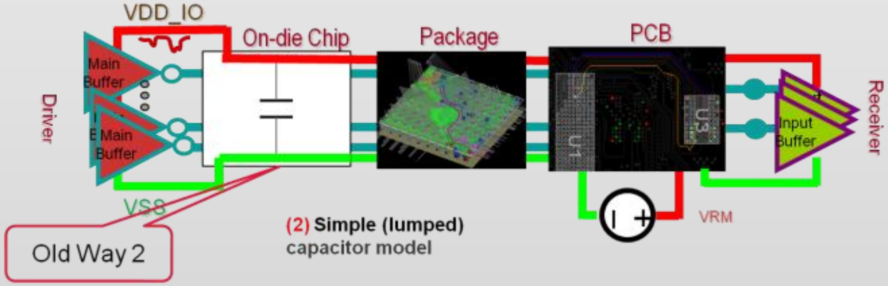
Red: Pessimistic without chip IO interconnect model

Blue: Optimistic with chip simple capacitor model

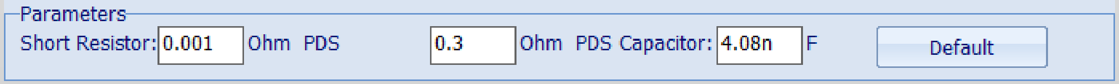




(1) Without die model



(2) Simple (lumped) capacitor model



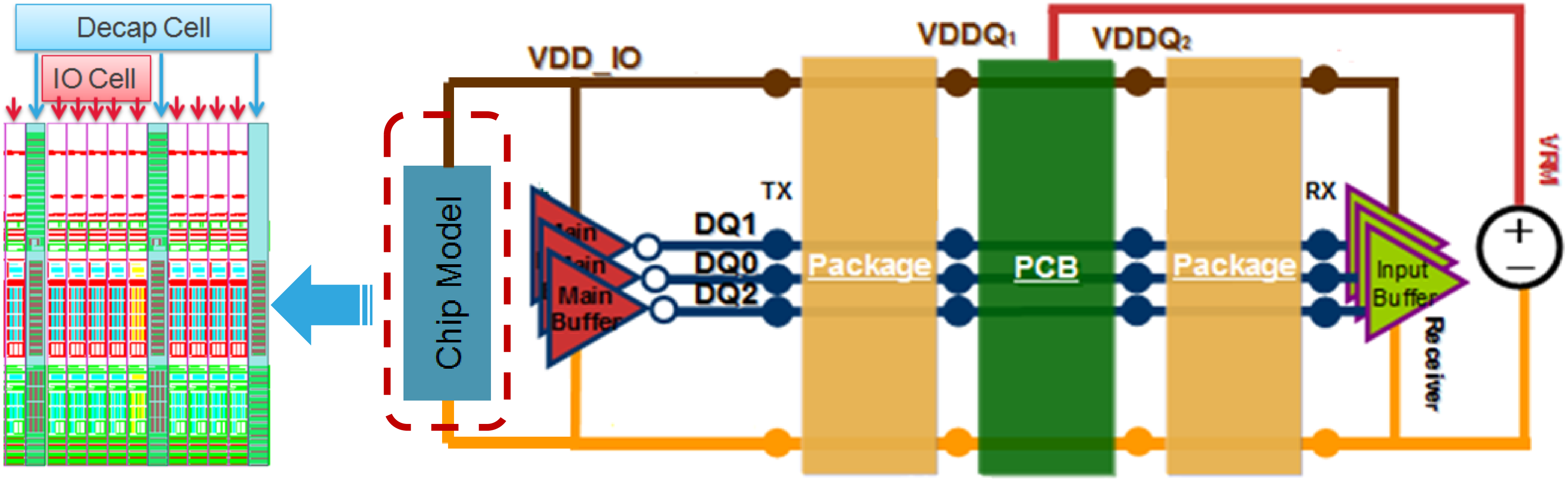
Parameters

Short Resistor: 0.001 Ohm PDS 0.3 Ohm PDS Capacitor: 4.08n F

Agenda

- What is IO-SSO?
- **Missing Components in Traditional IO-SSO Analysis**
- Accurate On-die and Package Effects in IBIS Models
- Creating IBIS Models with On-die Interconnect
- Case Study – IO-SSO Analysis with IBIS Models
- Summary

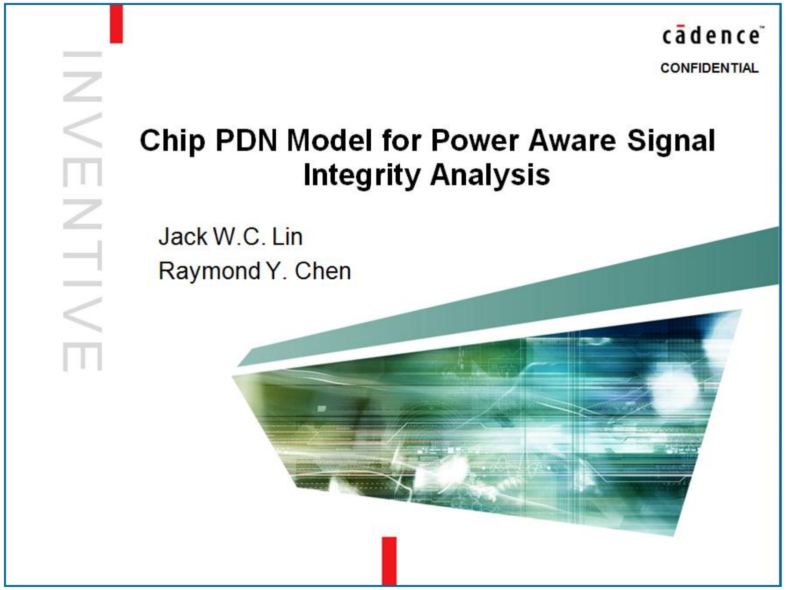
Missing Components in Traditional IO-SSO Analysis



- Post-sim transistor SPICE netlist only includes limited parasitic information.
- Distributed behavior of IO’s P/G impedance can’t be represented.
- Pin Mapping table may not be defined accurately.
- On-die decap model is not captured in IBIS model.
- All above problems make IO-SSO simulation lose accuracy.

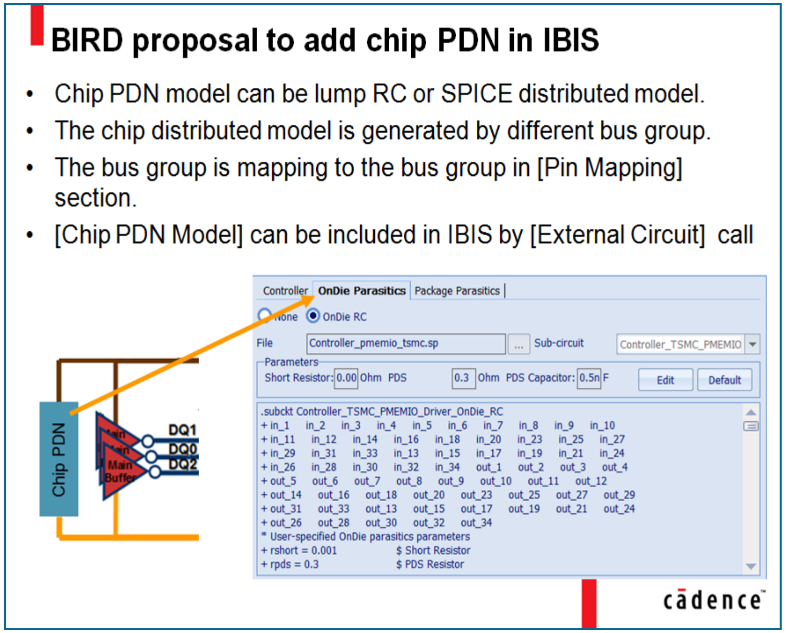
Asia IBIS Summit 2012

- Chip PDN model is crucial for IO-SSO analysis.
- Without Chip PDN model, artificially large power /ground noise impact the signal waveform significantly
- Chip PDN is responsible to filter high frequency noise
- On-die RC or better distributed chip PDN model can yield realistic power/ground noise analysis



Chip PDN Model for Power Aware Signal Integrity Analysis

Jack W.C. Lin
Raymond Y. Chen



BIRD proposal to add chip PDN in IBIS

- Chip PDN model can be lump RC or SPICE distributed model.
- The chip distributed model is generated by different bus group.
- The bus group is mapping to the bus group in [Pin Mapping] section.
- [Chip PDN Model] can be included in IBIS by [External Circuit] call

○ None ● OnDie RC

File: Controller_pmemio_tsmc.sp
Sub-circuit: Controller_TSMC_PMEMIO

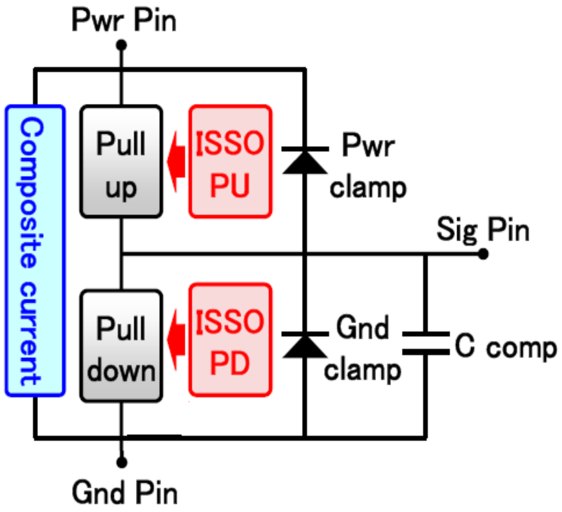
Parameters
Short Resistor: 0.00 Ohm PDS 0.3 Ohm PDS Capacitor: 0.5n F

```
.subckt Controller_TSMC_PMEMIO_Driver_OnDie_RC
+ in_1    in_2    in_3    in_4    in_5    in_6    in_7    in_8    in_9    in_10
+ in_11   in_12   in_14   in_16   in_18   in_20   in_23   in_25   in_27
+ in_29   in_31   in_33   in_13   in_15   in_17   in_19   in_21   in_24
+ in_26   in_28   in_30   in_32   in_34   out_1   out_2   out_3   out_4
+ out_5   out_6   out_7   out_8   out_9   out_10   out_11   out_12
+ out_14   out_16   out_18   out_20   out_23   out_25   out_27   out_29
+ out_31   out_33   out_13   out_15   out_17   out_19   out_21   out_24
+ out_26   out_28   out_30   out_32   out_34
* User-specified OnDie parasitics parameters
+ rshort = 0.001            $ Short Resistor
+ rpds = 0.3                $ PDS Resistor
```

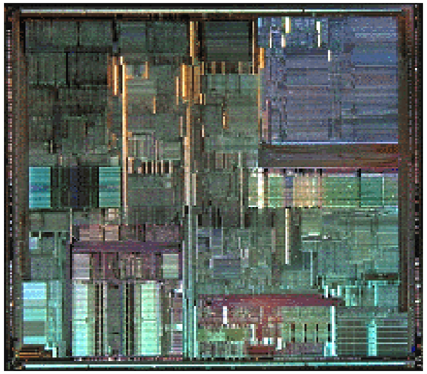
Agenda

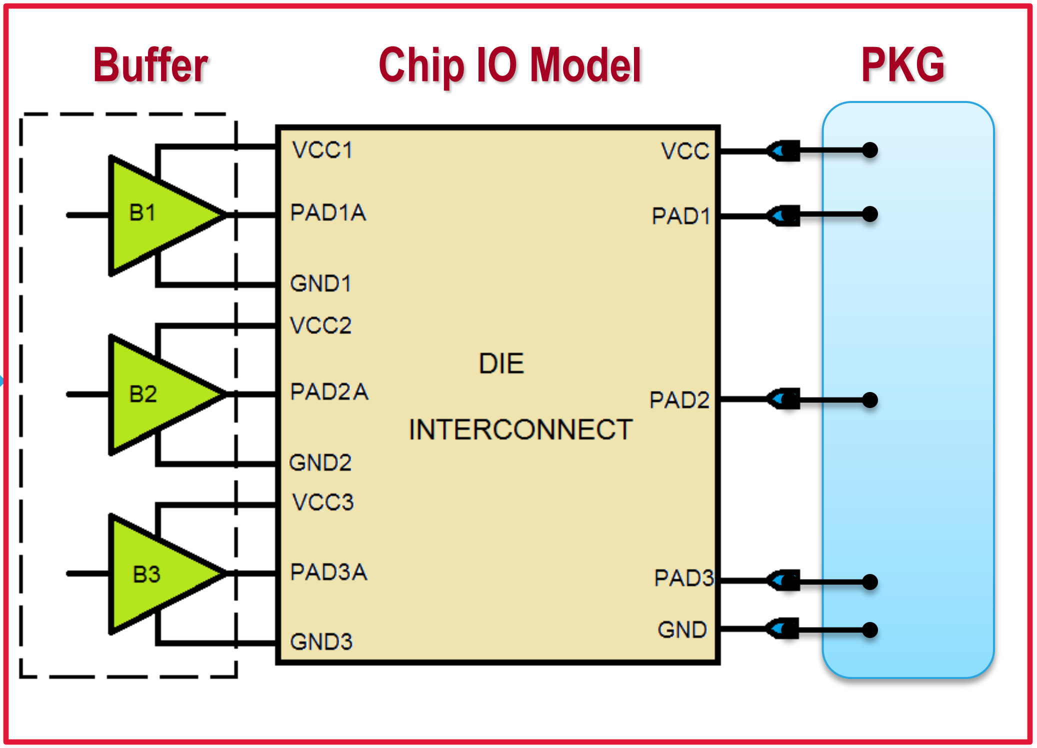
- What is IO-SSO?
- Missing Components in Traditional IO-SSO Analysis
- **Accurate On-die and Package Effects in IBIS Models**
- Creating IBIS Models with On-die Interconnect
- Case Study – IO-SSO Analysis with IBIS Models
- Summary

Adding On-die Effects to the IBIS Model



Chip IO Model

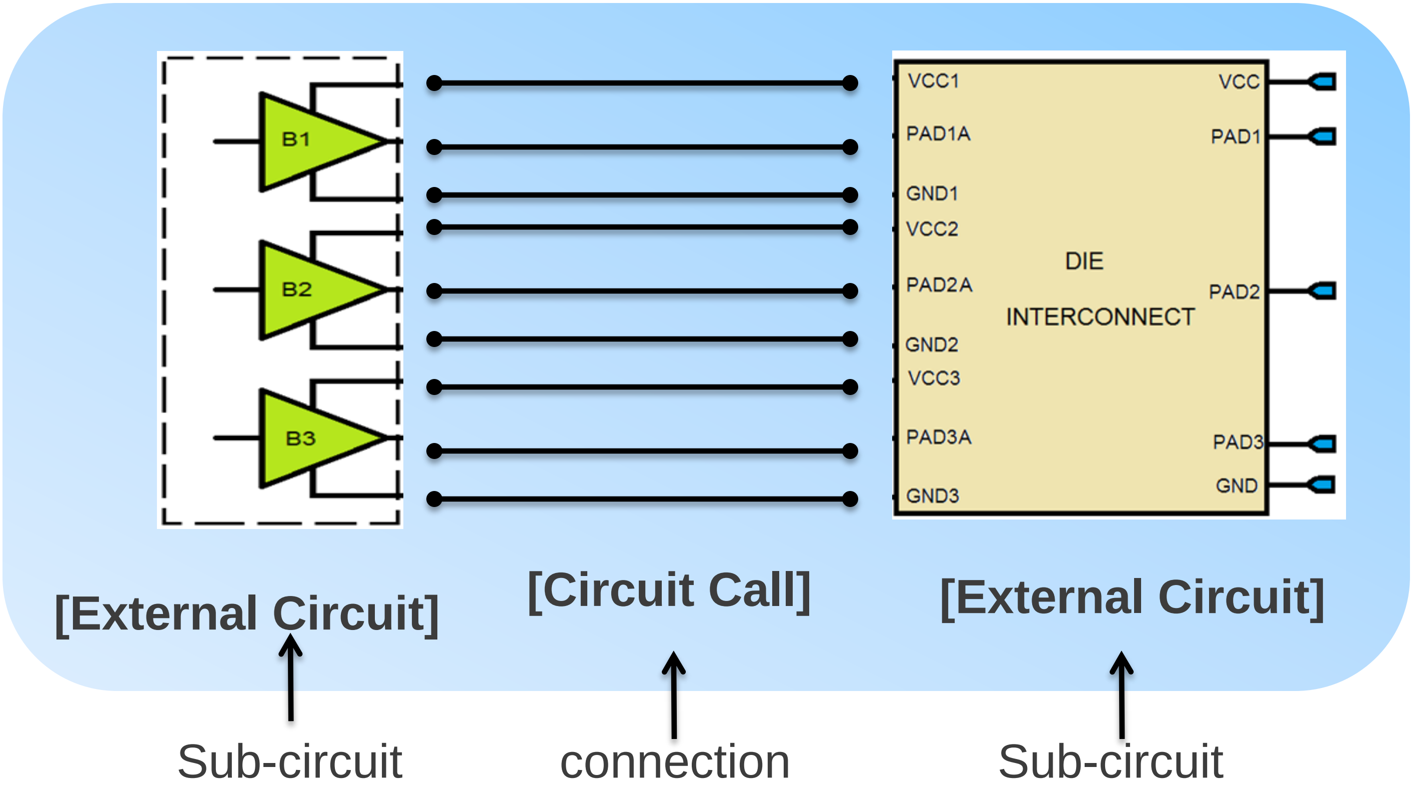




Buffer+ Chip IO model + PKG

Connecting Buffer, On-Die and Package Models

IBIS 5.1



[External Circuit]

[Circuit Call]

[External Circuit]

Sub-circuit

connection

Sub-circuit

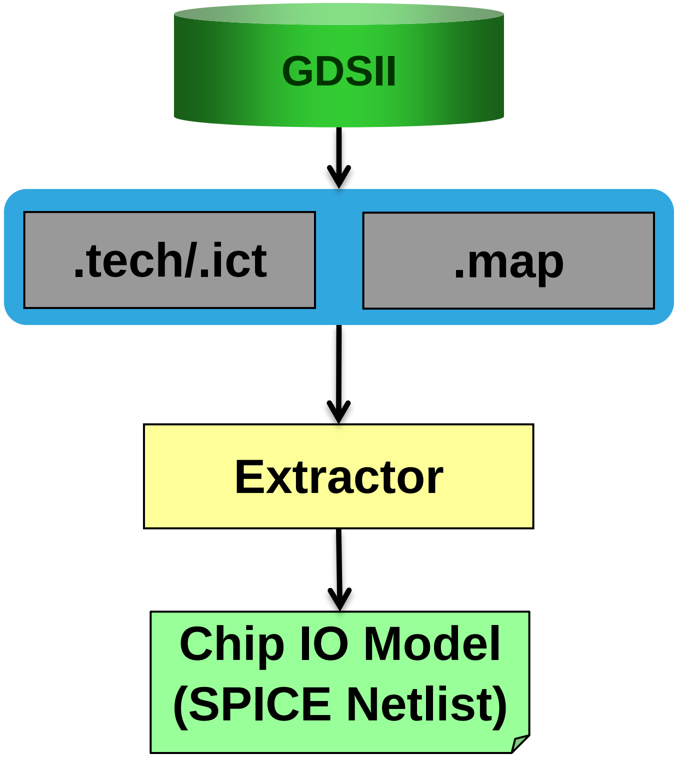
- Effectively incorporates the on-die and package models into the buffer
- The package and on-die models may be of arbitrary topology to include coupling, non-ideal power deliver and other effects
- Applying IBIS 5.1 [External Circuit] sub-components is similar to sub-circuit call and connections in HSPICE
- Future ISS based solution may be coming from committee

Agenda

- What is IO-SSO?
- Missing Components in Traditional IO-SSO Analysis
- Accurate On-die and Package Effects in IBIS Models
- **Creating IBIS Models with On-die Interconnect**
- Case Study – IO-SSO Analysis with IBIS Models
- Summary

Creating IBIS Models with On-die Interconnect (1/4)

- Generate chip IO model
  - LEF/DEF or GDSII data can represent physical geometry.
  - Includes Power/Ground/Signal routing with On-Die caps.
  - Define Chip stackup, circuit mapping
  - Chip IO model extraction is based on chip layout which includes metal_x to the top layers (x can be 1~N). Model builder needs to be aware what SPICE nest-list is from pre-sim or post-sim flow.
  - Generate SPICE netlist



GDSII

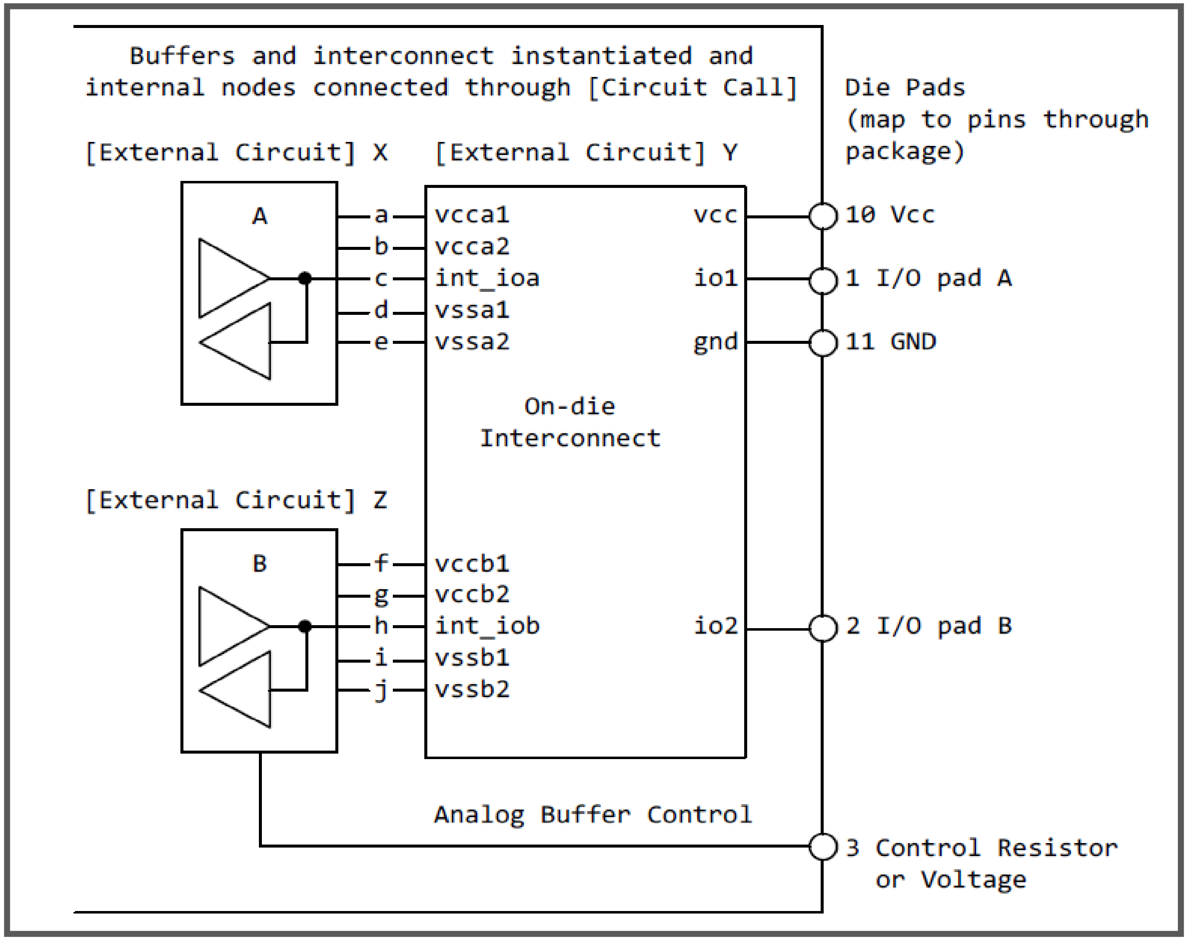
.tech/.ict

.map

Extractor

Chip IO Model (SPICE Netlist)

Creating IBIS Models with On-Die Interconnect (2/4)

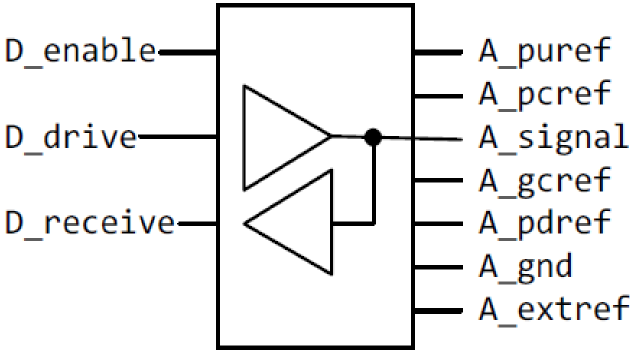


- [External Circuit] will be represented as IO buffer, chip IO, package…..
- Connect each [External Circuit] through [Circuit Call]

Creating IBIS Models with On-die Interconnect (3/4)

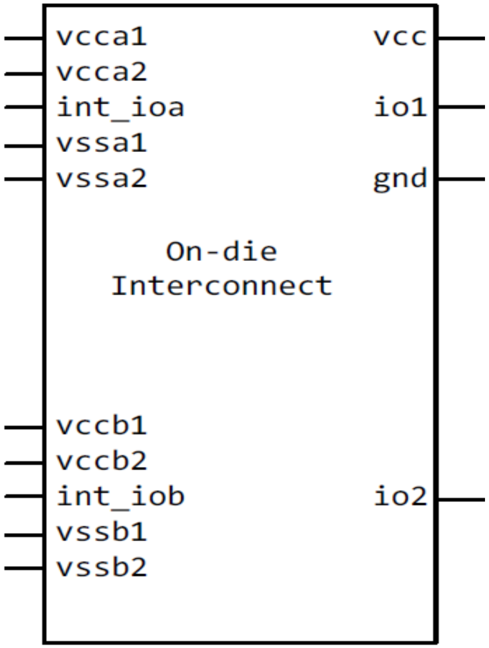
- Ports under [External Circuit]

The [External Circuit] keyword allows the user to define any number of ports and port functions on a circuit.



Port name for IO Buffer

Ports A_puref A_pdref A_signal A_drive
A_enable A_receive A_pcref A_gcref



Ports vcca1
Ports vcca2
……….

Creating IBIS Models with On-die Interconnect (4/4)

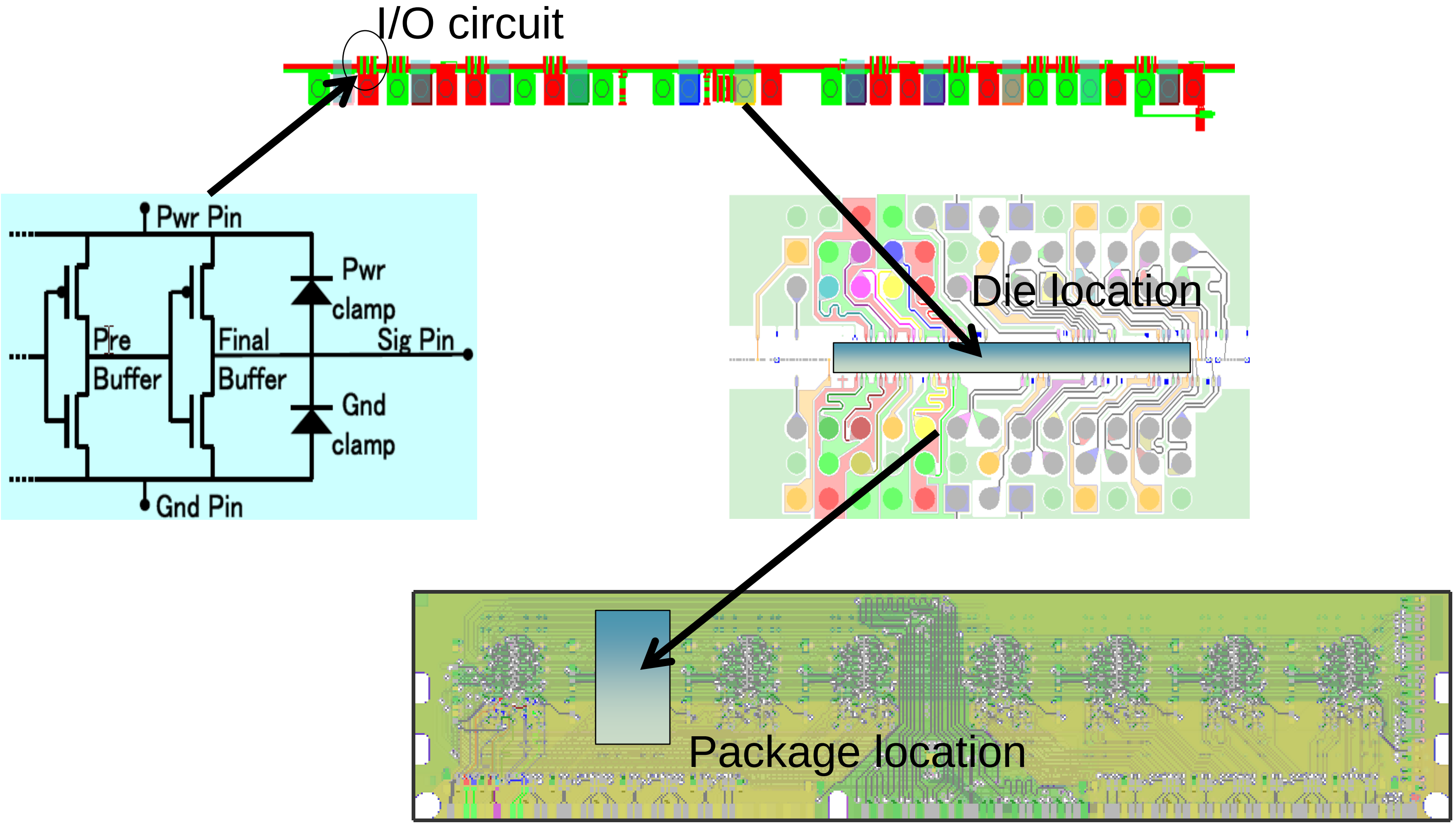
- Define [Pin] and [Node Declarations]
  - When a [Circuit Call] keyword defines any connections that involve one or more die pads (and consequently pins), the corresponding pins on the [Pin] list must use the reserved word “CIRCUITCALL” in the third column instead of a model name.
  - [Node Declaration] provides a list of internal die nodes and/or die pads for a [Component] to make unambiguous interconnection descriptions possible

```
[Node Declarations]     | Must appear before any [Circuit Call] keyword
| Die nodes:
pu1 pd1 io1p io1 in1 en1 outin1          | List of die nodes
pu2 pd2 io2p io2 in2 en2 outin2          | List of die nodes
pu3 pd3 io3p io3 in3 en3 outin3          | List of die nodes
[End Node Declarations]
```

Agenda

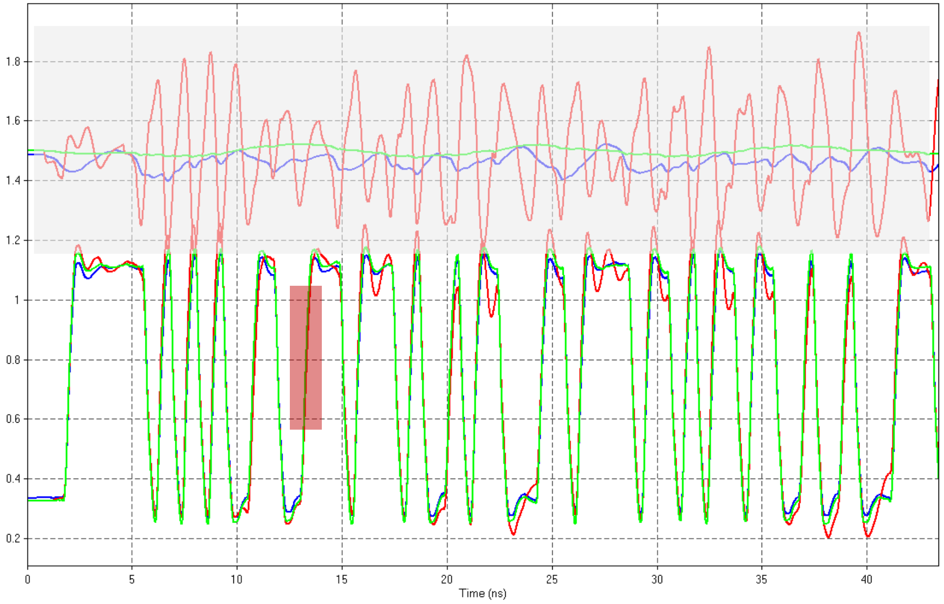
- What is IO-SSO?
- Missing Components in Traditional IO-SSO Analysis
- Accurate On-die and Package Effects in IBIS Models
- Creating IBIS Models with On-die Interconnect
- **Case Study – IO-SSO Analysis with IBIS Models**
- Summary

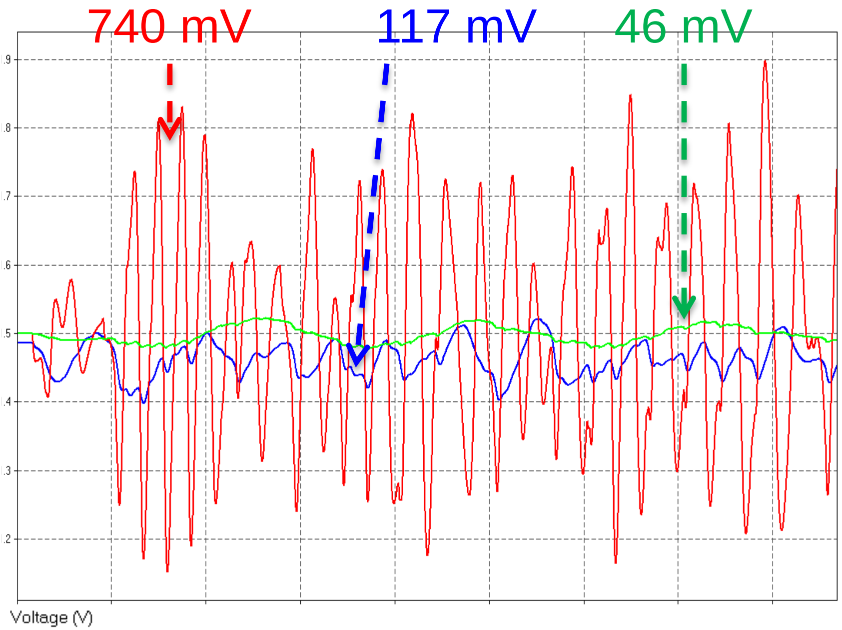
Case Study – IO-SSO Analysis with IBIS Models



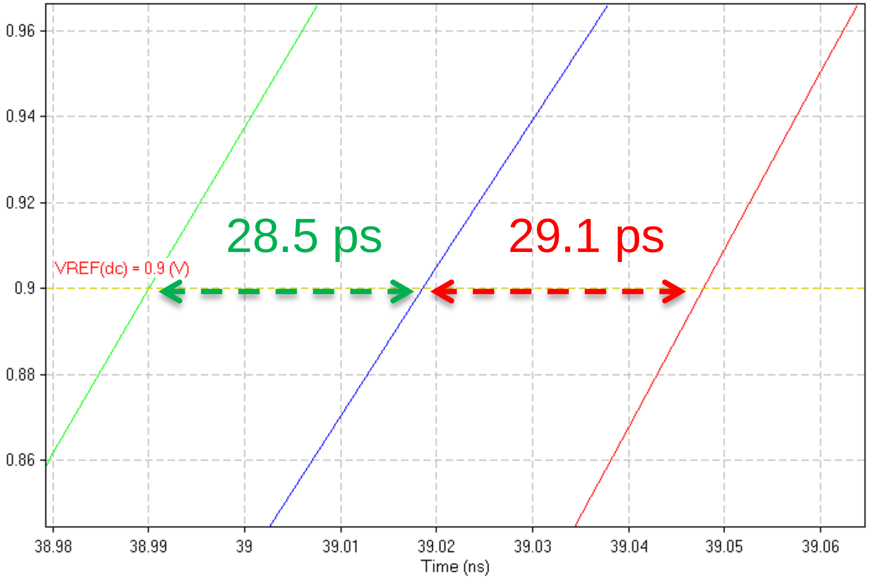
- I/O transistor circuit is converted into power-aware IBIS model
- Chip is extracted by chip level extractor which include RLCK elements.
- PCB and package S-parameters are extracted and converted to broadband SPICE models.
- Only 1 group DDR data is considered for this test

Case Study – IO-SSO Analysis with IBIS Models



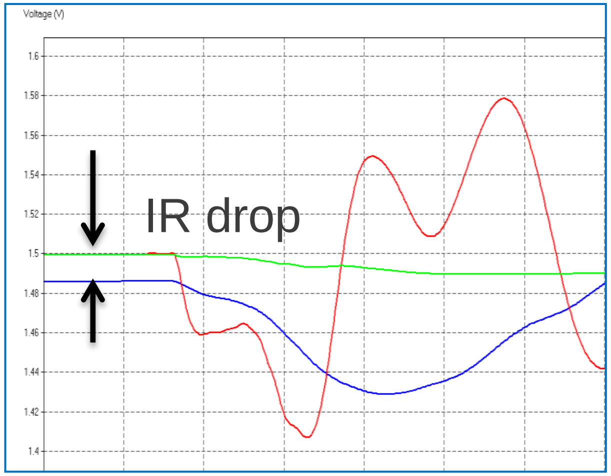


RED: without chip PDN
Green: with on-die RC
Blue: with distributed broadband model



- SSN from SSO will be over or under estimated without accurate chip IO model.
- Timing push in/out will become worse if more IOs are switching at the same time.

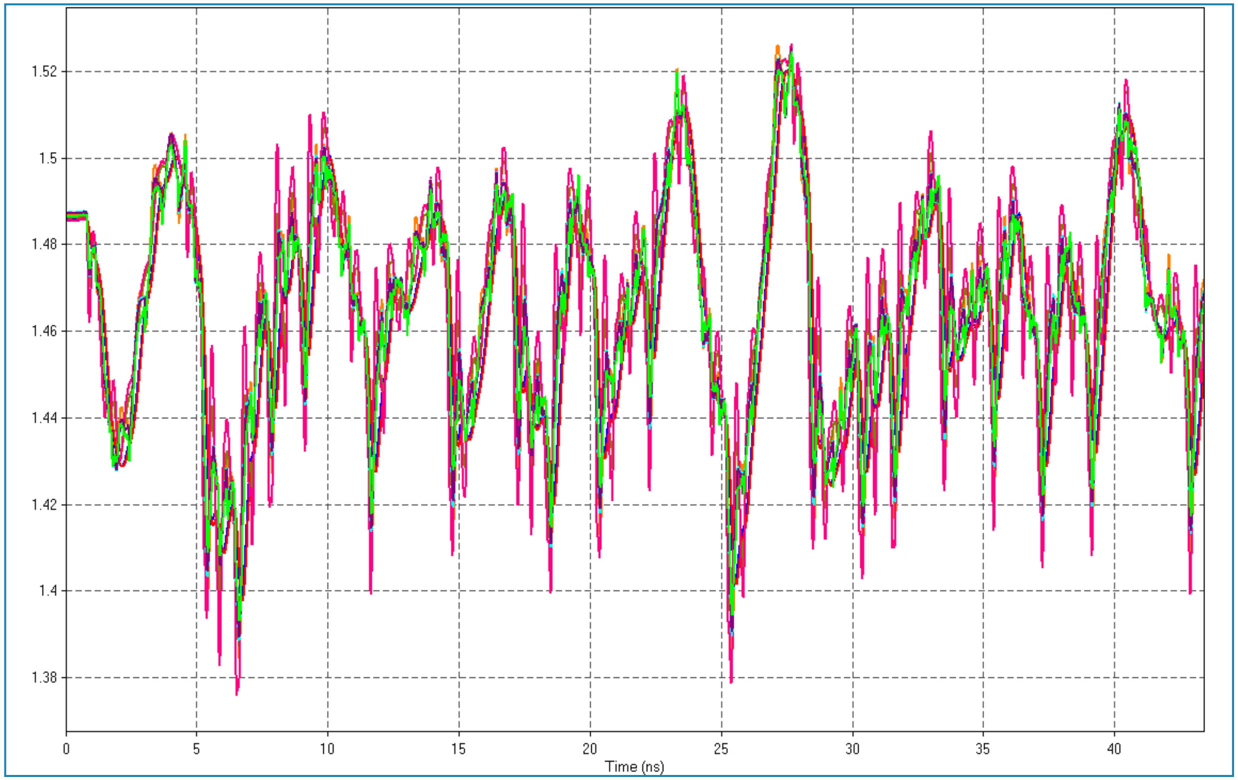
Case Study – IO-SSO Analysis with IBIS Models



RED: without chip PDN

Green: with on-die RC

Blue: with distributed broadband model



- IR drop becomes worse after including chip IO model.
- Noise level at each IO pad is different, which reveals the distributed behavior of the IO power deliver network.

Agenda

- What is IO-SSO?
- Missing Components in Traditional IO-SSO Analysis
- Accurate On-die and Package Effects in IBIS Models
- Creating IBIS Models with On-die Interconnect
- Case Study – IO-SSO Analysis with IBIS Models
- **Summary**

Summary

- For tighter timing and noise budgets in LPDDR3 or DDR4, system level IO-SSO analysis is helpful for design margin assessment

- IBIS 5.1 models may include power-aware IO buffer, chip P/G/S from IOs to bump pads, and arbitrary package models
  - existing IBIS syntax is applied (using [External Circuit])
  - additional techniques using ISS within the IBIS model are being discussed in committee

- The approach described allows chip vendors to deliver more complete IBIS models to their customers to enable faster and more accurate product design verification