# WELCOME FROM MICHAEL MIRMAK, INTEL CORPORATION

On behalf of the IBIS Open Forum, I would like to welcome you to the 2013 Asian IBIS Summit in Taipei. Thanks to you, our friends and colleagues on Taiwan, we have had three great events here since 2010, and we know we can make this year "lucky" as well for IBIS.

We are grateful to our generous co-sponsors ANSYS, Cadence Design Systems, Intel Corporation, IO Methodology, and Synopsys. Their assistance makes this event possible and we hope that you will encourage them to continue their support. Our thanks also go to our presenters and to you, the attendees, for your interest.

We hope that you enjoy the Summit and find the presentations and discussions useful. We wish you luck and success!

- Michael Mirmak
  Chair, IBIS Open Forum

各位 IBIS 開放論壇的与會代表，歡迎您参加我們的第三届亞洲 IBIS 台灣峰會。前兩次峰會的成功，這意味著我們正在建立一個“傳統”，也就是我們的 IBIS 的朋友和他的同事们在這裡的一年一度的技术讨论盛会。

我們非常感謝我們慷慨的赞助商 ANSYS， Cadence 設計系統公司，英特爾公司, IO Methodology (Avant) 和 Synopsys 公司。他們的協助使得本次活動成为可能，我們也希望他們能繼續支持以后的会议。我們還要感謝我們的演讲人和與會者的大力支持。

我們希望您能享受本次會議并發現有用的發言和討論。预祝本次会议圆满。也祝你好運和成功！

马梦宽
主席，IBIS 開放論壇

## WELCOME FROM DANIEL CHANG, ANSYS

Dear Experts,

On behalf of ANSYS, we would like to welcome you to join Asian IBIS Summit Taiwan and it is our pleasure can be the primary sponsor this year. We commend and thank you for taking time from your busy schedule to join us for this seminar.

Like the expectations of most of you, this seminar will help us through information on how the new technologies of IBIS improved and updated. The materials are designed to provide accurate and authoritative information. We also would like to extend a very special thanks to distinguished faculty of speakers who are experienced with the nuances and application of the IBIS models.

After a full day of new technologies and information update, we are sure that the experience of taking part in the seminar will be enriching. We eagerly await your participation in the seminar.

Thanks and regards

Daniel Chang
Regional Sales Director,
ANSYS Taiwan

尊敬的各位專家,

我仅代表 ANSYS 歡迎您参加亞洲 IBIS 台灣峰會，這是我們的榮幸能成为今年 IBIS 台灣峰會的主要贊助商。我們感謝您從百忙之中抽出時間来參加本次研討會。

和你的期望一樣，本次研討會將有助於我們通過的 IBIS 来讨论如何对新的技術进行改進和更新的信息。这些咨讯将对新的設計提供準確，權威的资料。我們特别感謝各位傑出的论文演讲者并他们在 IBIS 模型應用方面详细的經驗总结和讨论。

經過一整天的新技術和新信息的讨论，我們相信，本次研討會將给我们提供豐富的技术信息和經驗。我們熱切期待著您的參與研討會。

Daniel Chang

# AGENDA AND ORDER OF THE PRESENTATIONS

## (The actual agenda might be modified)

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I B I S  S U M M I T  M E E T I N G  A G E N D A

8:15 SIGN IN
- Vendor Tables Open at 8:30

9:00 **Welcome**
- Lance Wang
  (Vice-Chair IBIS Open Forum, IO Methodology, USA)
- Daniel Chang
  (ANSYS, ROC)

9:20 **Introducing IBIS 6.0** . . . . . **5**
Michael Mirmak (Intel Corporation, USA)

9:50 **IBIS Summary Documents** . . . . . **12**
Bob Ross (Teraspeed Consulting Group, USA)

10:20 BREAK (Refreshments and Vendor Tables)

10:45 **Modeling, Extracting and Verification of VCSEL Model for** . . . . . **18**
IBIS AMI
Zhaokai Yuan (Agilent technologies, PRC)

11:20 **Anisotropic Substrate for IBIS-AMI Simulation** . . . . . **26**
Naijen Hsuan (ANSYS, ROC)

12:00 FREE BUFFET LUNCH (Hosted by Sponsors)
- Vendor Tables

# AGENDA AND ORDER OF THE PRESENTATIONS (Continued)



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# Introducing IBIS 6.0

Michael Mirmak
Intel Corp.
Chair, IBIS Open Forum

Presented by Lance Wang
Vice-Chair, IBIS Open Forum

Asian IBIS Summit
Taipei, Taiwan
November 19, 2013

http://www.eda.org/ibis/



# Agenda

- IBIS 6.0 in Summary
  - Key Features
  - Changes from IBIS 5.1
- What problems does 6.0 address?
- Issues to Resolve
- What's Next?
- Questions

# Key Features of IBIS 6.0

- IBIS 6.0 was approved September 20, 2013
  - http://www.eda.org/ibis/ver6.0/
- Major additions focus on IBIS-AMI
  - Adds redriver and retimer support
  - Expands jitter/noise parameters
  - Clarifies analog buffer impedance descriptions
  - Supports IBIS-ISS (Interconnect SPICE Subcircuits) and Touchstone 1.x/2.0

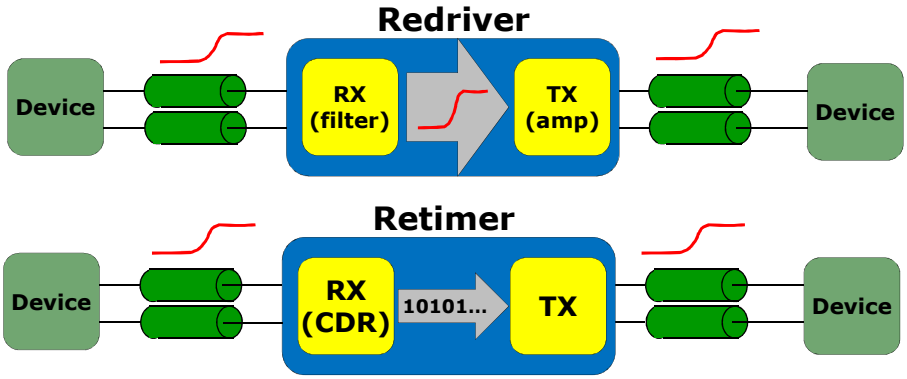


# Other Changes from IBIS 5.1

- Clarifications of A/D and D/A converters in [External Model] and [External Circuit]
  - Parameter passing now supported!
- Additional files supported for IBIS-AMI
  - Including explicit paths
  - Identifiers for individual IBIS-AMI model instances
- List Tips for IBIS-AMI Lists
  - Associates labels with parameter lists
- Improved organization of the document
  - Easier to read and use

# IBIS 6.0 Support Examples

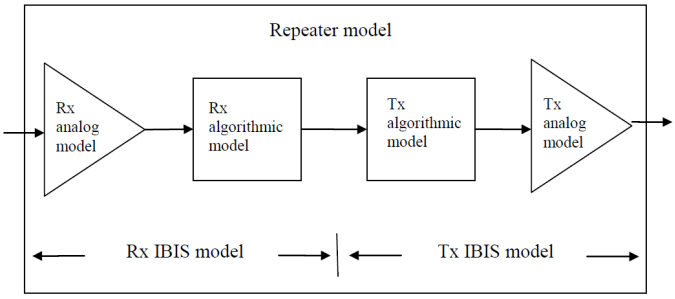
- How do I model a mid-bus repeater?
  - Recall the repeater types: retimers and redrivers
  - Think of redriver as filtering and/or amplifying analog *signals*
  - Think of retimer as using clock-data recovery to re-transmit *data*






# IBIS 6.0 Support Examples

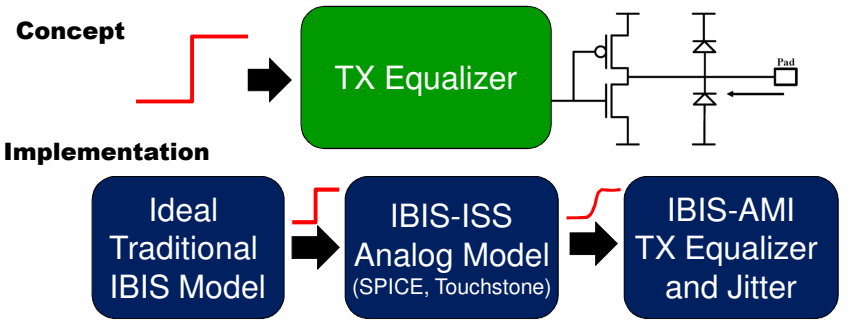
- How do I model a mid-bus repeater?
  - Use [Repeater Pin] to identify RX and TX pins
  - Define “Redriver” or “Retimer” in the .ami parameters file under “Repeater_Type”
  - For Retimers, ensure AMI_GetWave is defined and included




*from the IBIS 6.0 specification*

# IBIS 6.0 Support Examples

- Where to "put" the analog impedance of the buffer?
- What if I can't easily represent the analog behavior of my buffer using traditional IBIS?
  - In 6.0, use IBIS-ISS to represent complex analog buffer behavior
  - Traditional IBIS becomes ideal (TX or RX)

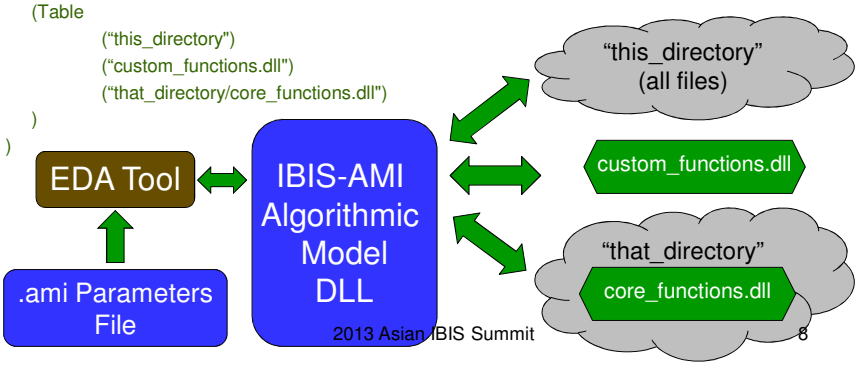





# IBIS 6.0 Support Examples

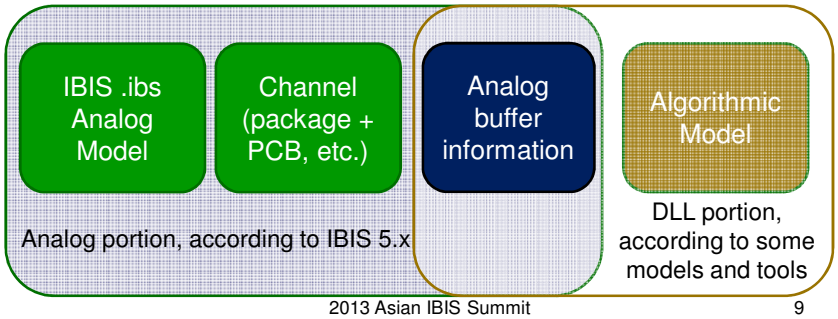
- What if your algorithmic model isn't a single file?
  - Multiple files, in different locations, now supported
  - From the .ami parameters file…

```
(Supporting_Files (Usage Info) (Type String)
   (Description "Additional files and directories required by this model")
   (Table
         ("this_directory")
         ("custom_functions.dll")
         ("that_directory/core_functions.dll")
   )
)
```



# Issues to Resolve

- Ensuring true IBIS-AMI model compatibility
  - Some models under IBIS 5.x place buffer analog information in the executable (DLL or SO file)
  - This may be a problem for some tools
  - Use of IBIS 6.0 improved analog modeling can help ensure portability

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# Issues to Resolve

- Ensuring true IBIS-AMI model compatibility
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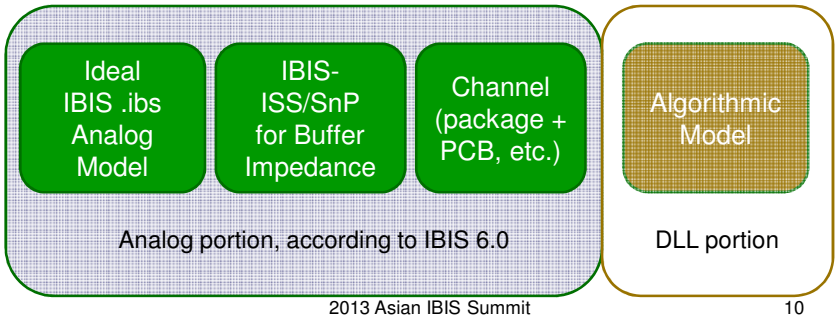


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# Issues to Resolve

- Improving IBIS packages
  - Two separate approaches being discussed
  - Objective is to finalize a package model format that…
    - *Can interact with IBIS and related files*
    - *Supports time- and frequency-domain modeling data in IBIS-ISS format*
    - *Supports arbitrary numbers of crosstalking signal lines in individual segments*
  - Target is to include this in the next major IBIS release



# What's Next?

- A parser: IBISCHK6
  - Check new keyword syntax
  - Check new IBIS-AMI parameter syntax
  - Simple checks for IBIS-AMI DLL/SO executables?
    - *Are the required IBIS-AMI functions present?*
    - *Do the functions execute (instead of crashing)?*
- Is a parser for IBIS-ISS required?
  - SPICE features used in IBIS-ISS are very common across EDA tools
- IBIS version updates
  - IBIS continues to target updates twice per year

# Questions?


# IBIS Summary Documents

Bob Ross
Asian IBIS Summit, Taipei, Taiwan
November 19, 2013
bob@teraspeed.com

(originally presented November 15, 2013)
(presented by Anders Ekholm, Ericsson)

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## Document Samples

- Keyword Hierarchy tree in IBIS Version 6.0, Section 3.1
- Expanded Keyword Hierarchy tree
- Evolution document
- IBIS-AMI parameter tables in IBIS Version 6.0, Section 10.7
- These documents summarize the IBIS elements

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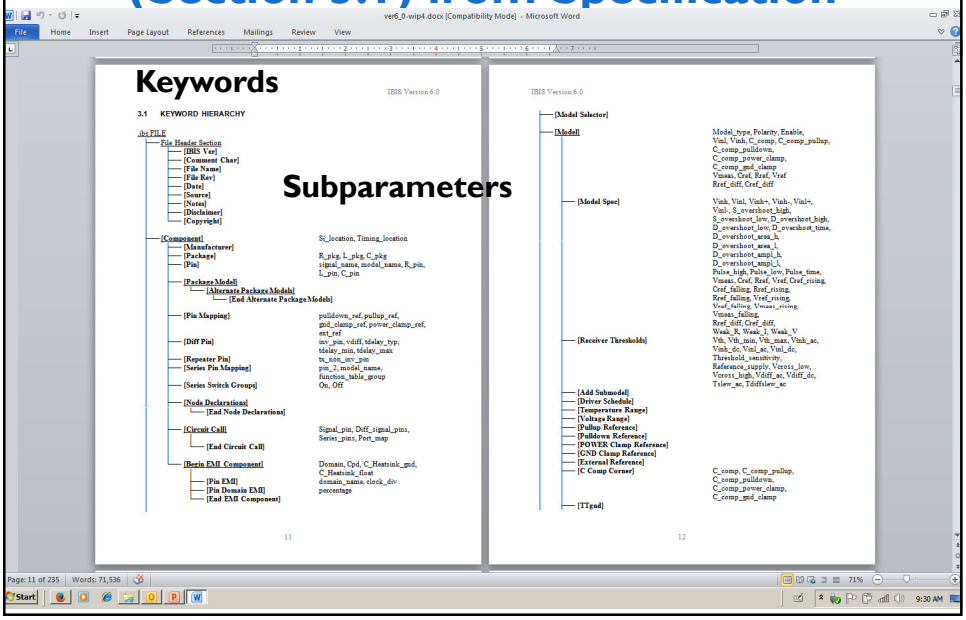
# Official Keyword Hierarchy (Section 3.1) from Specification




# Unofficial Keyword Hierarchy Updated from September, 2007

- Keyword Hierarchy tree
  - 165 distinct keyword usages
  - Some keywords are re-used in different contexts (e.g., [IBIS Ver], [End], [Rising Waveform], etc. and in .ibs, .pkg and .ebd files)
- Hierarchy documents updated with Version 5.1 and Version 6.0 information



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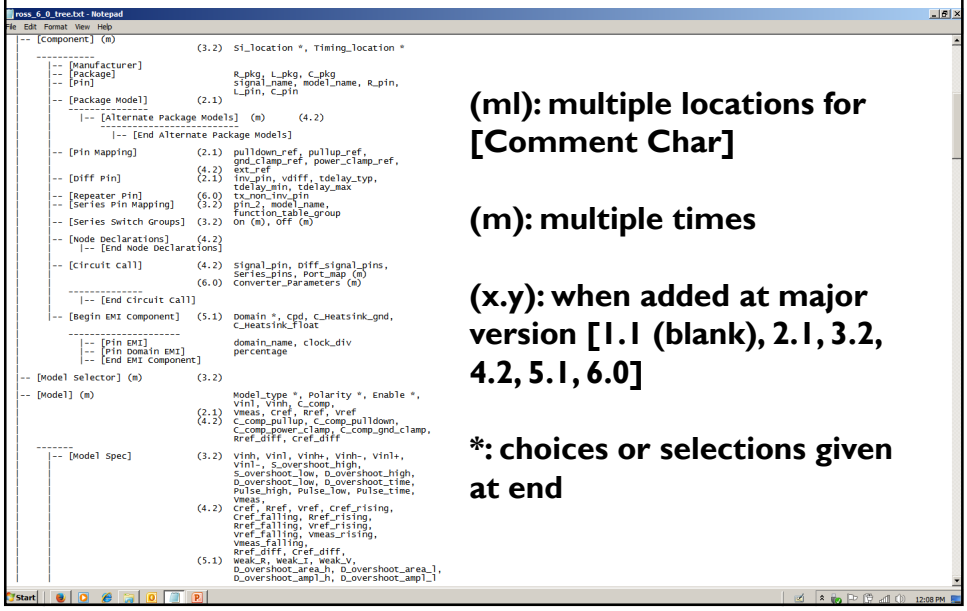
# Unofficial Keyword Hierarchy Tree with Extra Information



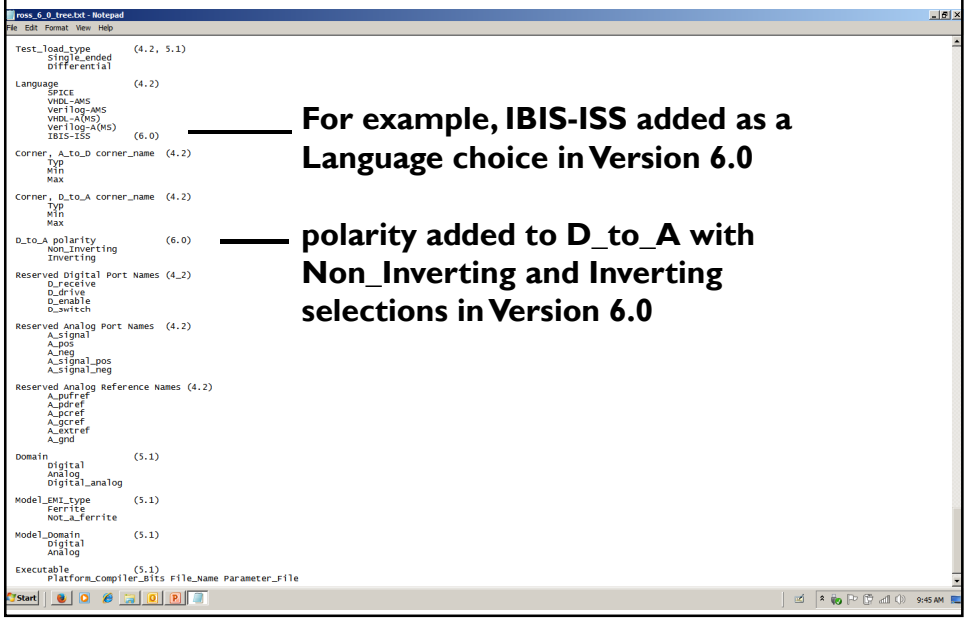

**(ml): multiple locations for [Comment Char]**

**(m): multiple times**

**(x.y): when added at major version [1.1 (blank), 2.1, 3.2, 4.2, 5.1, 6.0]**

***: choices or selections given at end**

# Enumerated Choices at End




**For example, IBIS-ISS added as a Language choice in Version 6.0**

**polarity added to D_to_A with Non_Inverting and Inverting selections in Version 6.0**

# Unofficial Evolution Document

- Evolution document features:
  - Updated columns show major version evolution
  - Rules and changes evolution
  - Significant subparameter selections such as the *_type subparameter choices
- Hierarchy and Evolution documents contain overlapping information, but expanded Hierarchy document has more detail
- Sample page shown next



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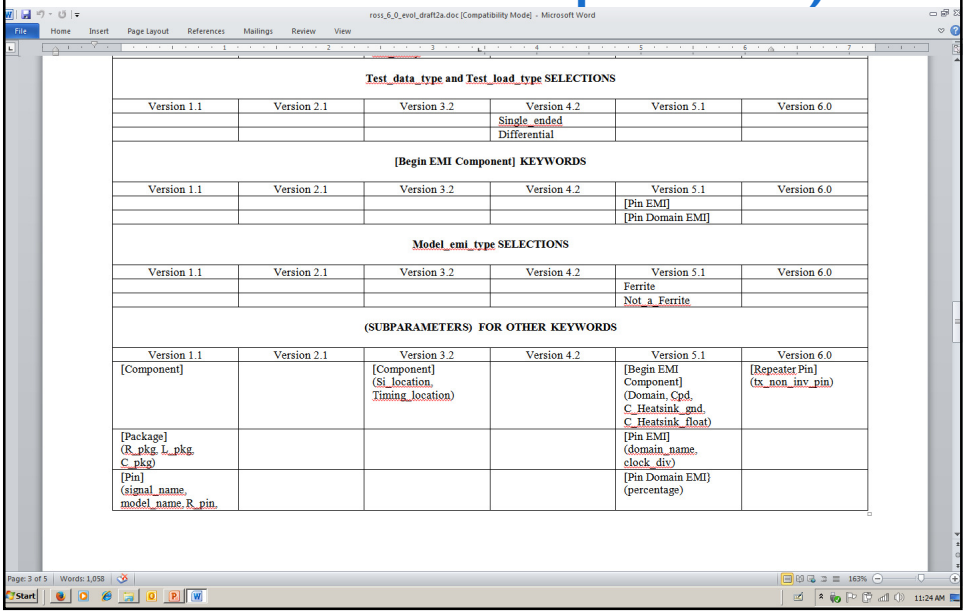
# Evolution Document (*_type, EMI Information and Repeater Pin)



**Test_data_type and Test_load_type SELECTIONS**

| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0 |
|---|---|---|---|---|---|
| | | | Single_ended | | |
| | | | Differential | | |

**[Begin EMI Component] KEYWORDS**

| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0 |
|---|---|---|---|---|---|
| | | | | [Pin EMI] | |
| | | | | [Pin Domain EMI] | |

**Model_emi_type SELECTIONS**

| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0 |
|---|---|---|---|---|---|
| | | | | Ferrite | |
| | | | | Not_a_Ferrite | |

**(SUBPARAMETERS) FOR OTHER KEYWORDS**

| Version 1.1 | Version 2.1 | Version 3.2 | Version 4.2 | Version 5.1 | Version 6.0 |
|---|---|---|---|---|---|
| [Component] | | [Component] (Si_location, Timing_location) | | [Begin EMI Component] (Domain, Cpd, C_Heatsink_gnd, C_Heatsink_float) | [Repeater Pin] (tx_non_inv_pin) |
| [Package] (R_pkg, L_pkg, C_pkg) | | | | [Pin EMI] (domain_name, clock_div) | |
| [Pin] (signal_name, model_name, R_pin, | | | | [Pin Domain EMI] (percentage) | |

# IBIS-AMI .ami File Parameter Syntax (Section 10.3)

(<parameter_name>
(**Usage** <usage>) | required
(**Type** <data_type>) | required
({**Format**} **<data_format>** <data>) | required *

(**List_Tip**) | optional with ({Format} **List**)
(**Default** <value>) | optional or illegal *
(**Description** <string>) | optional
)

* **Value** or **Default**, but not both, and other rules





# New - Four Summary Tables in Section 10.7 of the Specification

- **Usages** for **Reserved Parameters**
- **Types** for **Reserved Parameters**
- **Formats** for **Reserved Parameters**
- **Types** for **Format** values
- 28 **Reserved Parameters**, 18 new since Version 5.1
- Part of one table shown next

# IBIS-AMI Reserved Parameters and Allowable Data Types

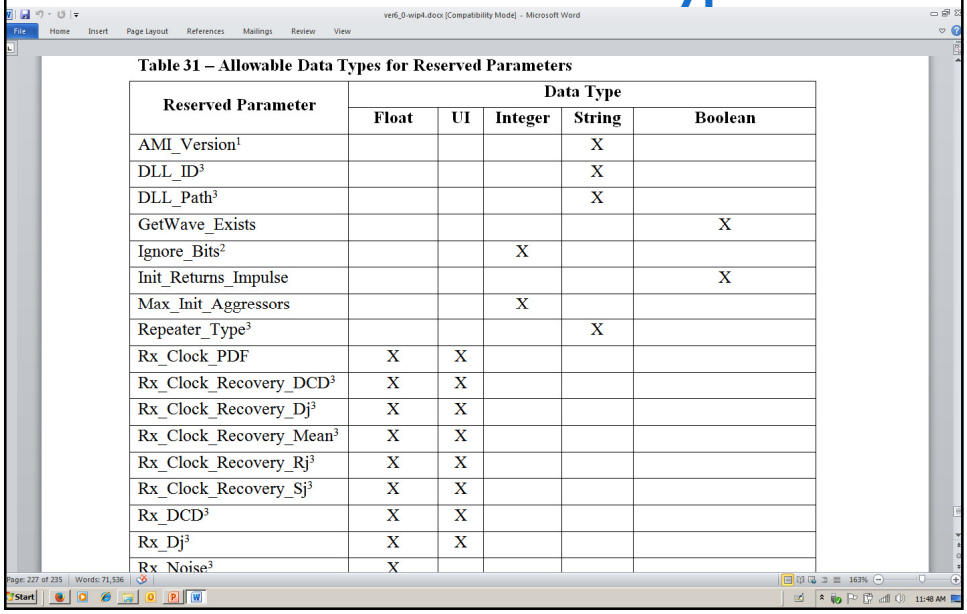


Table 31 – Allowable Data Types for Reserved Parameters

| Reserved Parameter | Data Type | | | | |
|---|---|---|---|---|---|
| | Float | UI | Integer | String | Boolean |
| AMI_Version[1] | | | | X | |
| DLL_ID[3] | | | | X | |
| DLL_Path[3] | | | | X | |
| GetWave_Exists | | | | | X |
| Ignore_Bits[2] | | | X | | |
| Init_Returns_Impulse | | | | | X |
| Max_Init_Aggressors | | | X | | |
| Repeater_Type[3] | | | | X | |
| Rx_Clock_PDF | X | X | | | |
| Rx_Clock_Recovery_DCD[3] | X | X | | | |
| Rx_Clock_Recovery_Dj[3] | X | X | | | |
| Rx_Clock_Recovery_Mean[3] | X | X | | | |
| Rx_Clock_Recovery_Rj[3] | X | X | | | |
| Rx_Clock_Recovery_Sj[3] | X | X | | | |
| Rx_DCD[3] | X | X | | | |
| Rx_Dj[3] | X | X | | | |
| Rx_Noise[3] | X | | | | |

# Conclusion

- Summary information provides quick references for IBIS and IBIS-AMI syntax
- Document references

  http://www.eda.org/ibis/ver6.0/

  **ver6_0.docx, .pdf** (official specification)

  **tree_6_0.txt** (unofficial)

  **evol_6_0.docx, .pdf** (unofficial)





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# Modeling, Extraction and Verification of VCSEL Model for IBIS AMI

Asian IBIS Summit
Taipei, Taiwan
November 19, 2013

Zhaokai YUAN
Agilent Technologies, Inc.

Agilent Technologies

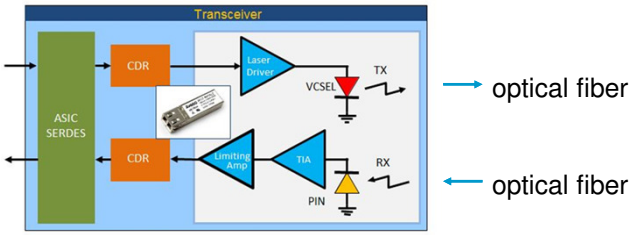
## Outline

- Introduction
  - Optical Link Simulation
  - VCSEL(Vertical Cavity Surface Emitting Laser) simulation under IBIS-AMI
- VCSEL Modeling and Extraction
  - Thermal based modeling
  - Curve fitting algorithm
- VCSEL Verification
  - Test case including VCSEL device
  - The comparison between simulation and measured data

Agilent Technologies

## Introduction
## *Optical Link System and Simulation(cont.)*

- Optical Link Simulation




**Inside SerDes Tx & Rx**

- Equalization (FFE, CTLE & DFE)
- Clock-data recovery (CDR)

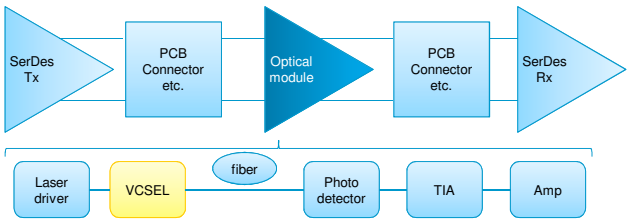
**Inside optical module**

- Input voltage signal drives VCSEL to emit photons
- Photons propagate along optical fiber
- Photons are converted into photocurrent in PIN
- TIA converts current into output voltage



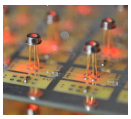
## Introduction
## *Optical Link System and Simulation(cont.)*

- Extending AMI to Optical Channel
  - Treat the entire optical module as a mid-channel repeater
  - Encapsulate all optical behaviors inside the optical model
  - Extend AMI simulation to include repeater



## Introduction
## *VCSEL Basic*

- VCSEL(Vertical Cavity Emitting Laser)
  - Characteristics
    - High Data Rate, up to 40GHz(state of art)
    - Low power cost(input ~ mA, output ~ mW)
    - Single-longitudinal-mode operation
    - Suitability for monolithic 2-D integration
  - Application
    - Very short range data transmission
    - Board to board data transmission



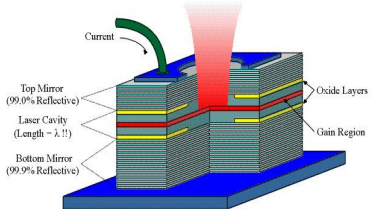


## Introduction
## *VCSEL Basic*

- VCSEL modeling
  - 3-D modeling and simulation
    - From the principle of laser point of view
    - Accurate but too complicated
  - SPICE simulation
    - As VCSEL is an optical device, SPICE model may not be the initial design, a new SPICE schematic is needed
    - Hard to communicate due to IP issue
  - IBIS-AMI(Algorithmic Modeling Interface)
    - Focusing on performance only
    - Treat the VCSEL as an algorithm unit

# VCSEL Modeling and Extraction
## *VCSEL Modeling*

- Modeling Principle
  - VCSEL's performance vs. Thermal behavior
  - Data flow based
  - The relationship between input current(I) and output power(Po) under the effect of temperature(T)
  - Peripheral simulation
  - Working schematic






# VCSEL Modeling and Extraction
## *VCSEL Modeling*

- Rate-Equation-Based Thermal VCSEL Model
  - Transient Analysis

$$P_o = kS$$

$$\frac{dS}{dt} = -\frac{S}{\tau_p} + \frac{\beta N}{\tau_n} + \frac{G_o(N-N_o)S}{1+\varepsilon S}$$

$$\frac{dN}{dt} = \frac{\eta_i(I-I_{off}(T))}{q} - \frac{N}{\tau_n} - \frac{G_o(N-N_o)S}{1+\varepsilon S}$$

Rate Equation

$$I_{off}(T) = a_0 + a_1T + a_2T^2 + a_3T^3 + a_4T^4$$

$$T = T_o + (IV - P_o)R_{th} - \tau_{th}\frac{dT}{dt}$$

$$V = \begin{cases} (b_0 + b_1T + b_2T^2)(c_0 + c_1I + c_2I^2) \\ (c_0 + c_1I + c_2I^2 + c_3I^3 + c_4I^4 + c_5I^5 + c_6I^6) \\ AI + B\ln(1 + \frac{I}{C}) \end{cases}$$

  - Stationary Analysis

$$P_o = \eta(I - I_{itho} - I_{off}(T))$$

$$I_{off}(T) = a_0 + a_1T + a_2T^2 + a_3T^3 + a_4T^4$$

$$T = T_o + (IV - P_o)R_{th}$$

$$V = \begin{cases} (b_0 + b_1T + b_2T^2)(c_0 + c_1I + c_2I^2) \\ (c_0 + c_1I + c_2I^2 + c_3I^3 + c_4I^4 + c_5I^5 + c_6I^6) \\ AI + B\ln(1 + \frac{I}{C}) \end{cases}$$

## VCSEL Modeling and Extraction
## *VCSEL Extraction*

- Extraction Basics
  - VCSEL's performance ↔ Parameter values in rate equations
  - Measured curves
    - LI ~ Po(I; T)
      - Measured stationary, shows the relationship between input current and the output power under different ambient temperature
    - VI ~ V(I; T)
      - Measured stationary, shows the relationship between input current and the voltage for connection, also with effect of ambient temperature
    - Frequency response ~ H(w)
      - Measured stationary, shows the frequency response, reveals the signal transmission characteristics

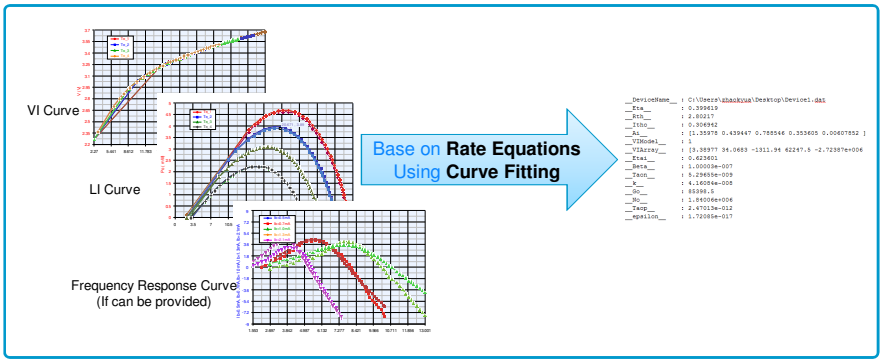


## VCSEL Modeling and Extraction
## *VCSEL Extraction*

- Extraction Method
  - Curve Fitting Algorithm
    - LS curve fitting
      - Just solve the matrix equations
      - Suitable for simple relationship equations, such as the polynomial
      - Accurate and less time cost
    - Minimal gradient curve fitting
      - Try to find the certain set of values which can generate the smallest error
      - Suitable for more complex equations, especially with iterations
      - Need some pre-knowledge of the range of the parameters
      - More time cost for accuracy

# VCSEL Modeling and Extraction
## *VCSEL Extraction*

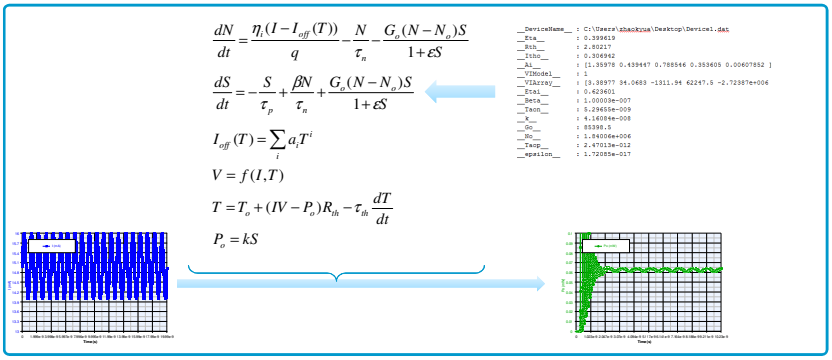
- Schematic





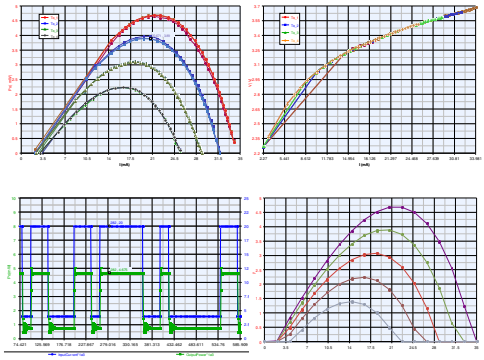

# VCSEL Verification

- VCSEL Simulation
  - Parameter values in rate equations ↔ VCSEL's performance
  - Schematic



## VCSEL Verification

- Case 1 ~ device verification
  - 863-nm bottom-emitting VCSEL, 16-mm diameter
  - Extraction
    - Curves fitting result
      - LI and VI curve
    - Behavior mode is generated with file format
  - Simulation
    - Po(I) under different To
    - Response for large signal



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## VCSEL Verification

- Case 2 ~ device verification
  - 3.1um diameter thin-oxide-aperture VCSEL
  - Extraction Result
    - Curves fitting result
      - LI(Fig 1)
      - VI(Fig 2)
      - Freq. response(Fig3)
    - Simulation
      - Po(I) simulation (Fig4)
      - Frequency response(Fig5)
      - Response for large signal(Fig6)

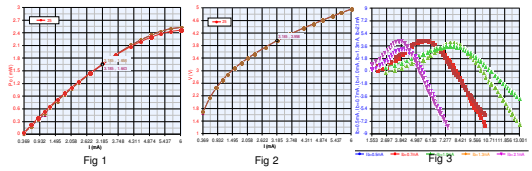

Fig 1 Fig 2 Fig 3

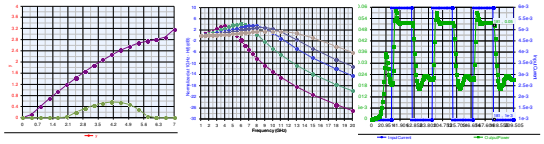

Fig 4 Fig 5 Fig 6

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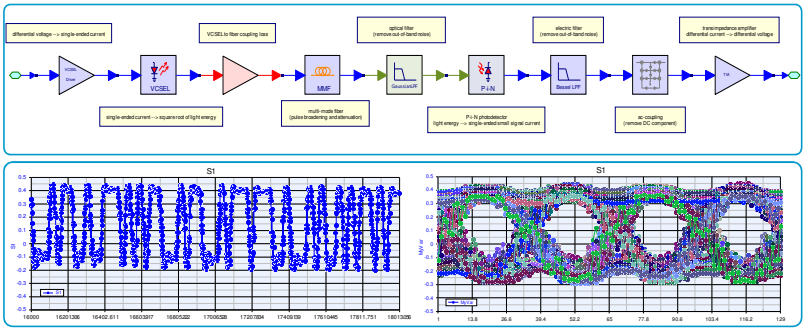
## VCSEL Verification

- Case 3 ~ optical link simulation
  - 25GHz signal transmission
  - A whole optical link: current → optical signal → current






## Thanks

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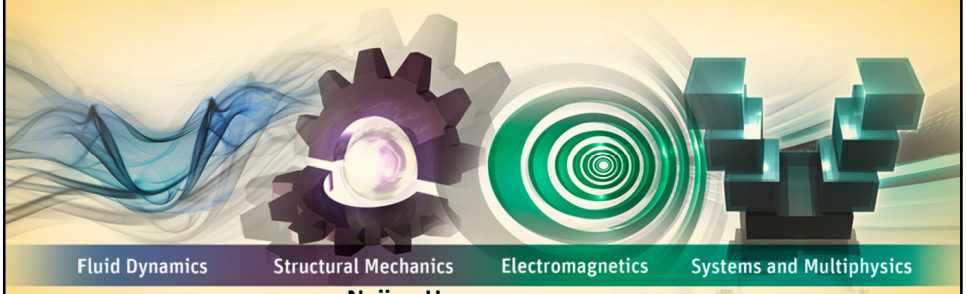
# Anisotropic Substrates Variance for *IBIS-AMI Simulation*




**Naijen Hsuan**
naijen.hsuan@ansys.com

***Asian IBIS Summit Taipei, Taiwan November 19, 2013***

ANSYS

## High speed Challenges Today

**(1) High Speed Data Rate Issue**

**(2) Anisotropic Substrates Variance**

**(3) FEM solution to analysis Anisotropic Substrates Variance**

**(4) Anisotropic Substrates Variance for IBIS-AMI Simulation**

**(5) DOE Solution**

## High speed IO Challenges Today

**As serial links become faster and more complex, it is ever more challenging to model the silicon in an accurate and efficient manner.**

**Models/Simulator need to handle current challenges:**

- **Need to accurately handle very high data rates**
- **Simulate large number of bits to achieve low BER**
- **Non-linear, Time Variant Systems**
- **TX/RX equalization**
- **Specific Data patterns and coding schemes**
- **Non-convergence due to unstable models**
- **Channel Issue**



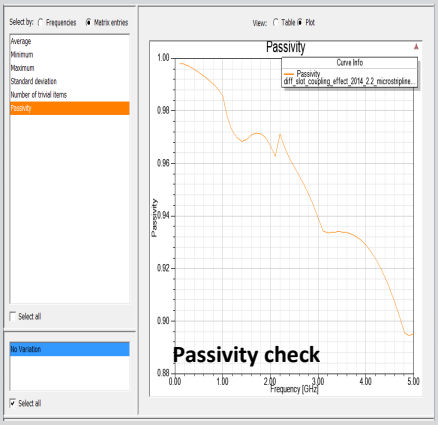
## Circuit Simulation Issues with S-parameters

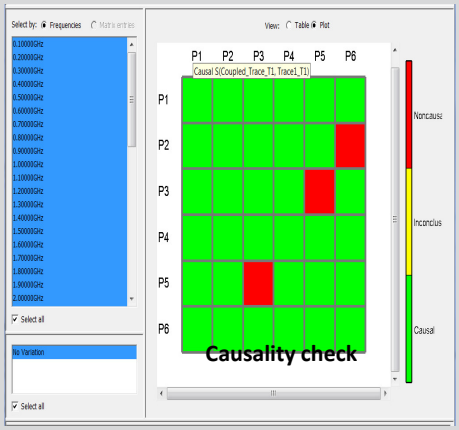
**Passivity and Causality**

- **Though S-parameters from a physics-based extraction tool should always be passive and causal, measured S-parameters often exhibit problems due to noise**
- **State-space model for S-parameter data guarantees causality of the circuit simulator model**
- **Two passivity enforcement algorithms**
  - **Convex programming**
  - **Perturbation**

## Check and Enforce Function

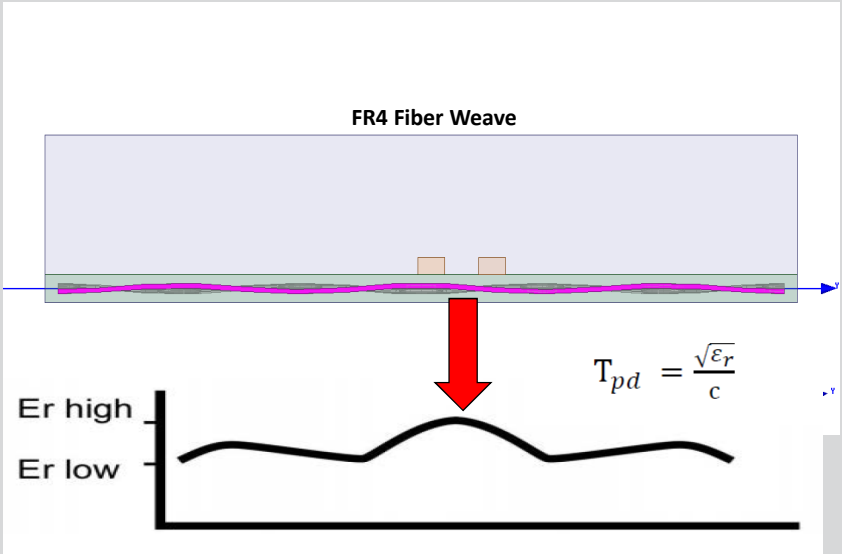
**Check and Enforce passivity and causality**



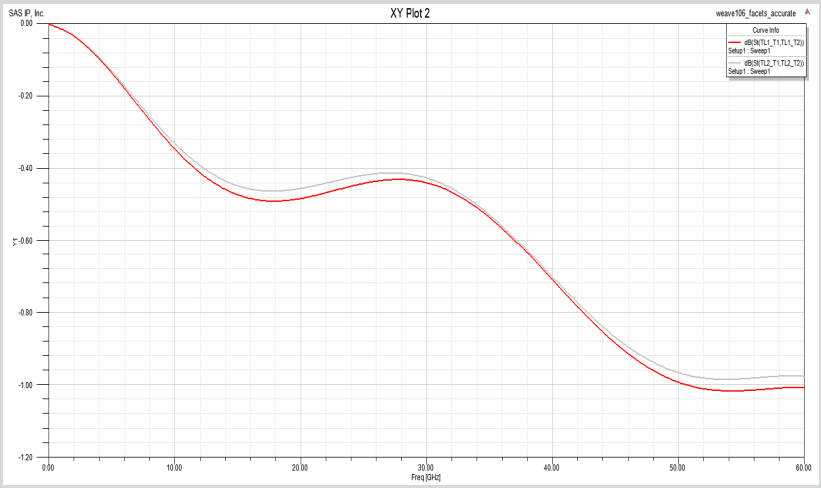






## Anisotropic Substrates

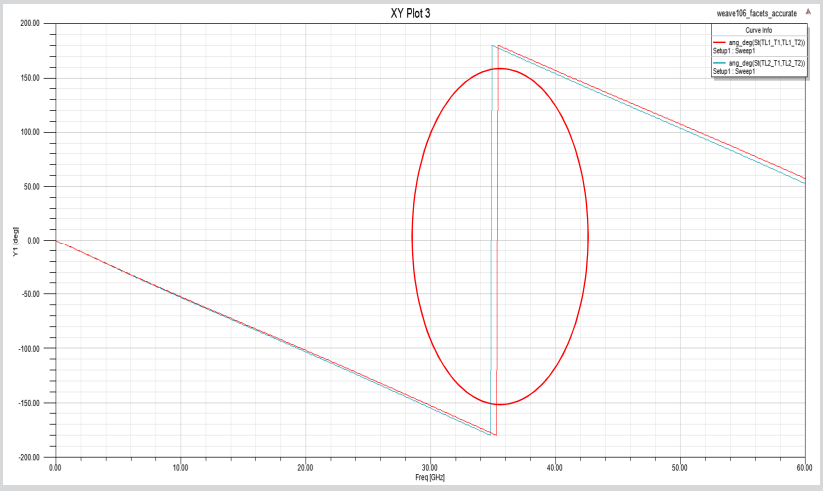


## Insertion loss for one net



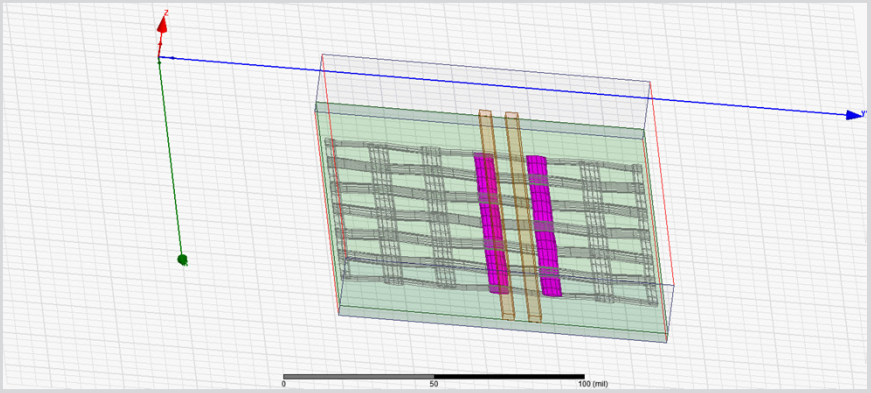

  

## Differential skew Problem



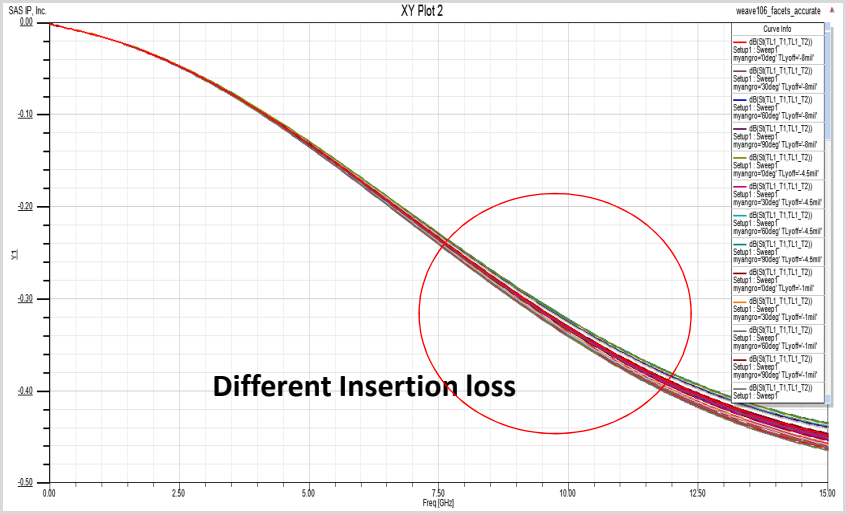
## Anisotropic Substrates Variance



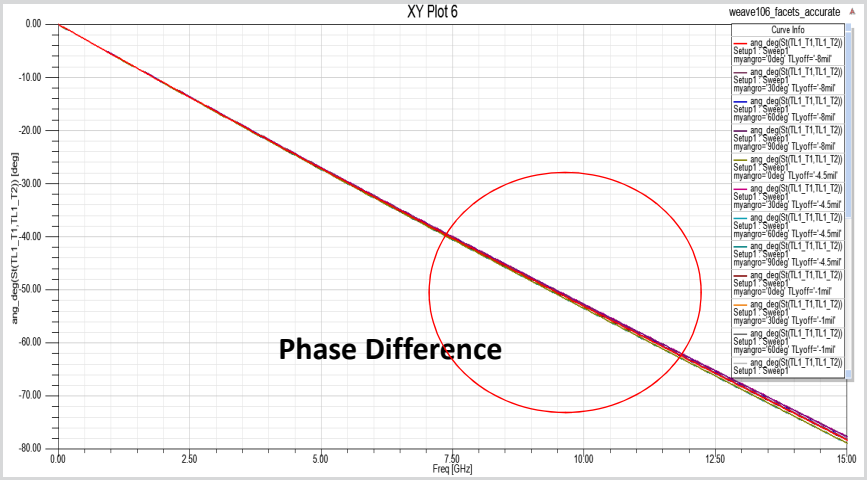

**Change degree angle of rotation**



## Anisotropic Substrates Variance

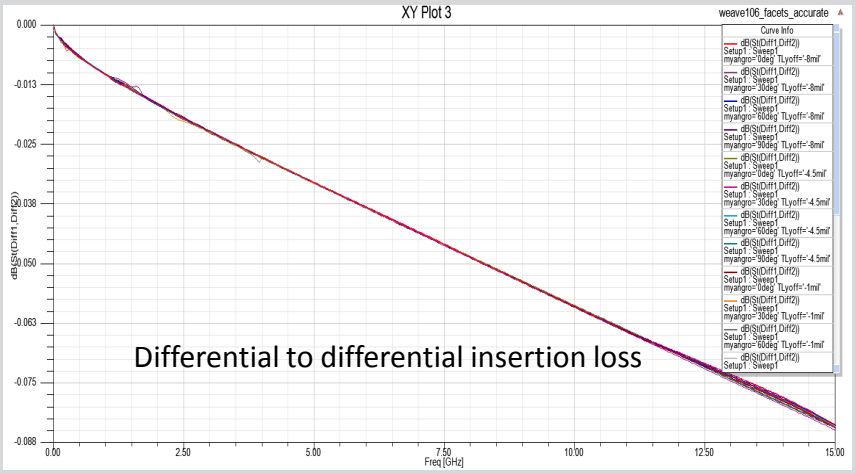


## Anisotropic Substrates Variance

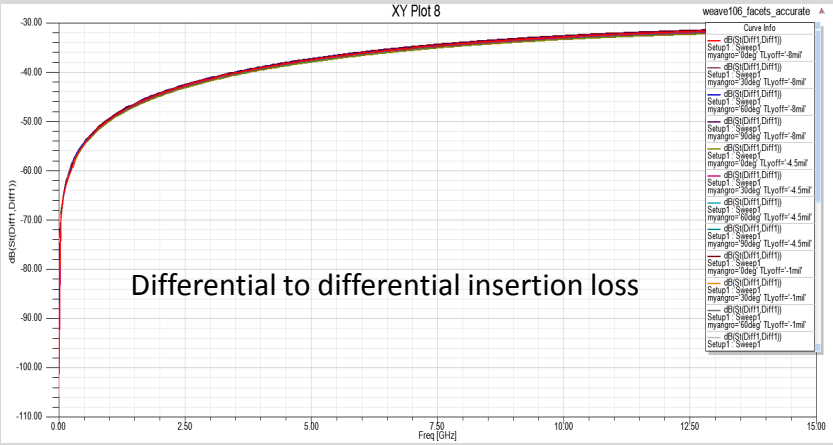





## Anisotropic Substrates Variance



## Anisotropic Substrates Variance



## IBIS-AMI and statistical eye analysis

- **Use the final impulse response from AMI analysis to run statistical eye analysis**
- **Linear modifications (AMI Init) from Tx and Rx AMI models taken into account**
- **AMI GetWave functionality cannot be used for statistical analysis as it is a purely time domain function**

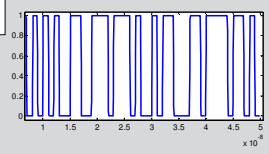
## Data flow

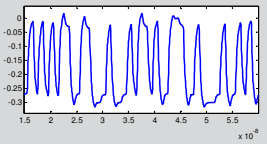
AMI Transmitter (Tx)

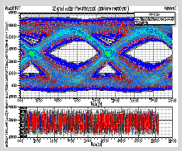
Linear Channel

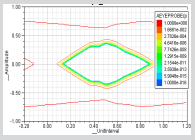
AMI Receiver (Rx)

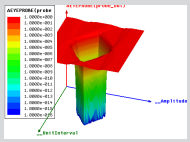
Engine post-processing











**Very similar to Fast Convolution**

- **No backward dependency**

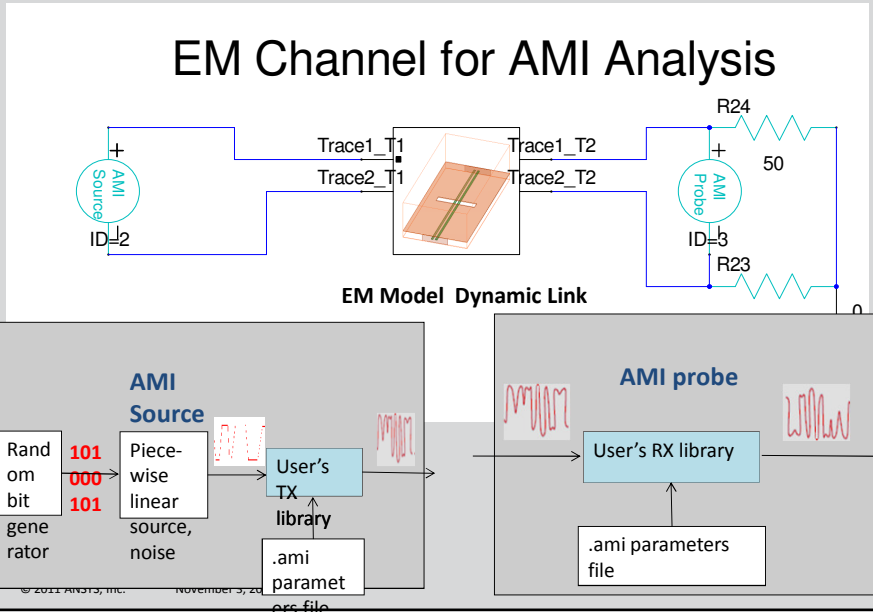
**Transmitter and receiver are based on user supplied libraries.**

**Channel is characterized with impulse response function(s)**

**All signals are sampled with the constant time step and handled in blocks.**

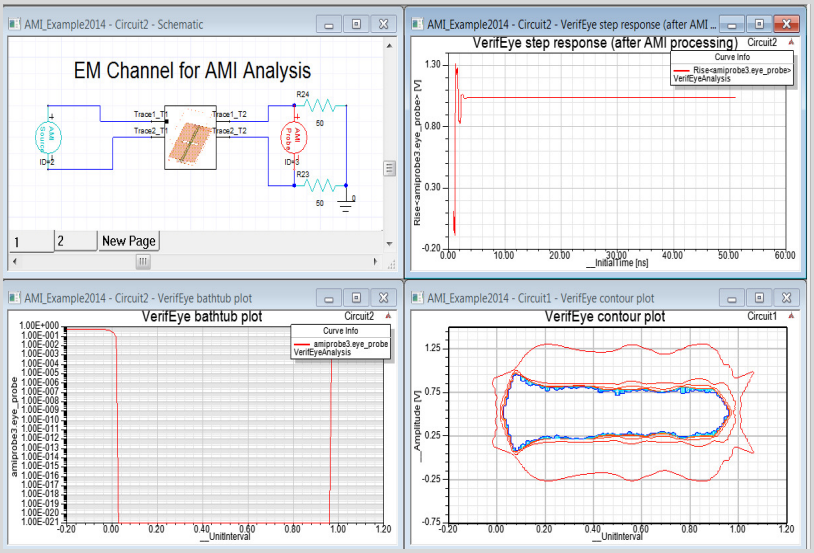
  

## EM and Circuit Co-simulation



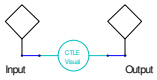
## Statistical Eye Analysis Result



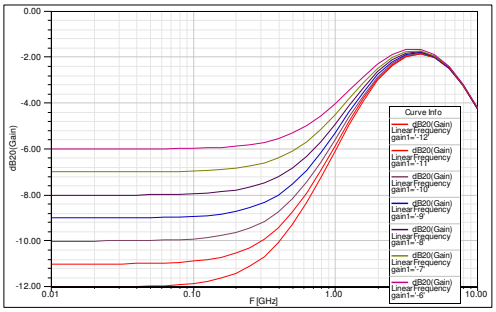



## Circuit equalization techniques problem

CTLE Gain with PCIe3.0 Parameters




This example shows the response plot of a CTLE for PCIe 3.0 for different values of gain. Parameters of the CTLE component are:
1. 'p1' LF Pole = 2 GHz
2. 'p2' HF Pole = 8 GHz
3. 'z' zero frequency = 'p1' * pow(10, 'gain'/20)
4. 'gain' DC gain in dB = gain1



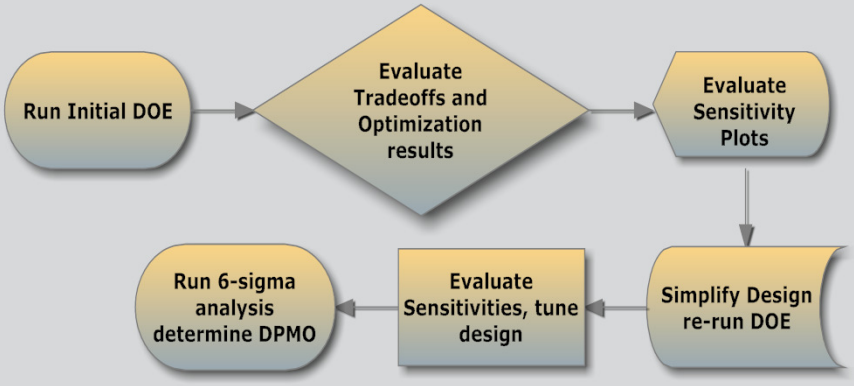

**How to decide gain and pole value ??**

## How to do that?

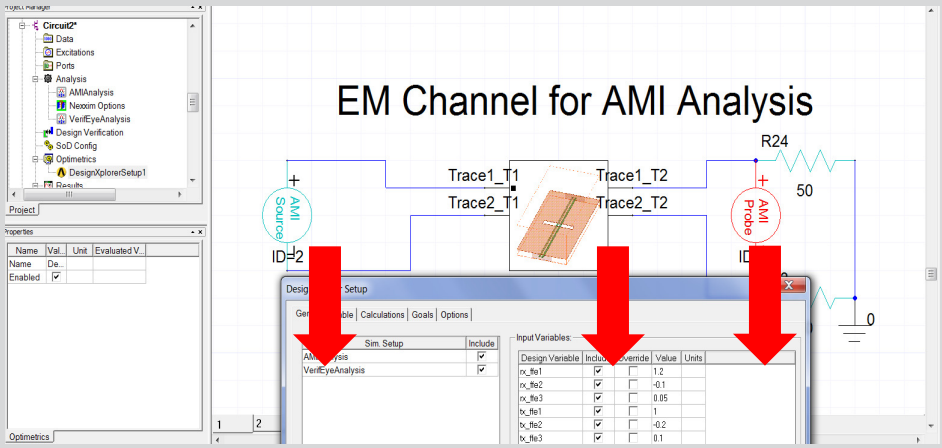
- Set up the DOE to sweep through the models to calculate the eye height and eye width for these cases
- The portions of the channel containing the PCB was modeled using a full-wave 3D electromagnetic extraction tool. A dynamic EM file was used to capture the channel's behavior. There are several variations of this structure that we want to include in the sensitivity analysis.
- To illustrate the results of this sensitivity analysis, we present sweeping of two of the variables: Change degree angle of rotation and equalization parameters



## DOE Methodology

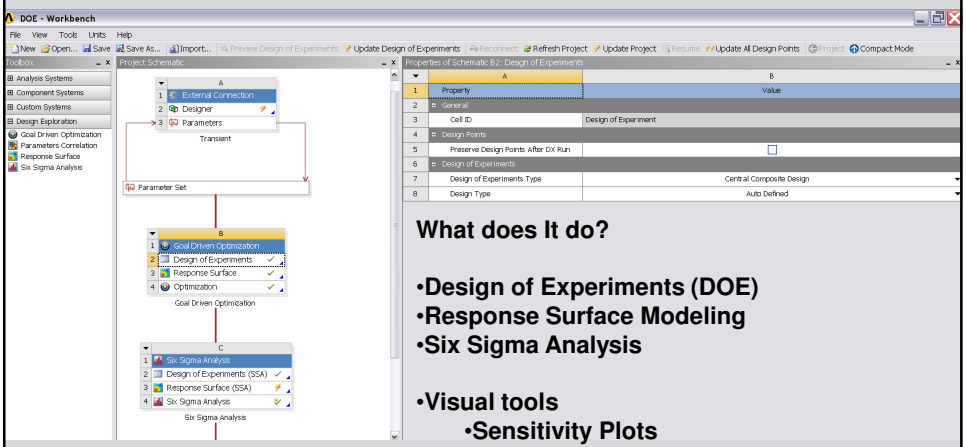


## DOE setup






## Any parametric analysis




**What does It do?**

- **Design of Experiments (DOE)**
- **Response Surface Modeling**
- **Six Sigma Analysis**

- **Visual tools**
  - **Sensitivity Plots**
  - **Correlation Matrices**
  - **Parallel charts w Pareto Front display**

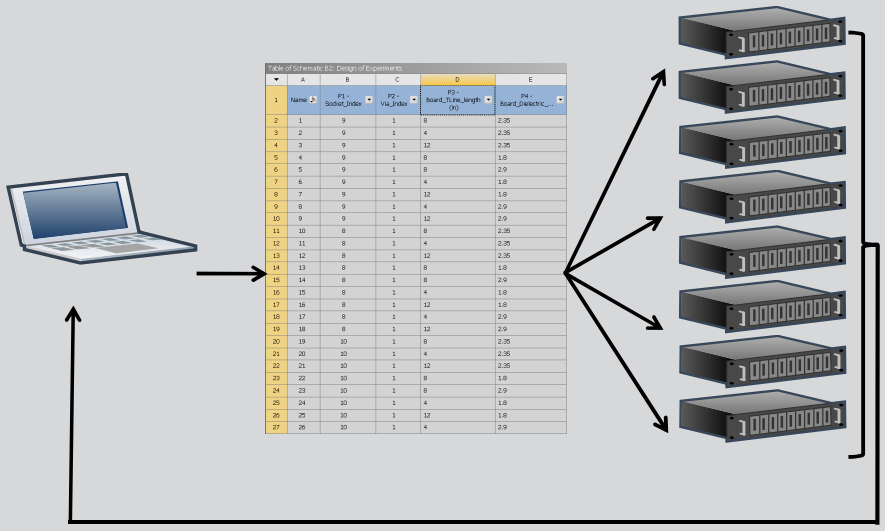
## Why Response Surface Modeling?

- Response Surface Modeling enables the designer to model and consider all aspects of a high speed channel design. Fit a statistical model to outputs of the design as a function of the change in input variables. A DOE table is used to select design points to solve explicitly for and the statistical model so to speak, "fills in the gaps"
- Optimized conditions and worst case scenarios are obtainable within the set of all possible design combinations within a realistic simulation timeframe.
- For example, this case, consider 8 variables or "factors", if each variable has only 5 variations or "levels" we are looking at a huge number of possible combinations in order to find optimal solutions and or worst case scenarios.

$$Combinations = Levels^{Factors} = 5^8!!!!$$



## Speed Issue – HPC solution



## Summary

- In this presentation, we can see the anisotropic substrates variance of PCBs, it effects phase difference between the differential pair
- Simulations on both EM dynamic models and IBIS-AMI models are applied to produce eye diagrams to check channel variance performance
- Circuit equalization techniques are applied at the Tx and Rx receiver to improve channel performance
- It is more efficient to get best channel performance by DOE and HPC solution

# More on IBIS Modeling for Load-Dependent Current-Mode Differential Drivers

Lance Wang (lwang@iometh.com)
IO Methodology Inc.
2013 IBIS Asian Summit
Nov. 19, 2013 Taipei

## Outlines

- Motivation
- Load-Dependent Current-Mode Differential Driver
- IBIS Extraction Method
  - Legacy method
  - Enhanced extraction method
- Summary

Note: The partial materials in this presentation have been presented in 2013 European IBIS Summit in Paris

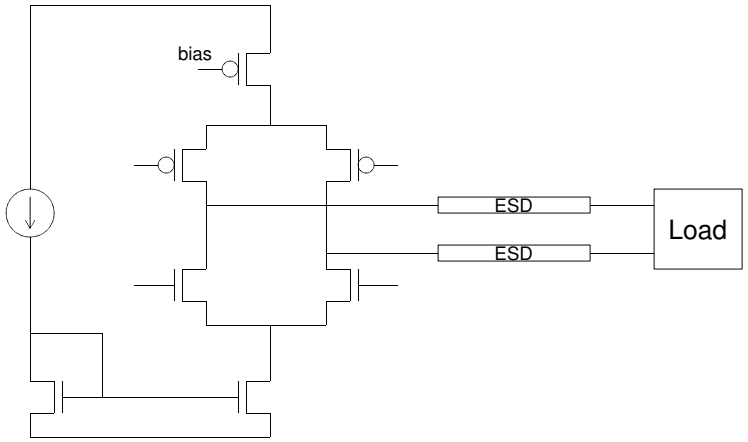
# Motivation

- Load-dependent current-mode differential pair buffers are found increasingly often in GHz serial link designs
  - Easy to control the output current and common-mode voltage
  - Often used in pre-emphasis buffers
- Using traditional IBIS buffer extraction method is not accurate enough

**Is it possible to use the current IBIS spec for this kind of differential buffer?**

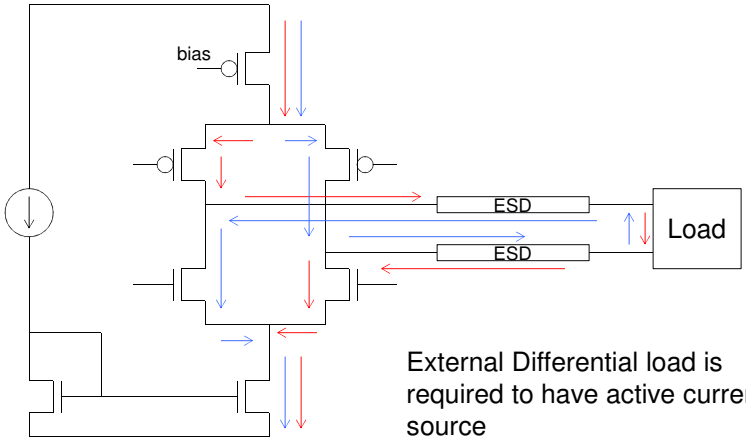
 

# Load-Dependent Current-Mode Differential Driver



# Load-Dependent Current-Mode Differential Driver (Current Flow)




External Differential load is required to have active current source




# IBIS Extraction Method (Modeling as 2 individual pins)

No load to be used for I-V curve extraction

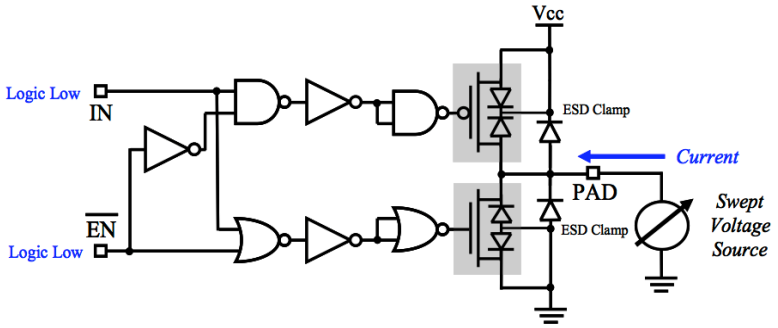



**Figure 3.1 – Standard 3-state Buffer (Pulldown I-V Table Extraction Shown)**

Pictures from IBIS cookbook

# IBIS Extraction Method (Modeling as 2 individual pins)

Load connected to GND or VCC to be used for V-T curve extraction

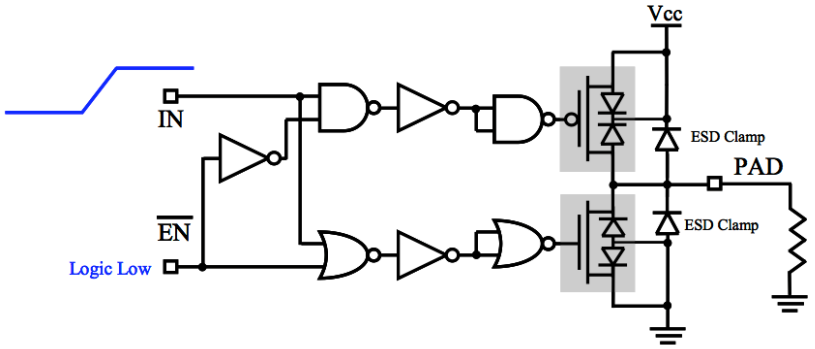


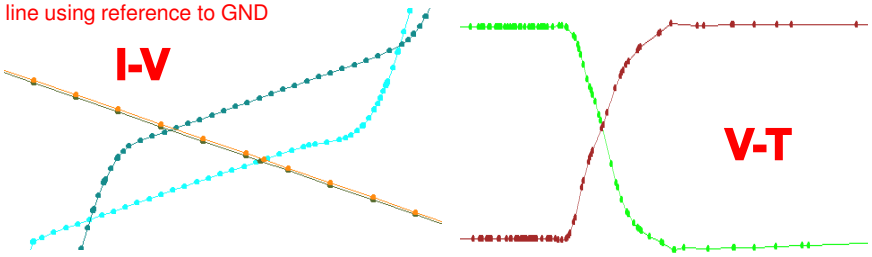

**Figure 3.2 – Simulation Setup for Extracting Ramp Rate Information (Rising Edge Shown)**

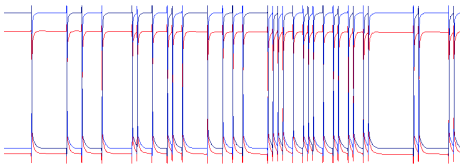
Pictures from IBIS cookbook

# Using normal extraction methods for I-V and V-T curves

* I-V curves shown are combined curves and load line using reference to GND

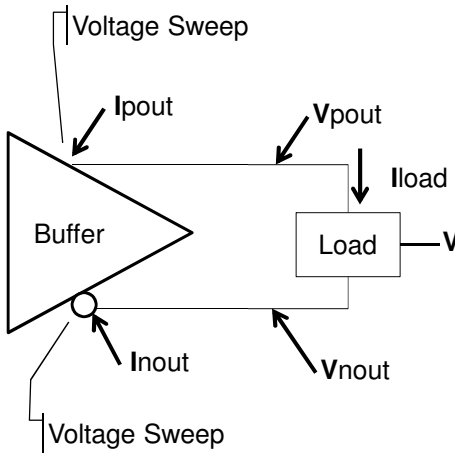


Correlation shows they are way off from the Spice result
RED – Spice, BLUE - IBIS

# Enhanced I-V Extraction Method



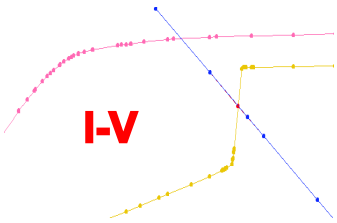

The IBIS I-V will be:
Ip(i-v) = Ipout – Iload
In(i-v) = Inout + Iload

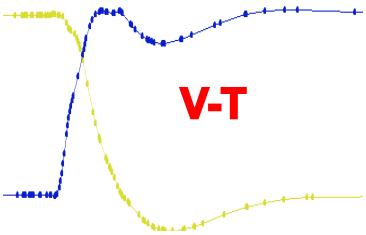
The IBIS V-T will be:
Vpout and Vnout with
V_fixture = Vcommon
R_fixture = Rload/2

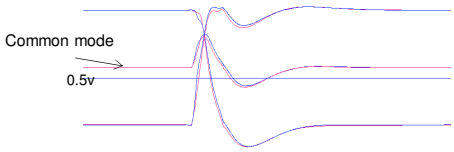
# Using enhanced extraction method with differential load

* I-V curves shown are combined curves and load line using reference to GND




Correlation shows matched result with Spice
RED – SPICE, BLUE - IBIS



# Summary

- Normal IBIS extraction method for load-dependent current-mode differential pair buffers produces inaccurate models
- Enhanced method considering differential load can solve this issue. It gives the matched results when correlating with Spice simulation results
- It would be better to have IBIS Spec accept “Rref_diff/Cref_diff” kind of differential loads for regular IBIS differential pair models
  - Rref_diff/Cref_diff is limited for External model use now
- IBIS Spec needs to be enhanced when modeling dynamic PLL current mode buffer
  - Various I-V tables for different diff_loads
  - Current dependent C-comp value table

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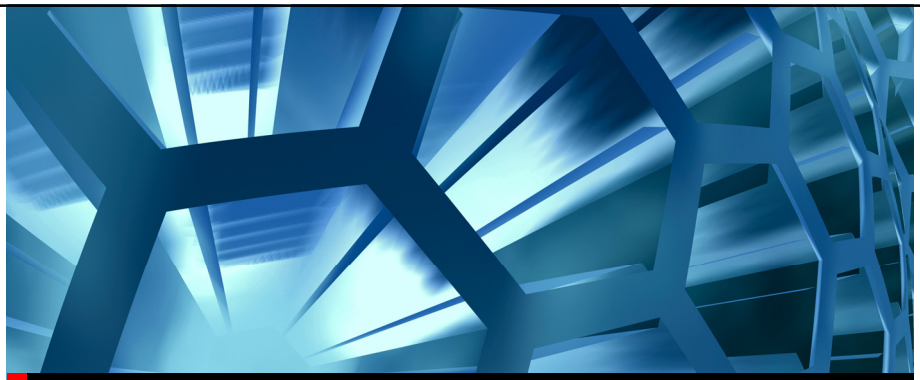
The Modeling Experts



# An Advanced Behavioral Buffer Model With Over-Clocking Solution

Yingxin Sun and Raymond Y. Chen
IBIS Asia Summit
Taipei, Taiwan
Nov. 19, 2013

cadence

## Agenda

1. SPICE Model and Behavioral Buffer Model
2. Over-Clocking Problem in IBIS
3. Proposed Solution and Results

cadence

# Agenda

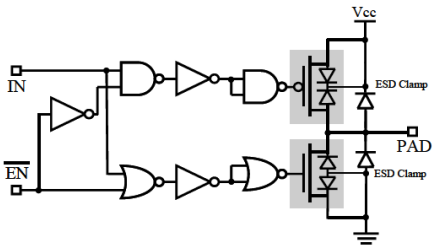
1. SPICE Model and Behavioral Buffer Model
2. Over-Clocking Problem in IBIS
3. Proposed Solution and Results

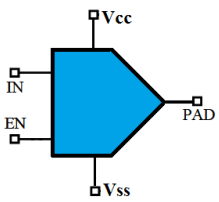
 

cadence

# SPICE Model and Behavioral Buffer Model

- SPICE model is a circuit netlist at transistor level, it contains detailed information about the circuit design and process parameters.
- Behavioral model is a black box model with certain terminal information, which is obtained from measurement or extracted from SPICE model. IBIS is a widely adopted standard behavioral model.



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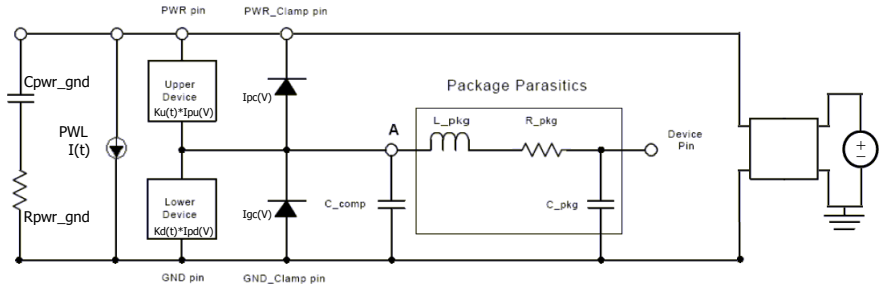
# A Simple Schematic for IBIS Model

- The non-linear behavior of pullup, pulldown and clamps are described by I/V tables, and modeled as voltage controlled current sources.
- The transition behavior is described by the V/T table of the rising/falling waveforms under specified loading condition. And they are used to derive/scale instantaneous value of the I/V curves.
- Other important parasitic elements
- IBIS, as a behavioral model, does not contain transistor equation, some of the physics and detailed response may not exist in a simple model, hence the issue that will be discussed next.



cadence

# Agenda

1. SPICE Model and Behavioral Buffer Model
2. Over-Clocking Problem in IBIS
3. Proposed Solution and Results

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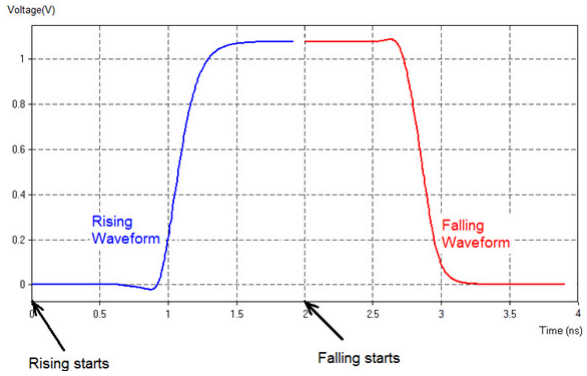
## Understand the Over-Clocking

- Normal operating, the input data bit width > the time range of the IBIS rising and falling waveform.




Normal operation



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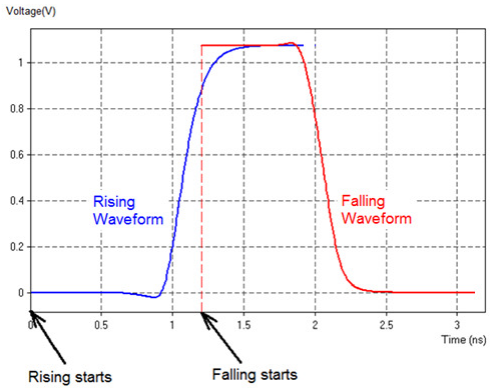
## Understand the Over-Clocking (cont.)

- If the input signal bit width is smaller than the time range of the IBIS waveforms, the next transition is triggered before this transition is finished.
- The behavior of the IBIS simulator may be unpredictable.
- Google “IBIS Overclocking” to find out more about this issue discussion since 2002




Over-clocking operation



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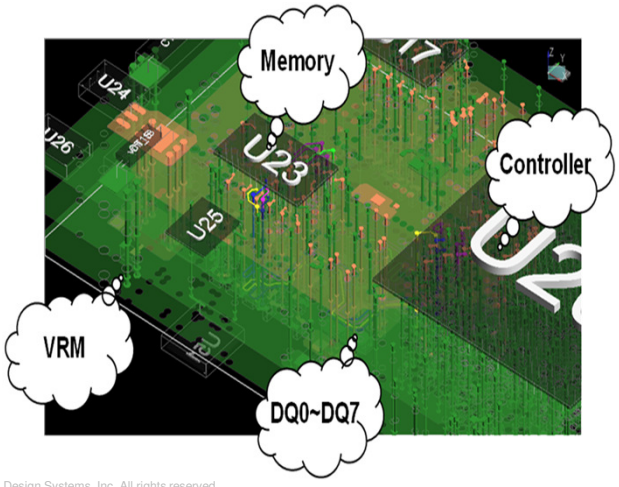
# Simulation Problem Is Shown with A DDR3 SSO Test Case

8 signal nets + 1 power nets + 1 ground net from a real PCB design. Bit width is 1ns, the pattern is 00010101110110011111001101010



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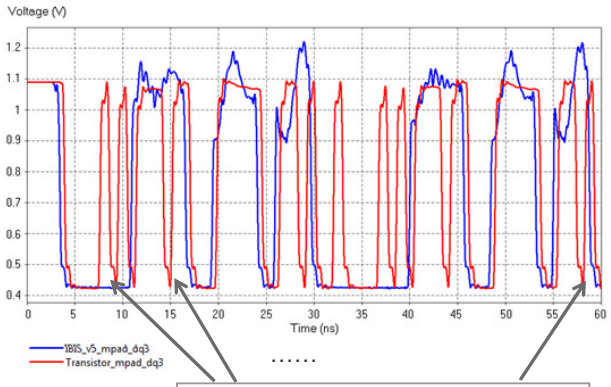
# Problematic Results from Over-Clocking

- A test case operating over-clocking
- Simulation results show missing bits



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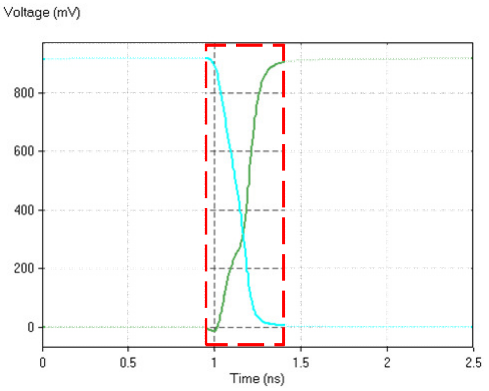
# Existing Solution to Solve Over-Clocking Problem

- V/T curve windowing by cutting the initial delay and the flat tail of the rising/falling waveforms of IBIS model to make the time range shorter
- The windowing can be done either in IBIS model creation or simulation tools



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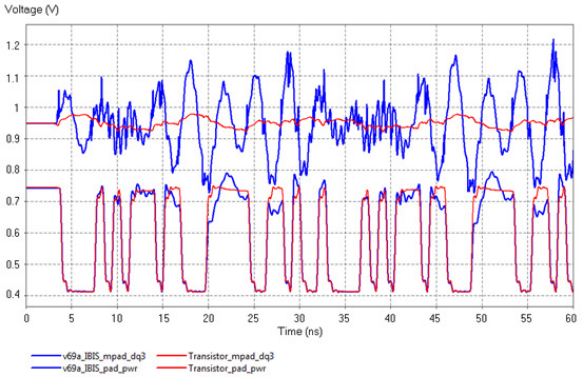
# Simulation Results with V/T Windowing

- The missing bits resolved
- Therefore, simulator with proper V/T windowing scheme should automatically handle overclocking issue in IBIS 4.2 model




- However, voltage on power net mismatches between transistor model and IBIS model due to the dynamic power noise not modeled.

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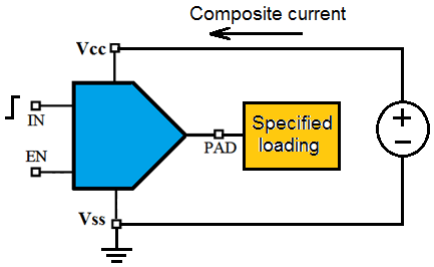
## New Challenge of Over-Clocking with Composite Current

- To accurate model the power-aware buffer model, the composite currents (I/T ) are introduced in IBIS V5.0 to give the current waveforms on power pin.
- The I/T data must be time correlated with the waveform V/T data which are extracted from pad pin.
- The composite current includes the contribution of the pre-driver and all the other on-die P/G paths. It has wider time range than V/T waveform.



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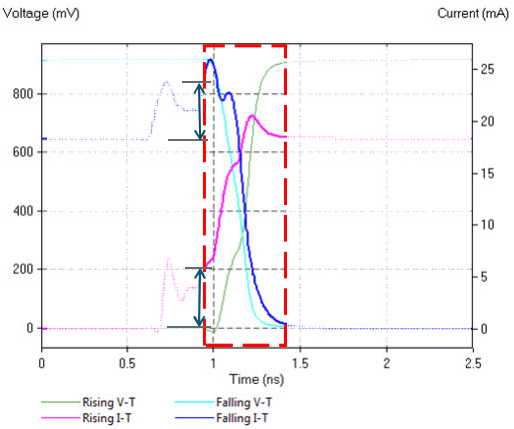
## Windowing with Composite Current

- Now both V/T and I/T need to be windowed.
- Choosing window based on wider I/T curve will not help, since over-clocking solution requires narrow timing window for higher frequency operation.
- Still choosing a window based on V/T will cut the composite current incomplete which will form a sharp step current.



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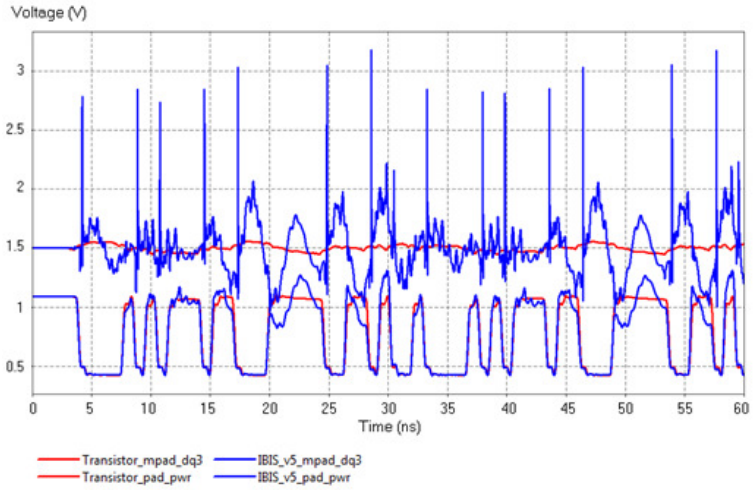
## The Sharp Step of Incomplete Composite Current Causes Unreal Large Voltage Spikes



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## Observation of This New Challenge

- With the addition of composite current (I/T) in IBIS 5.0, old windowing technique (V/T based) in IBIS simulator need to be improved, and can't be directly applied to I/T data to solve over-clocking issue.
- With IBIS 5.0 models become increasingly popular in the last few years, there are more awareness and discussion of this issue.
- A solution was developed by us two years ago to tackle this challenge.

 

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# Agenda

1. SPICE Model and Behavioral Buffer Model
2. Over-Clocking Problem in IBIS
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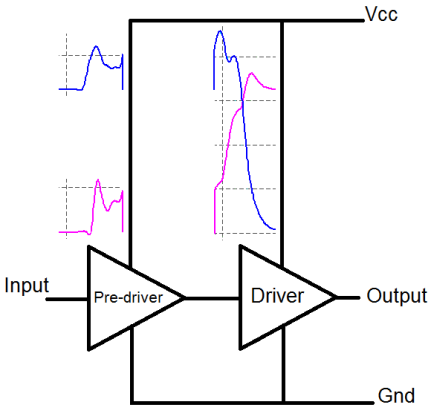
# Key Point of Advanced Over-Clocking Solution

- Using the V/T waveform windowing
- Adding one stage to the existing driver to keep the pre-driver behavior for the buffer switching delay and power current
- Taking the composite current compensation into two parts:
  - Driver contribution
  - Pre-driver contribution



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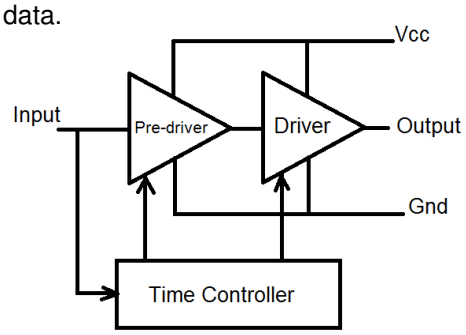
# Implementing the Proposed Over-Clocking Solution

- The proposed over-clocking solution can be implemented into an advanced IBIS model, which is a SPICE netlist with integrated model data and simulation algorithm.
- The proposed over-clocking solution can also be implemented into an advanced IBIS simulator to automatically handle the windowing of both V/T and I/T data.



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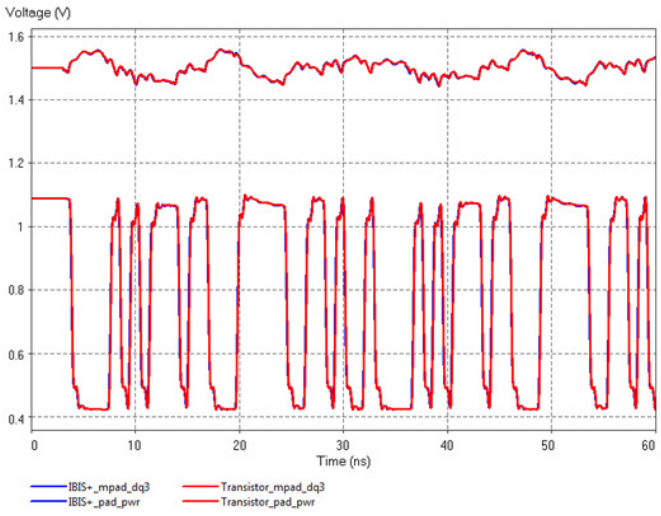
# Simulation results with Advanced Over-Clocking Solution



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## Simulation Performance Summary

- Very good correlation between IBIS and the original transistor model for real SSO simulation, both signals and power/ground waveforms match very well, even under over-clocking scenario.
- The 60ns simulation time is based on 32 clock cycles of data input.
- It takes 54 minutes for original transistor level SPICE model.
- It takes 55 seconds for the behavioral model with the advanced over-clocking solution.
- Note: HSPICE is used to run the simulations for all the models, including the advanced IBIS model with over-clocking solution.

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## Conclusion

- Power-aware buffer model generation has been implemented for IBIS 5.0 standard. When used in high-speed power-aware SSO simulations, user often has to deal with IBIS over-clocking issues.
- With the proposed algorithm for handling composite currents under over-clocking situation, more advanced model shows significant accuracy improvement compared with traditional IBIS models, while keeping the fast simulation advantages of IBIS.
- Advances in IBIS standard, together with advances in modeling and simulation algorithms, continue to make this behavioral model technique a great and practical engineering approach for high-speed design.

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# References


- [1] Perivand F. Tchrani, Yuzhe Chen, Jiayuan Fang, “Extraction of Transient Behavioral Model of Digital I/O Buffers from IBIS”, 46th IEEE Electronic Components & Technology Conference, Orlando, May 28-31, 1996, pp 1009-1015.
- [2] Ying Wang and Han Ngee Tan,“The Development of Analog SPICE Behavioral Model Based on IBIS Model”, Proceedings of the Ninth Great Lakes Symposium on VLSI, March 1999.
- [3] Sam Chitwood, Raymond Y. Chen, Jiayuan Fang, “An Initial Case Study for BIRD95 - Enhancing IBIS for SSO Power Integrity Simulation”, IBIS Summit DesignCon, January 2005.
- [4] Raymond Y. Chen, “Recent Development of IBIS and Related EDA Technologies”, Sigrity Annual User Forum, May 24, 2011


 

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# Combined I-V Table Checking Problem

Asian IBIS Summit
Taipei, Taiwan, November 19, 2013

Bob Ross
Teraspeed Consulting Group
bob@teraspeed.com

Yingxin Sun and Joy Li
Cadence Design Systems
sunyx@cadence .com
joyli@cadence.com

Presented by Anders Ekholm, Ericsson



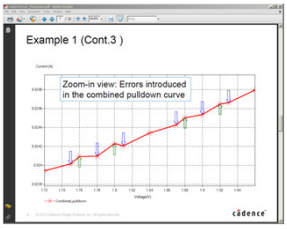


# Real Data from BUG140 and Cadence Presentations

- BUG140: http://www.eda.org/ibis/bugs/ibischk/bug140.txt
- (In all test cases, the [Gnd Clamp] data is 0.0 in the region of interest)
- Presentations
  - "Golden Parser Non-monotonic Warning's Investigation" by Yingxin Sun and Joy Li, November 9, 2012: http://tinyurl.com/byqu7yn (Presented at the IBIS Quality Committee November 27, 2012)
  - "Combined I-V Table Checks (BUG140)", January 31, 2013 IBIS Summit, Bob Ross, Yingxin Sun, and Joy Li
  - "Ibischk5 Specification and Parser", May 15, 2013 IBIS Summit, Bob Ross and Mike LaBonte (Signal Integrity Software)

# BUG140 Issue

- Unexpected Non-Monotonic Warnings for Combined I-V Tables (derived from monotonic data)




- Combined I-V table checks:
  - [Pulldown] + [Gnd Clamp] + [Power Clamp]
  - [Pullup] + [Gnd Clamp] + [Power Clamp]
- Ibischk5 parser is de facto standard for IBIS model correctness (and ibischk5 is embedded in tools)
- Some companies require 0 Errors, 0 Warnings
- IBIS Quality Spec, recommends 0 Errors and 0 Warnings
- **Warning messages create support issue for model authors or automatic modeling utilities**





# Facts

- No specification REQUIREMENT that individual or combined I-V tables be monotonic
- No stated method to sum mismatched voltage points (piecewise linear interpolation is allowed and used)
- Non-monotonicity often occurs outside of normal simulation region – in clamping region and not a problem
- Ibischk5 parser is working correctly

# Observations

- Non-monotonic behavior can occur
  - Combined I-V table slope is small
  - I-V table points are misaligned due to
    - Offset V intervals due to Gnd, Vdd and delta V
    - Different reference voltages (min/max)
    - Extraction done with piecewise linear interpolation calculations (if not done right)
  - Combination of above cases
- Example (y = x^2) next shows monotonic tables yielding non-monotonic summations

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# Example: x Step 2, Offset by 1 (Red: Interpolated Value)

| x | y1 = x^2 | y2 = x^2 | y1−y2 = 0? |
|---|---|---|---|
| 0 | 0 | | |
| 1 | 2 | 1 | 1 |
| 2 | 4 | 5 | −1 |
| 3 | 10 | 9 | 1 |
| 4 | 16 | 17 | −1 |
| 5 | 26 | 25 | 1 |
| 6 | 36 | | |

**Non-monotonic due to piecewise linear interpolation on both columns**

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# x Step 0.02, Offset by 0.01
# (Red: Interpolated Value)

| x | y1 = x^2 | y2 = x^2 | y1−y2 |
|---|---|---|---|
| 0.00 | 0.0000 | | |
| 0.01 | 0.0002 | 0.0001 | 0.0001 |
| 0.02 | 0.0004 | 0.0005 | −0.0001 |
| 0.03 | 0.0010 | 0.0009 | 0.0001 |
| 0.04 | 0.0016 | 0.0017 | −0.0001 |
| 0.05 | 0.0026 | 0.0025 | 0.0001 |
| 0.06 | 0.0036 | | |

**Still non-monotonic with higher resolution data**



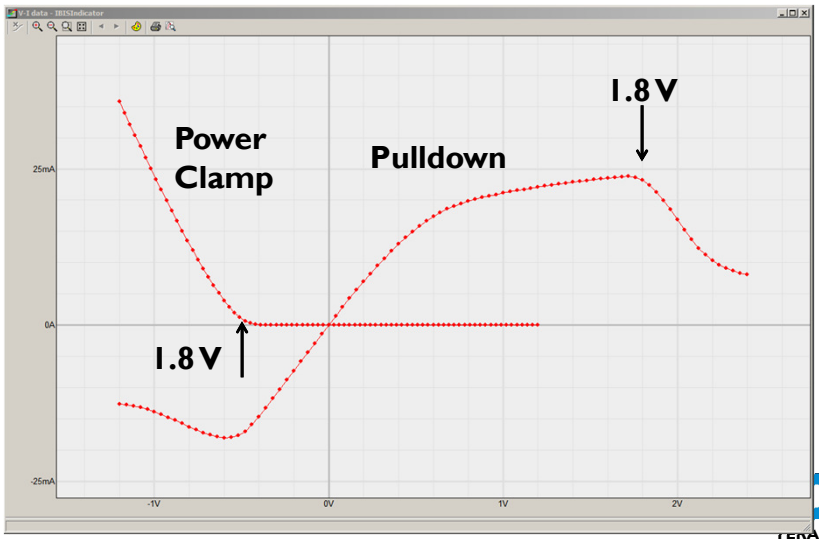


# x Steps 0.02 and 0.01, 0.00 Offset
# (Red: Interpolated Value)

| x | y1 = x^2 | y2 = x^2 | y1−y2 |
|---|---|---|---|
| 0.00 | 0.0000 | 0.0000 | 0.0000 |
| 0.01 | 0.0002 | 0.0001 | 0.0001 |
| 0.02 | 0.0004 | 0.0004 | 0.0000 |
| 0.03 | 0.0010 | 0.0009 | 0.0001 |
| 0.04 | 0.0016 | 0.0016 | 0.0000 |
| 0.05 | 0.0026 | 0.0025 | 0.0001 |
| 0.06 | 0.0036 | 0.0036 | 0.0000 |

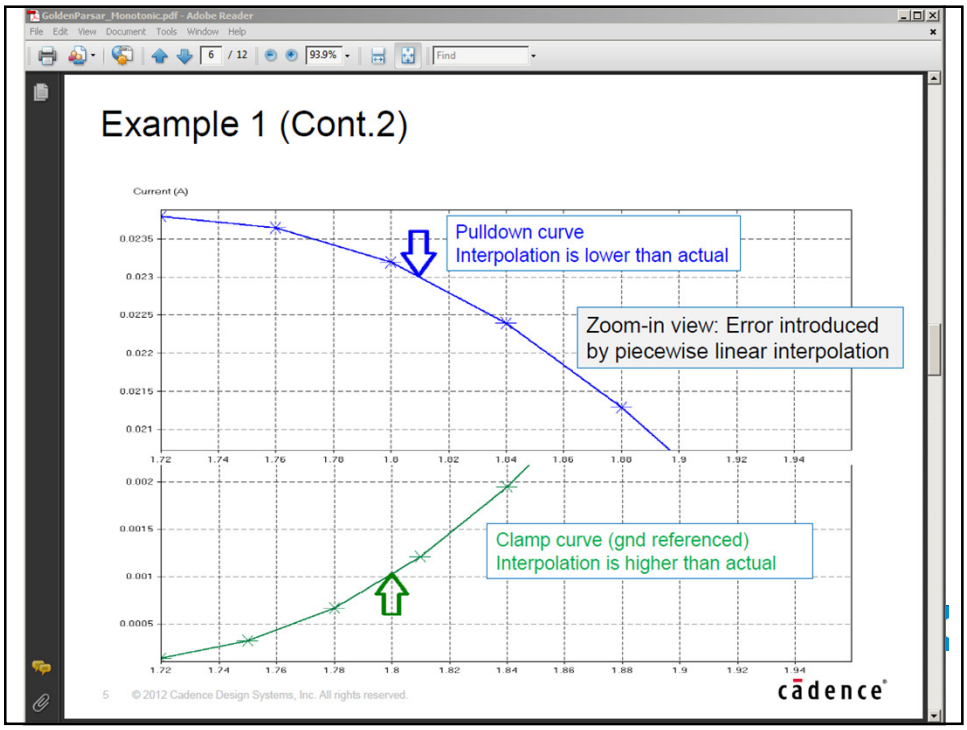
**Different resolution data causes non-monotonic combination**

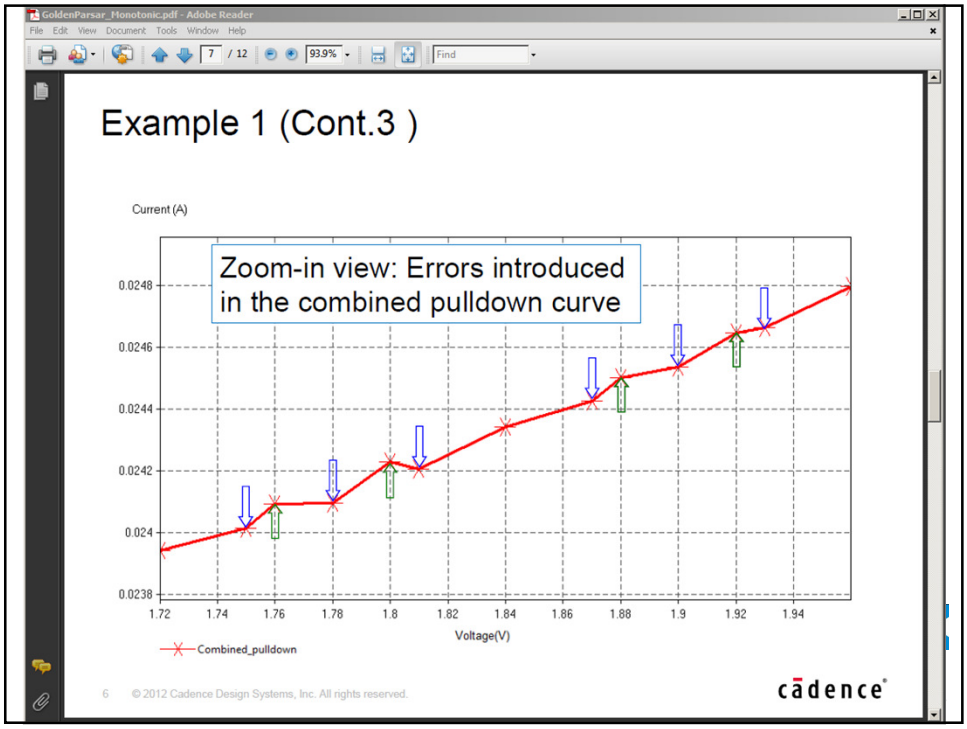
# bug140a.ibs Maximum Data (Vdd = 1.3 V)










# BUG140 Resolution

- Change WARNING to NOTE
  - Valid solution for user
  - Avoids tool and model developer support issues
- Add "based on piecewise linear interpolation" to message
- No practical fix
  - Still issues with higher resolution or choosing percentage threshold for non-monotonic warning
  - Piecewise linear interpolation is legal, and spline fitting would just hide information



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# Checking bug140a.ibs

```
IBISCHK5 V5.1.2

Checking bug140a.ibs for IBIS 3.2 Compatibility...

NOTE (line   39) - Pulldown Typical data is non-monotonic
NOTE (line   42) - Pulldown Minimum data is non-monotonic
NOTE (line   42) - Pulldown Maximum data is non-monotonic
NOTE (line  135) - Pullup Typical data is non-monotonic
NOTE (line  137) - Pullup Maximum data is non-monotonic
NOTE (line  138) - Pullup Minimum data is non-monotonic
WARNING - Combined Pulldown for Model: iobuf Maximum data is non-monotonic

Errors  : 0
Warnings: 1

File Passed
```





# Fixed bug140a.ibs in Version 5.1.3

```
IBISCHK5 V5.1.3

Checking bug140a.ibs for IBIS 3.2 Compatibility...

NOTE (line   39) - Pulldown Typical data is non-monotonic
NOTE (line   42) - Pulldown Minimum data is non-monotonic
NOTE (line   42) - Pulldown Maximum data is non-monotonic
NOTE (line  135) - Pullup Typical data is non-monotonic
NOTE (line  137) - Pullup Maximum data is non-monotonic
NOTE (line  138) - Pullup Minimum data is non-monotonic
NOTE - Combined Pulldown for Model: iobuf Maximum data is non-monotonic
based on piece-wise linear interpolation
Errors  : 0

File Passed
```

# Closure

- For best checking results, use the latest version of ibischk5
- Parser being updated as new BUG reports are submitted and processed.

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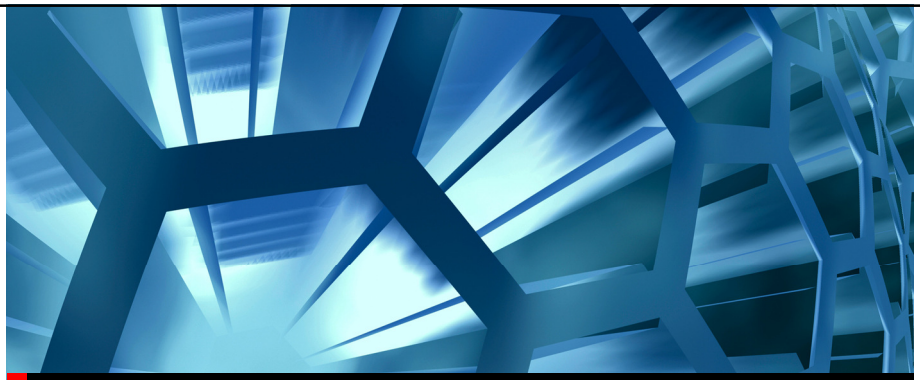

# IBIS Modeling for IO-SSO Analysis

Thunder Lay and Jack W.C. Lin
IBIS Asia Summit
Taipei, Taiwan
Nov. 19, 2013

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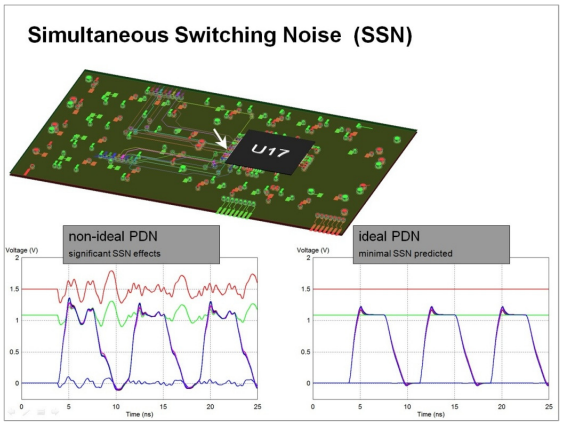
## Agenda

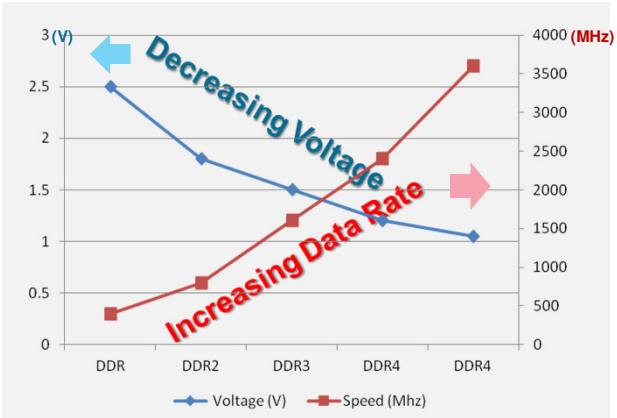
- What is IO-SSO?
- Missing Components in Traditional IO-SSO Analysis
- Accurate On-die and Package Effects in IBIS Models
- Creating IBIS Models with On-die Interconnect
- Case Study – IO-SSO Analysis with IBIS Models
- Summary

# What is IO-SSO?

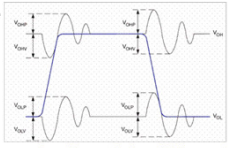
- A DDR memory interfaces is a parallel bus
  - Many signals represent a data byte/word/32-bit word/64-bit word
  - Simultaneous switching signals / outputs are referred to as SSO
  - The noise between power and ground created is referred to as simultaneous switching noise (SSN)
  - IC Designers refer to this phenomenon as IO-SSO
  - SI/PI can be verified by IO-SSO




# IO-SSO Impacts Timing and Noise Margin




- Data transfers are faster and more sensitive to instability of the PDN
  - DDR runs at 2.5 V
  - DDR2 runs at 1.8 V
  - DDR3 runs at 1.5V
  - DDR4 to run at 1.2 V – 1.05V



Ground bounce Peaks and Valleys must be minimized with low signal voltages

+

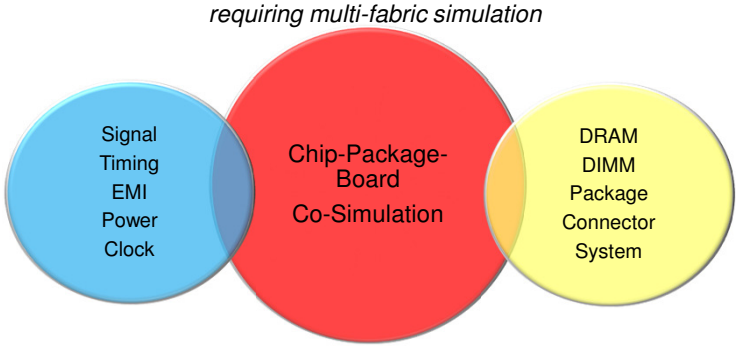
**Decreasing Timing Budget**

±600ps ➔ ±300ps ➔ ±150ps

**SSN effects impact timing and noise budget**

# Higher Data Rate ➔ High Level Interactions

*Electrical and Physical worlds collide requiring multi-fabric simulation*

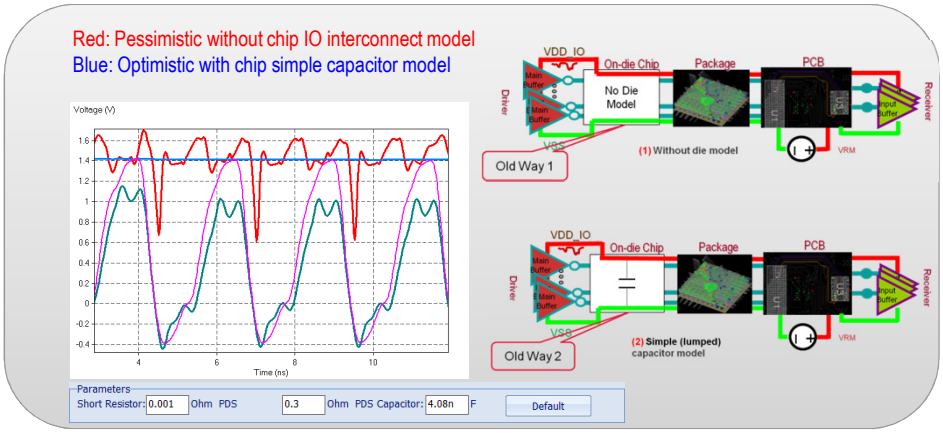



*Increased interaction between signals*

*Increased interaction between system hardware components*

# Traditional IO-SSO Simulation Scenarios

- Pessimistic result when analyzed without on-die model.
- Optimistic result when analyzed with estimated on-die model.



# Agenda

- What is IO-SSO?
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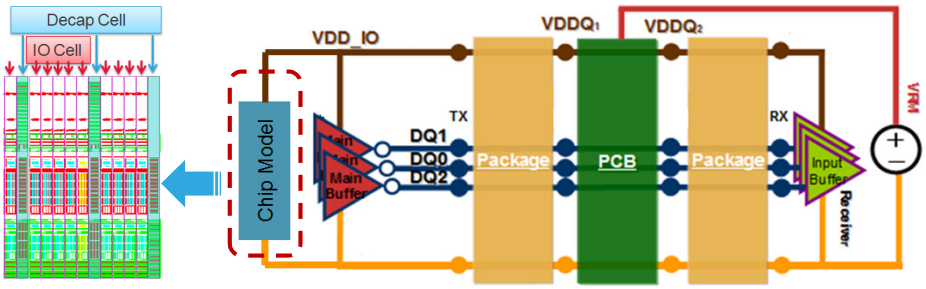
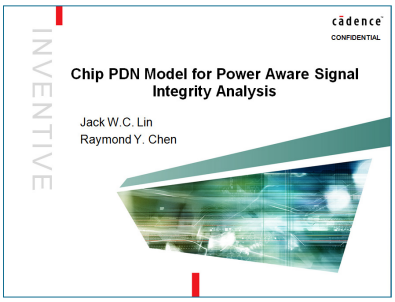
# Missing Components in Traditional IO-SSO Analysis

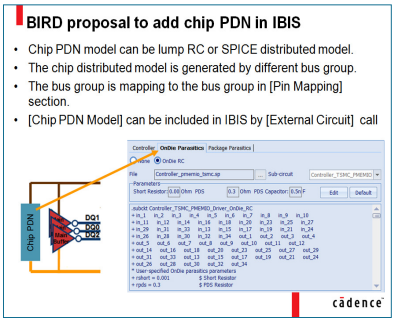



- Post-sim transistor SPICE netlist only includes limited parasitic information.
- Distributed behavior of IO's P/G impedance can't be represented.
- Pin Mapping table may not be defined accurately.
- On-die decap model is not captured in IBIS model.
- All above problems make IO-SSO simulation lose accuracy.

## Asia IBIS Summit 2012

- Chip PDN model is crucial for IO-SSO analysis.
- Without Chip PDN model, artificially large power /ground noise impact the signal waveform significantly
- Chip PDN is responsible to filter high frequency noise
- On-die RC or better distributed chip PDN model can yield realistic power/ground noise analysis




## Agenda

- What is IO-SSO?
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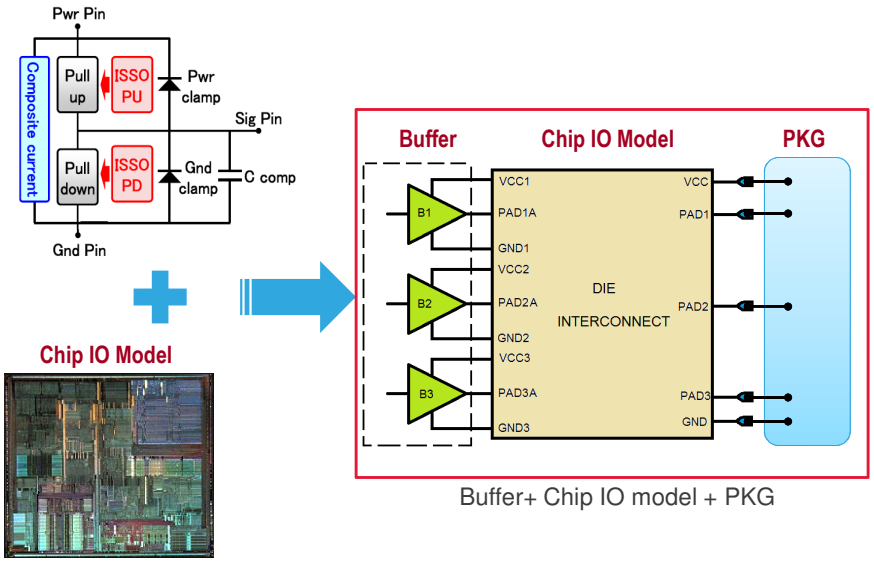
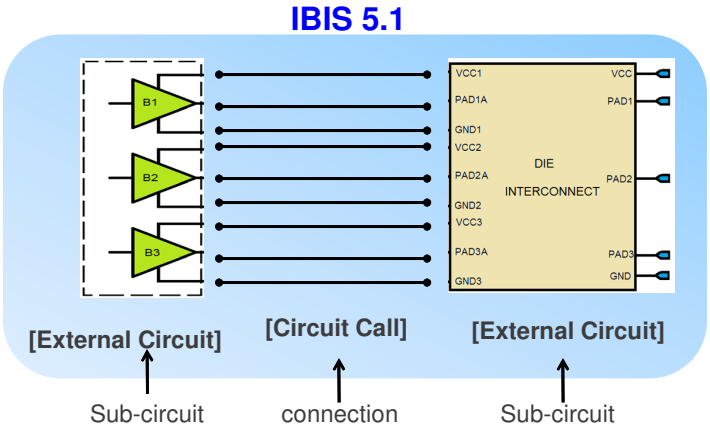
# Adding On-die Effects to the IBIS Model




Buffer+ Chip IO model + PKG

# Connecting Buffer, On-Die and Package Models




- Effectively incorporates the on-die and package models into the buffer
- The package and on-die models may be of arbitrary topology to include coupling, non-ideal power deliver and other effects
- Applying IBIS 5.1 [External Circuit] sub-components is similar to sub-circuit call and connections in HSPICE
- Future ISS based solution may be coming from committee

# Agenda

- What is IO-SSO?
- Missing Components in Traditional IO-SSO Analysis
- Accurate On-die and Package Effects in IBIS Models
- **Creating IBIS Models with On-die Interconnect**
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- Summary

 

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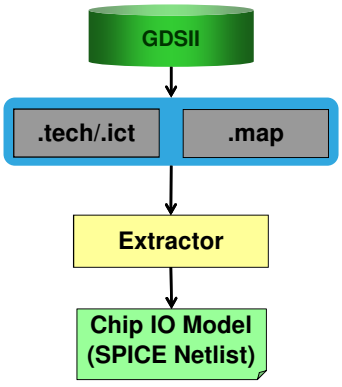
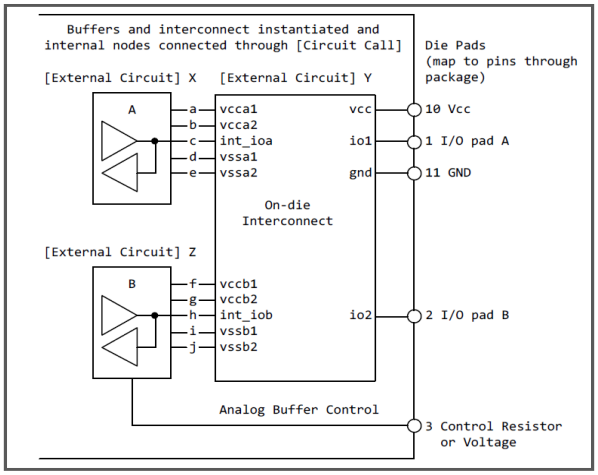
# Creating IBIS Models with On-die Interconnect (1/4)

- Generate chip IO model
  - LEF/DEF or GDSII data can represent physical geometry.
  - Includes Power/Ground/Signal routing with On-Die caps.
  - Define Chip stackup, circuit mapping
  - Chip IO model extraction is based on chip layout which includes metal_x to the top layers (x can be 1~N). Model builder needs to be aware what SPICE nest-list is from pre-sim or post-sim flow.
  - Generate SPICE netlist



## Creating IBIS Models with On-Die Interconnect (2/4)

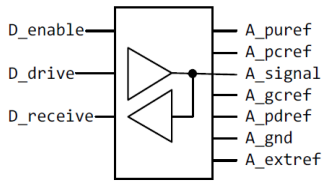



- [External Circuit] will be represented as IO buffer, chip IO, package…..
- Connect each [External Circuit] through [Circuit Call]

## Creating IBIS Models with On-die Interconnect (3/4)

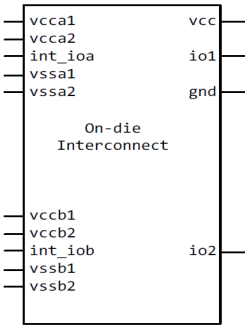
- Ports under [External Circuit]

  The [External Circuit] keyword allows the user to define any number of ports and port functions on a circuit.




**Port name for IO Buffer**

Ports A_puref A_pdref A_signal A_drive A_enable A_receive A_pcref A_gcref




Ports vcca1
Ports vcca2
…….

## Creating IBIS Models with On-die Interconnect (4/4)

- Define [Pin] and [Node Declarations]
  - When a [Circuit Call] keyword defines any connections that involve one or more die pads (and consequently pins), the corresponding pins on the [Pin] list must use the reserved word “CIRCUITCALL” in the third column instead of a model name.
  - [Node Declaration] provides a list of internal die nodes and/or die pads for a [Component] to make unambiguous interconnection descriptions possible

```
[Node Declarations]     | Must appear before any [Circuit Call] keyword
| Die nodes:
pu1 pd1 io1p io1 in1 en1 outin1          | List of die nodes
pu2 pd2 io2p io2 in2 en2 outin2          | List of die nodes
pu3 pd3 io3p io3 in3 en3 outin3          | List of die nodes
[End Node Declarations]
```

## Agenda



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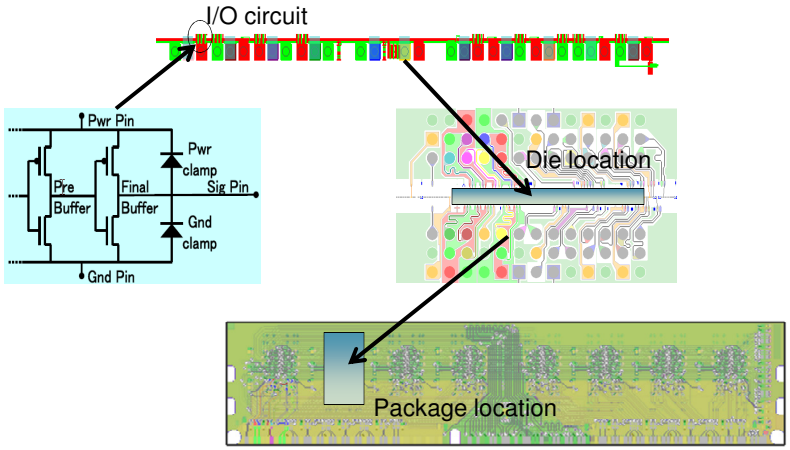
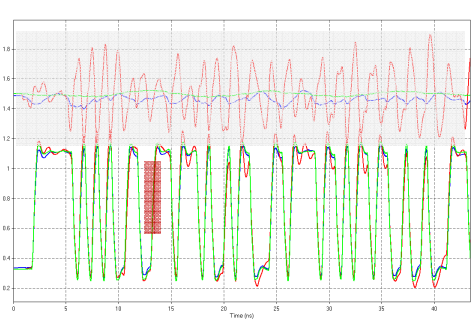
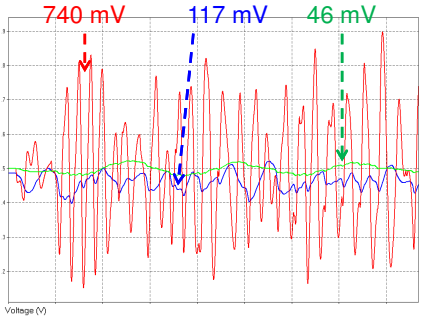
## Case Study – IO-SSO Analysis with IBIS Models



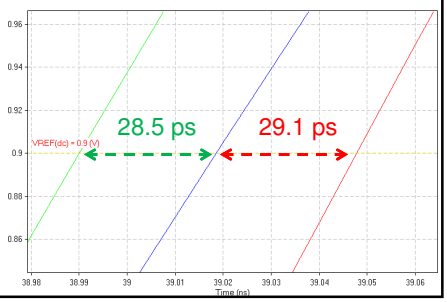

- I/O transistor circuit is converted into power-aware IBIS model
- Chip is extracted by chip level extractor which include RLCK elements.
- PCB and package S-parameters are extracted and converted to broadband SPICE models.
- Only 1 group DDR data is considered for this test

## Case Study – IO-SSO Analysis with IBIS Models



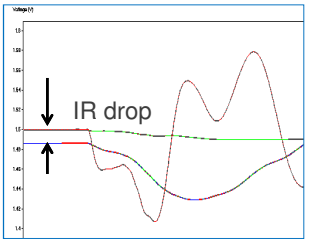


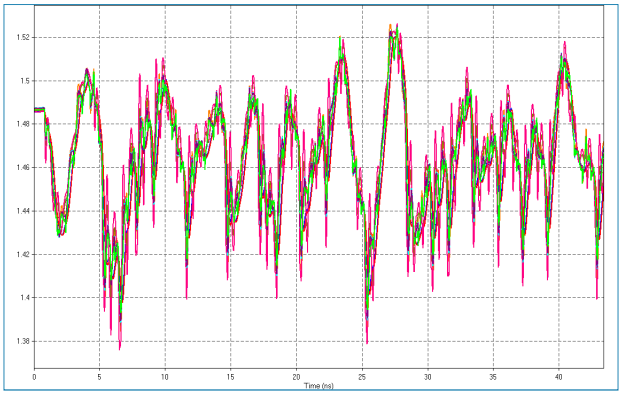

**RED: without chip PDN**
**Green: with on-die RC**
**Blue: with distributed broadband model**




- SSN from SSO will be over or under estimated without accurate chip IO model.
- Timing push in/out will become worse if more IOs are switching at the same time.

## Case Study – IO-SSO Analysis with IBIS Models



**RED: without chip PDN**
**Green: with on-die RC**
**Blue: with distributed broadband model**

- IR drop becomes worse after including chip IO model.
- Noise level at each IO pad is different, which reveals the distributed behavior of the IO power deliver network.

## Agenda



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## Summary

- For tighter timing and noise budgets in LPDDR3 or DDR4, system level IO-SSO analysis is helpful for design margin assessment
- IBIS 5.1 models may include power-aware IO buffer, chip P/G/S from IOs to bump pads, and arbitrary package models
  - existing IBIS syntax is applied (using [External Circuit])
  - additional techniques using ISS within the IBIS model are being discussed in committee
- The approach described allows chip vendors to deliver more complete IBIS models to their customers to enable faster and more accurate product design verification