DDRn Interface Signoff Analysis with Distributed Chip IO Interconnect Model

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Agenda

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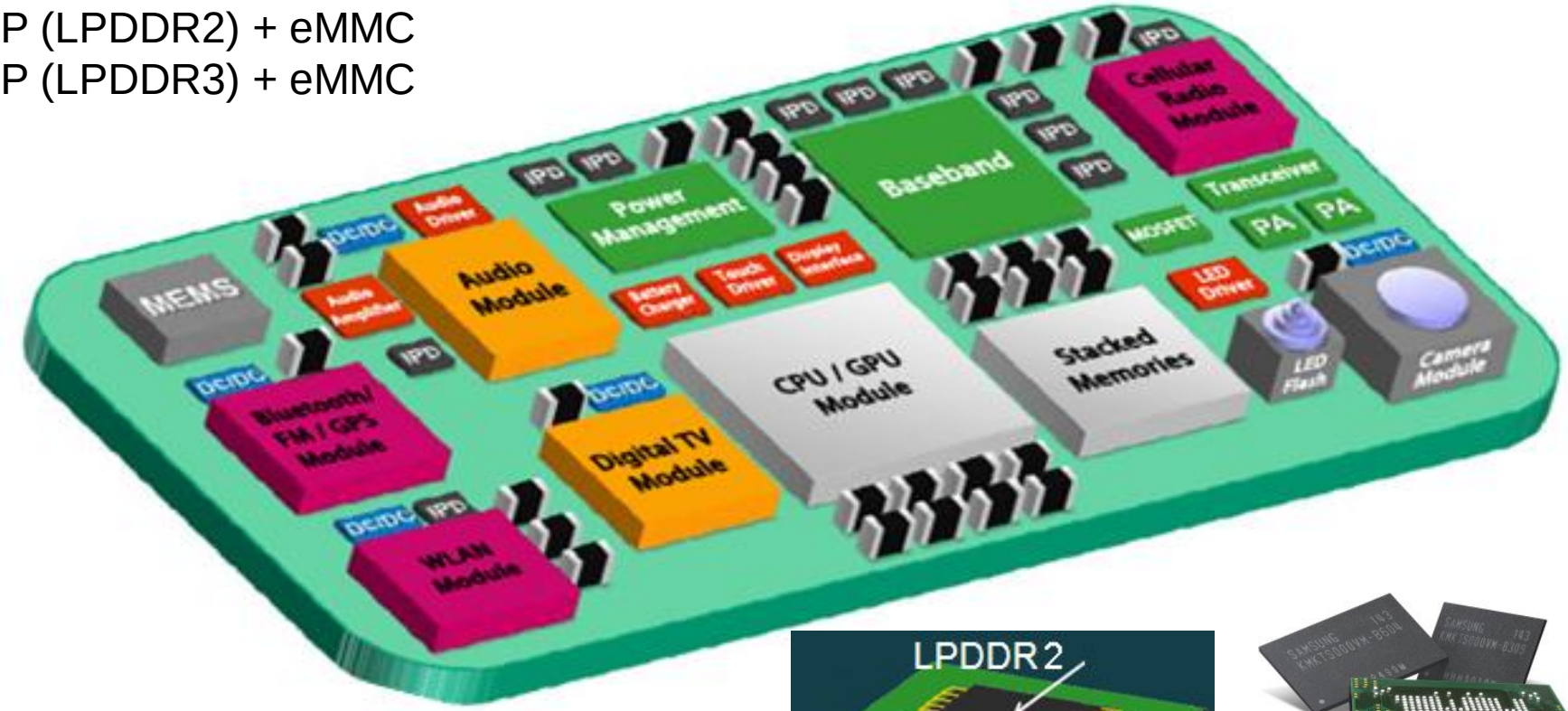
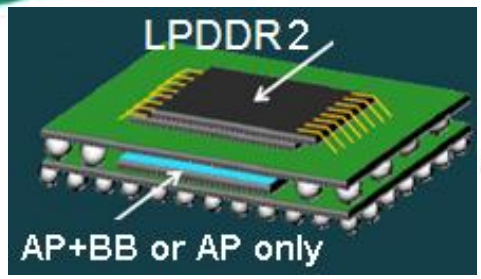
- Introduction About the Chip IO Interconnection
- Chip IO Interconnect Model Extraction and Analysis
- Case Study – DDR SSO and Chip IO Power Decap
- Summary

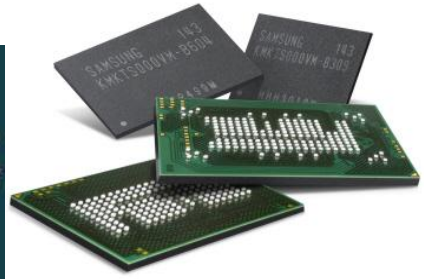
Simplified View of a Smartphone Board

PoP (LPDDR2) + eMMC
PoP (LPDDR3) + eMMC



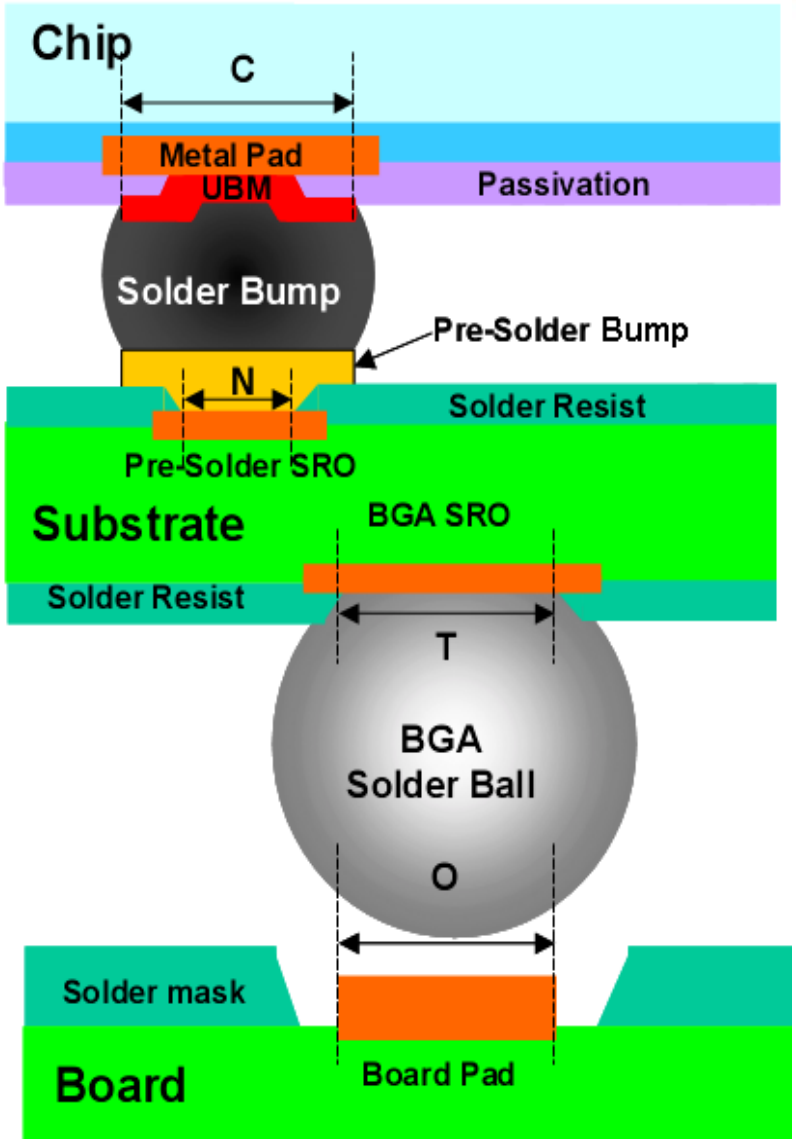
eMCP (LPDDR2+ eMMC)
eMCP (LPDDR3+ eMMC)

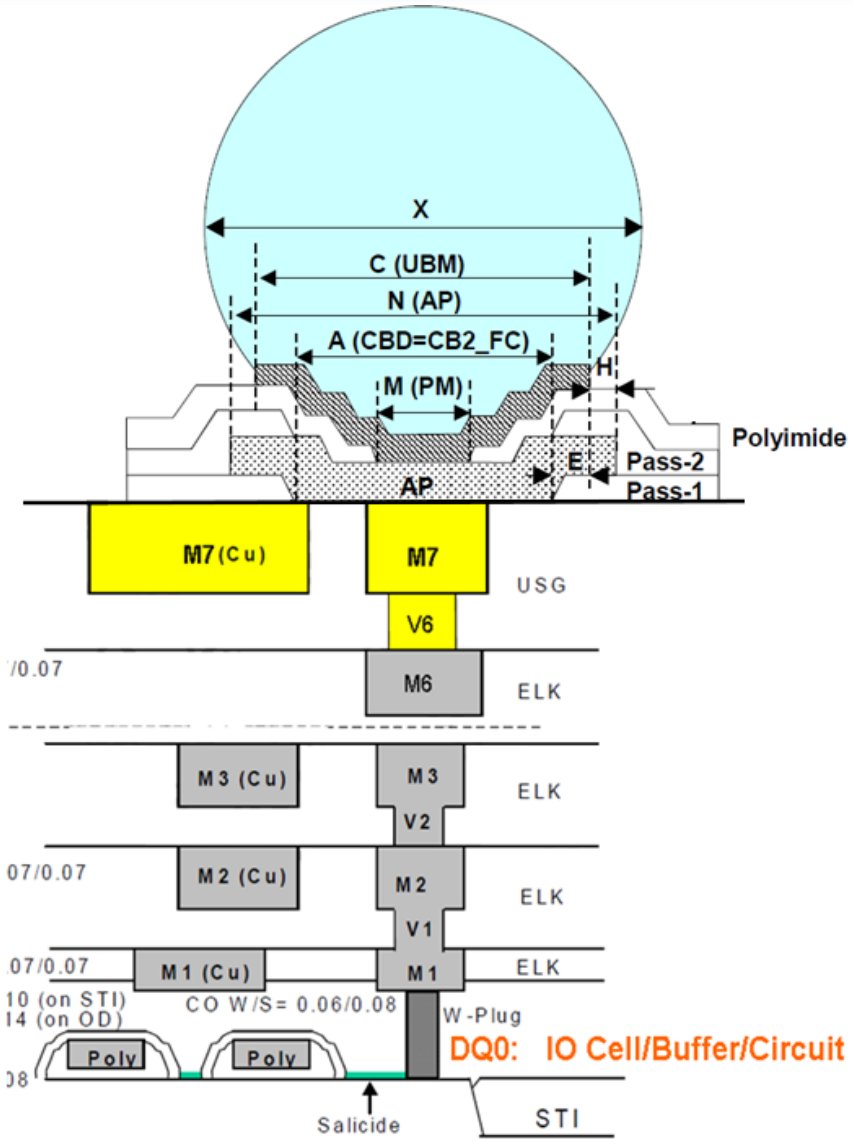




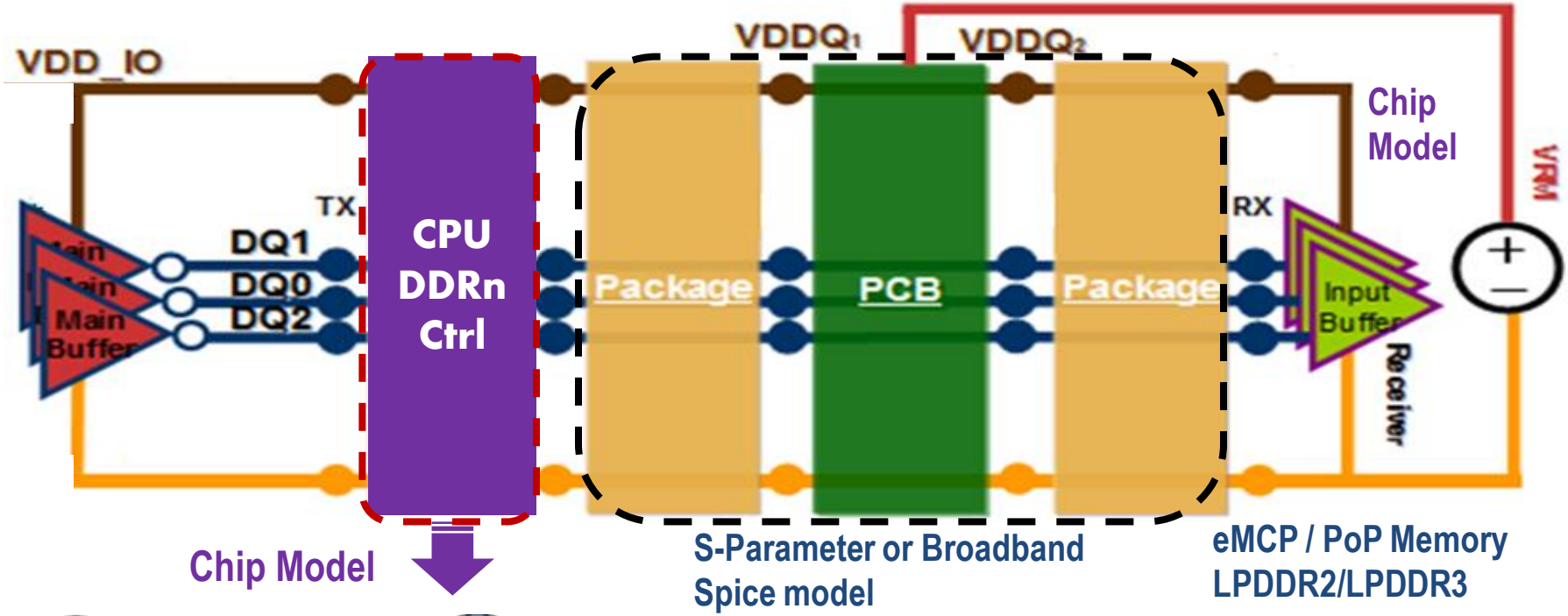
4Gb eMMC +8Gb LPDDR2 Memory
eMCP (LPDDR2+eMMC) 11.5x13x1.0mm3 162b FBGA 0.5mm pitch
12x12 PoP + eMMC $_{only}$ 11.5x13x1.0mm3 153b FBGA 0.5mm pitch

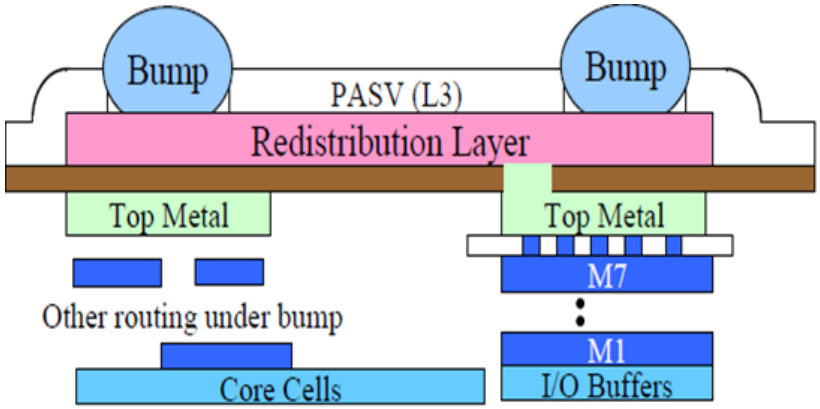
Chip IO interconnection Structure

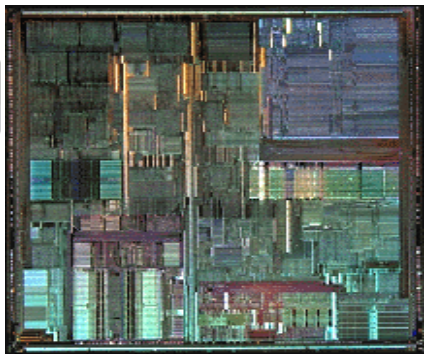




DDRn System Interconnection Topology

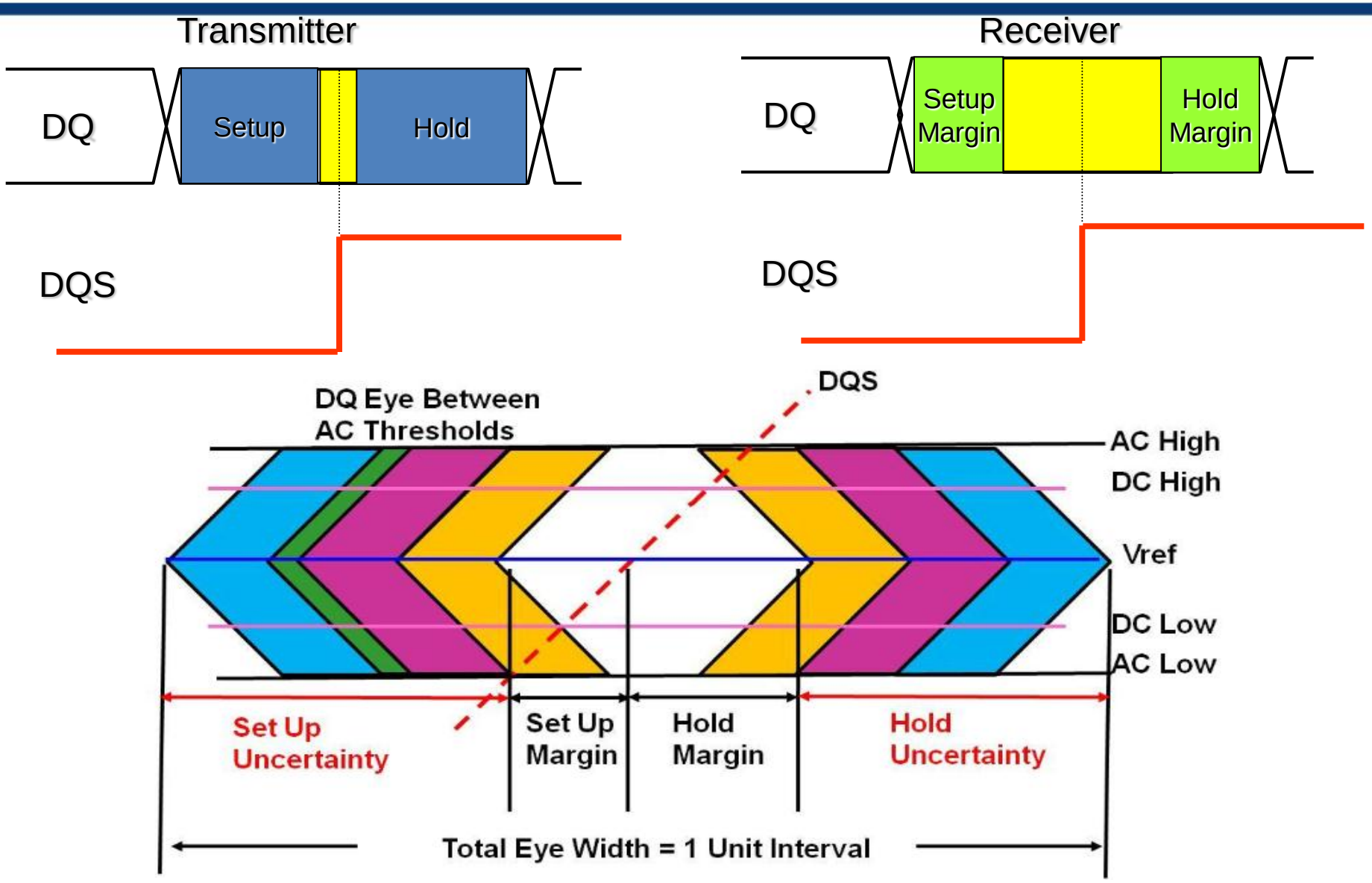






Chip Model = Distributed IO Power/Ground/Signal Interconnect Model (from M1 to Bump)

Uncertainties Vs Timing Margin



DDRn Setup/Hold Timing Budgets
(Uncertainties : Skew & Jitter)

Transmitter Contributions	Interconnection Contributions	Receiver Contributions
DDL (Data Delay Line) Granularity and bit offset (BDL and LCDL) (Static)	**Signal Length Mismatches (On-chip interconnection M1 to Bump , RDL Routing , Package Substrate and PCB layout Skew) (Static)**	Input Rise /Fall Slew Factor (Static)
Register Mismatch within the PHY (Static)	Crosstalk (Pushout/Pullin from nearby aggressor signals and serpentine routing) (Dynamic)	DDRn Data Set Up and Hold specifications (tDS, tDH) (Static)
DLL Jitter including Clock Source Jitter (Dynamic)	Reflections,Inter-Symbol Interference (ISI) (Impedance discontinuities, topology,loading) (Dynamic)	Setup and Hold Slew rate Derating (Static)
DLL Phase Error (Dynamic)	High frequency losses (Dielectric and Conductor losses) (Dynamic)	
PHY Skew between DQS/DQS# and DQ signals (Static)	Dielectric mismatches between layers (Dynamic)	
Process Variation Effects (Static)		
IO Output Rise Fall Delay Mismatch (Static)		
SSO/SSN Pushout (Effects of non-ideal power distribution network-PDN) (Dynamic)		
VT Drift (BDL and LCDL Setting) (Dynamic)		

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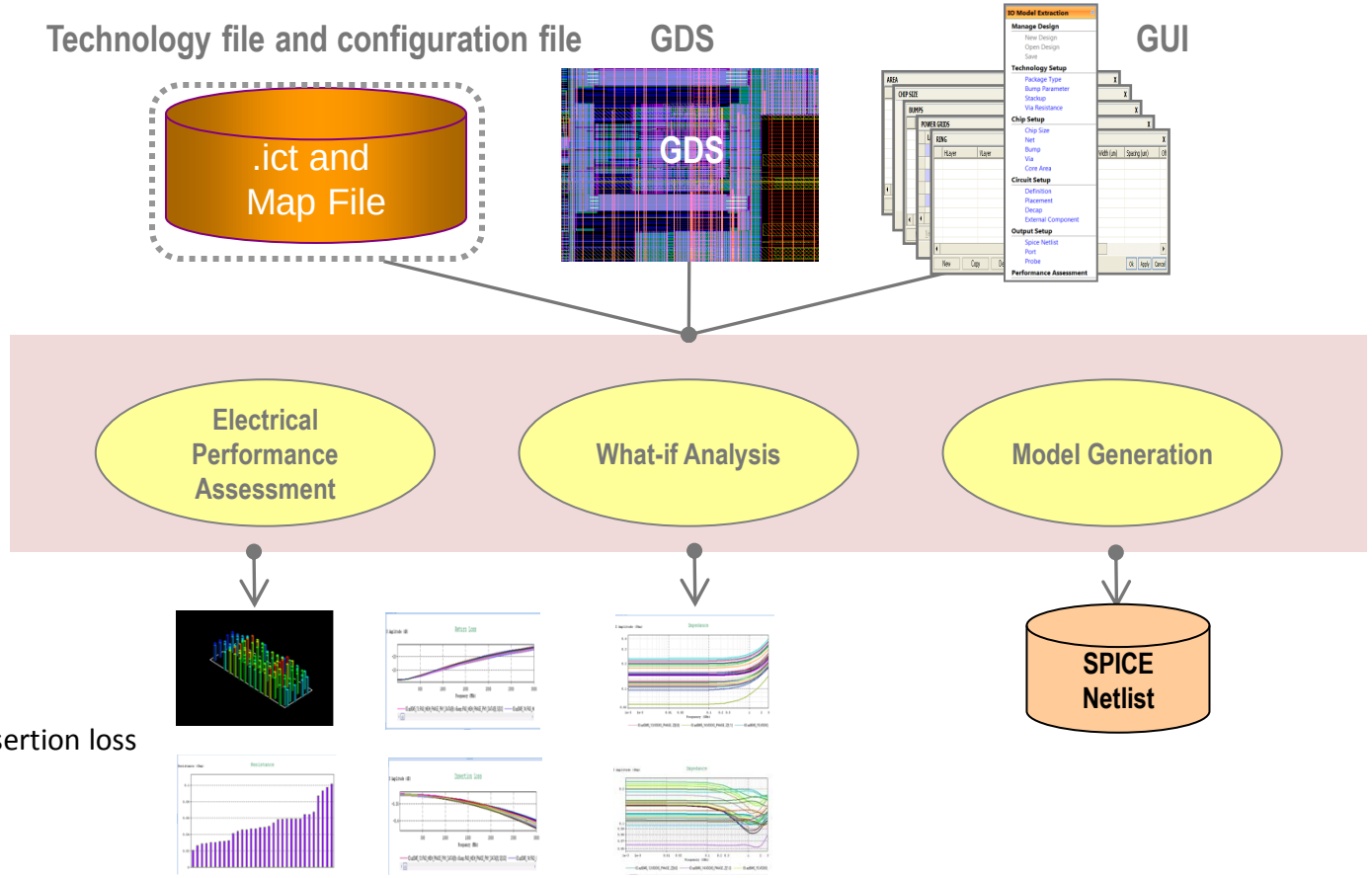
Chip IO Interconnect Model Extraction Diagram

Inputs

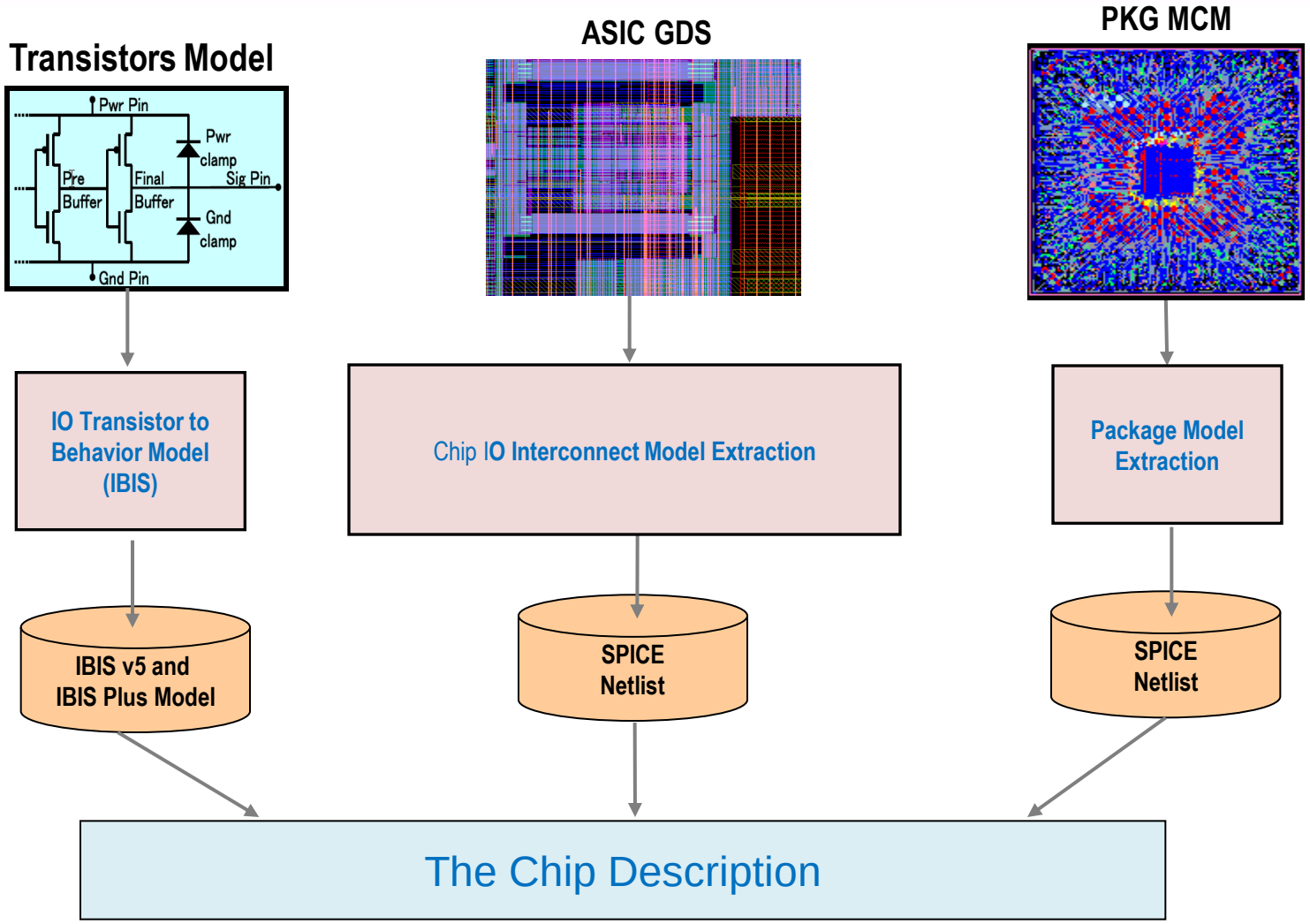
- LEF/DEF or GDS
- Technology file (.ict)
- Layer map file

Outputs

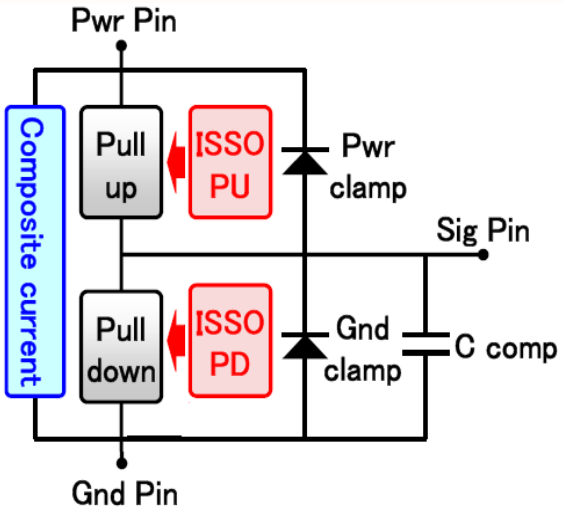
- IO interconnect model
  - SPICE netlist
- EPA results
  - Power pin RL
  - Power net capacitance
  - Power net impedance
  - Signal net RLC
  - Signal net return and insertion loss

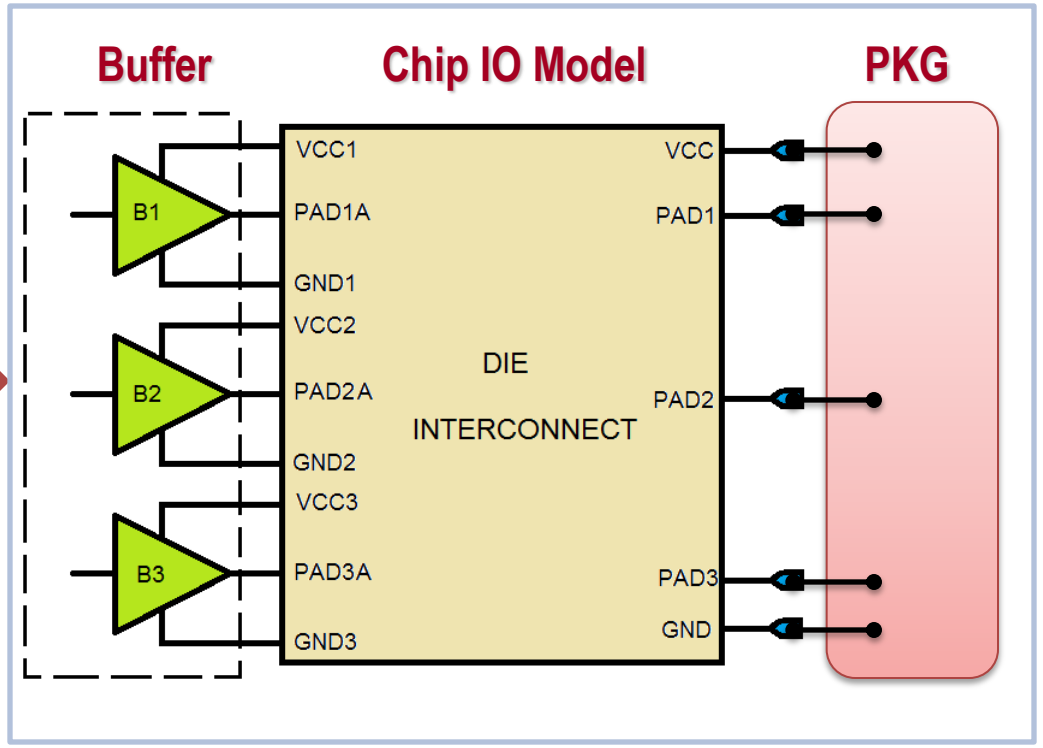


Chip Model Parts



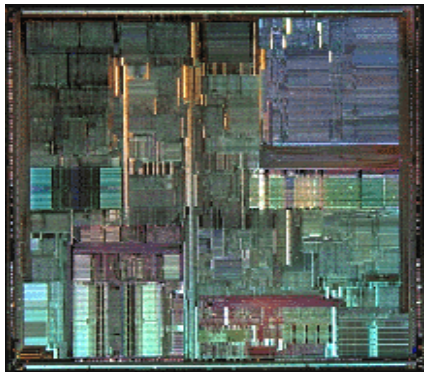
Chip IO Model Add in the IBIS Model Simulation



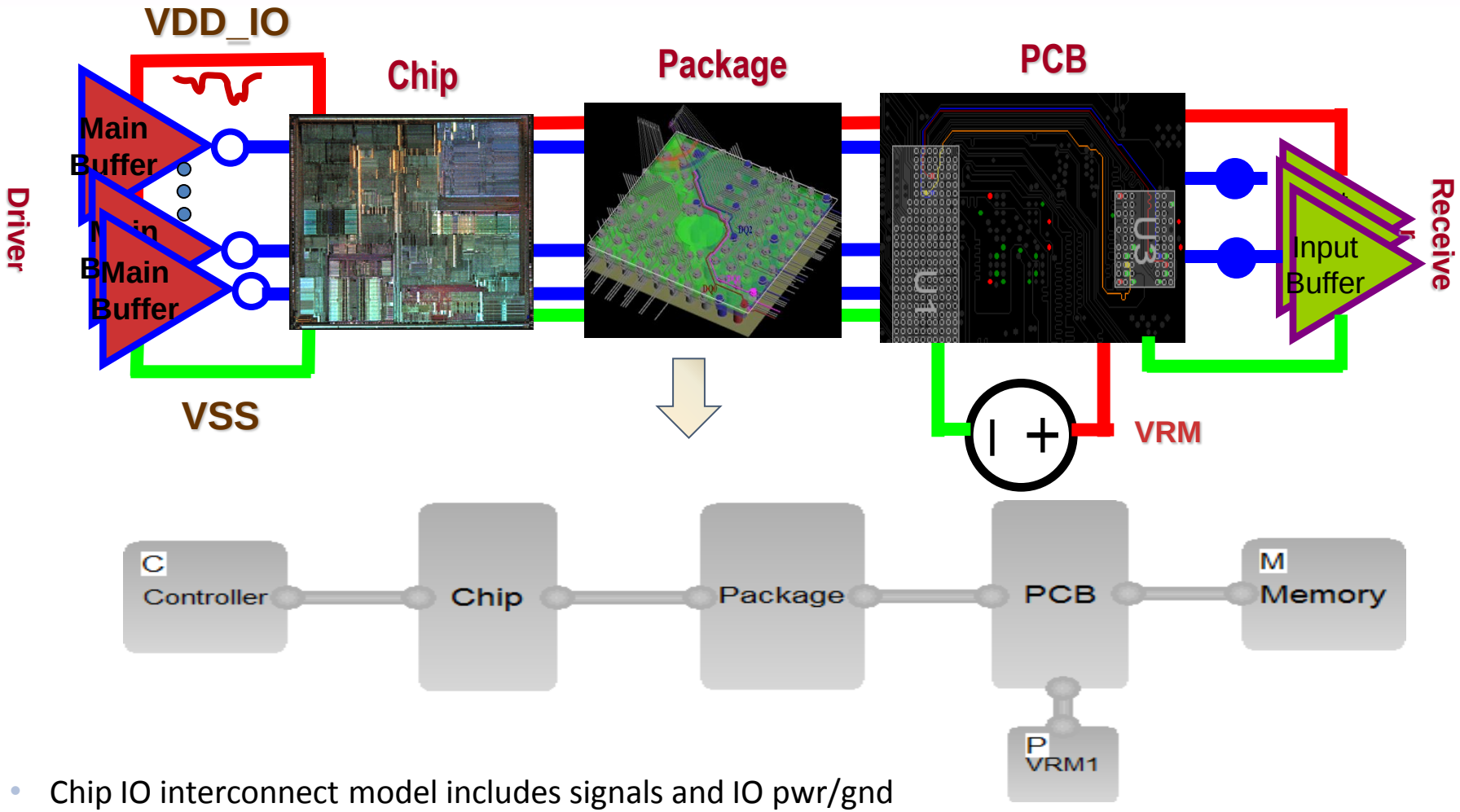


IBIS + Chip IO model + PKG

Chip IO Model



System Interconnection Analysis for DDRn



- Chip IO interconnect model includes signals and IO pwr/gnd
- Chip IO interconnect model is extracted by chip level extractor which include RLCK elements.
- PCB and package are extracted by EM solver and converted into broadband SPICE model.

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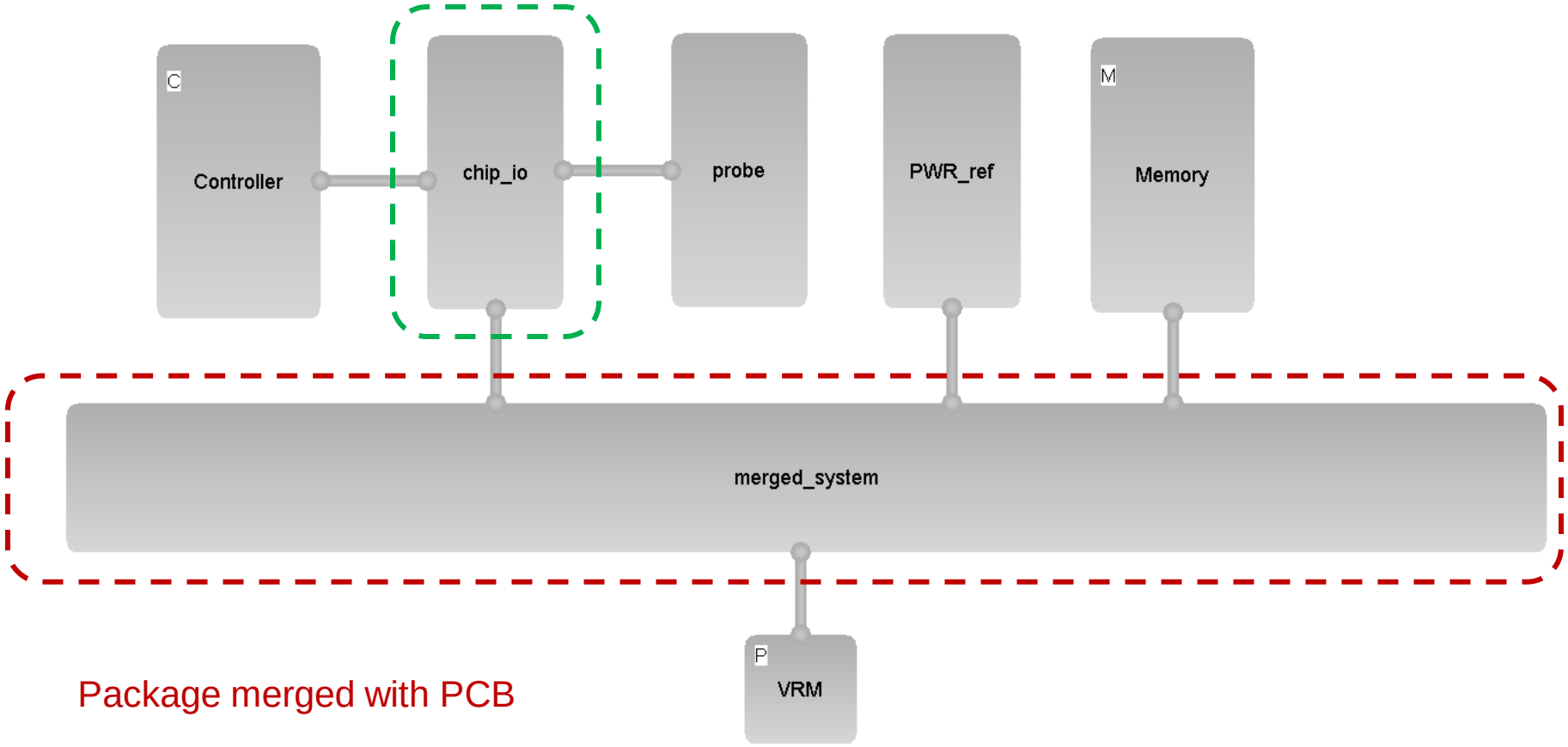
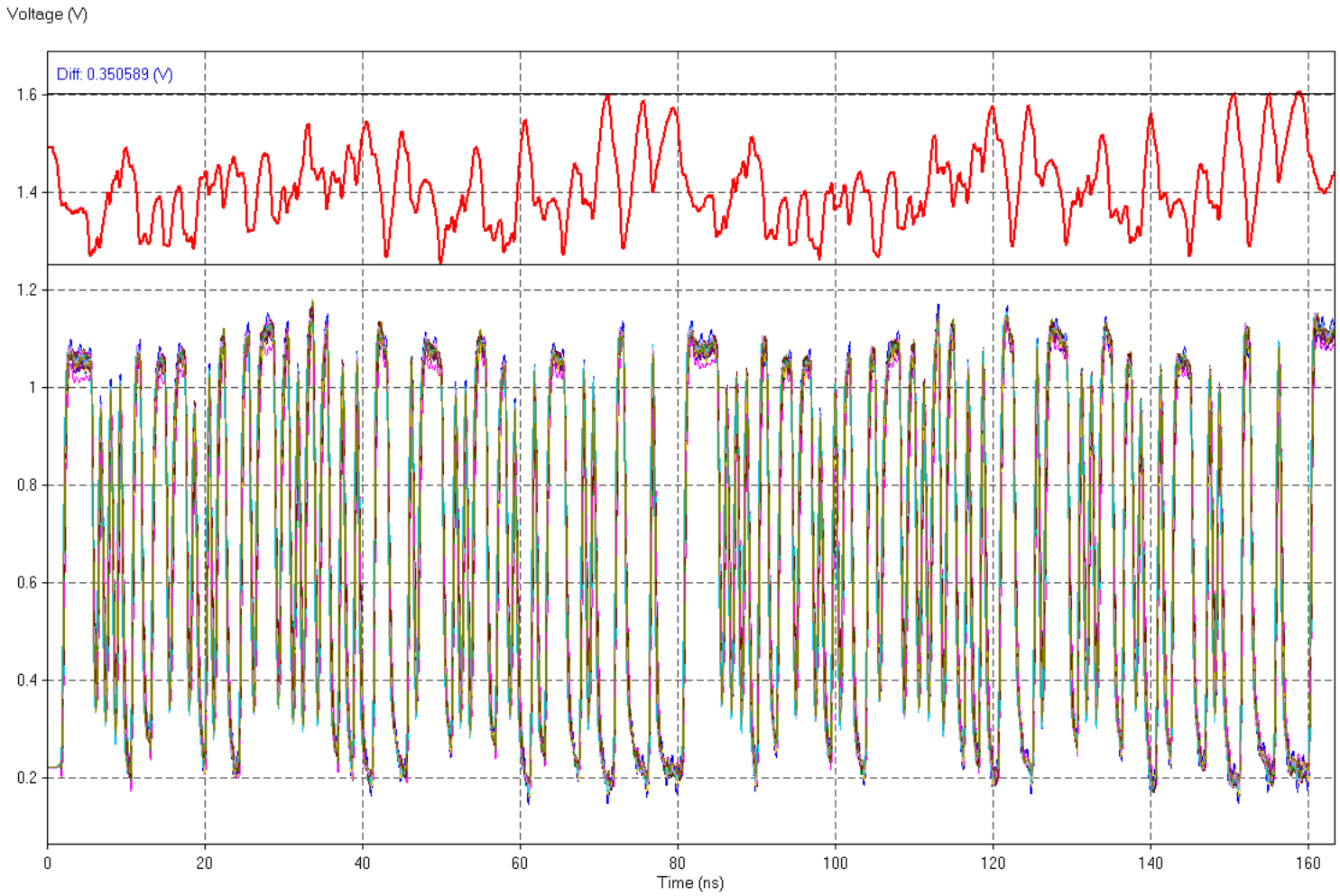
Test vehicle of system level SI/PI analysis (DQ/DQS)

Chip IO interconnection model extraction



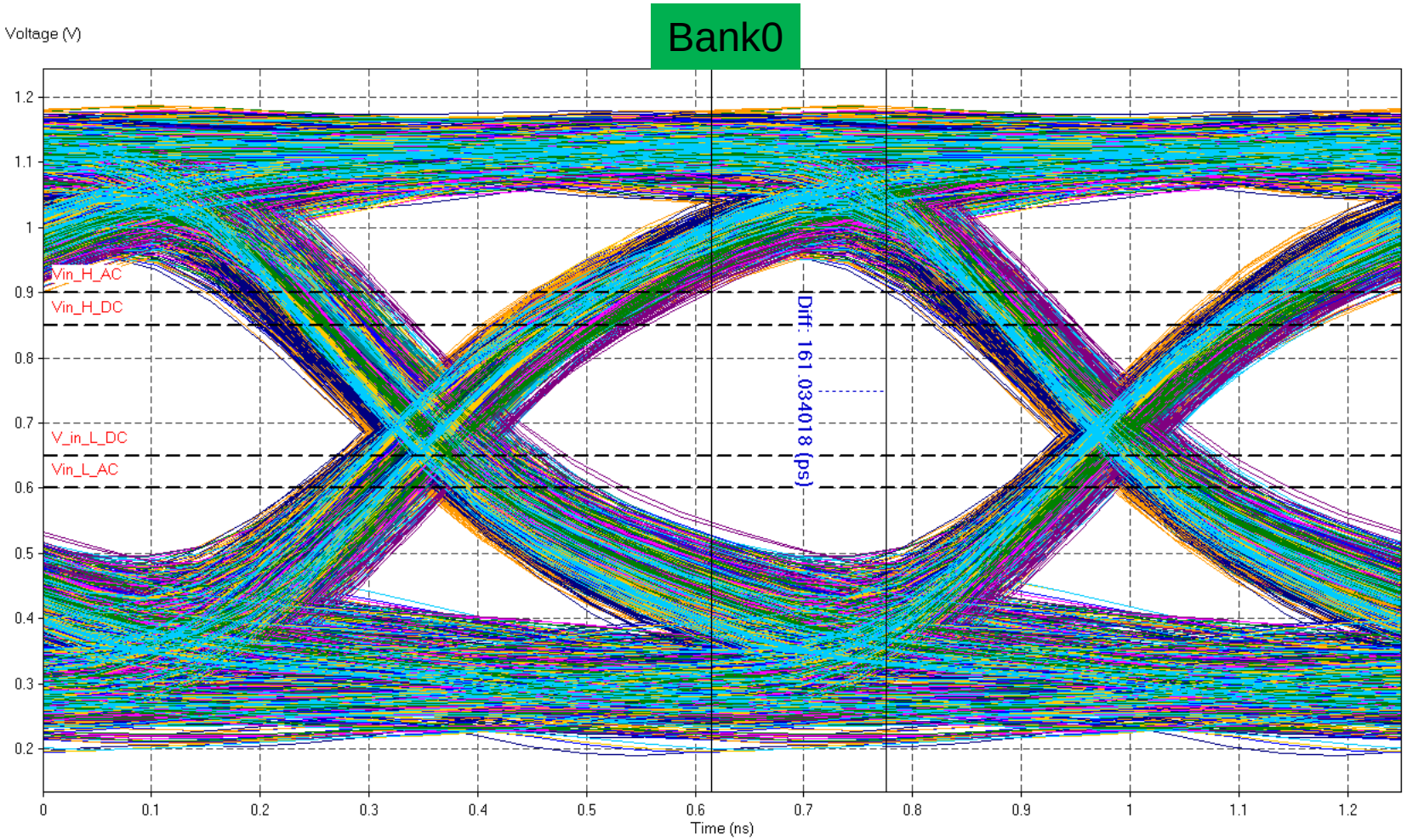
Package merged with PCB

DDRn Bank0 SSO



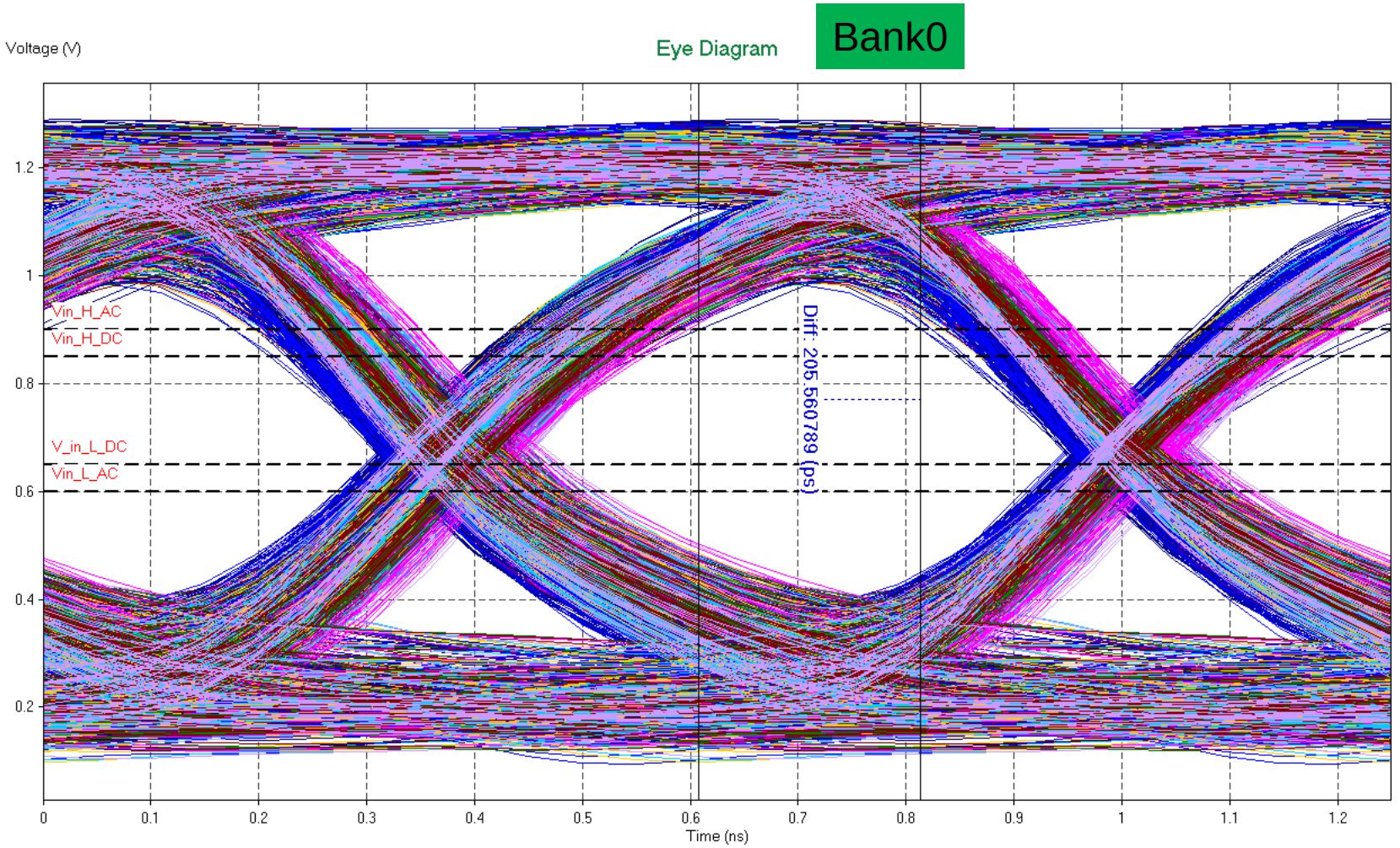
Power aware signal integrity analysis

System level SI/PI analysis (DQ/DQS) with memory write in TD—ODT40

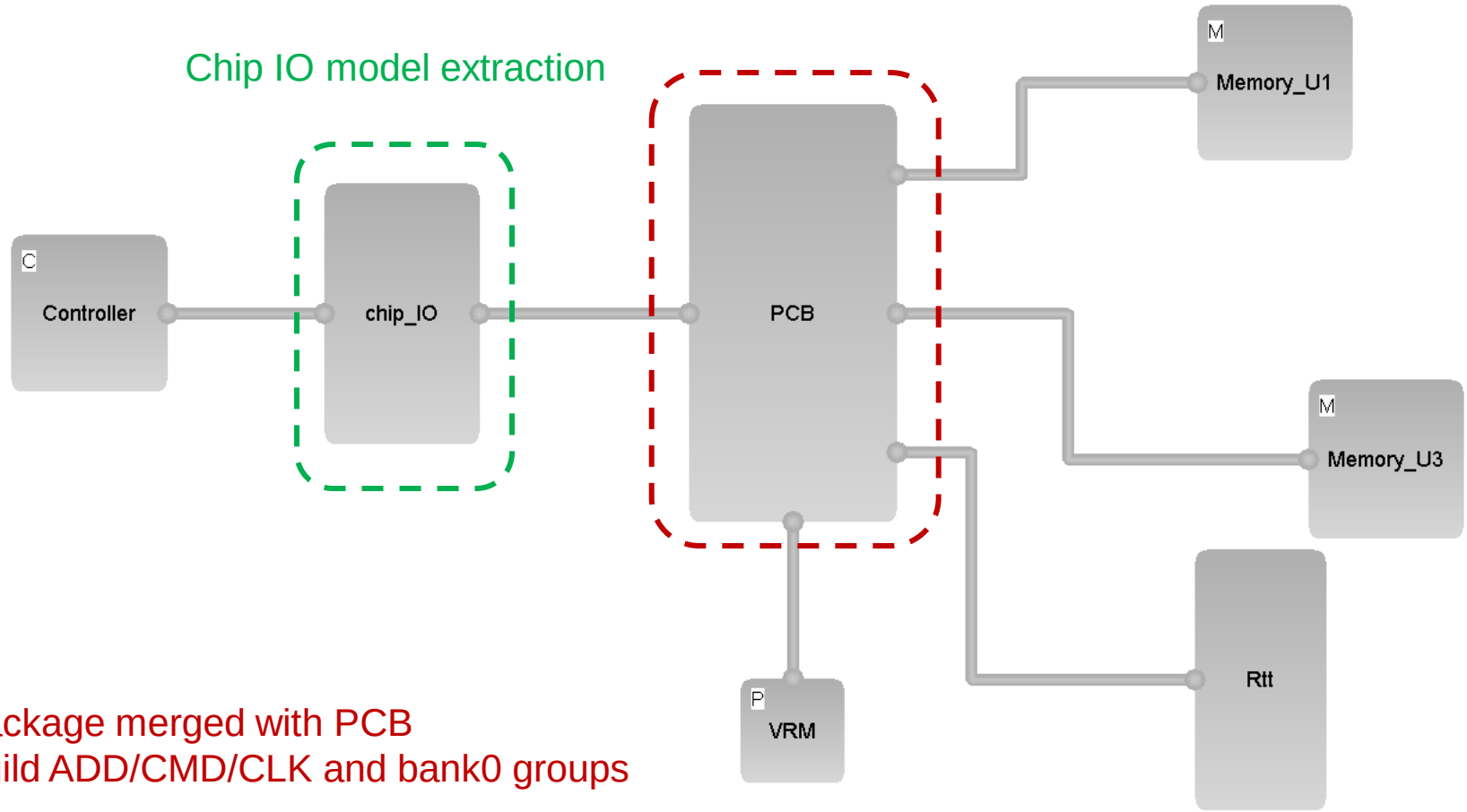


Power aware signal integrity analysis

System level SI/PI analysis (DQ/DQS) with memory write in TD—ODT60



Test vehicle of system level SI/PI analysis coupling among ADD/CMD/CLK and DQ/DQS



Package merged with PCB
Build ADD/CMD/CLK and bank0 groups

Test vehicle of system level SI/PI analysis coupling among ADD/CMD/CLK and DQ/DQS

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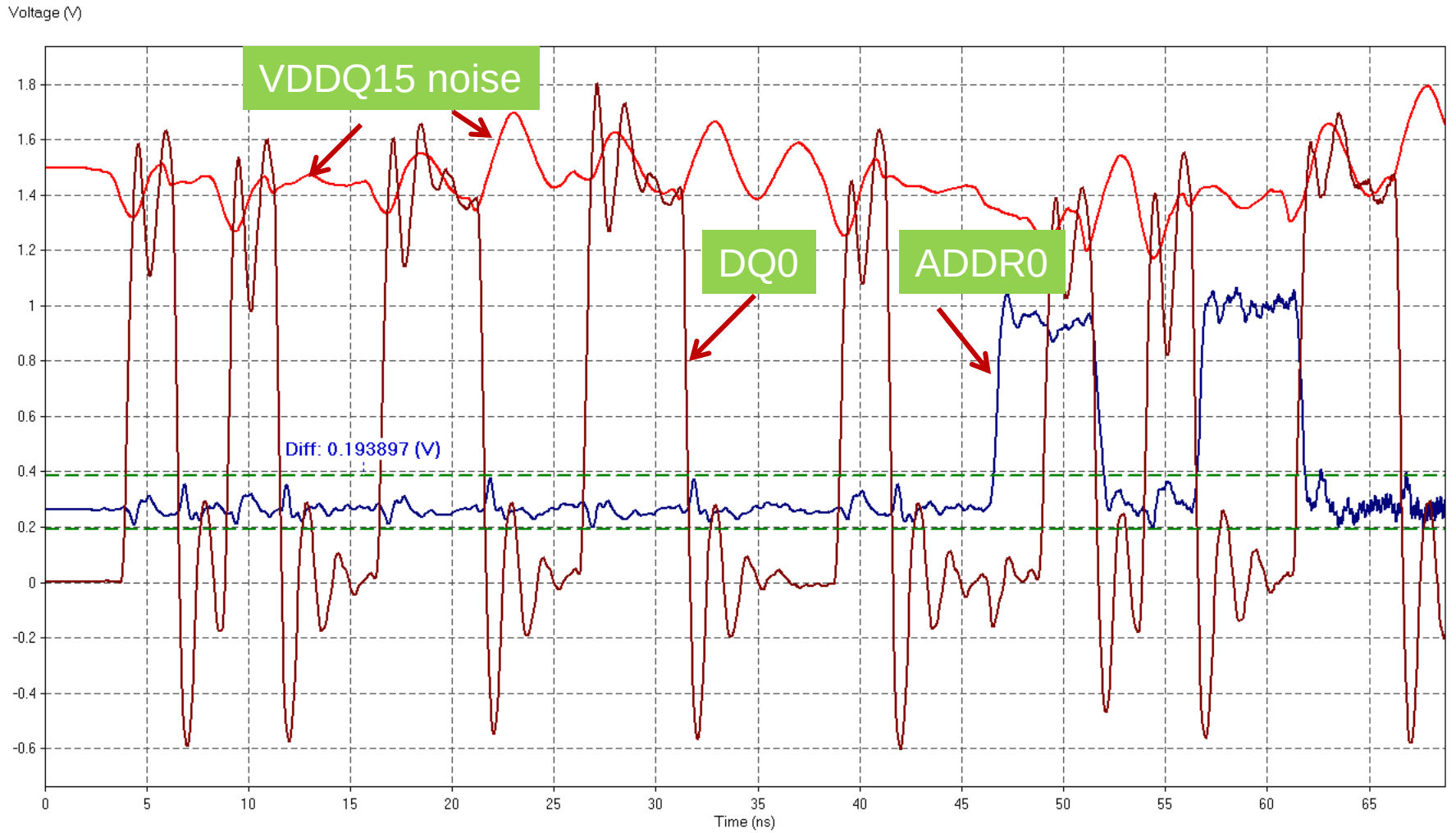
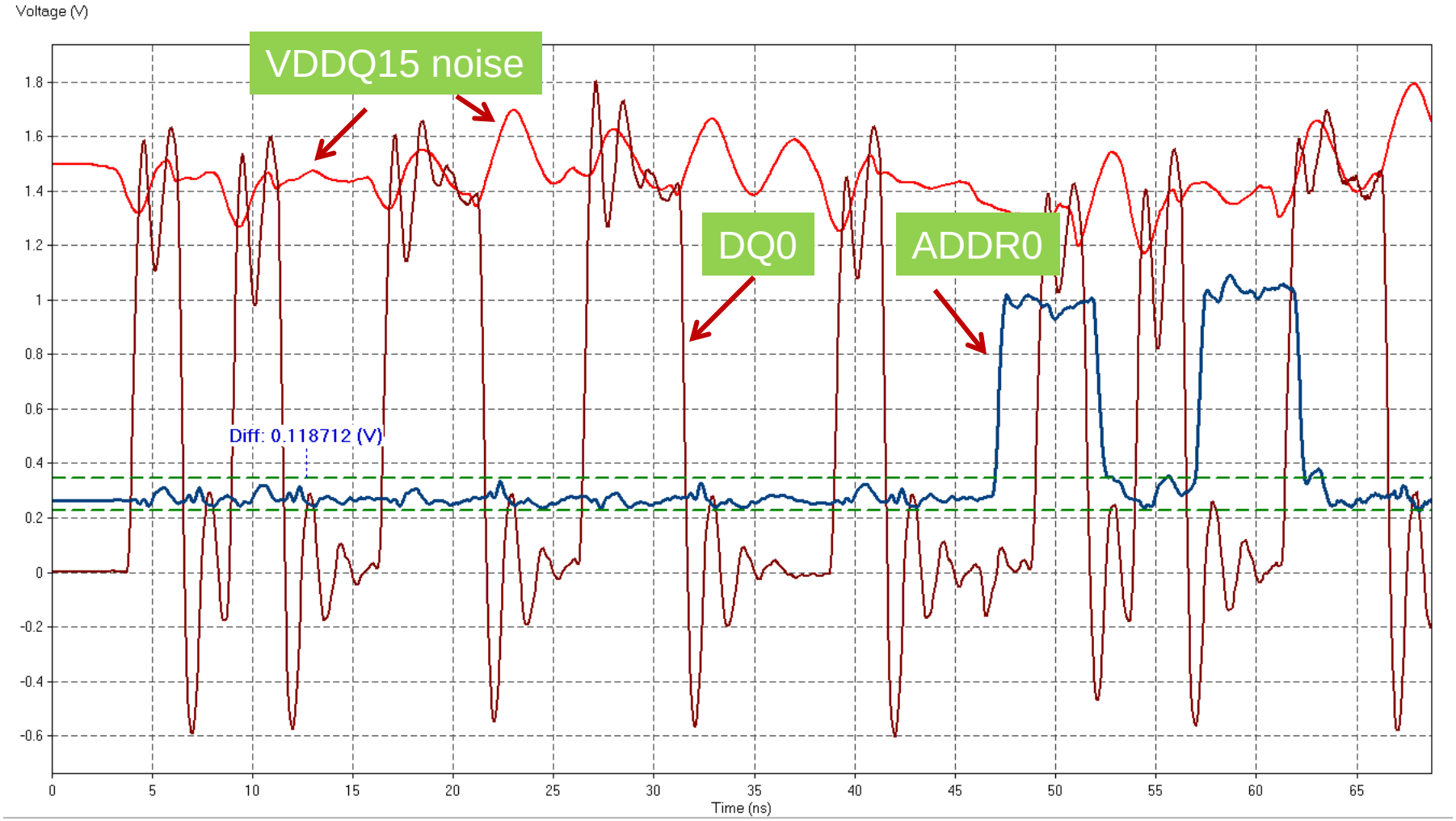
Bus Group/Signal	Stimulus Pattern	Stimulus Offset (ns)	Transmit IO Model	Status
ADD_GP	00000000000000000001100110000111100000111100l100..	0		
ADDR0	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR1			se_drv15_odtoff	Not Connected
ADDR2	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR3	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR4	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR5	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR6	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR7	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR8	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR9	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR10	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR11	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR12	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR13	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR14	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
ADDR15	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
BA0	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
BA1	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
BA2			se_drv15_odtoff	Not Connected
CASN	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
CKE	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
CS_N	00000000000000000001100110000111100000111100l100..	0	se_drv15_odtoff	Signal
dm0	0101001100110001000..	0	se_drv15_odtoff	Signal
dm1	0101001100110001000..	0	se_drv15_odtoff	Signal
dq0	0101001100110001000..	0	se_drv15_odtoff	Signal
dq1	0101001100110001000..	0	se_drv15_odtoff	Signal
dq2	0101001100110001000..	0	se_drv15_odtoff	Signal
dq3	0101001100110001000..	0	se_drv15_odtoff	Signal
dq4	0101001100110001000..	0	se_drv15_odtoff	Signal
dq5	0101001100110001000..	0	se_drv15_odtoff	Signal

- Running DQ/DQS patterns first then turn on ADD/CLK.
- To measure ADD/CLK lines noise while DQ/DQS are toggling.
- To monitor ADD/CLK waveform and see if they are affected by DQ/DQS
- All DQ/DQS are in ODT-off

Coupling among bank0 and ADD/CMD (measured at U1)

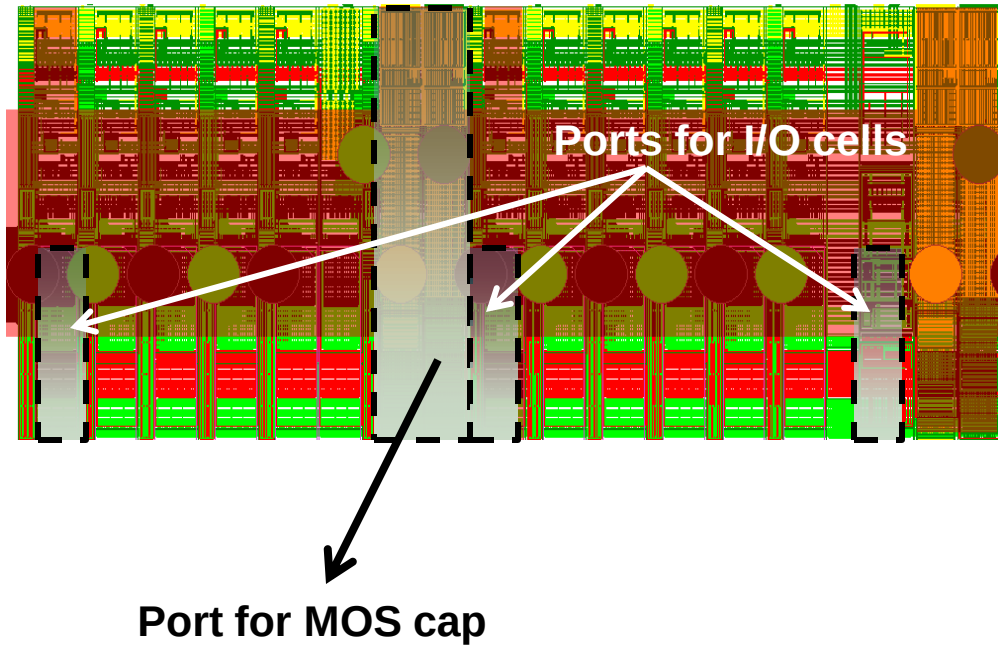


Coupling among bank0 and ADD/CMD (measured at U3)

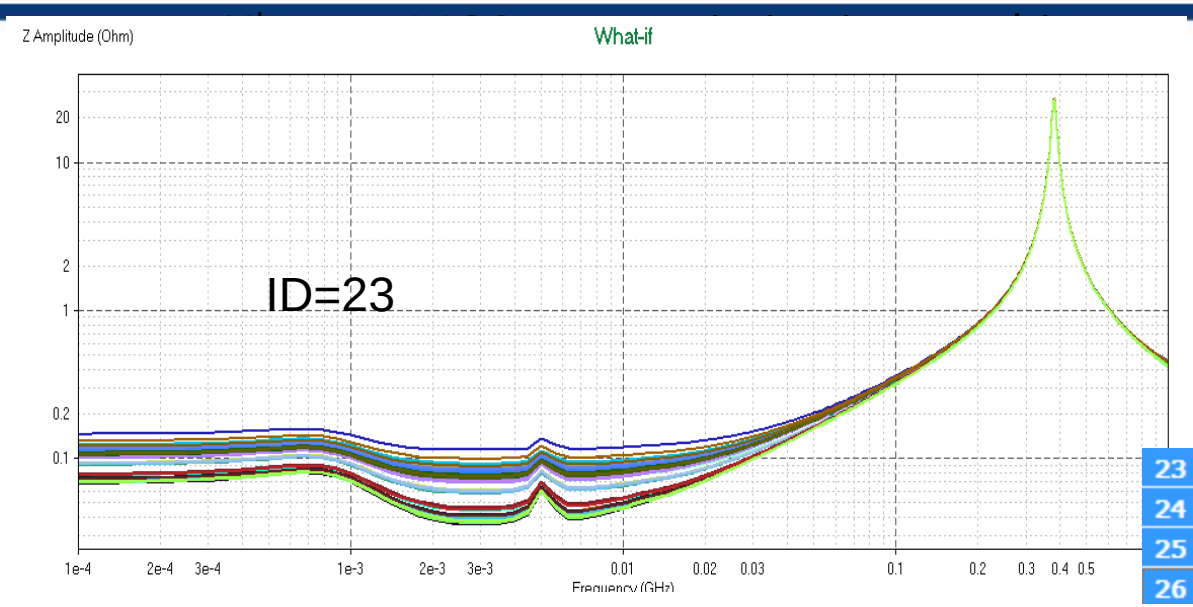


Chip Decap What-if Analysis and Optimization

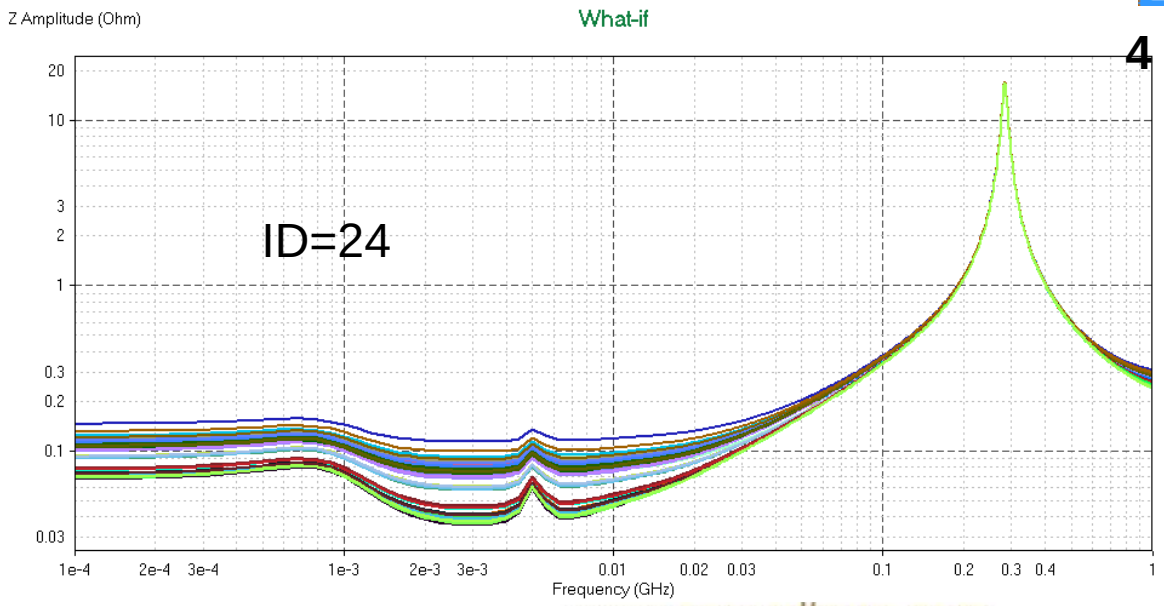
- Ports for IO cells which can be impedance observations
- Ports for PSCAP/MOS cap cells which can be decaps and optimized



Power integrity analysis



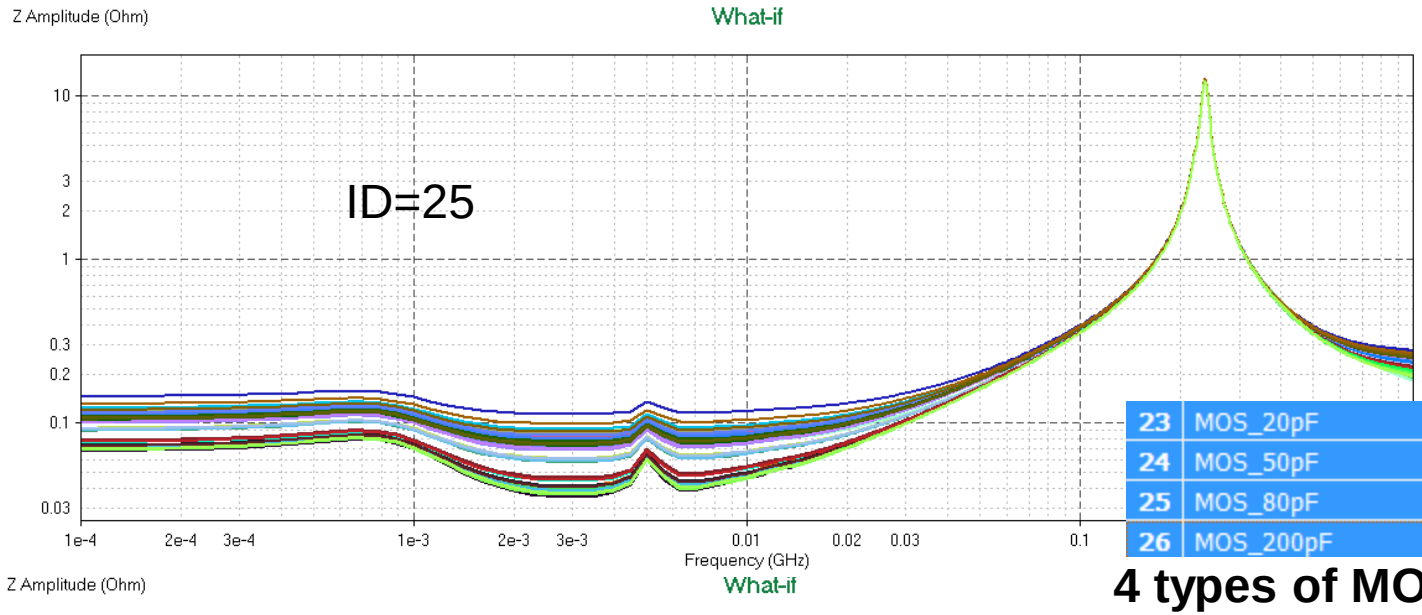
23	MOS_20pF
24	MOS_50pF
25	MOS_80pF
26	MOS_200pF



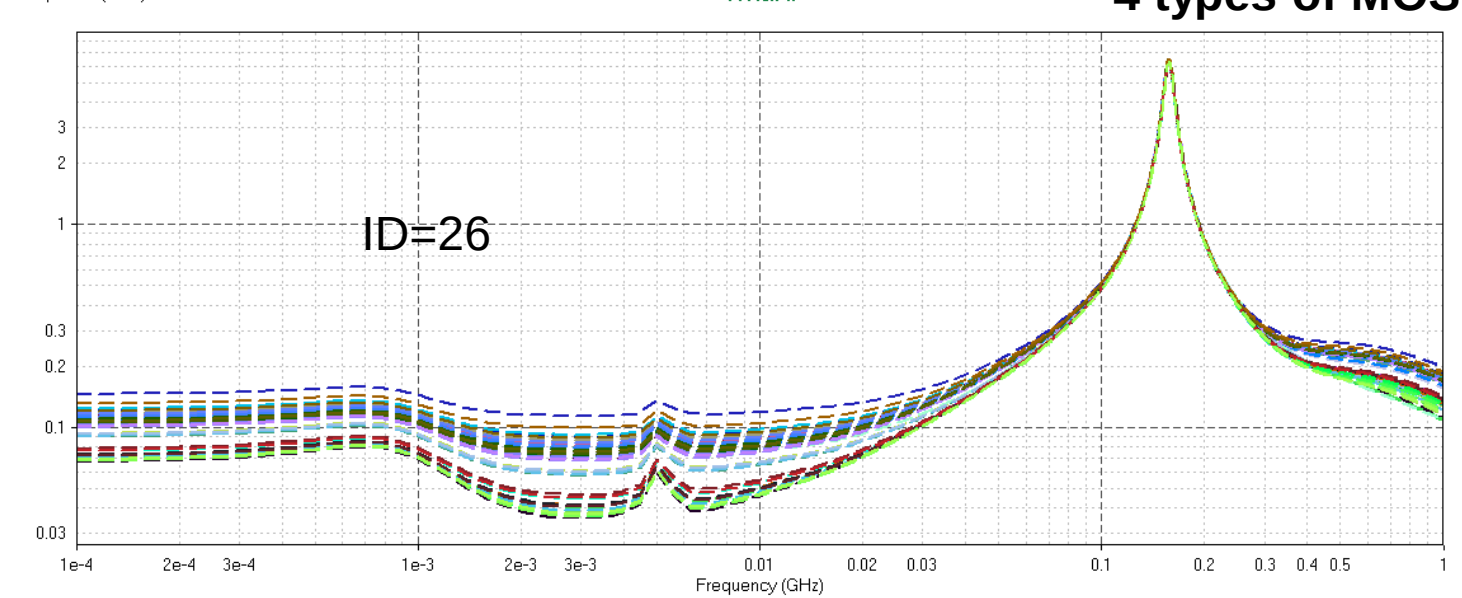
4 types of MOS cap value

Power integrity analysis

--1st stage MOS caps optimization on chip



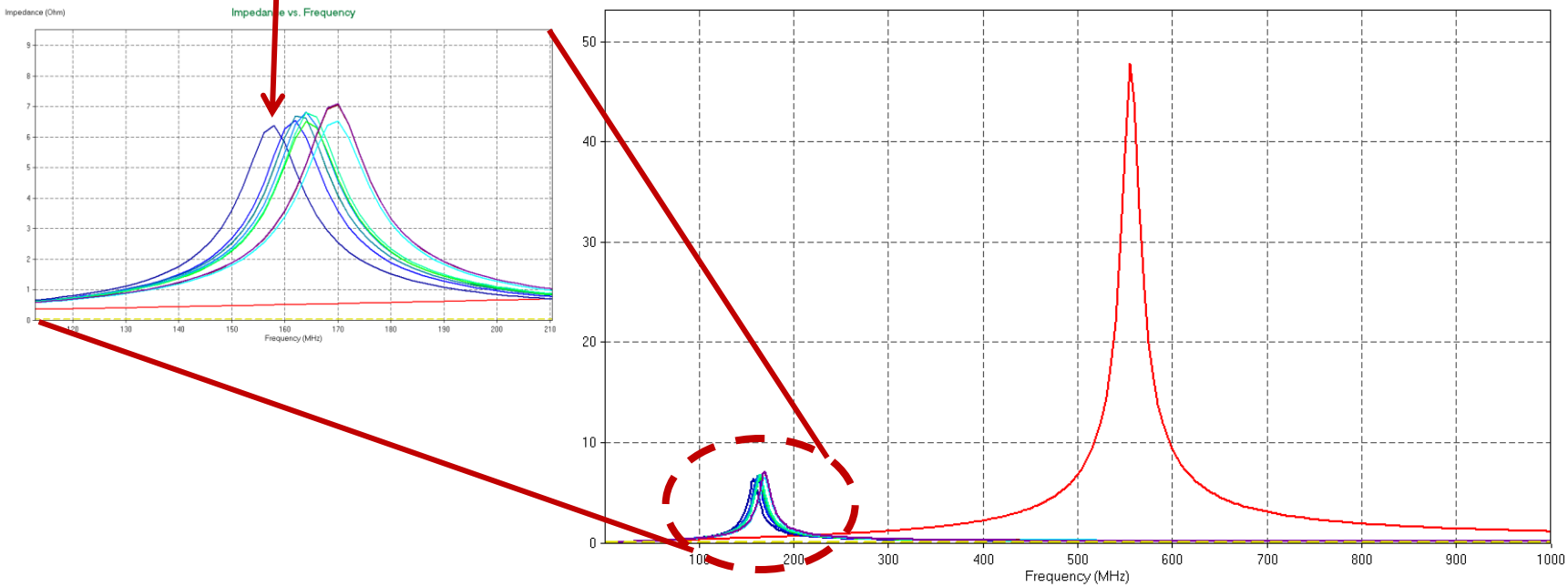
4 types of MOS cap value



Power integrity analysis

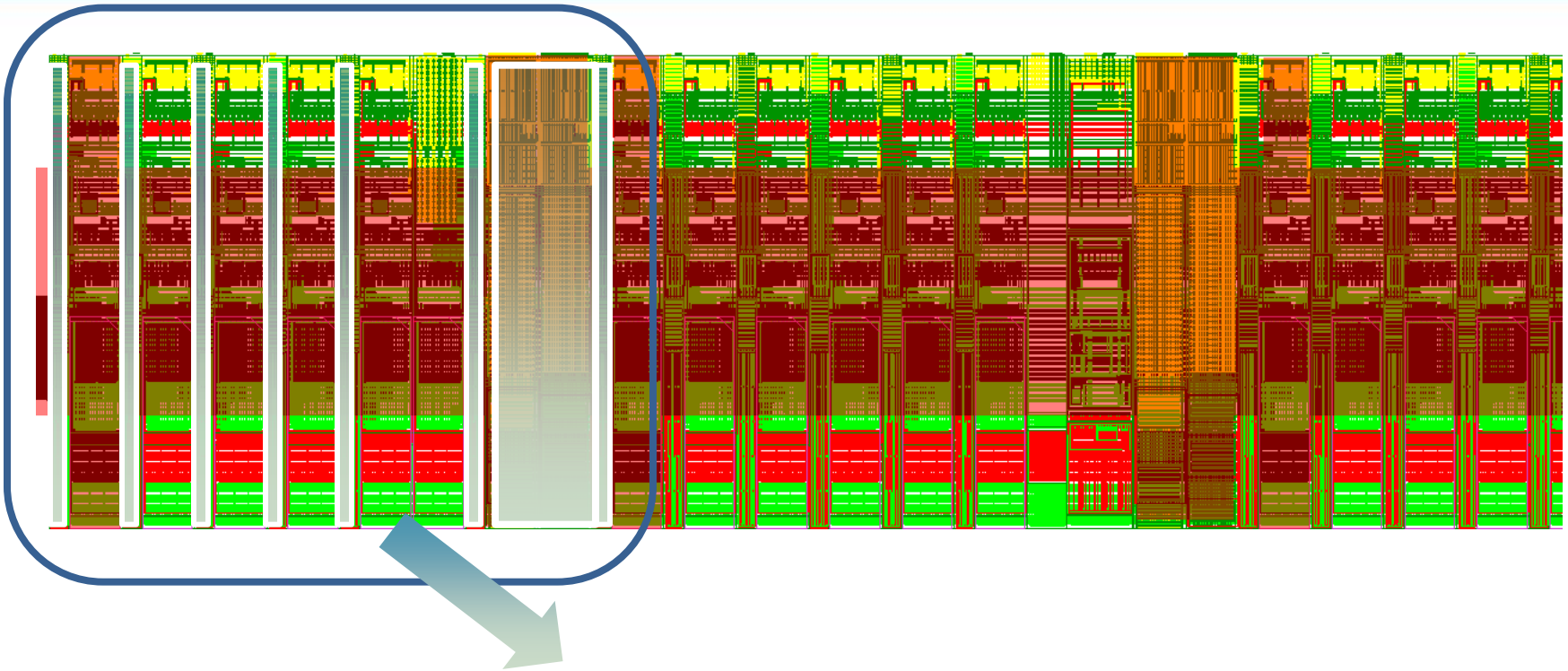
--1st stage MOS caps optimization on chip

A	G	H	I	J	K	L	M	N	O	P	Q
Scheme ID	**chio_io_pdn_**	**chio_io_pd**	**chio_io_pd**	**chio_io_pd**	**chio_io_pd**	**chio_io_pd**	**chio_io_pd**	**chio_io_pd**	**chio_io_pd**	**chio_io_pd**	**chio_io_pd**
Original Scheme	X	X	X	X	X	X	X	X	X	X	X
Scheme 1	26	26	26	26	26	26	26	26	26	26	26
Scheme 2	26	26	26	26	26	26	26	26	25	26	26
Scheme 3	26	26	26	26	24	26	26	26	26	26	26
Scheme 4	26	26	24	26	26	26	26	26	26	26	26
Scheme 5	26	26	26	26	23	26	26	26	26	26	26
Scheme 6	26	26	26	26	26	26	26	26	26	26	X
Scheme 7	26	26	26	26	X	26	26	26	26	26	26
Scheme 8	26	26	26	26	26	26	26	26	26	24	23
Scheme 9	26	26	25	26	X	26	26	26	26	26	26
Scheme 10	26	26	25	X	26	26	26	26	26	26	26



MOS caps with 200pF for each cell will have best impedance profile

Chip Decap What-if Analysis and Optimization



- This is the definition of big cell with x7 small and x1 large cells
- Total value for this big cell is ranging from 20,50,80,200PF.
- A strongly recommendation that places MOS caps as much as possible

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- Chip IO interconnect model should include IO Power/Ground/Signal Interconnect Model
- For high speed and low power DDR systems (LPDDR3/DDR3L/DDR4), Chip IO interconnect model is crucial for IO-SSO analysis.
- Chip IO interconnect model is one part for Chip but not in IBIS model.
- With Chip IO Interconnection model, Chip vendor can do more accurate DDRn signoff analysis to predict System electrical performace before ASIC tapeout.
- On-die RC or better distributed chip IO interconnect model can be more realistic for signal/power analysis
- New System Signoff methodology enable to avoid overdesign or under-design for on-die Decap Cell

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