WELCOME FROM MICHAEL MIRMAK, INTEL CORPORATION

On behalf of the I/O Buffer Information Specification (IBIS) Open Forum, I would like to welcome our presenters and guests to the Asian IBIS Summit in Shanghai.

This year, we celebrate our ninth annual IBIS Summit in the People's Republic. Since the first summit in China, four separate revisions of the IBIS specification have been released. The Open Forum is lucky to have a solid nine-year history of working alongside our friends and colleagues in the People's Republic to improve IBIS. We are thankful for your help and for another challenging technical program this year.

We are especially grateful to our sponsors Huawei Technologies, Agilent Technologies, ANSYS, Cadence Design Systems, Intel Corporation, IO Methodology Inc., Synopsys, and Teledyne LeCroy for making this Summit possible.

Our thanks to you for participating and best wishes for a successful summit!

Sincerely,

马梦宽
Michael Mirmak
Chair, IBIS Open Forum

我仅代表 I / O 缓冲信息规范（IBIS）开放论坛，欢迎我们的嘉宾来参加在上海举行的亚洲 IBIS 峰会。

今年是在中华人民共和国举行的第九个年度的 IBIS 峰会。在这九年中，我们已推出了四个 IBIS 更新版本。IBIS 开放论坛非常幸运的能和大家一起来进行技术更新的工作。我们也感谢有机会在中华人民共和国再次和我们的朋友和同仁一起研讨更深入的技术方案。

我们要特别感谢我们的赞助商华为技术有限公司，安捷伦科技公司，ANSYS，Cadence Design Systems，IO Methodology，英特尔公司, Synopsys 公司 和 Teledyne LeCroy, 他们使本次峰会成为可能。

感谢您的参与并预祝会议圆满成功！

马梦宽
主席，IBIS 开放论坛

WELCOME FROM LI JINJUN, HUAWEI TECHNOLOGIES

Ladies and Gentleman,

On behalf of Huawei Technologies, welcome to the eighth annual Asian IBIS Summit (China). I would like to express my appreciation to IBIS Open Forum and all the sponsors for co-organizing this event.

Since 2005, IBIS Asian Summit in China has been the top-level international conference in high speed digital design society in China. I am looking forward to work with IBIS members in China, and to expand our participations in the region.

Huawei has actively involved in all IBIS society's events. We hope to resolve high speed link issues with IBIS Open Forum, EDA vendors and IC vendors. Your comments and suggestions will be deeply appreciated!

Welcome all of you to Shanghai! Hope you will enjoy all the technical discussions and sharing throughout the meeting, and have a nice journey!

Thank you!
Li Jinjun
Huawei Technologies

各位专家，各位来宾：

我代表华为公司，欢迎大家来参加第 8 届亚洲 IBIS 技术研讨会，衷心地感谢 IBIS 协会组织本次会议。

自从 2005 年以来，IBIS 技术研讨会已经成为了中国高速设计领域的一次盛会。我很高兴有机会与 IBIS 协会一起促进和扩大在该领域的分享。

华为积极参与各项 IBIS 活动，希望与 IBIS 协会、EDA 软件、芯片公司一道来共同解决许多高速链路设计上的挑战，欢迎大家会上讨论和建议。

欢迎 IBIS 专家来到上海，希望你们能够喜欢所有的技术讨论和会议分享，度过美好一天。

谢谢大家
华为公司 厉进军

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

8:15 SIGN IN
- Vendor Tables Open at 8:30

8:45 **Welcome**
- Li, JinJun
  (Huawei Technologies, China)
- Wang, Lance
  (Vice-Chair, IBIS Open Forum, IO Methodology, USA)

9:00 **Introducing IBIS 6.0** **5**
Mirmak, Michael (Intel Corporation, USA)

9:30 **IBIS Summary Documents** **12**
Ross, Bob (Teraspeed Consulting Group, USA)

10:00 **More on IBIS Modeling for Load-Dependent Current-Mode Differential Drivers** **18**
Wang, Lance (IO Methodology, USA)

10:30 BREAK (Refreshments and Vendor Tables)

10:50 **Combined I-V Table Checking Problem** **24**
Ross, Bob*; Sun, YingXin** and Li, Joy**
(*Teraspeed Consulting Group and **Cadence Design Systems, USA)

11:20 **An Advanced Behavioral Buffer Model With Over-Clocking Solution** . . **32**
Sun, YingXin and Chen, Raymond Y. (Cadence Design Systems, USA)

12:00 FREE BUFFET LUNCH (Hosted by Sponsors)
- Vendor Tables

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

Introducing IBIS 6.0

Michael Mirmak
Intel Corp.
Chair, IBIS Open Forum

Asian IBIS Summit
Shanghai, People's Republic of China
November 15, 2013

http://www.eda.org/ibis/

Agenda

- IBIS 6.0 in Summary
  - Key Features
  - Changes from IBIS 5.1
- What problems does 6.0 address?
- Issues to Resolve
- What's Next?
- Questions

Key Features of IBIS 6.0

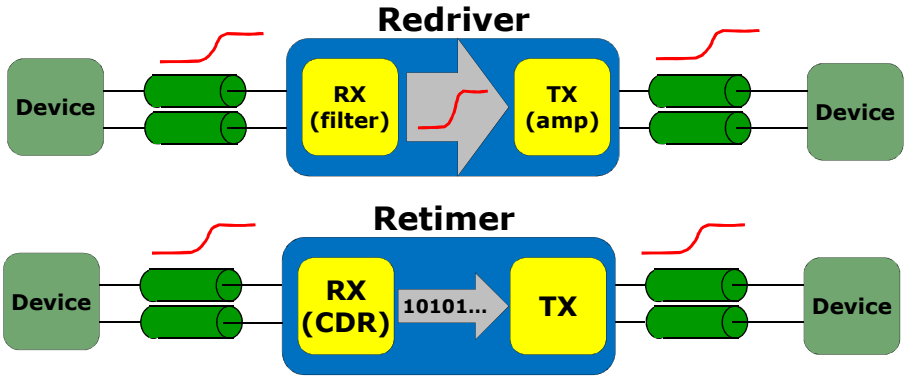
- IBIS 6.0 was approved September 20, 2013
  - http://www.eda.org/ibis/ver6.0/
- Major additions focus on IBIS-AMI
  - Adds redriver and retimer support
  - Expands jitter/noise parameters
  - Clarifies analog buffer impedance descriptions
  - Supports IBIS-ISS (Interconnect SPICE Subcircuits) and Touchstone 1.x/2.0

Other Changes from IBIS 5.1

- Clarifications of A/D and D/A converters in [External Model] and [External Circuit]
  - Parameter passing now supported!
- Additional files supported for IBIS-AMI
  - Including explicit paths
  - Identifiers for individual IBIS-AMI model instances
- List Tips for IBIS-AMI Lists
  - Associates labels with parameter lists
- Improved organization of the document
  - Easier to read and use

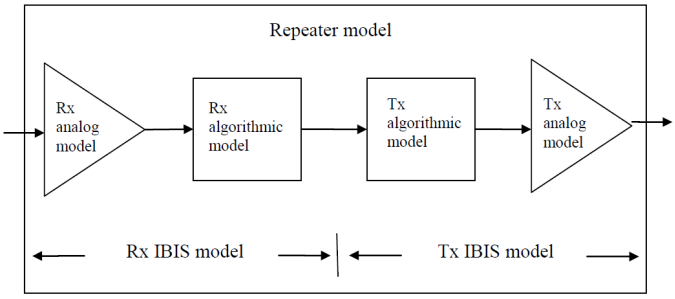
IBIS 6.0 Support Examples

- How do I model a mid-bus repeater?
  - Recall the repeater types: retimers and redrivers
  - Think of redriver as filtering and/or amplifying analog *signals*
  - Think of retimer as using clock-data recovery to re-transmit *data*



IBIS 6.0 Support Examples

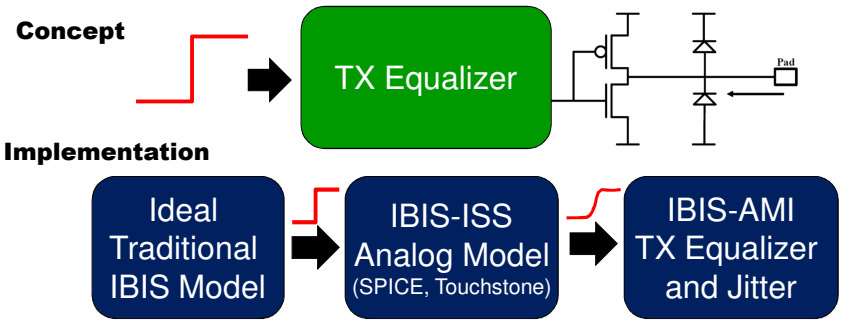
- How do I model a mid-bus repeater?
  - Use [Repeater Pin] to identify RX and TX pins
  - Define “Redriver” or “Retimer” in the .ami parameters file under “Repeater_Type”
  - For Retimers, ensure AMI_GetWave is defined and included



from the IBIS 6.0 specification

IBIS 6.0 Support Examples

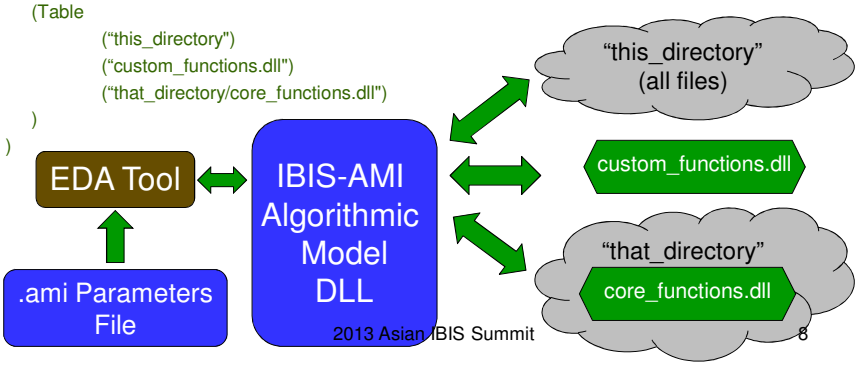
- Where to "put" the analog impedance of the buffer?
- What if I can't easily represent the analog behavior of my buffer using traditional IBIS?
  - In 6.0, use IBIS-ISS to represent complex analog buffer behavior
  - Traditional IBIS becomes ideal (TX or RX)



IBIS 6.0 Support Examples

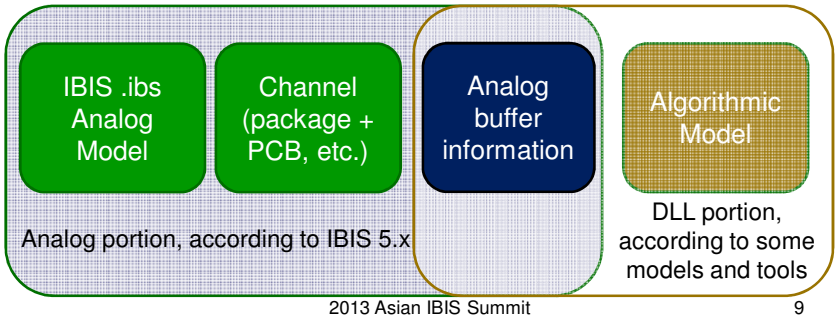
- What if your algorithmic model isn't a single file?
  - Multiple files, in different locations, now supported
  - From the .ami parameters file…

```
(Supporting_Files (Usage Info) (Type String)
   (Description "Additional files and directories required by this model")
   (Table
         ("this_directory")
         ("custom_functions.dll")
         ("that_directory/core_functions.dll")
   )
)
```



Issues to Resolve

- Ensuring true IBIS-AMI model compatibility
  - Some models under IBIS 5.x place buffer analog information in the executable (DLL or SO file)
  - This may be a problem for some tools
  - Use of IBIS 6.0 improved analog modeling can help ensure portability



Issues to Resolve

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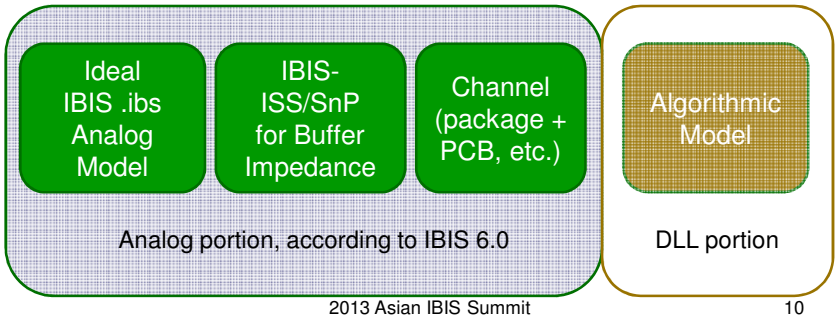

Issues to Resolve

- Improving IBIS packages
  - Two separate approaches being discussed
  - Objective is to finalize a package model format that…
    - *Can interact with IBIS and related files*
    - *Supports time- and frequency-domain modeling data in IBIS-ISS format*
    - *Supports arbitrary numbers of crosstalking signal lines in individual segments*
  - Target is to include this in the next major IBIS release

What's Next?

- A parser: IBISCHK6
  - Check new keyword syntax
  - Check new IBIS-AMI parameter syntax
  - Simple checks for IBIS-AMI DLL/SO executables?
    - *Are the required IBIS-AMI functions present?*
    - *Do the functions execute (instead of crashing)?*
- Is a parser for IBIS-ISS required?
  - SPICE features used in IBIS-ISS are very common across EDA tools
- IBIS version updates
  - IBIS continues to target updates twice per year

Questions?

IBIS Summary Documents

Bob Ross
Asian IBIS Summit, Shanghai, China
November 15, 2013
bob@teraspeed.com

(presented by Anders Ekholm, Ericsson)

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Document Samples

- Keyword Hierarchy tree in IBIS Version 6.0, Section 3.1
- Expanded Keyword Hierarchy tree
- Evolution document
- IBIS-AMI parameter tables in IBIS Version 6.0, Section 10.7
- These documents summarize the IBIS elements

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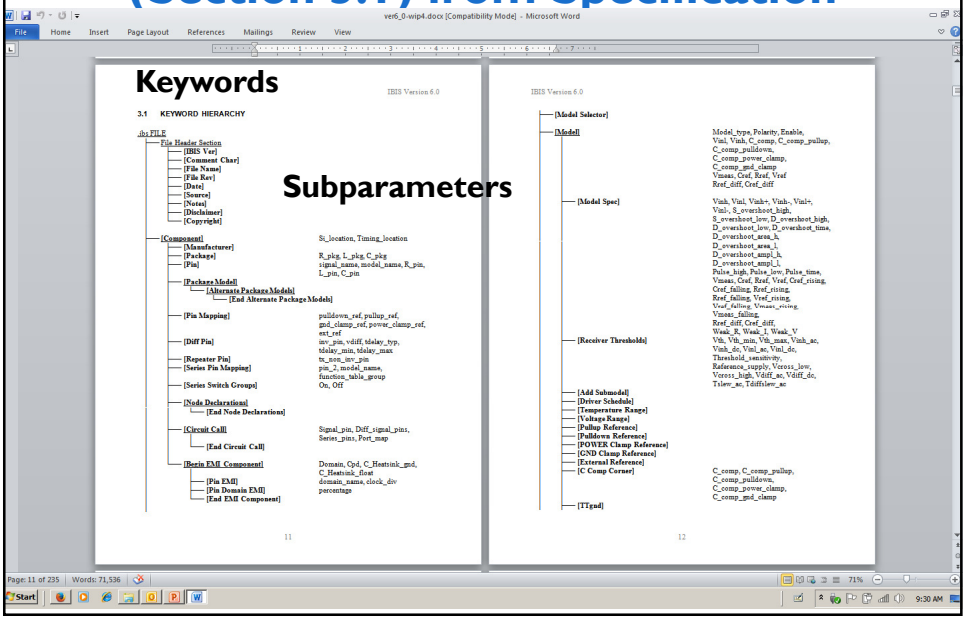
Official Keyword Hierarchy (Section 3.1) from Specification



Unofficial Keyword Hierarchy Updated from September, 2007

- Keyword Hierarchy tree
  - 165 distinct keyword usages
  - Some keywords are re-used in different contexts (e.g., [IBIS Ver], [End], [Rising Waveform], etc. and in .ibs, .pkg and .ebd files)
- Hierarchy documents updated with Version 5.1 and Version 6.0 information

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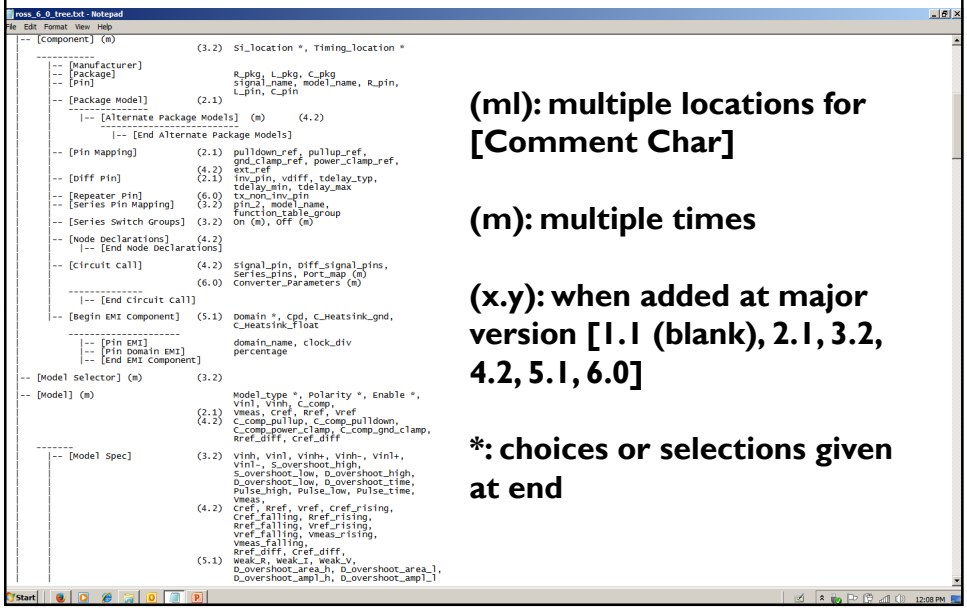
Unofficial Keyword Hierarchy Tree with Extra Information



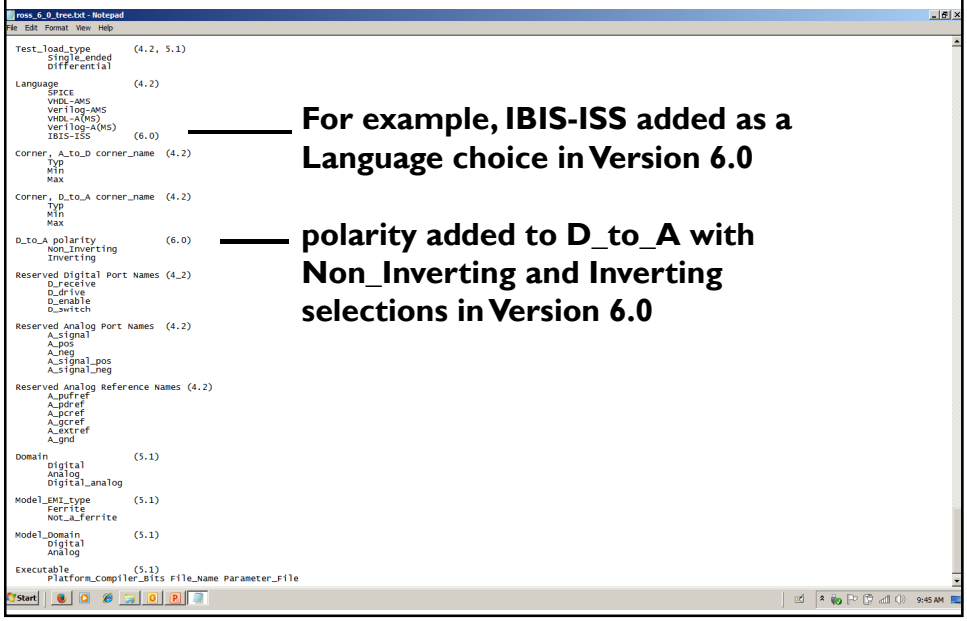
(ml): multiple locations for [Comment Char]

(m): multiple times

(x.y): when added at major version [1.1 (blank), 2.1, 3.2, 4.2, 5.1, 6.0]

***: choices or selections given at end**

Enumerated Choices at End



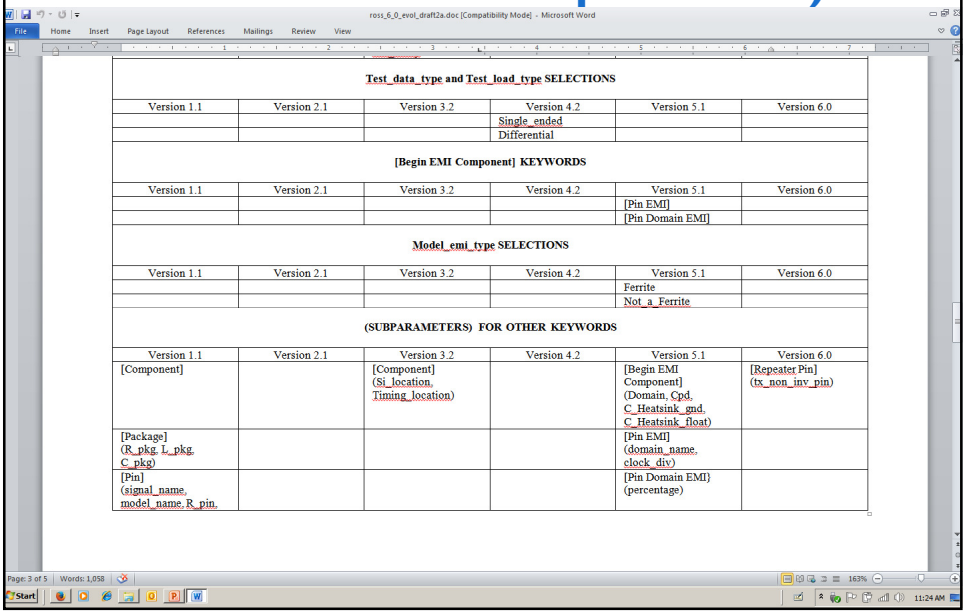
For example, IBIS-ISS added as a Language choice in Version 6.0

polarity added to D_to_A with Non_Inverting and Inverting selections in Version 6.0

Unofficial Evolution Document

- Evolution document features:
  - Updated columns show major version evolution
  - Rules and changes evolution
  - Significant subparameter selections such as the *_type subparameter choices
- Hierarchy and Evolution documents contain overlapping information, but expanded Hierarchy document has more detail
- Sample page shown next

Evolution Document (*_type, EMI Information and Repeater Pin)



Test_data_type and Test_load_type SELECTIONS

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0
			Single_ended		
			Differential		

[Begin EMI Component] KEYWORDS

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0
				[Pin EMI]	
				[Pin Domain EMI]	

Model_emi_type SELECTIONS

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0
				Ferrite	
				Not_a_Ferrite	

(SUBPARAMETERS) FOR OTHER KEYWORDS

Version 1.1	Version 2.1	Version 3.2	Version 4.2	Version 5.1	Version 6.0
[Component]		[Component] (Si_location, Timing_location)		[Begin EMI Component] (Domain, Cpd, C_Heatsink_gnd, C_Heatsink_float)	[Repeater Pin] (tx_non_inv_pin)
[Package] (R_pkg, L_pkg, C_pkg)				[Pin EMI] (domain_name, clock_div)	
[Pin] (signal_name, model_name, R_pin,				[Pin Domain EMI] (percentage)	

IBIS-AMI .ami File Parameter Syntax (Section 10.3)

(<parameter_name>
(**Usage** <usage>) | required
(**Type** <data_type>) | required
({**Format**} <**data_format**> <data>) | required *

(**List_Tip**) | optional with ({Format} **List**)
(**Default** <value>) | optional or illegal *
(**Description** <string>) | optional
)

* **Value** or **Default**, but not both, and other rules

New - Four Summary Tables in Section 10.7 of the Specification

- **Usages** for **Reserved Parameters**
- **Types** for **Reserved Parameters**
- **Formats** for **Reserved Parameters**
- **Types** for **Format** values
- 28 **Reserved Parameters**, 18 new since Version 5.1
- Part of one table shown next

IBIS-AMI Reserved Parameters and Allowable Data Types

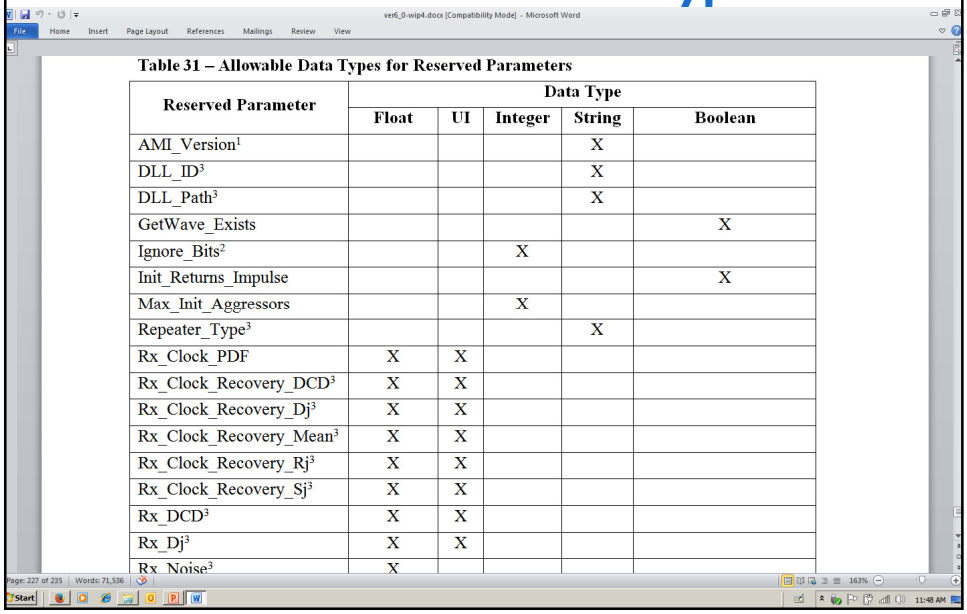


Table 31 – Allowable Data Types for Reserved Parameters

Reserved Parameter	Data Type				
	Float	UI	Integer	String	Boolean
AMI_Version[1]				X	
DLL_ID[3]				X	
DLL_Path[3]				X	
GetWave_Exists					X
Ignore_Bits[2]			X		
Init_Returns_Impulse					X
Max_Init_Aggressors			X		
Repeater_Type[3]				X	
Rx_Clock_PDF	X	X			
Rx_Clock_Recovery_DCD[3]	X	X			
Rx_Clock_Recovery_Dj[3]	X	X			
Rx_Clock_Recovery_Mean[3]	X	X			
Rx_Clock_Recovery_Rj[3]	X	X			
Rx_Clock_Recovery_Sj[3]	X	X			
Rx_DCD[3]	X	X			
Rx_Dj[3]	X	X			
Rx_Noise[3]	X				

Conclusion

- Summary information provides quick references for IBIS and IBIS-AMI syntax
- Document references

  http://www.eda.org/ibis/ver6.0/

  ver6_0.docx, .pdf (official specification)

  tree_6_0.txt (unofficial)

  evol_6_0.docx, .pdf (unofficial)

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More on IBIS Modeling for Load-Dependent Current-Mode Differential Drivers

Lance Wang (lwang@iometh.com)
IO Methodology Inc.
2013 IBIS Asian Summit
Nov. 15, 2013 Shanghai

Outlines

- Motivation
- Load-Dependent Current-Mode Differential Driver
- IBIS Extraction Method
  - Legacy method
  - Enhanced extraction method
- Summary

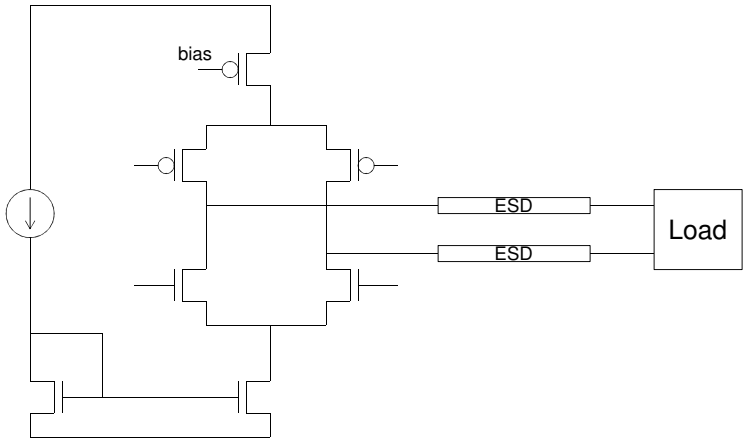
Note: The partial materials in this presentation have been presented in 2013 European IBIS Summit in Paris

Motivation

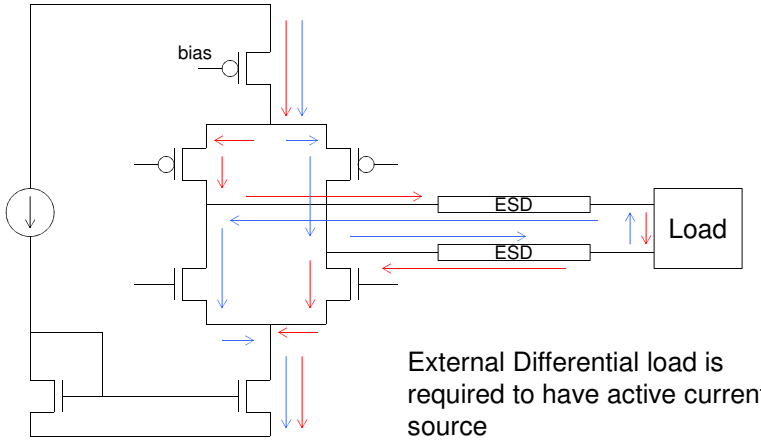
- Load-dependent current-mode differential pair buffers are found increasingly often in GHz serial link designs
  - Easy to control the output current and common-mode voltage
  - Often used in pre-emphasis buffers
- Using traditional IBIS buffer extraction method is not accurate enough

Is it possible to use the current IBIS spec for this kind of differential buffer?

Load-Dependent Current-Mode Differential Driver



Load-Dependent Current-Mode Differential Driver (Current Flow)



External Differential load is required to have active current source

IBIS Extraction Method (Modeling as 2 individual pins)

No load to be used for I-V curve extraction

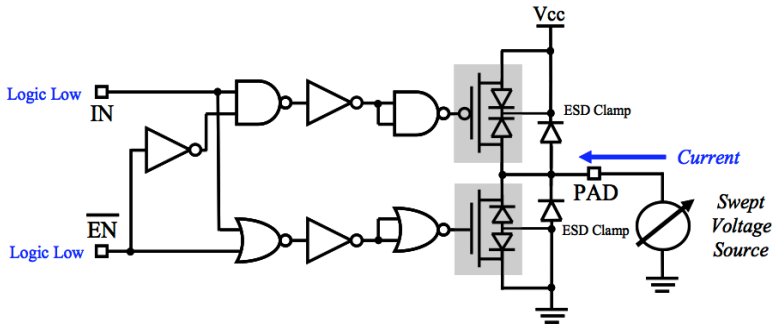


Figure 3.1 – Standard 3-state Buffer (Pulldown I-V Table Extraction Shown)

Pictures from IBIS cookbook

IBIS Extraction Method (Modeling as 2 individual pins)

Load connected to GND or VCC to be used for V-T curve extraction

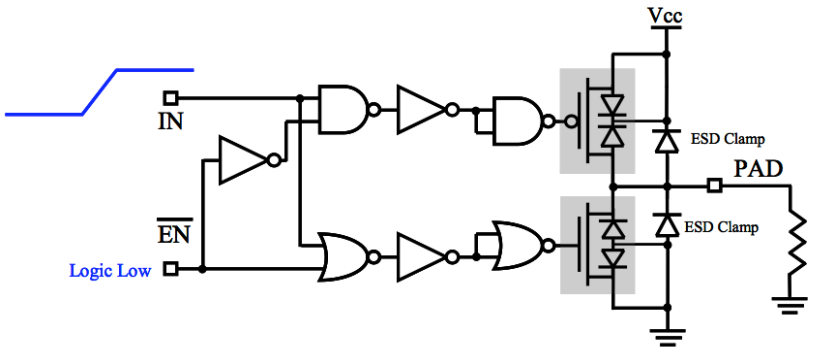
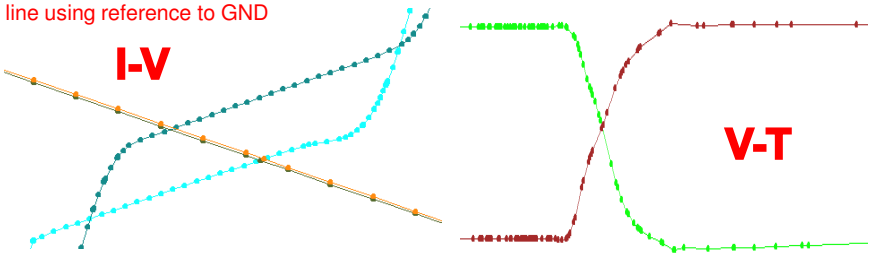


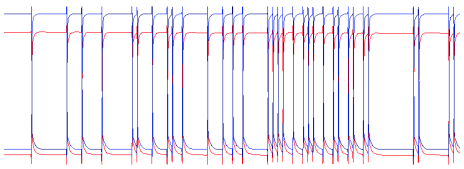
Figure 3.2 – Simulation Setup for Extracting Ramp Rate Information (Rising Edge Shown)

Pictures from IBIS cookbook

Using normal extraction methods for I-V and V-T curves

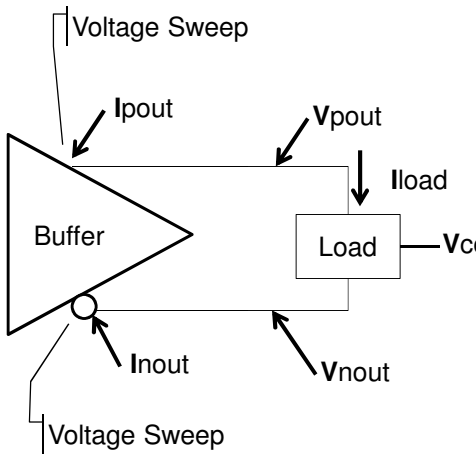
* I-V curves shown are combined curves and load line using reference to GND





Correlation shows they are way off from the Spice result
RED – Spice, BLUE - IBIS

Enhanced I-V Extraction Method

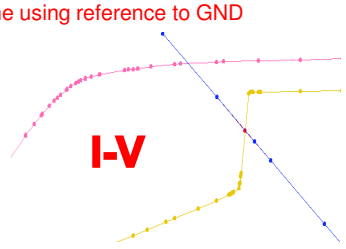


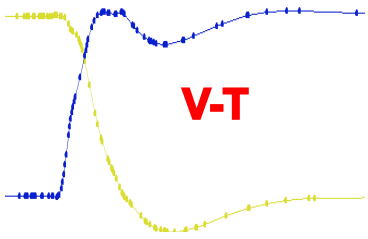
The IBIS I-V will be:
Ip(i-v) = Ipout – Iload
In(i-v) = Inout + Iload

The IBIS V-T will be:
Vpout and Vnout with
V_fixture = Vcommon
R_fixture = Rload/2

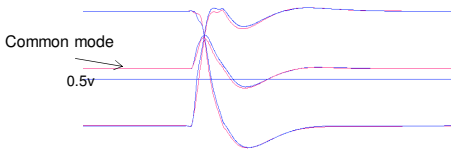
Using enhanced extraction method with differential load

* I-V curves shown are combined curves and load line using reference to GND





Correlation shows matched result with Spice
RED – SPICE, BLUE - IBIS



Summary

- Normal IBIS extraction method for load-dependent current-mode differential pair buffers produces inaccurate models
- Enhanced method considering differential load can solve this issue. It gives the matched results when correlating with Spice simulation results
- It would be better to have IBIS Spec accept “Rref_diff/Cref_diff” kind of differential loads for regular IBIS differential pair models
  - Rref_diff/Cref_diff is limited for External model use now
- IBIS Spec needs to be enhanced when modeling dynamic PLL current mode buffer
  - Various I-V tables for different diff_loads
  - Current dependent C-comp value table

Combined I-V Table Checking Problem

Asian IBIS Summit
Shanghai, China, November 15, 2013

Bob Ross
Teraspeed Consulting Group
bob@teraspeed.com

Yingxin Sun and Joy Li
Cadence Design Systems
sunyx@cadence .com
joyli@cadence.com

Presented by Anders Ekholm, Ericsson

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Real Data from BUG140 and Cadence Presentations

- BUG140: http://www.eda.org/ibis/bugs/ibischk/bug140.txt
- (In all test cases, the [Gnd Clamp] data is 0.0 in the region of interest)
- Presentations
  - "Golden Parser Non-monotonic Warning's Investigation" by Yingxin Sun and Joy Li, November 9, 2012: http://tinyurl.com/byqu7yn (Presented at the IBIS Quality Committee November 27, 2012)
  - "Combined I-V Table Checks (BUG140)", January 31, 2013 IBIS Summit, Bob Ross, Yingxin Sun, and Joy Li
  - "Ibischk5 Specification and Parser", May 15, 2013 IBIS Summit, Bob Ross and Mike LaBonte (Signal Integrity Software)

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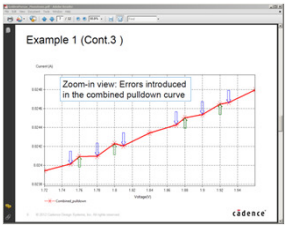
BUG140 Issue

- Unexpected Non-Monotonic Warnings for Combined I-V Tables (derived from monotonic data)



- Combined I-V table checks:
  - [Pulldown] + [Gnd Clamp] + [Power Clamp]
  - [Pullup] + [Gnd Clamp] + [Power Clamp]
- Ibischk5 parser is de facto standard for IBIS model correctness (and ibischk5 is embedded in tools)
- Some companies require 0 Errors, 0 Warnings
- IBIS Quality Spec, recommends 0 Errors and 0 Warnings
- **Warning messages create support issue for model authors or automatic modeling utilities**

Facts

- No specification REQUIREMENT that individual or combined I-V tables be monotonic
- No stated method to sum mismatched voltage points (piecewise linear interpolation is allowed and used)
- Non-monotonicity often occurs outside of normal simulation region – in clamping region and not a problem
- Ibischk5 parser is working correctly

Observations

- Non-monotonic behavior can occur
  - Combined I-V table slope is small
  - I-V table points are misaligned due to
    - Offset V intervals due to Gnd, Vdd and delta V
    - Different reference voltages (min/max)
    - Extraction done with piecewise linear interpolation calculations (if not done right)
  - Combination of above cases
- Example (y = x^2) next shows monotonic tables yielding non-monotonic summations

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Example: x Step 2, Offset by 1 (Red: Interpolated Value)

x	y1 = x^2	y2 = x^2	y1−y2 = 0?
0	0		
1	2	1	1
2	4	5	−1
3	10	9	1
4	16	17	−1
5	26	25	1
6	36		

Non-monotonic due to piecewise linear interpolation on both columns

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x Step 0.02, Offset by 0.01
(Red: Interpolated Value)

x	y1 = x^2	y2 = x^2	y1−y2
0.00	0.0000		
0.01	0.0002	0.0001	0.0001
0.02	0.0004	0.0005	−0.0001
0.03	0.0010	0.0009	0.0001
0.04	0.0016	0.0017	−0.0001
0.05	0.0026	0.0025	0.0001
0.06	0.0036		

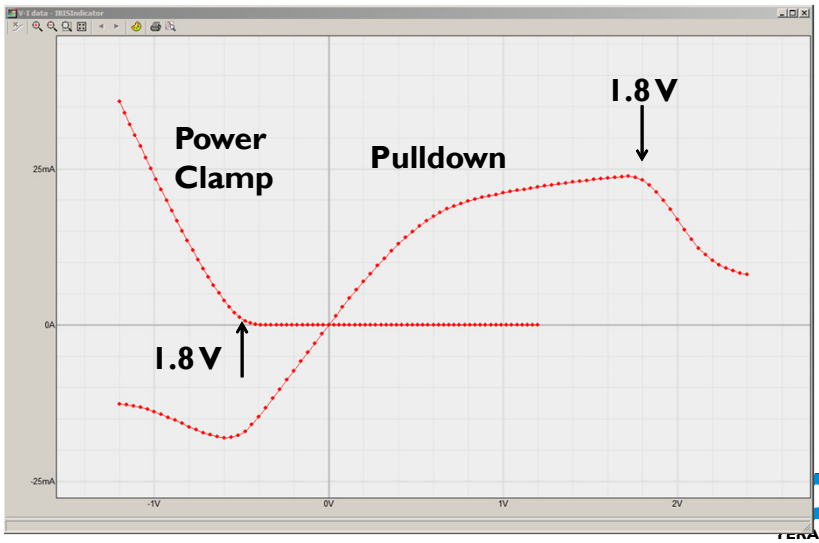
Still non-monotonic with higher resolution data

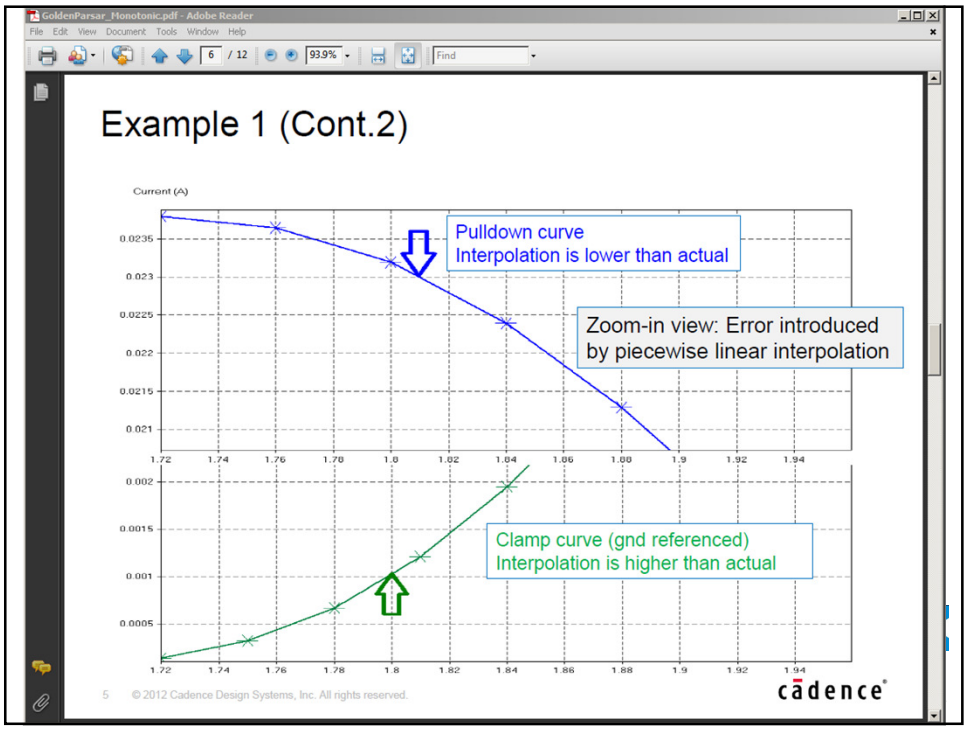
x Steps 0.02 and 0.01, 0.00 Offset
(Red: Interpolated Value)

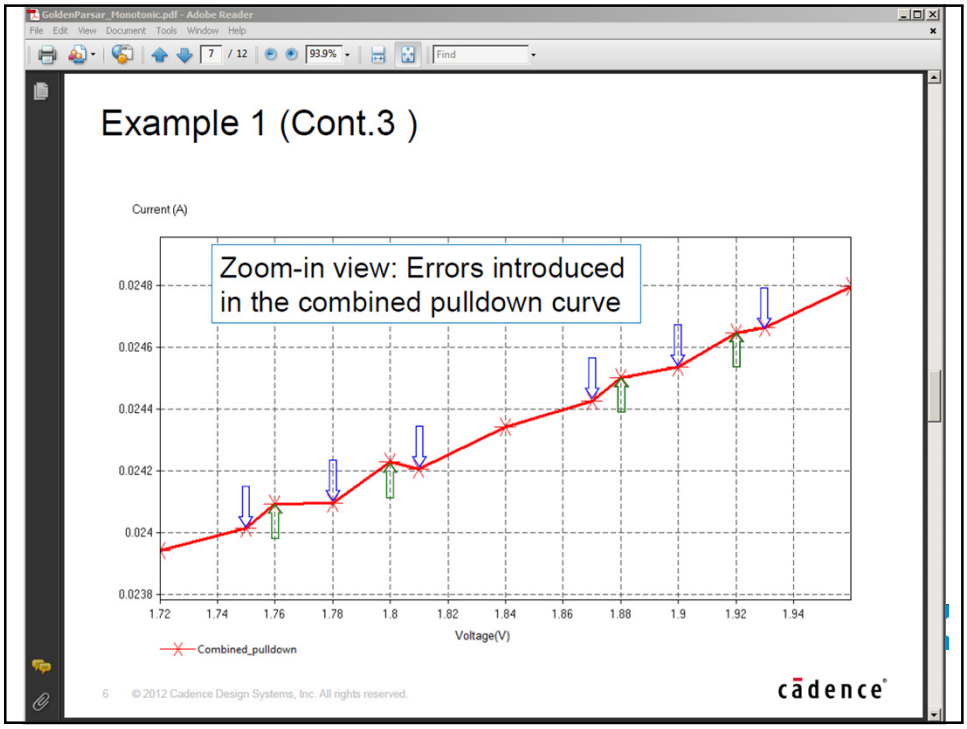
x	y1 = x^2	y2 = x^2	y1−y2
0.00	0.0000	0.0000	0.0000
0.01	0.0002	0.0001	0.0001
0.02	0.0004	0.0004	0.0000
0.03	0.0010	0.0009	0.0001
0.04	0.0016	0.0016	0.0000
0.05	0.0026	0.0025	0.0001
0.06	0.0036	0.0036	0.0000

Different resolution data causes non-monotonic combination

bug140a.ibs Maximum Data (Vdd = 1.3 V)







BUG140 Resolution

- Change WARNING to NOTE
  - Valid solution for user
  - Avoids tool and model developer support issues
- Add "based on piecewise linear interpolation" to message
- No practical fix
  - Still issues with higher resolution or choosing percentage threshold for non-monotonic warning
  - Piecewise linear interpolation is legal, and spline fitting would just hide information

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Checking bug140a.ibs

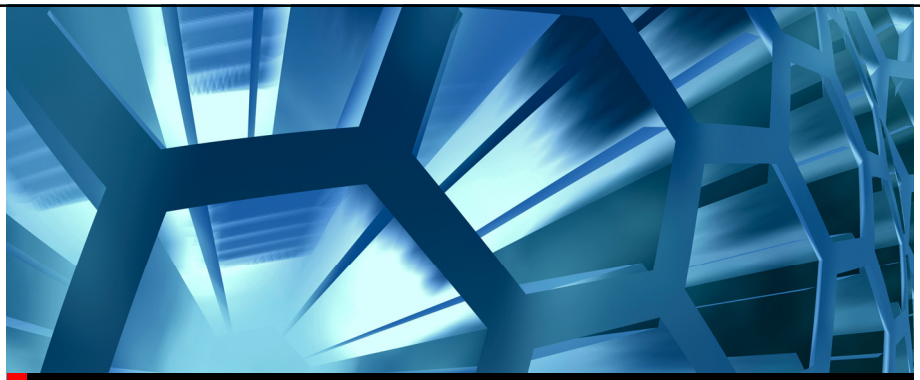
```
IBISCHK5 V5.1.2

Checking bug140a.ibs for IBIS 3.2 Compatibility...

NOTE (line   39) - Pulldown Typical data is non-monotonic
NOTE (line   42) - Pulldown Minimum data is non-monotonic
NOTE (line   42) - Pulldown Maximum data is non-monotonic
NOTE (line  135) - Pullup Typical data is non-monotonic
NOTE (line  137) - Pullup Maximum data is non-monotonic
NOTE (line  138) - Pullup Minimum data is non-monotonic
WARNING - Combined Pulldown for Model: iobuf Maximum data is non-monotonic

Errors  : 0
Warnings: 1

File Passed
```


Fixed bug140a.ibs in Version 5.1.3

```
IBISCHK5 V5.1.3

Checking bug140a.ibs for IBIS 3.2 Compatibility...

NOTE (line   39) - Pulldown Typical data is non-monotonic
NOTE (line   42) - Pulldown Minimum data is non-monotonic
NOTE (line   42) - Pulldown Maximum data is non-monotonic
NOTE (line  135) - Pullup Typical data is non-monotonic
NOTE (line  137) - Pullup Maximum data is non-monotonic
NOTE (line  138) - Pullup Minimum data is non-monotonic
NOTE - Combined Pulldown for Model: iobuf Maximum data is non-monotonic
based on piece-wise linear interpolation
Errors  : 0

File Passed
```

Closure

- For best checking results, use the latest version of ibischk5
- Parser being updated as new BUG reports are submitted and processed.



An Advanced Behavioral Buffer Model With Over-Clocking Solution

Yingxin Sun and Raymond Y. Chen
IBIS Asia Summit
Shanghai, China
Nov. 15, 2013

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Agenda

1. SPICE Model and Behavioral Buffer Model
2. Over-Clocking Problem in IBIS
3. Proposed Solution and Results

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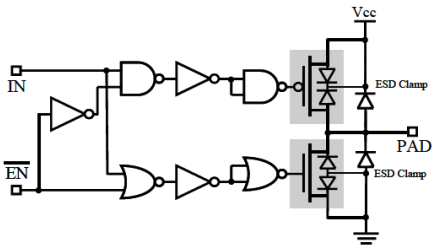
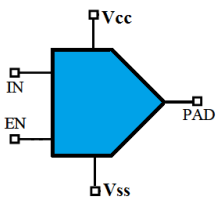
SPICE Model and Behavioral Buffer Model

- SPICE model is a circuit netlist at transistor level, it contains detailed information about the circuit design and process parameters.
- Behavioral model is a black box model with certain terminal information, which is obtained from measurement or extracted from SPICE model. IBIS is a widely adopted standard behavioral model.





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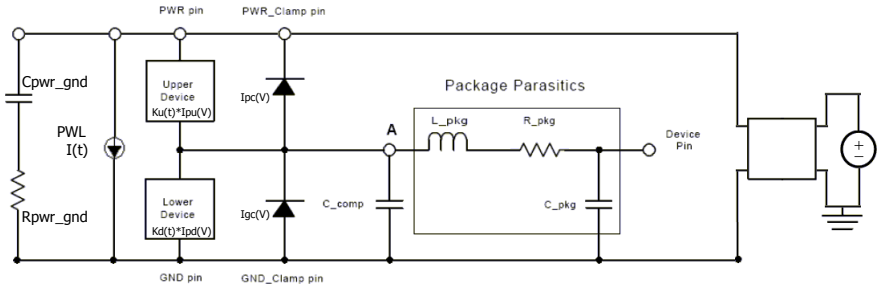
A Simple Schematic for IBIS Model

- The non-linear behavior of pullup, pulldown and clamps are described by I/V tables, and modeled as voltage controlled current sources.
- The transition behavior is described by the V/T table of the rising/falling waveforms under specified loading condition. And they are used to derive/scale instantaneous value of the I/V curves.
- Other important parasitic elements
- IBIS, as a behavioral model, does not contain transistor equation, some of the physics and detailed response may not exist in a simple model, hence the issue that will be discussed next.



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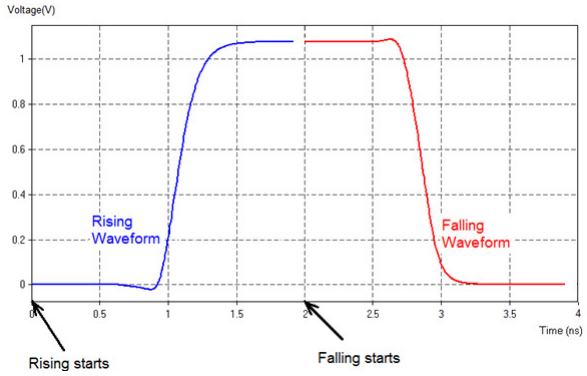
Understand the Over-Clocking

- Normal operating, the input data bit width > the time range of the IBIS rising and falling waveform.



Normal operation

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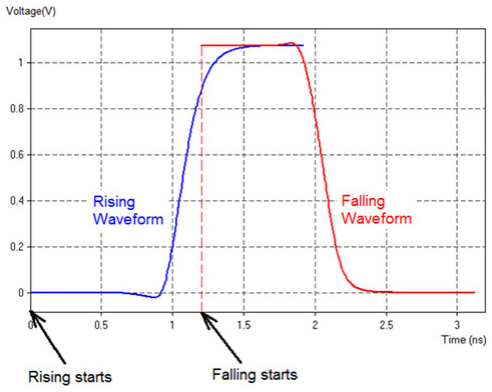
Understand the Over-Clocking (cont.)

- If the input signal bit width is smaller than the time range of the IBIS waveforms, the next transition is triggered before this transition is finished.
- The behavior of the IBIS simulator may be unpredictable.
- Google “IBIS Overclocking” to find out more about this issue discussion since 2002



Over-clocking operation

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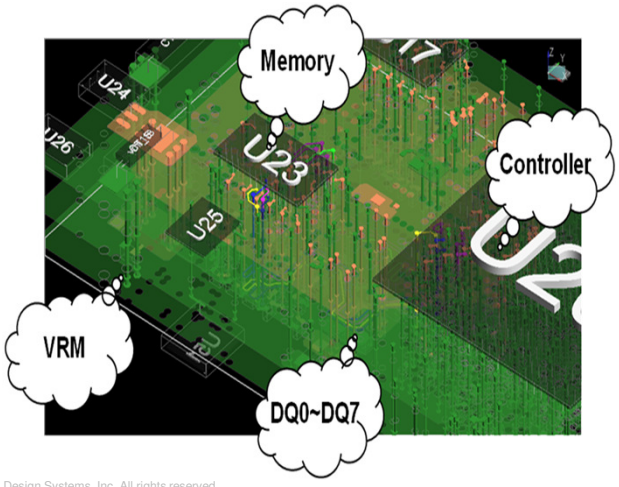
Simulation Problem Is Shown with A DDR3 SSO Test Case

8 signal nets + 1 power nets + 1 ground net from a real PCB design. Bit width is 1ns, the pattern is 00010101110110011111001101010



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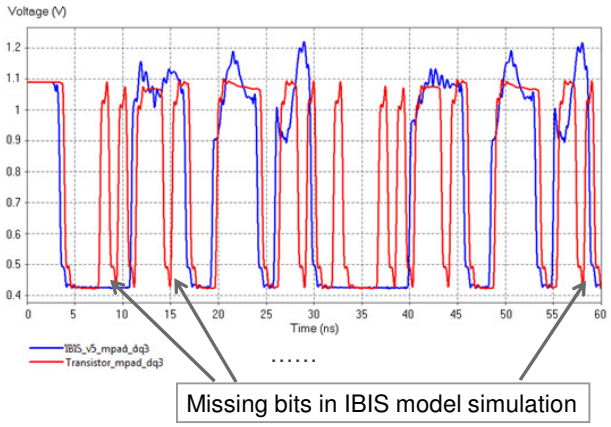
Problematic Results from Over-Clocking

- A test case operating over-clocking
- Simulation results show missing bits



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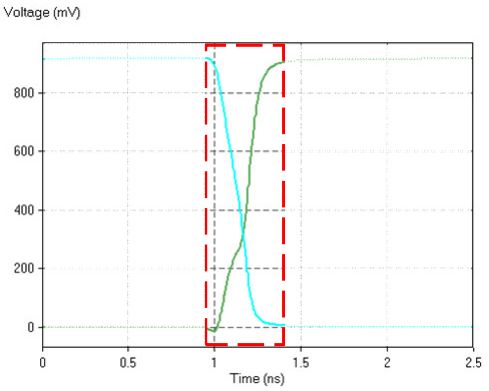
Existing Solution to Solve Over-Clocking Problem

- V/T curve windowing by cutting the initial delay and the flat tail of the rising/falling waveforms of IBIS model to make the time range shorter
- The windowing can be done either in IBIS model creation or simulation tools



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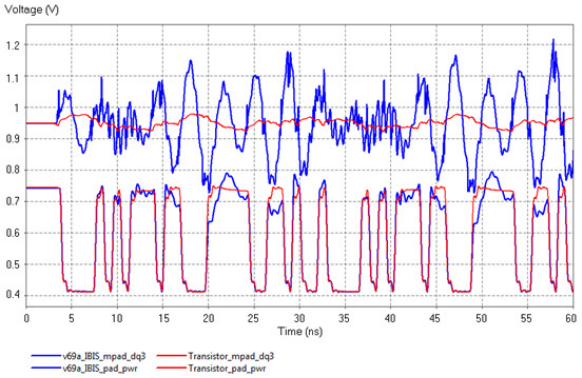
Simulation Results with V/T Windowing

- The missing bits resolved
- Therefore, simulator with proper V/T windowing scheme should automatically handle overclocking issue in IBIS 4.2 model



- However, voltage on power net mismatches between transistor model and IBIS model due to the dynamic power noise not modeled.

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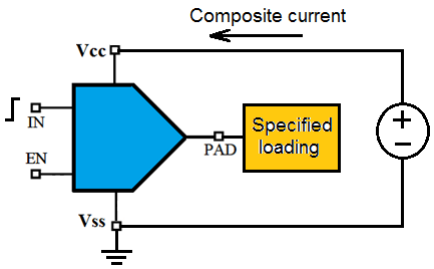
New Challenge of Over-Clocking with Composite Current

- To accurate model the power-aware buffer model, the composite currents (I/T) are introduced in IBIS V5.0 to give the current waveforms on power pin.
- The I/T data must be time correlated with the waveform V/T data which are extracted from pad pin.
- The composite current includes the contribution of the pre-driver and all the other on-die P/G paths. It has wider time range than V/T waveform.



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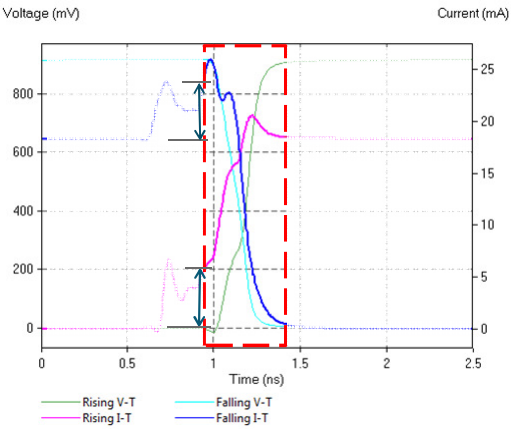
Windowing with Composite Current

- Now both V/T and I/T need to be windowed.
- Choosing window based on wider I/T curve will not help, since over-clocking solution requires narrow timing window for higher frequency operation.
- Still choosing a window based on V/T will cut the composite current incomplete which will form a sharp step current.



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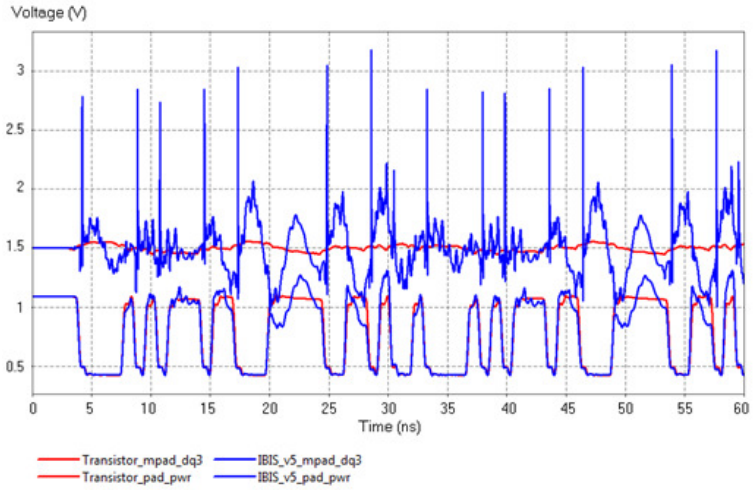
The Sharp Step of Incomplete Composite Current Causes Unreal Large Voltage Spikes



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Observation of This New Challenge

- With the addition of composite current (I/T) in IBIS 5.0, old windowing technique (V/T based) in IBIS simulator need to be improved, and can't be directly applied to I/T data to solve over-clocking issue.
- With IBIS 5.0 models become increasingly popular in the last few years, there are more awareness and discussion of this issue.
- A solution was developed by us two years ago to tackle this challenge.

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Agenda

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3. Proposed Solution and Results

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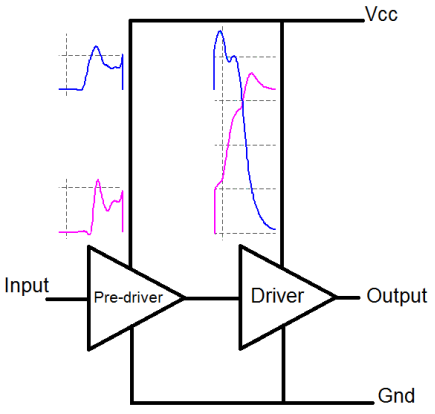
Key Point of Advanced Over-Clocking Solution

- Using the V/T waveform windowing
- Adding one stage to the existing driver to keep the pre-driver behavior for the buffer switching delay and power current
- Taking the composite current compensation into two parts:
  - Driver contribution
  - Pre-driver contribution



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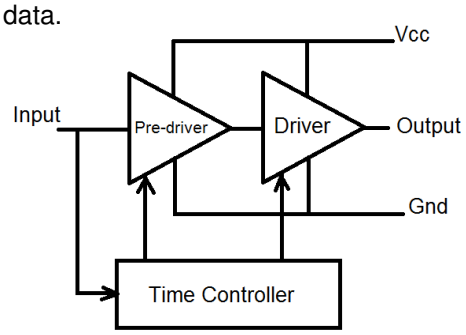
Implementing the Proposed Over-Clocking Solution

- The proposed over-clocking solution can be implemented into an advanced IBIS model, which is a SPICE netlist with integrated model data and simulation algorithm.
- The proposed over-clocking solution can also be implemented into an advanced IBIS simulator to automatically handle the windowing of both V/T and I/T data.



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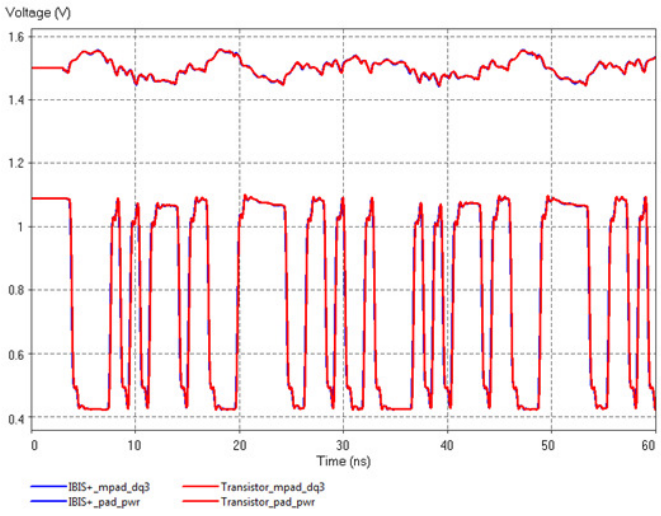
Simulation results with Advanced Over-Clocking Solution



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Simulation Performance Summary

- Very good correlation between IBIS and the original transistor model for real SSO simulation, both signals and power/ground waveforms match very well, even under over-clocking scenario.
- The 60ns simulation time is based on 32 clock cycles of data input.
- It takes 54 minutes for original transistor level SPICE model.
- It takes 55 seconds for the behavioral model with the advanced over-clocking solution.
- Note: HSPICE is used to run the simulations for all the models, including the advanced IBIS model with over-clocking solution.

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Conclusion

- Power-aware buffer model generation has been implemented for IBIS 5.0 standard. When used in high-speed power-aware SSO simulations, user often has to deal with IBIS over-clocking issues.
- With the proposed algorithm for handling composite currents under over-clocking situation, more advanced model shows significant accuracy improvement compared with traditional IBIS models, while keeping the fast simulation advantages of IBIS.
- Advances in IBIS standard, together with advances in modeling and simulation algorithms, continue to make this behavioral model technique a great and practical engineering approach for high-speed design.

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References

- [1] Perivand F. Tchrani, Yuzhe Chen, Jiayuan Fang, “Extraction of Transient Behavioral Model of Digital I/O Buffers from IBIS”, 46th IEEE Electronic Components & Technology Conference, Orlando, May 28-31, 1996, pp 1009-1015.
- [2] Ying Wang and Han Ngee Tan,“The Development of Analog SPICE Behavioral Model Based on IBIS Model”, Proceedings of the Ninth Great Lakes Symposium on VLSI, March 1999.
- [3] Sam Chitwood, Raymond Y. Chen, Jiayuan Fang, “An Initial Case Study for BIRD95 - Enhancing IBIS for SSO Power Integrity Simulation”, IBIS Summit DesignCon, January 2005.
- [4] Raymond Y. Chen, “Recent Development of IBIS and Related EDA Technologies”, Sigrity Annual User Forum, May 24, 2011

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When Could PCB and PKG PDN Lumped Loop Inductance be Extracted Separately?

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November 15, 2013

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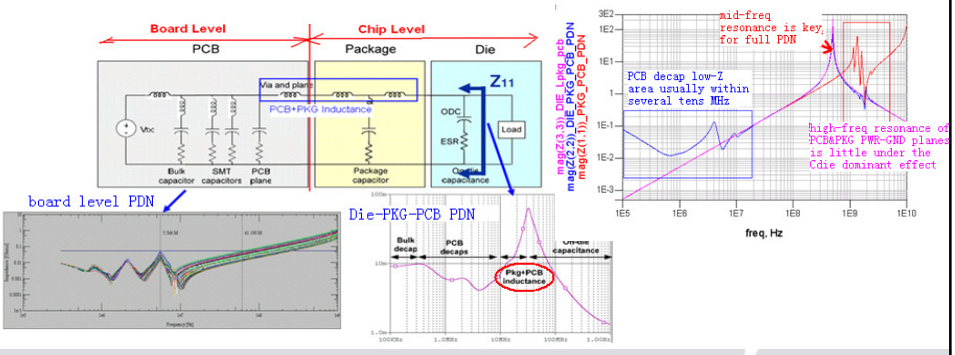
HUAWEI

Background: Importance of Lpkg-pcb Constraint

- Die-PKG-PCB PDN mid-freq resonance is the crucial factor in chip self-generated power supply noise
- PDN mid-freq resonance without On-Package-Decap(OPD) can be approximately treated as simple parallel resonance of lumped Rdie-pkg-pcb, Lpkg-pcb, Cdie
- Traditional target impedance and effective frequency requirement is to control the Lpcb in nature



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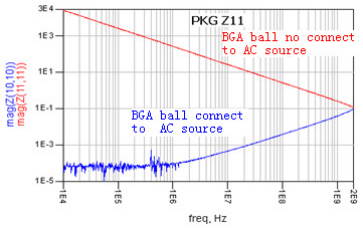
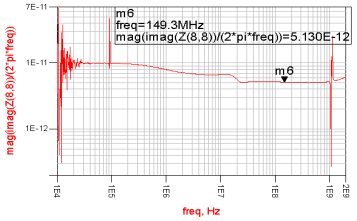
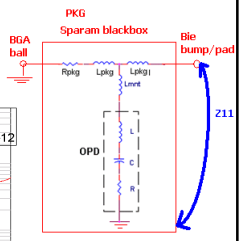
Lpcb/Lpkg Extraction from Sparam

- PCB and PKG are belong to different teams or companies, so Lpcb/Lpkg is usually extracted from Sparam separately
- Inductance is dominant in high frequency, so it can be extracted from imaginary part of Zin in flat area $Z(f) = R + j\omega L + \frac{1}{j\omega C} = R + j(\omega L - \frac{1}{\omega C})$
- For Lpkg extraction, BGA ball should be connected to AC ground or AC source to specify the source
- For Lpcb extraction, see next page
- Then Lpkg-pcb=Lpkg+Lpcb



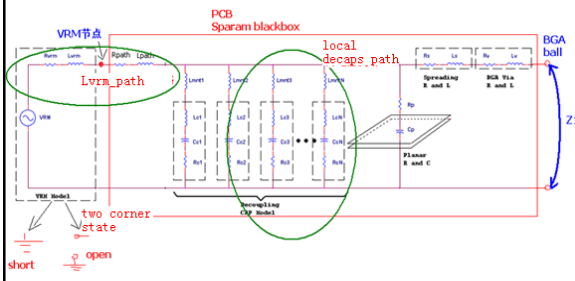


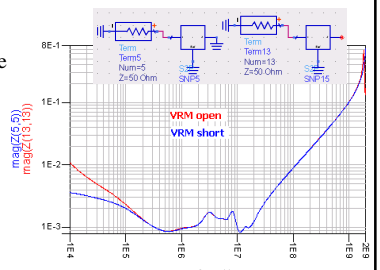


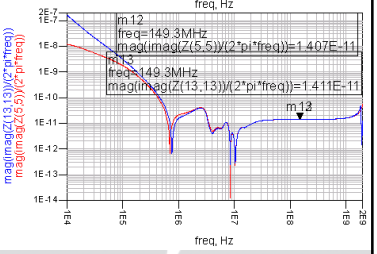
PKG-only Lpkg Extraction

Lpcb/Lpkg Extraction from Sparam(Cont.)

- For Lpcb extraction, VRM should be added as source
- For lack of accurate VRM model, both open and short state of PDN can be simulated to view the VRM effect on PDN and Lpcb
- VRM has little effect on Lpcb when PCB decaps provide good enough local low-Z bypass



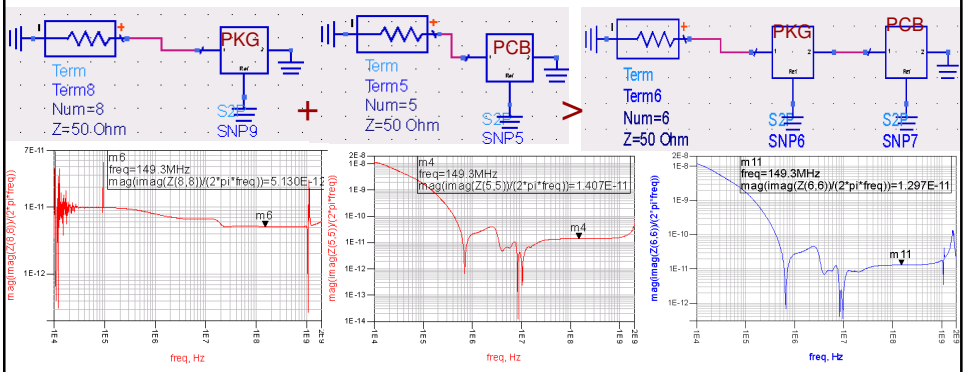




Could Lpkg/Lpcb be Extracted Separately?

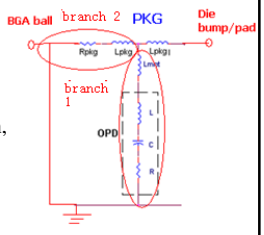
- An interesting example: It's weird that Lpkg+Lpcb=5.13+14.07=19.2pF>Lpkg-pcb=12.97pF, even if Lpcb>Lpkg-pcb
- It seems Lpkg and Lpcb can't be extracted separately . Is it right?

Why?

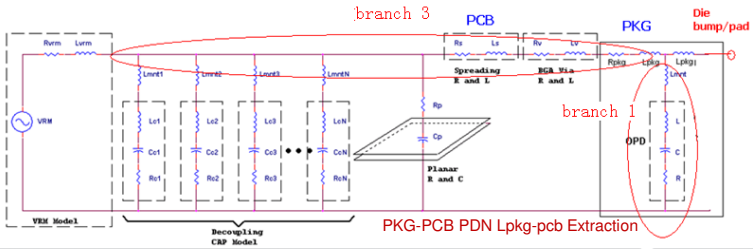


On-Package-Decap(OPD) Change the Loop Inductance

- With the increase of data rate, OPDs are more and more added for better PI performance
- OPDs add a local low-Z path and change feature of Lpkg-pcb
- PKG-only extraction doesn't include Lpcb into the parallel calculation, so Lpkg+Lpcb>Lpkg-pcb
- On one hand, OPDs improve the full PDN performance. On the other hand, PCB decaps take less effect on full PDN with OPDs and less PCB decaps are needed



PKG-only Lpkg Extraction

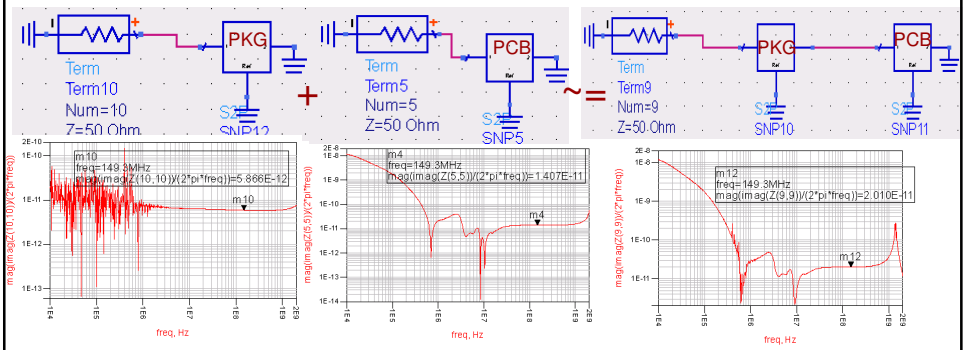


PKG-PCB PDN Lpkg-pcb Extraction

Could Lpkg/Lpcb be extracted Separately?(Cont.)

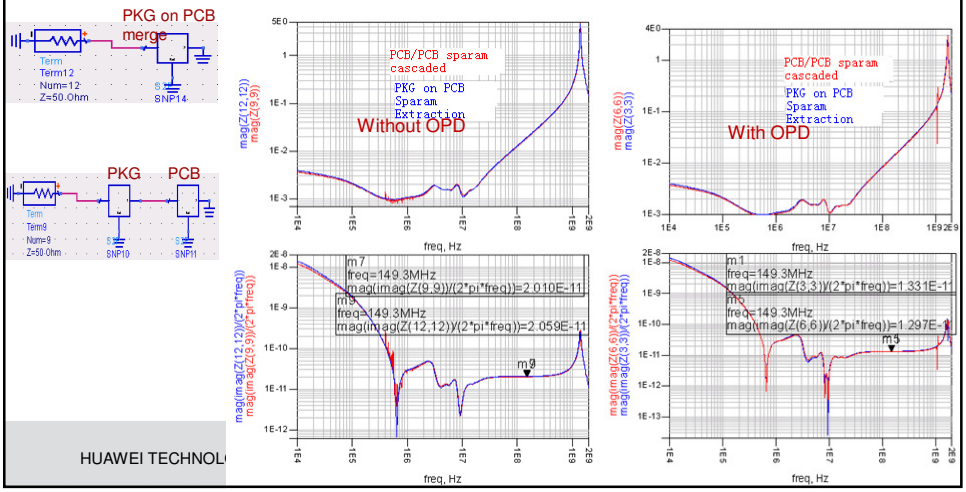
- If no OPD is added, Lpkg/Lpcb can be extracted separately and then sum both.

  Lpkg+Lpcb=5.86+14.07=19.93pF~=Lpkg-pcb=20.10pF



PKG/PCB Sparam Cascaded vs. PKG on PCB Merge Extraction

- When PKG/PCB have the integral pwr-gnd plane and can be treated as pin-group, there's almost no difference on full PDN impedance between PKG/PCB extraction separately and PKG on PCB extraction



The Limitation of IBIS PKG PWR/GND RLC Model

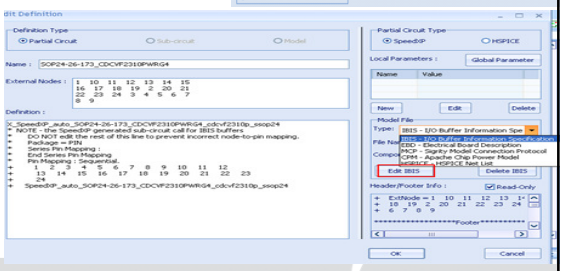
- As we discussed, with OPDs it is not suitable to use PKG-only Lpkg like IBIS RLC PKG model to do the full PDN simulation
- For the present, we have to edit the netlist manually to include IBIS with other format PKG model
- We propose that the IBIS grammar be compatible with more complex models based on Sparam or Spice(.ckt) to make IBIS models easier to use in EDA tools

IBIS Version 6.0

7 PACKAGE MODELING

The [Package Model] keyword is optional. If more than the default RLC package model is desired, use the [Define Package Model] keyword.

```
| The inductance matrix has sparse coupling
|
[Inductance Matrix]     Sparse_matrix
[Row]     Y21
Y21       1.88315e-009
AA26      1.62658e-012
AA22      3.03324e-012
AA10      1.66893e-012
AC20      2.4359e-011
AC21      1.19519e-011
AJ21      1.2311e-012
AB20      1.91878e-011
AA21      1.08181e-010
AA20      4.80607e-011
AB21      3.45745e-011
[Row]     AA26
AA26      1.55486e-011
AC20      2.14604e-012
```



Summary

- With OPDs, Lpkg-pcb can't be summed with Lpkg and Lpcb extracted from sparam separately, but should be extracted from PKG-PCB sparam cascaded
- OPDs not only improve the full PDN performance, but weaken the PCB decaps effect on full PDN as well, which make PCB decaps more simplified
- IBIS PKG RLC model is not suitable for PDN simulation with OPDs. We propose the IBIS grammar be compatible with Sparam or Spice(.ckt) models to make IBIS models easier to use in commercial EDA tools

Thank you

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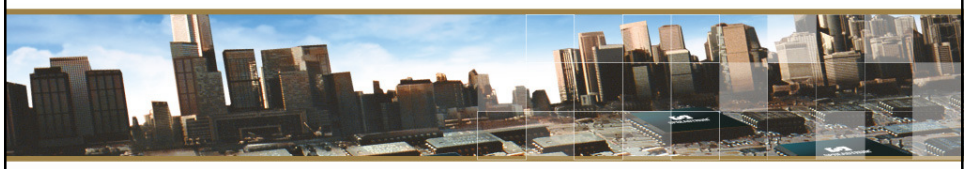
DDRn Interface Signoff Analysis with Distributed Chip IO Interconnect Model



Steven Guo Spreadtrum
Zuli Qin Zhangmin Zhong Cadence

IBIS Asia Summit
Shanghai,China
Nov. 15, 2013

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Agenda

- Introduction About the Chip IO Interconnection
- Chip IO Interconnect Model Extraction and Analysis
- Case Study – DDR SSO and Chip IO Power Decap
- Summary

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Simplified View of a Smartphone Board

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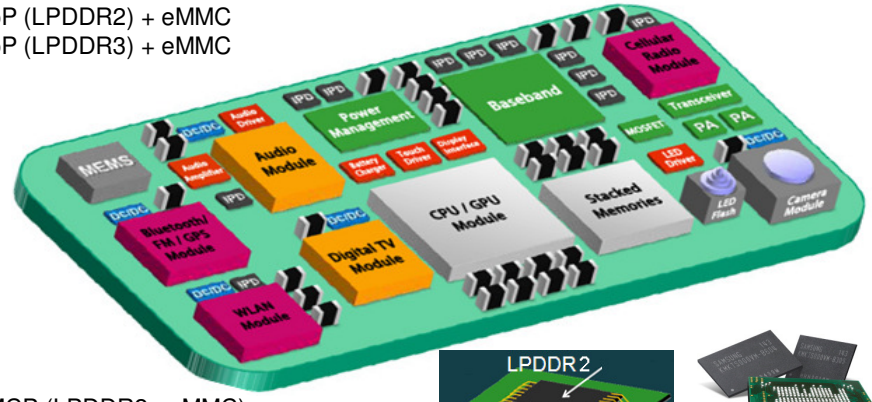
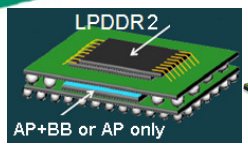
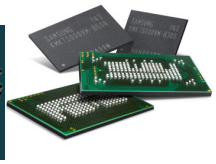
PoP (LPDDR2) + eMMC
PoP (LPDDR3) + eMMC







eMCP (LPDDR2+ eMMC)
eMCP (LPDDR3+ eMMC)

4Gb eMMC +8Gb LPDDR2 Memory
eMCP (LPDDR2+eMMC) 11.5x13x1.0mm3 162b FBGA 0.5mm pitch
12x12 PoP + eMMC $_{only}$ 11.5x13x1.0mm3 153b FBGA 0.5mm pitch

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. 3

Chip IO interconnection Structure

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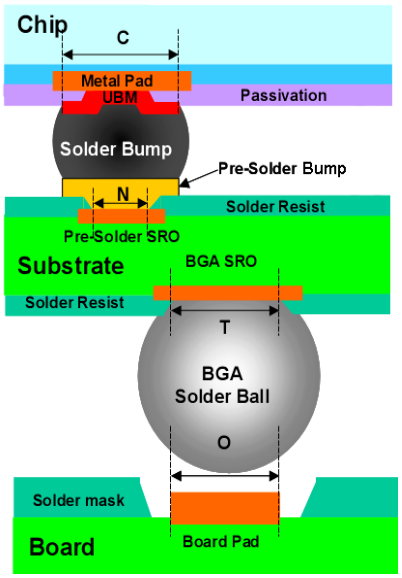

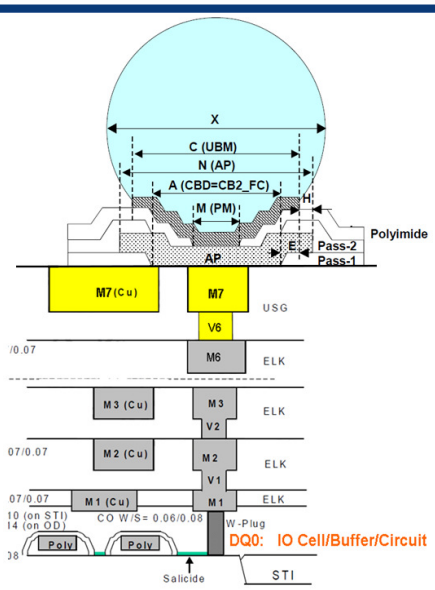

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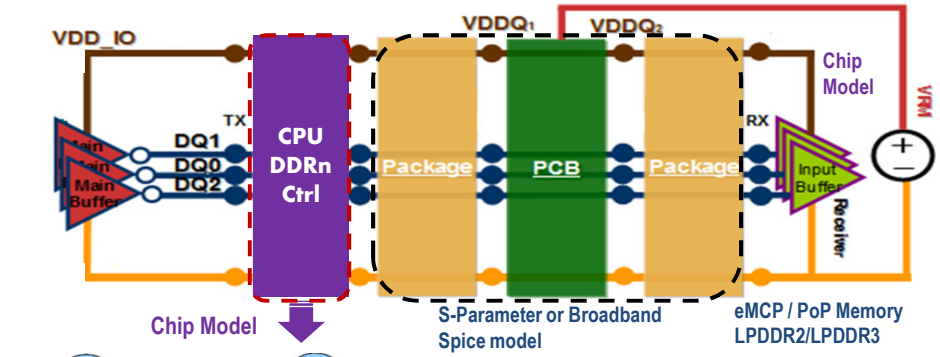
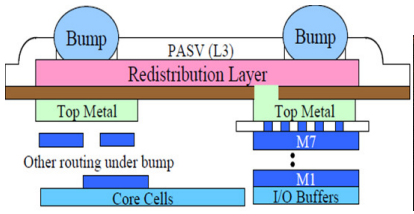
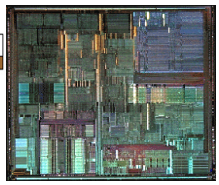
DDRn System Interconnection Topology







Chip Model = Distributed IO Power/Ground/Signal Interconnect Model (from M1 to Bump)

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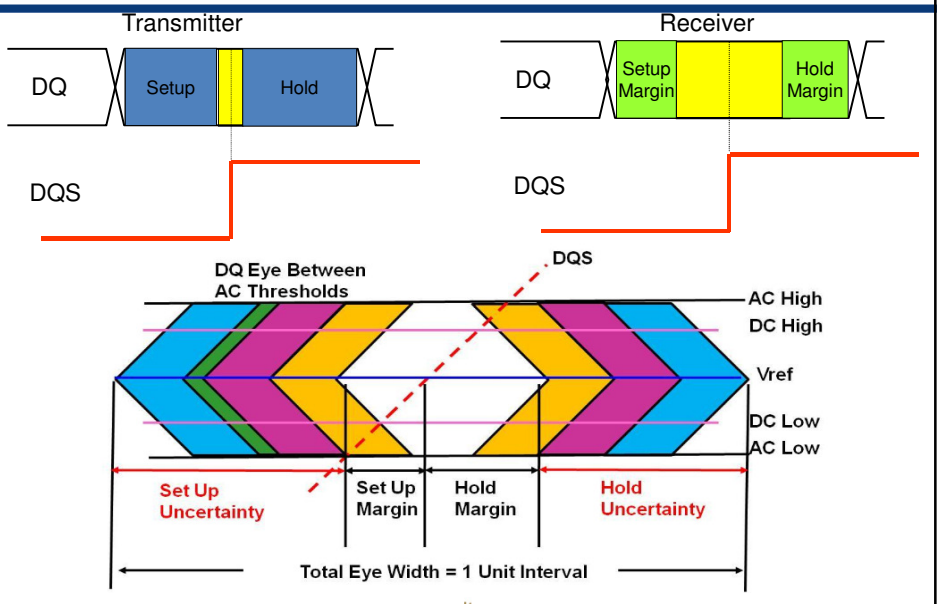
Uncertainties Vs Timing Margin



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DDRn Setup/Hold Timing Budgets
(Uncertainties : Skew & Jitter)

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Transmitter Contributions	Interconnection Contributions	Receiver Contributions
DDL (Data Delay Line) Granularity and bit offset (BDL and LCDL) (Static)	**Signal Length Mismatches (On-chip interconnection M1 to Bump , RDL Routing , Package Substrate and PCB layout Skew) (Static)**	Input Rise /Fall Slew Factor (Static)
Register Mismatch within the PHY (Static)	Crosstalk (Pushout/Pullin from nearby aggressor signals and serpentine routing) (Dynamic)	DDRn Data Set Up and Hold specifications (tDS, tDH) (Static)
DLL Jitter including Clock Source Jitter (Dynamic)	Reflections,Inter-Symbol Interference (ISI) (Impedance discontinuities, topology,loading) (Dynamic)	Setup and Hold Slew rate Derating (Static)
DLL Phase Error (Dynamic)	High frequency losses (Dielectric and Conductor losses) (Dynamic)	
PHY Skew between DQS/DQS# and DQ signals (Static)	Dielectric mismatches between layers (Dynamic)	
Process Variation Effects (Static)		
IO Output Rise Fall Delay Mismatch (Static)		
SSO/SSN Pushout (Effects of non-ideal power distribution network-PDN) (Dynamic)		
VT Drift (BDL and LCDL Setting) (Dynamic)		

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Agenda

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Chip IO Interconnect Model Extraction Diagram

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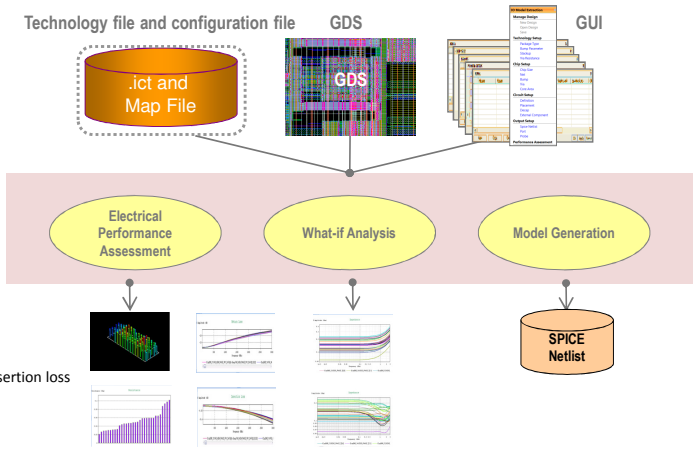
Inputs
- LEF/DEF or GDS
- Technology file (.ict)
- Layer map file

Outputs
- IO interconnect model
  - SPICE netlist
- EPA results
  - Power pin RL
  - Power net capacitance
  - Power net impedance
  - Signal net RLC
  - Signal net return and insertion loss



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Chip Model Parts

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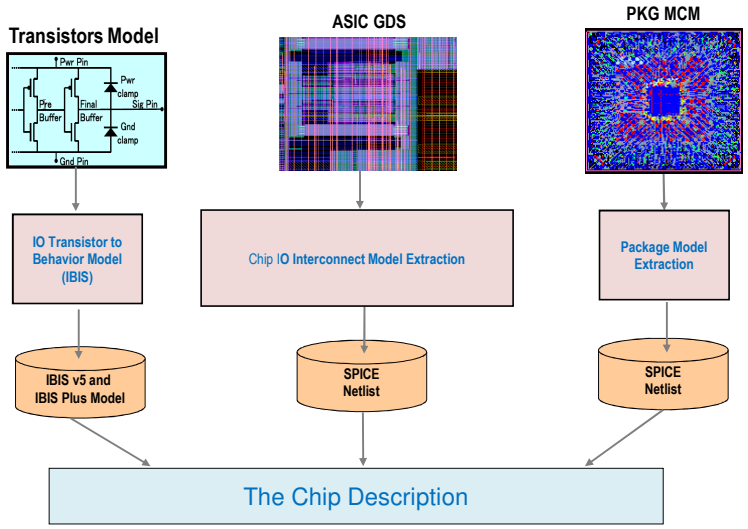

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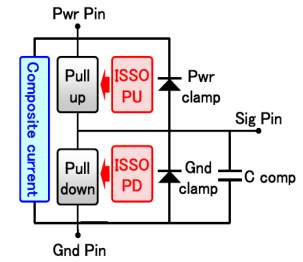
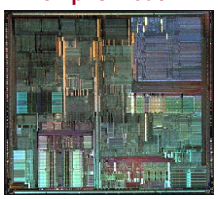
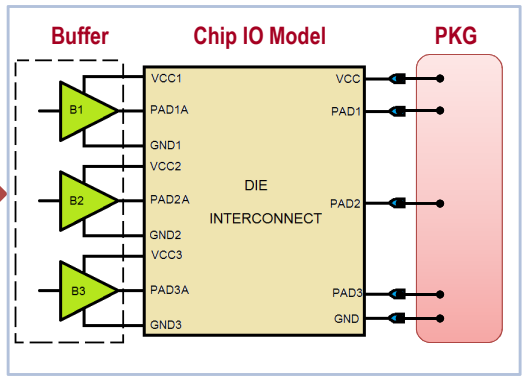
Chip IO Model Add in the IBIS Model Simulation





Chip IO Model



IBIS + Chip IO model + PKG

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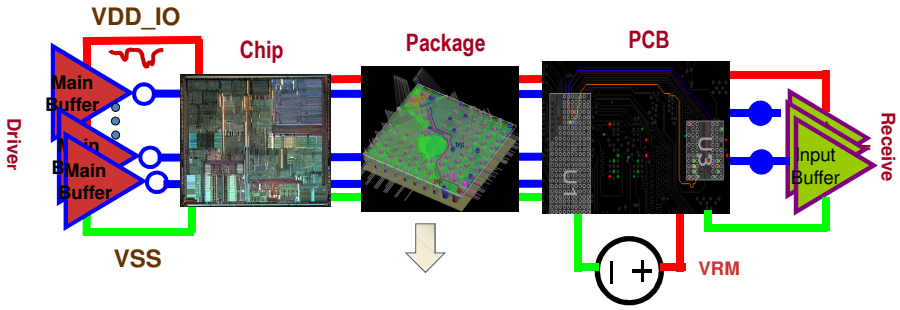
System Interconnection Analysis for DDRn



- Chip IO interconnect model includes signals and IO pwr/gnd
- Chip IO interconnect model is extracted by chip level extractor which include RLCK elements.
- PCB and package are extracted by EM solver and converted into broadband SPICE model.

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Agenda

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Test vehicle of system level SI/PI analysis (DQ/DQS)

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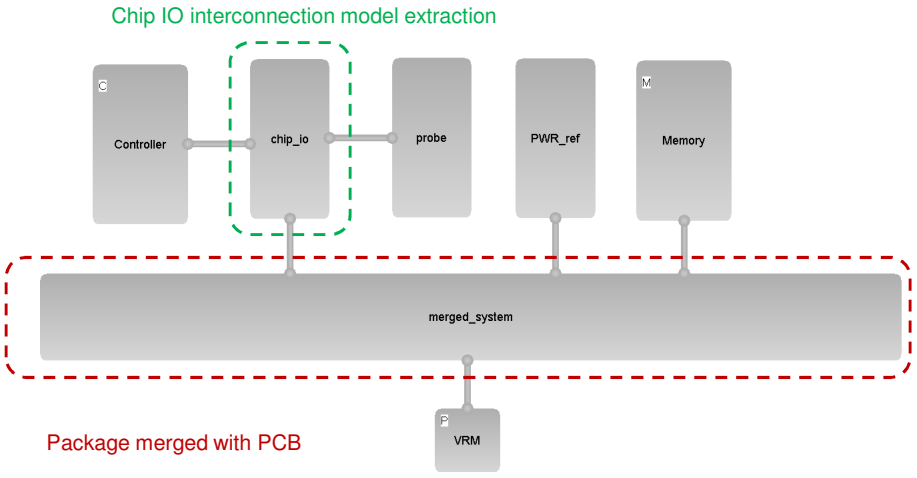

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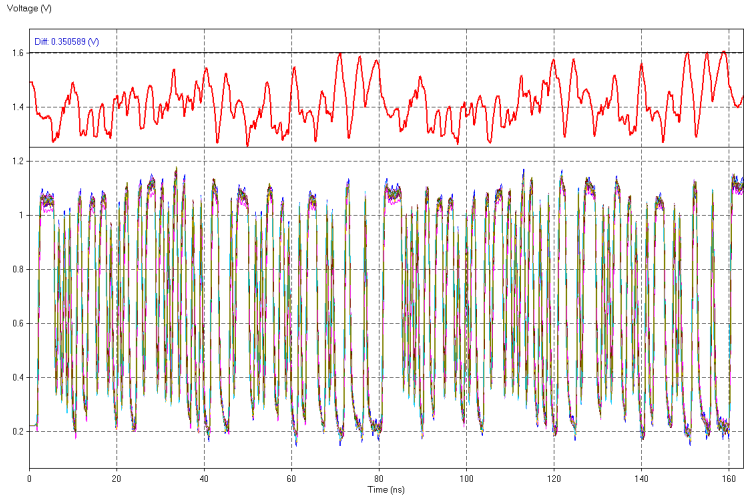
DDRn Bank0 SSO



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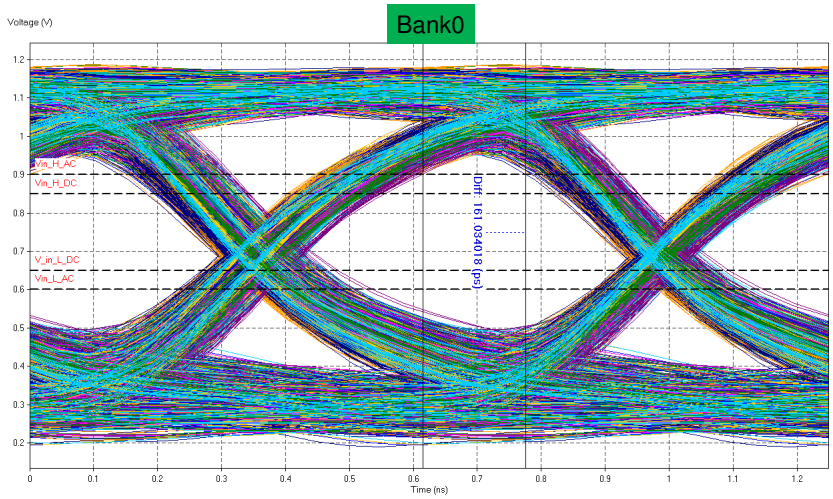
Power aware signal integrity analysis

System level SI/PI analysis (DQ/DQS) with memory write in TD—ODT40



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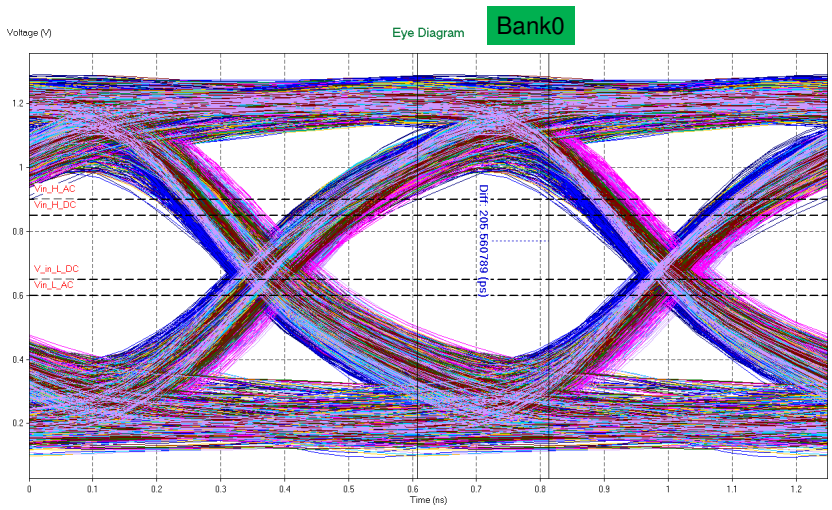
Power aware signal integrity analysis

System level SI/PI analysis (DQ/DQS) with memory write in TD—ODT60



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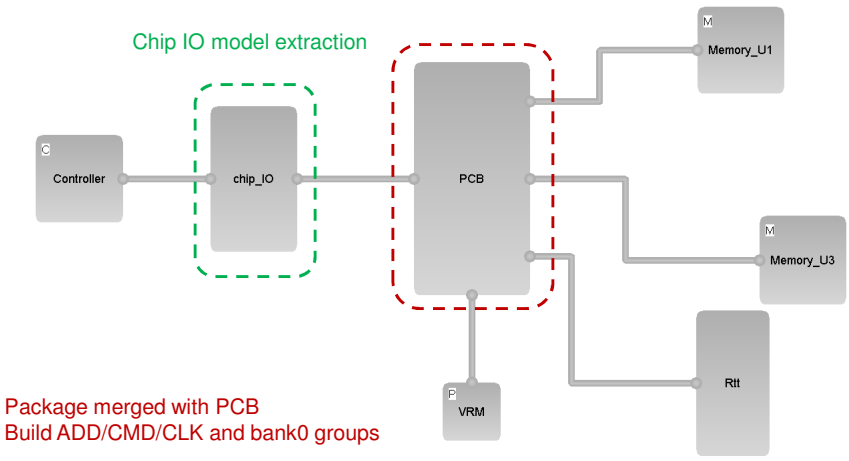
Test vehicle of system level SI/PI analysis coupling among ADD/CMD/CLK and DQ/DQS



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Test vehicle of system level SI/PI analysis coupling among ADD/CMD/CLK and DQ/DQS

Bus Group/Signal	Stimulus Pattern	Stimulus Offset (ns)	Transmit IO Model	Status
ADD_GP	00000000000000000001100110000111100001111001100..	0		
ADDR0	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR1			se_drv15_odtoff	Not Connected
ADDR2	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR3	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR4	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR5	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR6	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR7	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR8	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR9	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR10	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR11	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR12	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR13	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR14	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
ADDR15	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
BA0	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
BA1	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
BA2			se_drv15_odtoff	Not Connected
CASN	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
CKE	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
CS_N	00000000000000000001100110000111100001111001100..	0	se_drv15_odtoff	Signal
dm0	0101001100110001 00..	0	se_drv15_odtoff	Signal
dm1	0101001100110001 00..	0	se_drv15_odtoff	Signal
dq0	0101001100110001 00..	0	se_drv15_odtoff	Signal
dq1	0101001100110001 00..	0	se_drv15_odtoff	Signal
dq2	0101001100110001 00..	0	se_drv15_odtoff	Signal
dq3	0101001100110001 00..	0	se_drv15_odtoff	Signal
dq4	0101001100110001 00..	0	se_drv15_odtoff	Signal
dq5	0101001100110001 00..	0	se_drv15_odtoff	Signal

- Running DQ/DQS patterns first then turn on ADD/CLK.
- To measure ADD/CLK lines noise while DQ/DQS are toggling.
- To monitor ADD/CLK waveform and see if they are affected by DQ/DQS
- All DQ/DQS are in ODT-off

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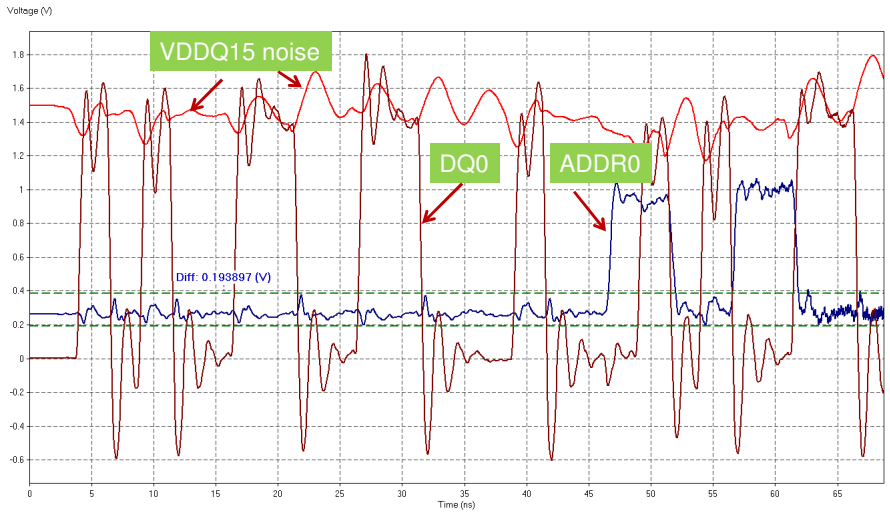
Coupling among bank0 and ADD/CMD (measured at U1)



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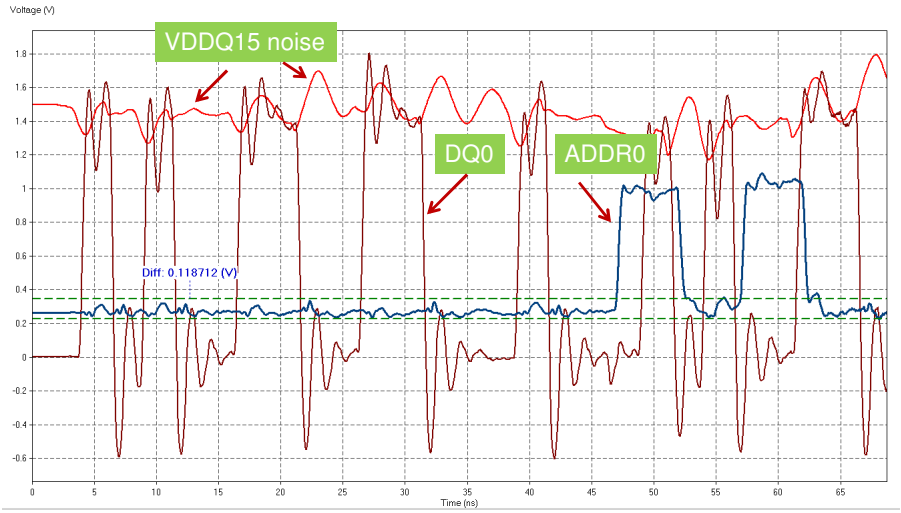
Coupling among bank0 and ADD/CMD (measured at U3)



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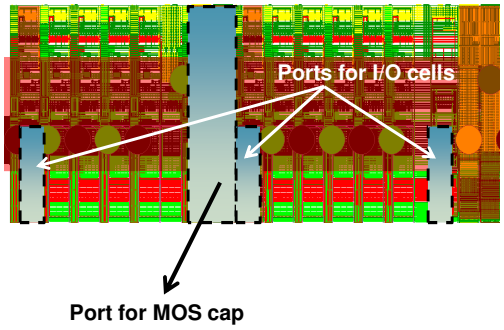
Chip Decap What-if Analysis and Optimization

- Ports for IO cells which can be impedance observations
- Ports for PSCAP/MOS cap cells which can be decaps and optimized



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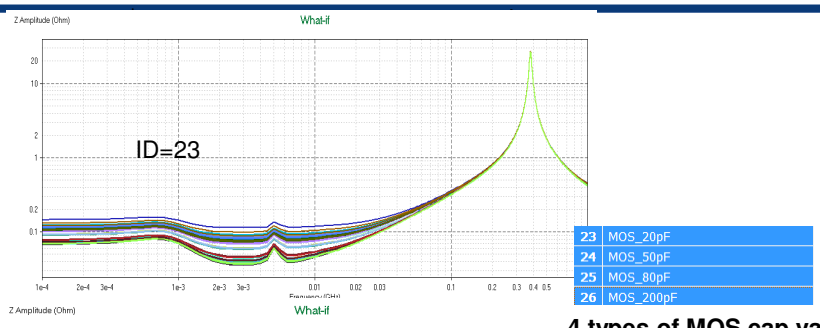
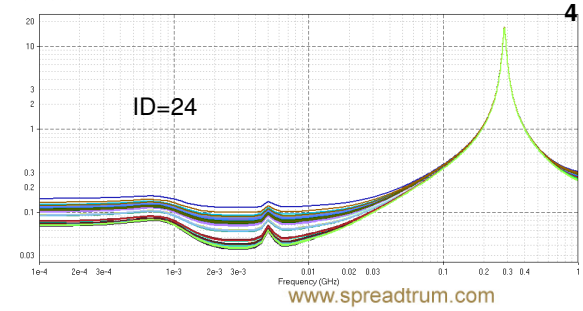
Power integrity analysis





4 types of MOS cap value

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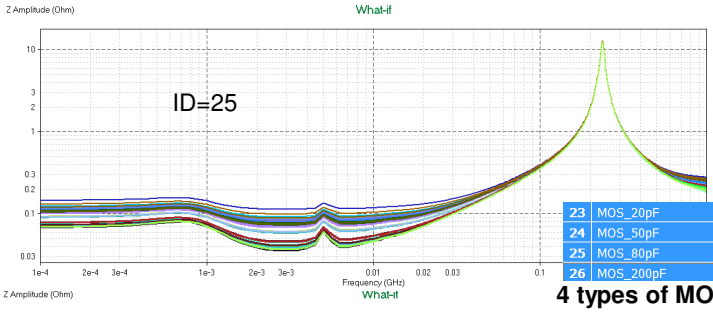
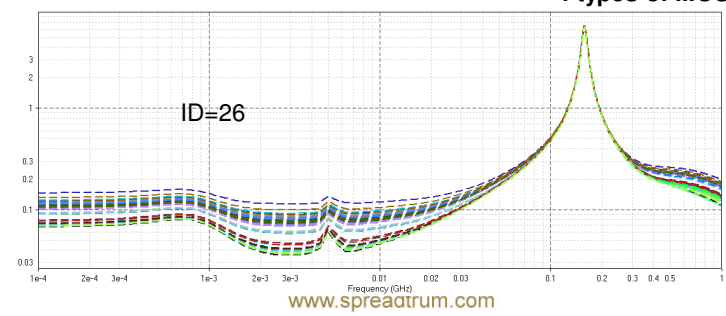
Power integrity analysis

--1st stage MOS caps optimization on chip





4 types of MOS cap value

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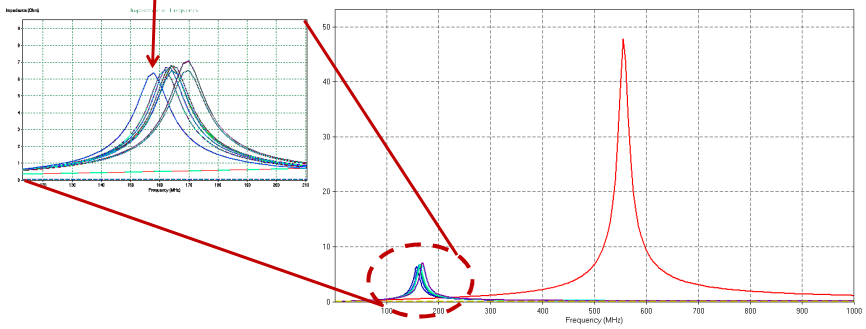
Power integrity analysis
--1st stage MOS caps optimization on chip

A	G	H	I	J	K	L	M	N	O	P	Q
Scheme ID	chio_io_pdn	chio_io_pd	chio_io_pd	chio_io_pd	chio_io_pd	chio_io_pd	chio_io_pd	chio_io_pd	chio_io_pd	chio_io_pd	chio_io_pd
Original Scheme	X	X	X	X	X	X	X	X	X	X	X
Scheme 1	26	26	26	26	26	26	26	26	26	26	26
Scheme 2	26	26	26	26	26	26	26	26	25	26	26
Scheme 3	26	26	26	26	24	26	26	26	26	26	26
Scheme 4	26	26	24	26	26	26	26	26	26	26	26
Scheme 5	26	26	26	26	23	26	26	26	26	26	26
Scheme 6	26	26	26	26	26	26	26	26	26	26	X
Scheme 7	26	26	26	26	X	26	26	26	26	26	26
Scheme 8	26	26	26	26	26	26	26	26	26	24	23
Scheme 9	26	26	25	26	X	26	26	26	26	26	26
Scheme 10	26	26	25	X	26	26	26	26	26	26	26



MOS caps with 200pF for each cell will have best impedance profile

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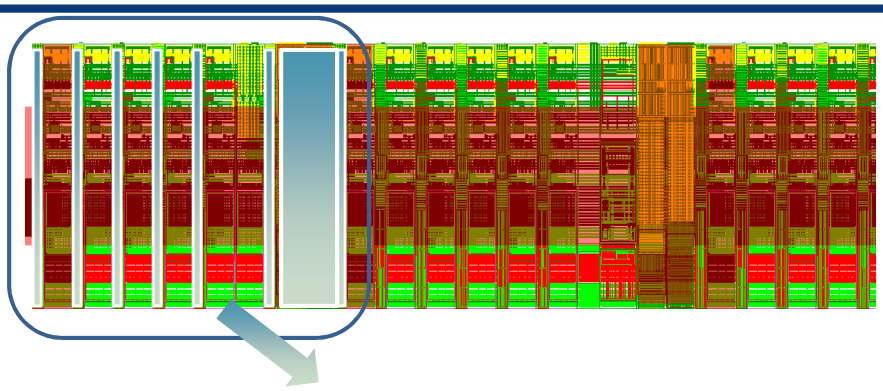
Chip Decap What-if Analysis and Optimization



- This is the definition of big cell with x7 small and x1 large cells
- Total value for this big cell is ranging from 20,50,80,200PF.
- A strongly recommendation that places MOS caps as much as possible

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Agenda

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Summary

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- Chip IO interconnect model should include IO Power/Ground/Signal Interconnect Model
- For high speed and low power DDR systems (LPDDR3/DDR3L/DDR4), Chip IO interconnect model is crucial for IO-SSO analysis.
- Chip IO interconnect model is one part for Chip but not in IBIS model.
- With Chip IO Interconnection model, Chip vendor can do more accurate DDRn signoff analysis to predict System electrical performace before ASIC tapeout.
- On-die RC or better distributed chip IO interconnect model can be more realistic for signal/power analysis
- New System Signoff methodology enable to avoid overdesign or under-design for on-die Decap Cell

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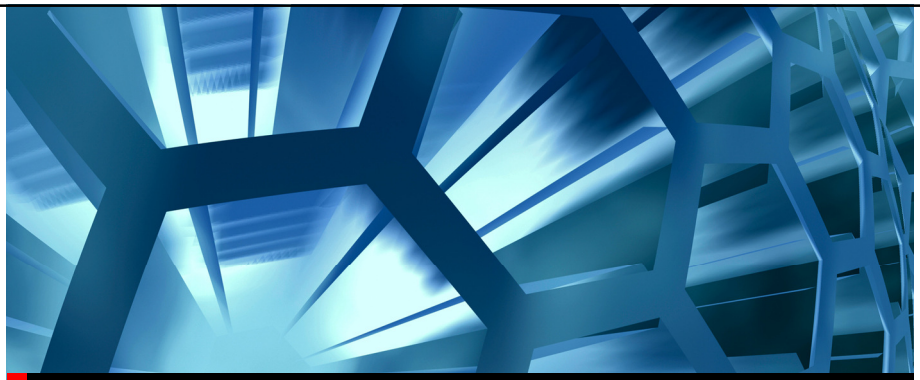


IBIS Modeling for IO-SSO Analysis

Thunder Lay and Jack W.C. Lin
IBIS Asia Summit
Shanghai, China
Nov. 15, 2013

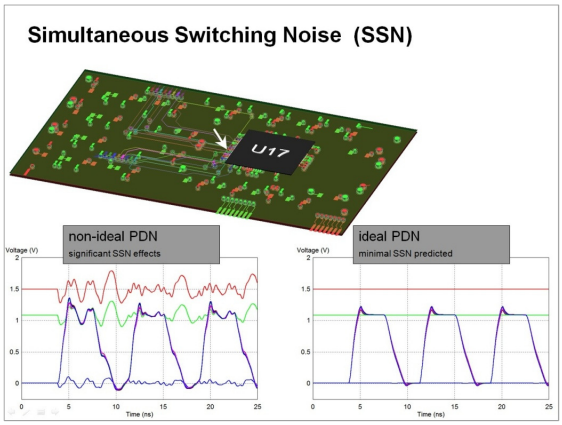
cadence

Agenda

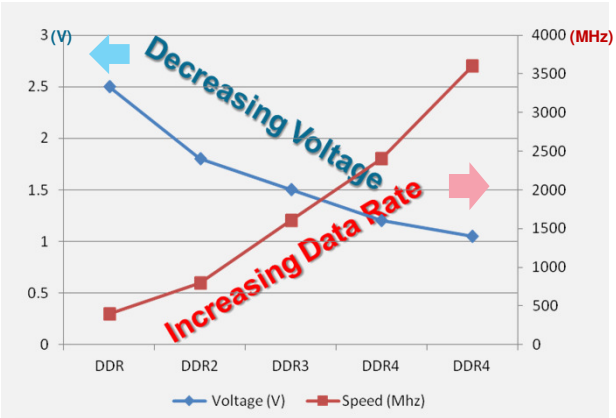
- What is IO-SSO?
- Missing Components in Traditional IO-SSO Analysis
- Accurate On-die and Package Effects in IBIS Models
- Creating IBIS Models with On-die Interconnect
- Case Study – IO-SSO Analysis with IBIS Models
- Summary

What is IO-SSO?

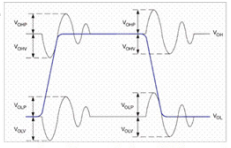
- A DDR memory interfaces is a parallel bus
  - Many signals represent a data byte/word/32-bit word/64-bit word
  - Simultaneous switching signals / outputs are referred to as SSO
  - The noise between power and ground created is referred to as simultaneous switching noise (SSN)
  - IC Designers refer to this phenomenon as IO-SSO
  - SI/PI can be verified by IO-SSO



IO-SSO Impacts Timing and Noise Margin



- Data transfers are faster and more sensitive to instability of the PDN
  - DDR runs at 2.5 V
  - DDR2 runs at 1.8 V
  - DDR3 runs at 1.5V
  - DDR4 to run at 1.2 V – 1.05V



Ground bounce Peaks and Valleys must be minimized with low signal voltages

+

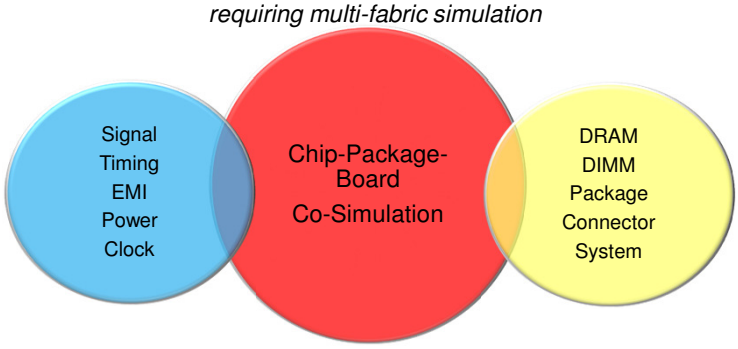
Decreasing Timing Budget

±600ps ➔ ±300ps ➔ ±150ps

SSN effects impact timing and noise budget

Higher Data Rate ➔ High Level Interactions

Electrical and Physical worlds collide requiring multi-fabric simulation

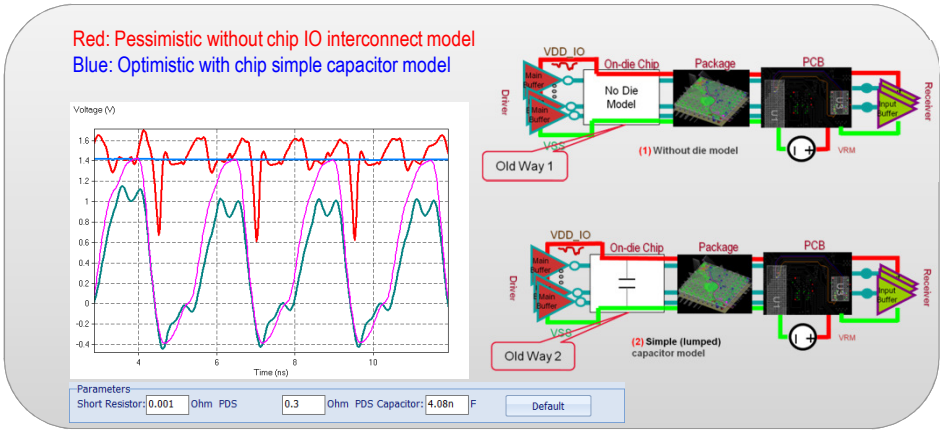


Increased interaction between signals

Increased interaction between system hardware components

Traditional IO-SSO Simulation Scenarios

- Pessimistic result when analyzed without on-die model.
- Optimistic result when analyzed with estimated on-die model.

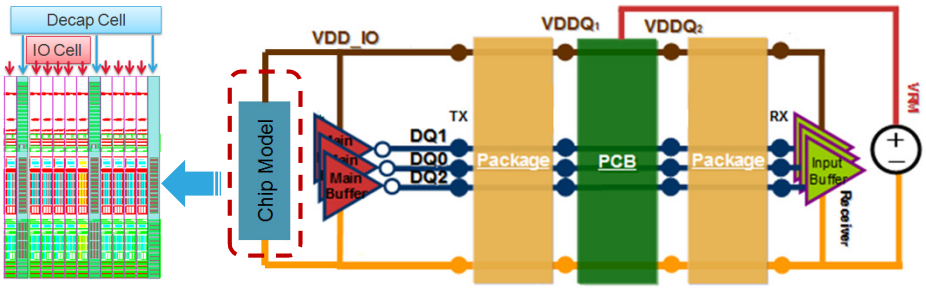


Agenda

- What is IO-SSO?
- Missing Components in Traditional IO-SSO Analysis
- Accurate On-die and Package Effects in IBIS Models
- Creating IBIS Models with On-die Interconnect
- Case Study – IO-SSO Analysis with IBIS Models
- Summary

cadence

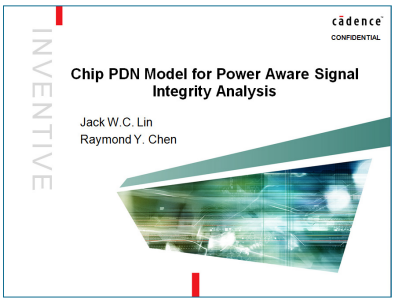
Missing Components in Traditional IO-SSO Analysis

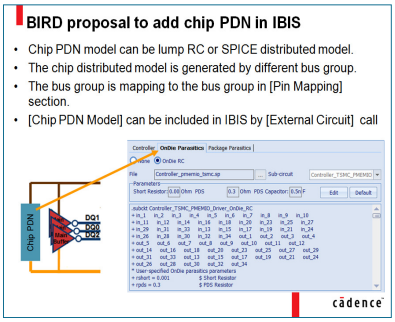


- Post-sim transistor SPICE netlist only includes limited parasitic information.
- Distributed behavior of IO's P/G impedance can't be represented.
- Pin Mapping table may not be defined accurately.
- On-die decap model is not captured in IBIS model.
- All above problems make IO-SSO simulation lose accuracy.

Asia IBIS Summit 2012

- Chip PDN model is crucial for IO-SSO analysis.
- Without Chip PDN model, artificially large power /ground noise impact the signal waveform significantly
- Chip PDN is responsible to filter high frequency noise
- On-die RC or better distributed chip PDN model can yield realistic power/ground noise analysis





Agenda

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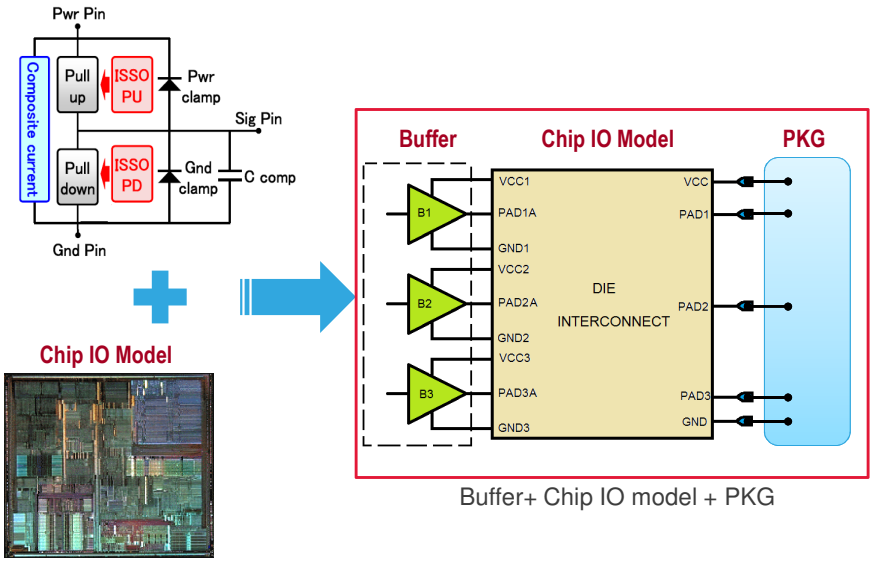
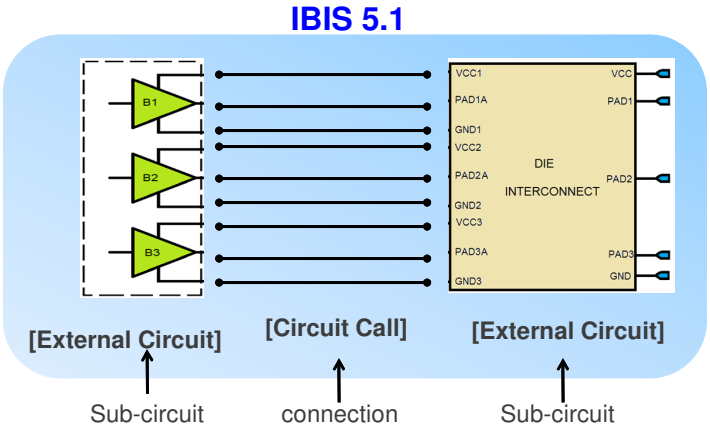
Adding On-die Effects to the IBIS Model



Buffer+ Chip IO model + PKG

Connecting Buffer, On-Die and Package Models



- Effectively incorporates the on-die and package models into the buffer
- The package and on-die models may be of arbitrary topology to include coupling, non-ideal power deliver and other effects
- Applying IBIS 5.1 [External Circuit] sub-components is similar to sub-circuit call and connections in HSPICE
- Future ISS based solution may be coming from committee

Agenda

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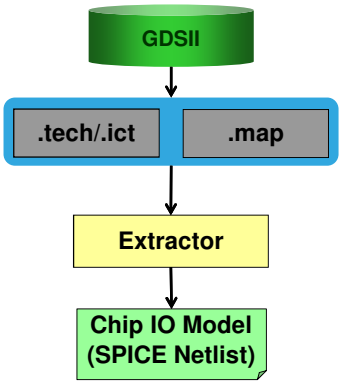
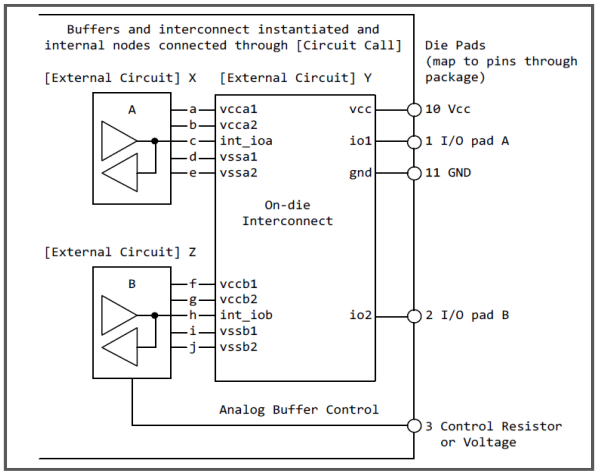
cadence

Creating IBIS Models with On-die Interconnect (1/4)

- Generate chip IO model
  - LEF/DEF or GDSII data can represent physical geometry.
  - Includes Power/Ground/Signal routing with On-Die caps.
  - Define Chip stackup, circuit mapping
  - Chip IO model extraction is based on chip layout which includes metal_x to the top layers (x can be 1~N). Model builder needs to be aware what SPICE nest-list is from pre-sim or post-sim flow.
  - Generate SPICE netlist



Creating IBIS Models with On-Die Interconnect (2/4)

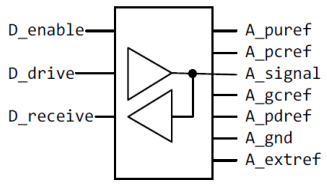


- [External Circuit] will be represented as IO buffer, chip IO, package…..
- Connect each [External Circuit] through [Circuit Call]

Creating IBIS Models with On-die Interconnect (3/4)

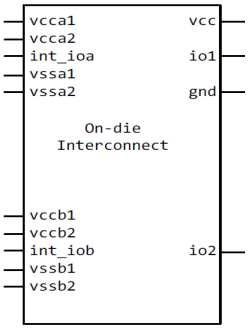
- Ports under [External Circuit]

  The [External Circuit] keyword allows the user to define any number of ports and port functions on a circuit.



Port name for IO Buffer

Ports A_puref A_pdref A_signal A_drive A_enable A_receive A_pcref A_gcref



Ports vcca1
Ports vcca2
…….

Creating IBIS Models with On-die Interconnect (4/4)

- Define [Pin] and [Node Declarations]
  - When a [Circuit Call] keyword defines any connections that involve one or more die pads (and consequently pins), the corresponding pins on the [Pin] list must use the reserved word “CIRCUITCALL” in the third column instead of a model name.
  - [Node Declaration] provides a list of internal die nodes and/or die pads for a [Component] to make unambiguous interconnection descriptions possible

```
[Node Declarations]     | Must appear before any [Circuit Call] keyword
| Die nodes:
pu1 pd1 io1p io1 in1 en1 outin1          | List of die nodes
pu2 pd2 io2p io2 in2 en2 outin2          | List of die nodes
pu3 pd3 io3p io3 in3 en3 outin3          | List of die nodes
[End Node Declarations]
```

Agenda

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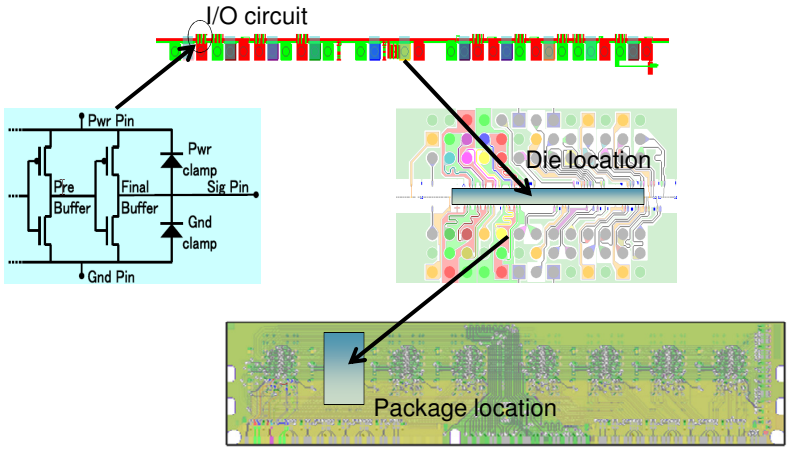
- **Case Study – IO-SSO Analysis with IBIS Models**
- Summary

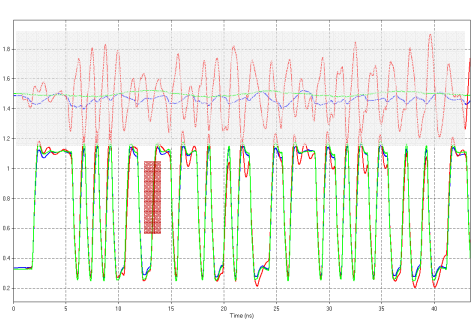
  cadence

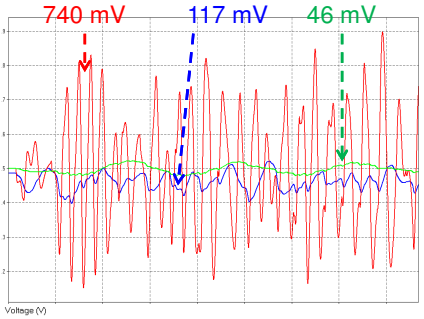
Case Study – IO-SSO Analysis with IBIS Models



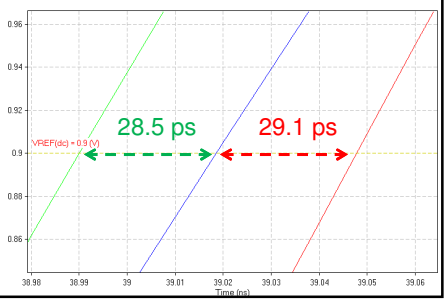
- I/O transistor circuit is converted into power-aware IBIS model
- Chip is extracted by chip level extractor which include RLCK elements.
- PCB and package S-parameters are extracted and converted to broadband SPICE models.
- Only 1 group DDR data is considered for this test

Case Study – IO-SSO Analysis with IBIS Models



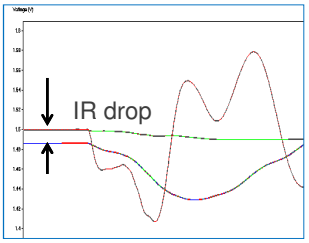


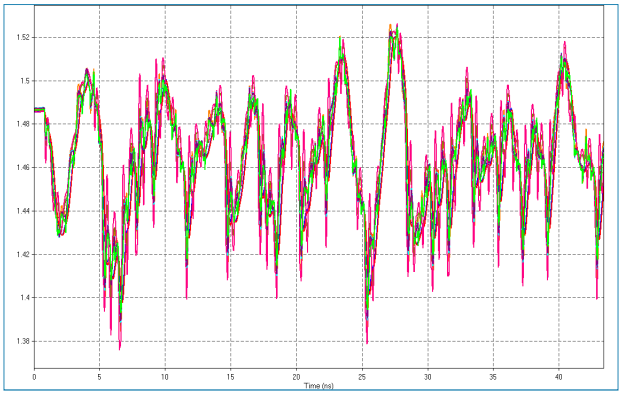
RED: without chip PDN
Green: with on-die RC
Blue: with distributed broadband model



- SSN from SSO will be over or under estimated without accurate chip IO model.
- Timing push in/out will become worse if more IOs are switching at the same time.

Case Study – IO-SSO Analysis with IBIS Models





RED: without chip PDN
Green: with on-die RC
Blue: with distributed broadband model

- IR drop becomes worse after including chip IO model.
- Noise level at each IO pad is different, which reveals the distributed behavior of the IO power deliver network.

Agenda

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- **Summary**

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Summary

- For tighter timing and noise budgets in LPDDR3 or DDR4, system level IO-SSO analysis is helpful for design margin assessment
- IBIS 5.1 models may include power-aware IO buffer, chip P/G/S from IOs to bump pads, and arbitrary package models
  - existing IBIS syntax is applied (using [External Circuit])
  - additional techniques using ISS within the IBIS model are being discussed in committee
- The approach described allows chip vendors to deliver more complete IBIS models to their customers to enable faster and more accurate product design verification

Modeling, Extraction and Verification of VCSEL Model for IBIS AMI

Asian IBIS Summit
Shanghai, China
November 15, 2013

Zhaokai YUAN
Agilent Technologies, Inc.

Agilent Technologies

Outline

- Introduction
  - Optical Link Simulation
  - VCSEL(Vertical Cavity Surface Emitting Laser) simulation under IBIS-AMI
- VCSEL Modeling and Extraction
  - Thermal based modeling
  - Curve fitting algorithm
- VCSEL Verification
  - Test case including VCSEL device
  - The comparison between simulation and measured data

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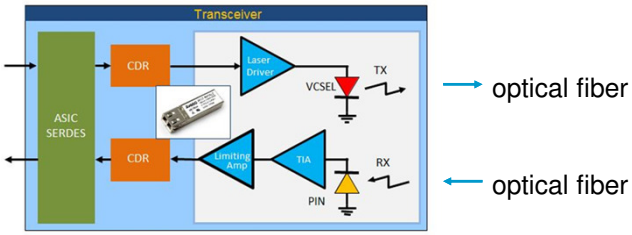
Introduction
Optical Link System and Simulation(cont.)

- Optical Link Simulation



Inside SerDes Tx & Rx

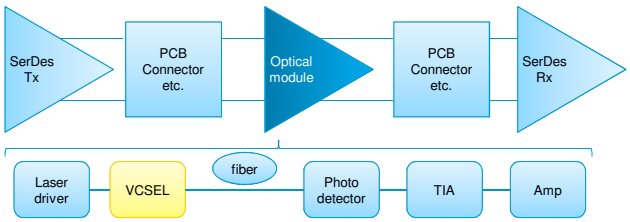
- Equalization (FFE, CTLE & DFE)
- Clock-data recovery (CDR)

Inside optical module

- Input voltage signal drives VCSEL to emit photons
- Photons propagate along optical fiber
- Photons are converted into photocurrent in PIN
- TIA converts current into output voltage

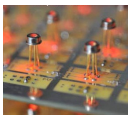
Introduction
Optical Link System and Simulation(cont.)

- Extending AMI to Optical Channel
  - Treat the entire optical module as a mid-channel repeater
  - Encapsulate all optical behaviors inside the optical model
  - Extend AMI simulation to include repeater



Introduction
VCSEL Basic

- VCSEL(Vertical Cavity Emitting Laser)
  - Characteristics
    - High Data Rate, up to 40GHz(state of art)
    - Low power cost(input ~ mA, output ~ mW)
    - Single-longitudinal-mode operation
    - Suitability for monolithic 2-D integration
  - Application
    - Very short range data transmission
    - Board to board data transmission

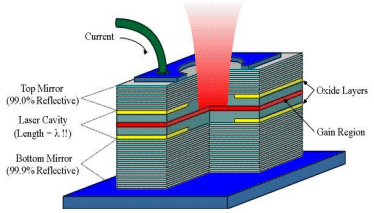


Introduction
VCSEL Basic

- VCSEL modeling
  - 3-D modeling and simulation
    - From the principle of laser point of view
    - Accurate but too complicated
  - SPICE simulation
    - As VCSEL is an optical device, SPICE model may not be the initial design, a new SPICE schematic is needed
    - Hard to communicate due to IP issue
  - IBIS-AMI(Algorithmic Modeling Interface)
    - Focusing on performance only
    - Treat the VCSEL as an algorithm unit

VCSEL Modeling and Extraction
VCSEL Modeling

- Modeling Principle
  - VCSEL's performance vs. Thermal behavior
  - Data flow based
  - The relationship between input current(I) and output power(Po) under the effect of temperature(T)
  - Peripheral simulation
  - Working schematic



VCSEL Modeling and Extraction
VCSEL Modeling

- Rate-Equation-Based Thermal VCSEL Model
  - Transient Analysis

$$P_o = kS$$

$$\frac{dS}{dt} = -\frac{S}{\tau_p} + \frac{\beta N}{\tau_n} + \frac{G_o(N-N_o)S}{1+\varepsilon S}$$

$$\frac{dN}{dt} = \frac{\eta_i(I-I_{off}(T))}{q} - \frac{N}{\tau_n} - \frac{G_o(N-N_o)S}{1+\varepsilon S}$$

Rate Equation

$$I_{off}(T) = a_0 + a_1T + a_2T^2 + a_3T^3 + a_4T^4$$

$$T = T_o + (IV - P_o)R_{th} - \tau_{th}\frac{dT}{dt}$$

$$V = \begin{cases} (b_0 + b_1T + b_2T^2)(c_0 + c_1I + c_2I^2) \\ (c_0 + c_1I + c_2I^2 + c_3I^3 + c_4I^4 + c_5I^5 + c_6I^6) \\ AI + B\ln(1 + \frac{I}{C}) \end{cases}$$

  - Stationary Analysis

$$P_o = \eta(I - I_{itho} - I_{off}(T))$$

$$I_{off}(T) = a_0 + a_1T + a_2T^2 + a_3T^3 + a_4T^4$$

$$T = T_o + (IV - P_o)R_{th}$$

$$V = \begin{cases} (b_0 + b_1T + b_2T^2)(c_0 + c_1I + c_2I^2) \\ (c_0 + c_1I + c_2I^2 + c_3I^3 + c_4I^4 + c_5I^5 + c_6I^6) \\ AI + B\ln(1 + \frac{I}{C}) \end{cases}$$

VCSEL Modeling and Extraction
VCSEL Extraction

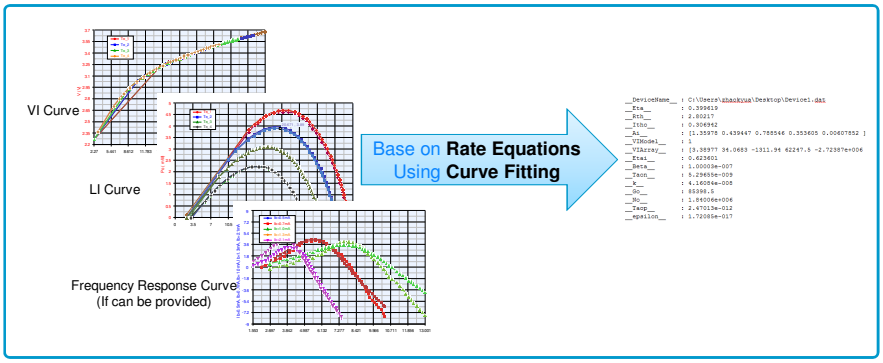
- Extraction Basics
  - VCSEL's performance ↔ Parameter values in rate equations
  - Measured curves
    - LI ~ Po(I; T)
      - Measured stationary, shows the relationship between input current and the output power under different ambient temperature
    - VI ~ V(I; T)
      - Measured stationary, shows the relationship between input current and the voltage for connection, also with effect of ambient temperature
    - Frequency response ~ H(w)
      - Measured stationary, shows the frequency response, reveals the signal transmission characteristics

VCSEL Modeling and Extraction
VCSEL Extraction

- Extraction Method
  - Curve Fitting Algorithm
    - LS curve fitting
      - Just solve the matrix equations
      - Suitable for simple relationship equations, such as the polynomial
      - Accurate and less time cost
    - Minimal gradient curve fitting
      - Try to find the certain set of values which can generate the smallest error
      - Suitable for more complex equations, especially with iterations
      - Need some pre-knowledge of the range of the parameters
      - More time cost for accuracy

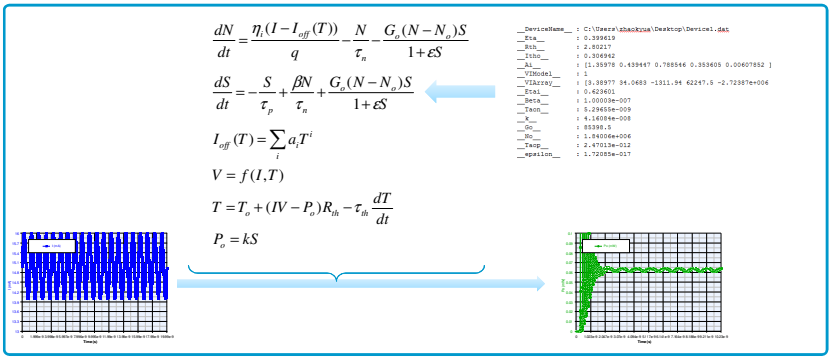
VCSEL Modeling and Extraction
VCSEL Extraction

- Schematic



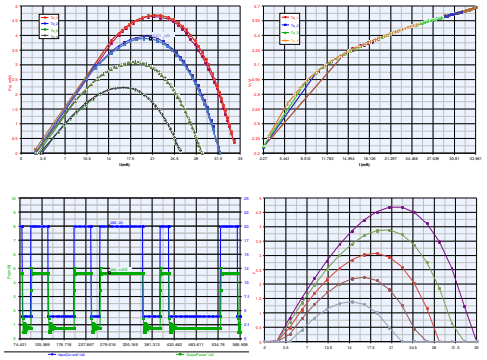
VCSEL Verification

- VCSEL Simulation
  - Parameter values in rate equations ↔ VCSEL's performance
  - Schematic



VCSEL Verification

- Case 1 ~ device verification
  - 863-nm bottom-emitting VCSEL, 16-mm diameter
  - Extraction
    - Curves fitting result
      - LI and VI curve
    - Behavior mode is generated with file format
  - Simulation
    - Po(I) under different To
    - Response for large signal



VCSEL Verification

- Case 2 ~ device verification
  - 3.1um diameter thin-oxide-aperture VCSEL
  - Extraction Result
    - Curves fitting result
      - LI(Fig 1)
      - VI(Fig 2)
      - Freq. response(Fig3)
    - Simulation
      - Po(I) simulation (Fig4)
      - Frequency response(Fig5)
      - Response for large signal(Fig6)

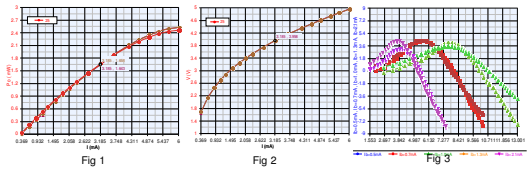


Fig 1 Fig 2 Fig 3

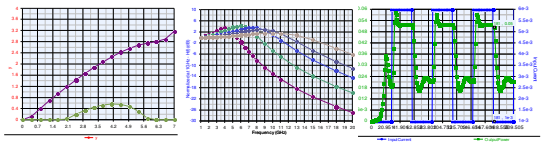
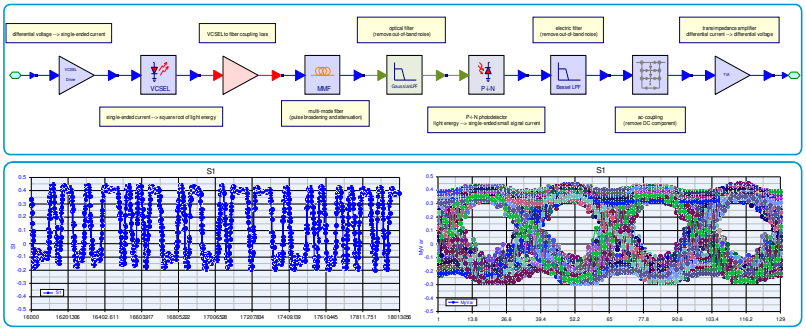


Fig 4 Fig 5 Fig 6

VCSEL Verification

- Case 3 ~ optical link simulation
  - 25GHz signal transmission
  - A whole optical link: current → optical signal → current



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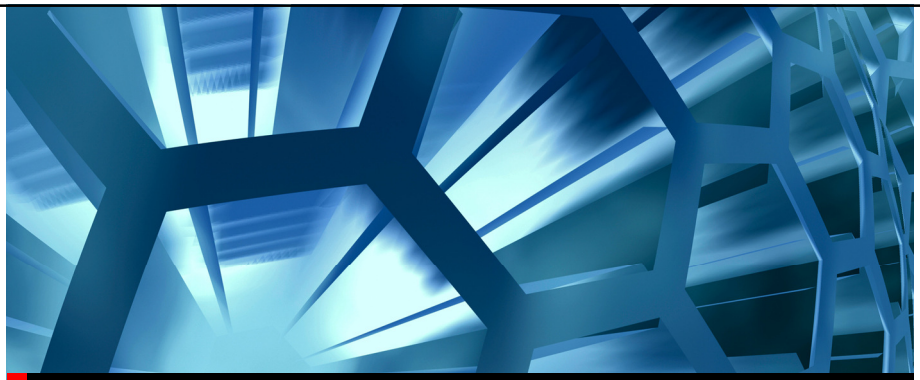

Adaptive Crosstalk Cancellation Block for SERDES and its AMI Implementation

Taranjit Kukal, Shivani Sharma, Zhangmin Zhong

IBIS Asia Summit
Shanghai, China
Nov. 15, 2013

cadence

Agenda

- Crosstalk in differential buffers
- Overview of Crosstalk Cancellation block
- Need for Adaptive Crosstalk Cancellation
- AMI Modeling of Crosstalk Cancellation block
- Simulation results and Conclusion

cadence

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  cadence

Crosstalk in Differential PCB Interconnects

- Crosstalk from neighboring channels at high frequencies causes Crosstalk-Induced Jitter (CIJ).
- Depends on the length, width and spacing of the traces.
- However, it is also a function of data-pattern. Faster switching increases crosstalk.
- Cancellation of crosstalk can result in smaller spacing between the traces or higher BER

  cadence

Agenda

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  cadence

Crosstalk Induced Jitter (CIJ)

- CIJ causes Far End Crosstalk (FEXT) and Near End Crosstalk (NEXT). FEXT is more dominant for PCB traces.
- Far End Crosstalk (FEXT) from aggressor channel to the victim channel is proportional to the derivative of aggressor channel impulse response:

$$h(t)_{FEXT} = -K\frac{\partial h(t)_{aggressor}}{\partial t}$$

  cadence

Crosstalk Induced Jitter (CIJ)

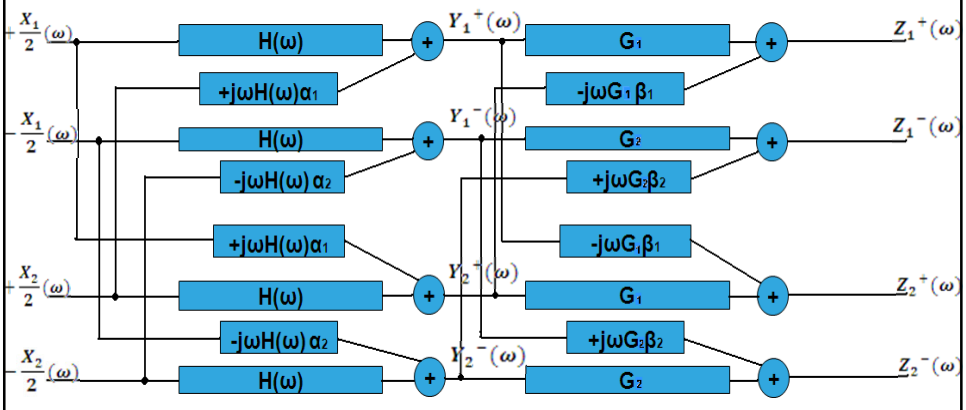
$$h(t)_{FEXT} = -K\frac{\partial h(t)_{aggressor}}{\partial t}$$

- Here K is the crosstalk coupling coefficient that depends on length, height and spacing between traces.
- Crosstalk also depends on data transitions. More transitions increase crosstalk

  cadence

CIJ Cancellation using MIMO

- Block Diagram of crosstalk cancellation at Rx



- MIMO: Multiple Input Multiple Output
- Based on inverse system modeling

  cadence

CIJ Cancellation using MIMO

- Output as a function of Inputs can be expressed as:

$$\begin{bmatrix} Z_1^+(\omega) \\ Z_1^-(\omega) \\ Z_2^+(\omega) \\ Z_2^-(\omega) \end{bmatrix}$$

$$= \begin{bmatrix} h(\omega) & 0 & j\omega h(\omega)\alpha_1 & 0 \\ 0 & h(\omega) & 0 & -j\omega h(\omega)\alpha_2 \\ j\omega h(\omega)\alpha_1 & 0 & h(\omega) & 0 \\ 0 & -j\omega h(\omega)\alpha_2 & 0 & h(\omega) \end{bmatrix} \begin{bmatrix} G_1 & 0 & -j\omega G_1\beta_1 & 0 \\ 0 & G_2 & 0 & +j\omega G_2\beta_2 \\ -j\omega G_1\beta_1 & 0 & G_1 & 0 \\ 0 & +j\omega G_2\beta_2 & 0 & G_2 \end{bmatrix} \begin{bmatrix} +\frac{X_1}{2}(\omega) \\ -\frac{X_1}{2}(\omega) \\ +\frac{X_2}{2}(\omega) \\ -\frac{X_2}{2}(\omega) \end{bmatrix}$$

$$= \begin{bmatrix} G_1h(\omega)(1+\omega^2\alpha_1\beta_1) & 0 & j\omega G_1h(\omega)(\alpha_1-\beta_1) & 0 \\ 0 & G_2h(\omega)(1+\omega^2\alpha_2\beta_2) & 0 & -j\omega G_2h(\omega)(\alpha_2-\beta_2) \\ j\omega G_1h(\omega)(\alpha_1-\beta_1) & 0 & G_1h(\omega)(1+\omega^2\alpha_1\beta_1) & 0 \\ 0 & -j\omega G_2h(\omega)(\alpha_2-\beta_2) & 0 & G_2h(\omega)(1+\omega^2\alpha_2\beta_2) \end{bmatrix} \begin{bmatrix} +\frac{X_1}{2}(\omega) \\ -\frac{X_1}{2}(\omega) \\ +\frac{X_2}{2}(\omega) \\ -\frac{X_2}{2}(\omega) \end{bmatrix}$$

•If α1= β1 α2= β2, crosstalk becomes zero!!

  cadence

Agenda

- Crosstalk in differential buffers
- Overview of Crosstalk Cancellation block
- Need for Adaptive Crosstalk Cancellation
- AMI Modeling of Crosstalk Cancellation block
- Simulation results and Conclusion

  cadence

Need for Adaptive Crosstalk Cancellation

- Limitations:
  - Coupling coefficient needs to be known to the receiver.
  - Power required for crosstalk cancellation block
- Proposal
  - Determine crosstalk coupling coefficient on the fly based on crosstalk activity.
  - If the coupling coefficient is too small then the cancellation scheme can be switched off to save power.

  cadence

Agenda

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  cadence

Adaptive CIJ Cancellation: AMI Implementation

- Crosstalk is a function of channel length, spacing between channels and amount of data transitions. The number of data transitions varies with data pattern.
- Effectively, crosstalk between two interconnects keeps varying with data pattern.
- Effective coupling coefficient can be considered directly proportional to the transitions in the data-pattern.

  cadence

Adaptive CIJ Cancellation: AMI Implementation

$$\frac{Z_1}{2}^{+}(\omega) = Gh(\omega)(1+\omega^2\alpha_1\beta_1)\frac{X_1}{2}(\omega) + j\omega Gh(\omega)(\alpha_1-\beta_1)\frac{X_2}{2}(\omega)$$

$$G_i = \frac{1}{1+sR_iC_i}\Big| i = 1,2 \qquad \beta_i = R_iC_i$$

- Apply bilinear transformation to Gi **(fs – sampling rate)**
  - To be coded as FIR filter

$$G_i = \frac{1+z^{-1}}{z^{-1}\left(1-\frac{1}{\tan\left(\frac{1}{2RiCif_s}\right)}\right)+1+\frac{1}{\tan\left(\frac{1}{2RiCif_s}\right)}}$$

- Training sequence is be used to train the crosstalk cancellation block
  - Input is applied only at one channel, and the crosstalk signal is measured at the output of other channel
  - Intent is to minimize (zero) the crosstalk at other channel

  cadence

Adaptive CIJ Cancellation: AMI Implementation using Varactor

- Integrate the crosstalk signal to obtain Vf (Reverse-bias voltage) that would control the capacitance of the varactor (voltage dependent capacitor)
- Compute Ci using Varactor equation

$$C_i = \frac{C_0}{\sqrt{1 + \frac{V_f}{V_{bi}}}}$$

  - With C_0 (0 bias capacitance) = 0.025 and V_{bi} (Built in voltage potential)= 0.5 as constants.
  - Ci modifies the crosstalk cancellation block Gi such that the crosstalk becomes zero.

$$G_i = \frac{1}{1 + sR_iC_i} \Big| i = 1, 2$$

  cadence

Agenda

- Crosstalk in differential buffers
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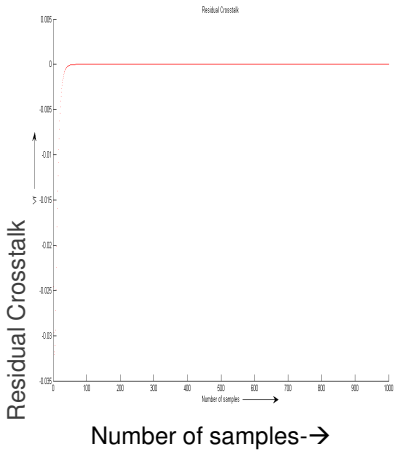
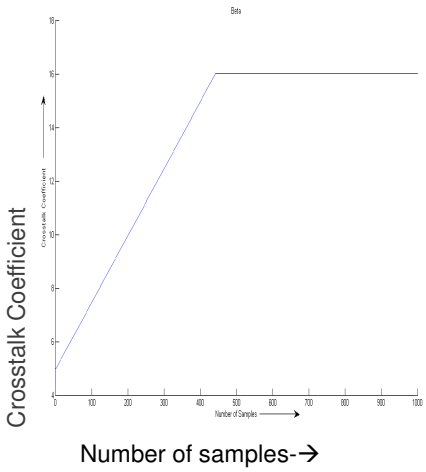
  cadence

MATLAB Simulation:
- Adaptive Crosstalk Cancellation





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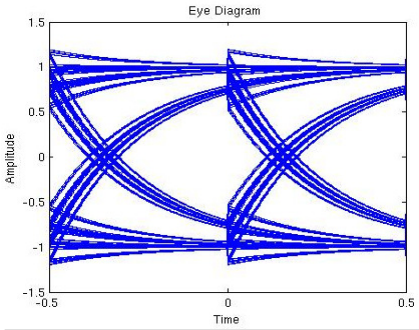
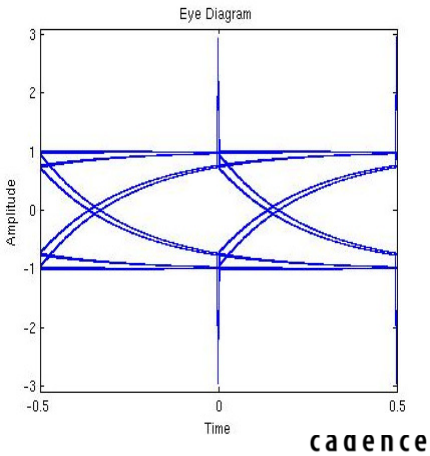
MATLAB Simulation:
- Adaptive Crosstalk Cancellation

Without Crosstalk cancellation	With Crosstalk cancellation





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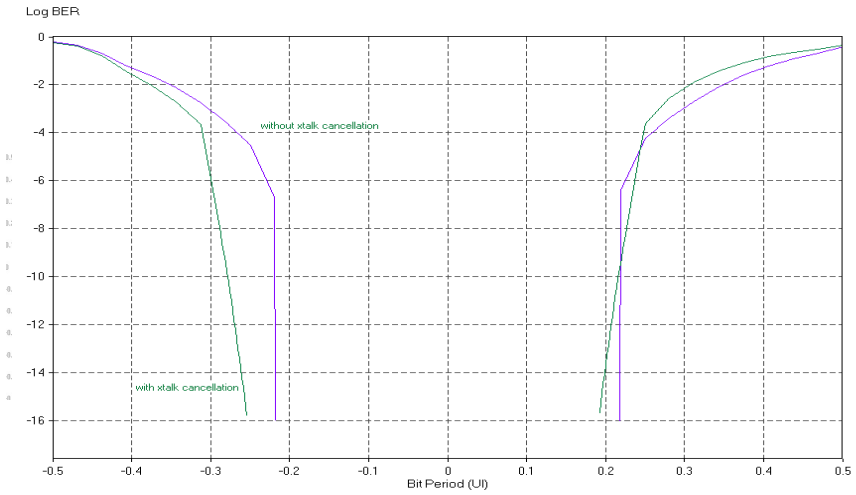
AMI Simulation:
- Adaptive Crosstalk Cancellation



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Conclusion

- At higher data-rates, crosstalk is becoming issue for differential buffers.
- Crosstalk induced jitter can be cancelled by crosstalk cancellation block
- Since crosstalk jitter is pattern dependent, it is important that crosstalk cancellation adapts itself based on data-induced jitter

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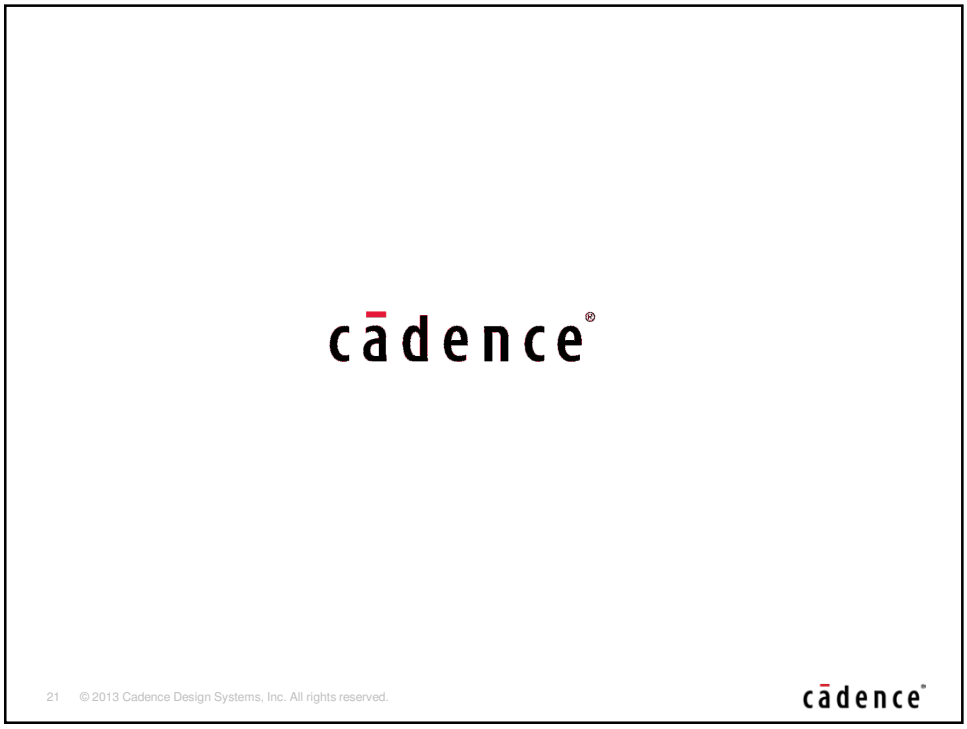
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Realize Your Product Promise™

Anisotropic Substrates Variance for *IBIS-AMI Simulation*

Naijen Hsuan
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Asian IBIS Summit Shanghai, China November 15, 2013

ANSYS

High speed Challenges Today

(1) High Speed Data Rate Issue

(2) Anisotropic Substrates Variance

(3) FEM solution to analysis Anisotropic Substrates Variance

(4) Anisotropic Substrates Variance for IBIS-AMI Simulation

(5) DOE Solution

High speed IO Challenges Today

As serial links become faster and more complex, it is ever more challenging to model the silicon in an accurate and efficient manner.

Models/Simulator need to handle current challenges:

- **Need to accurately handle very high data rates**
- **Simulate large number of bits to achieve low BER**
- **Non-linear, Time Variant Systems**
- **TX/RX equalization**
- **Specific Data patterns and coding schemes**
- **Non-convergence due to unstable models**
- **Channel Issue**

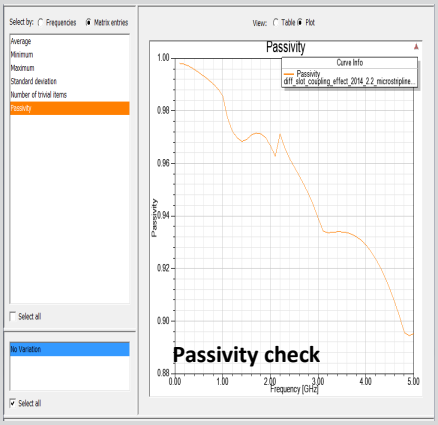
Circuit Simulation Issues with S-parameters

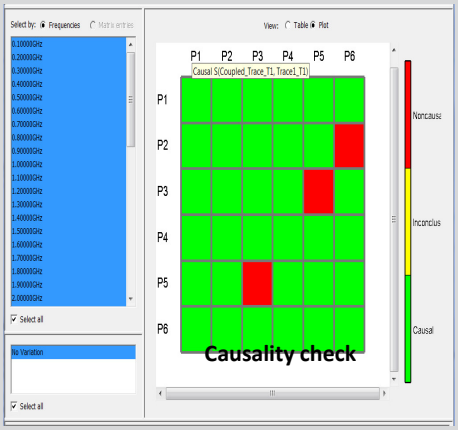
Passivity and Causality

- **Though S-parameters from a physics-based extraction tool should always be passive and causal, measured S-parameters often exhibit problems due to noise**
- **State-space model for S-parameter data guarantees causality of the circuit simulator model**
- **Two passivity enforcement algorithms**
  - **Convex programming**
  - **Perturbation**

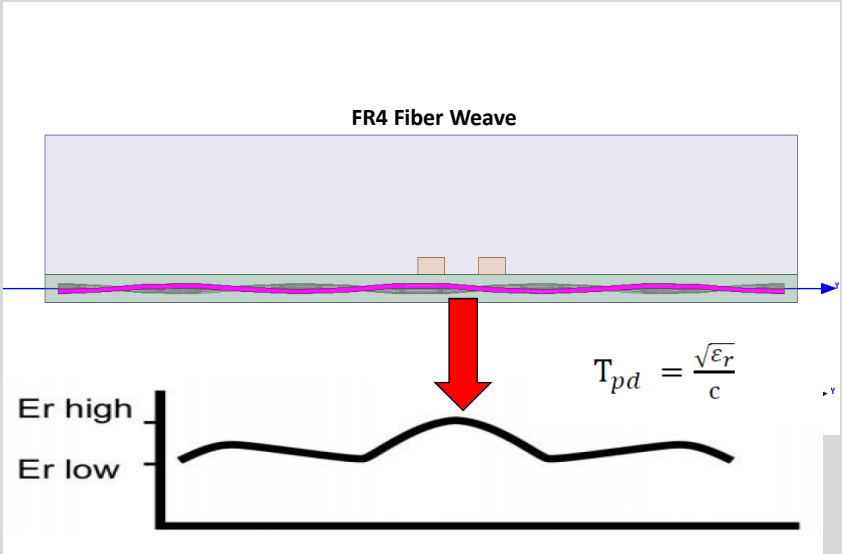
Check and Enforce Function

Check and Enforce passivity and causality

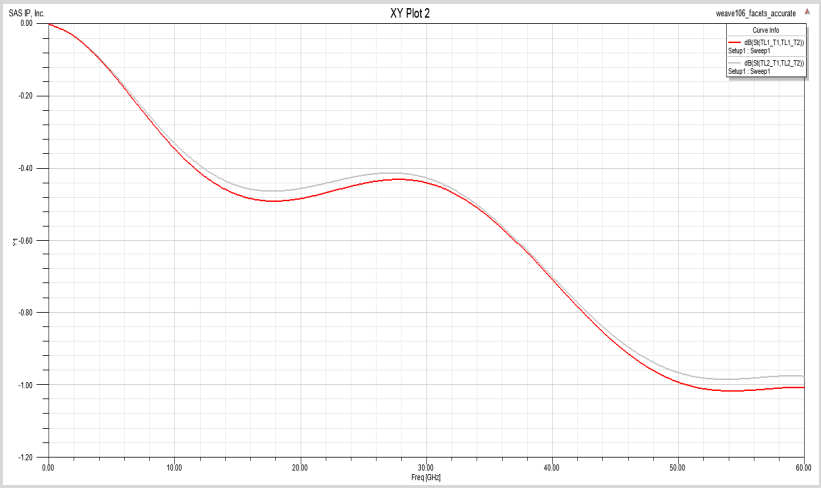




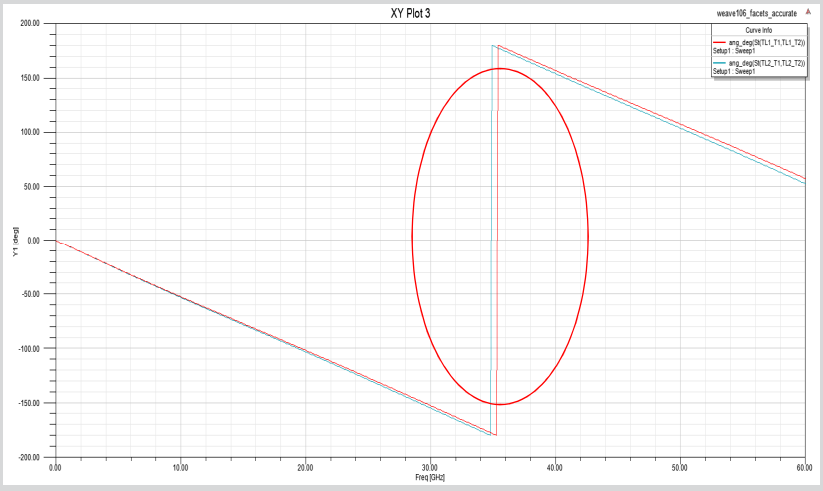
Anisotropic Substrates



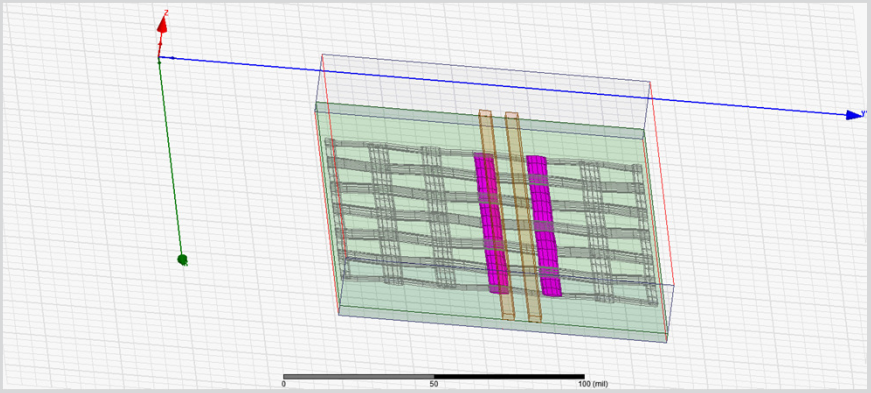
Insertion loss for one net



Differential skew Problem

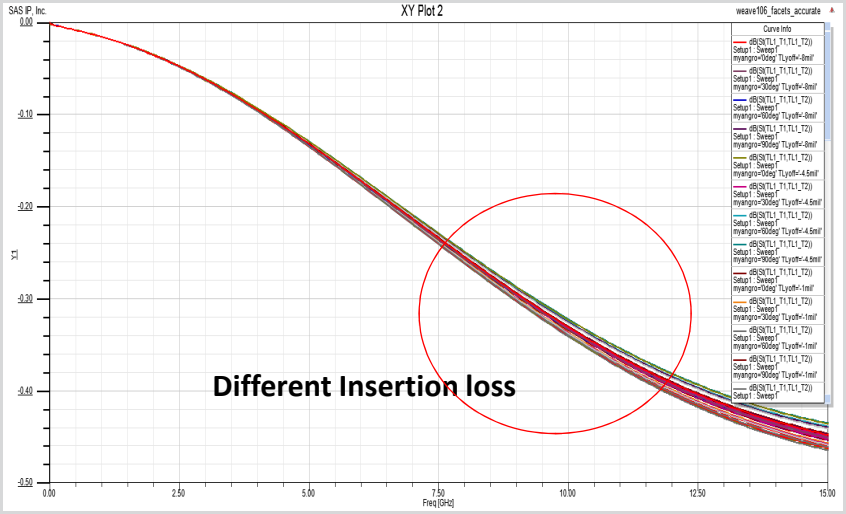


Anisotropic Substrates Variance

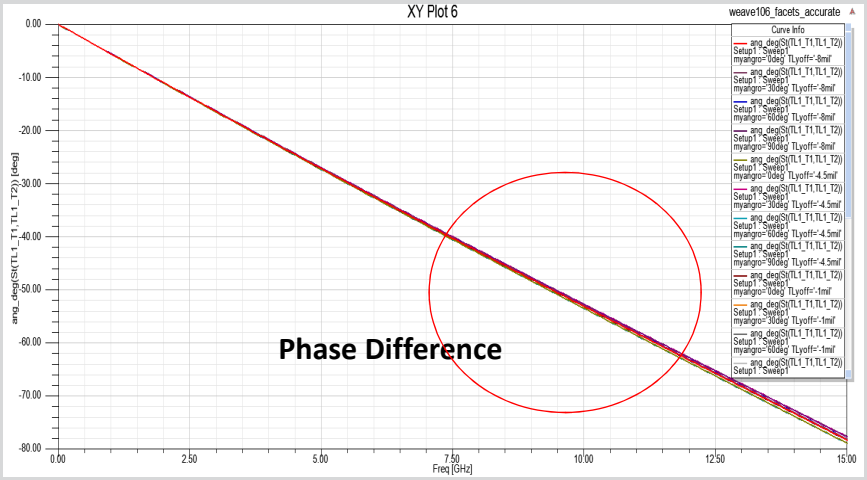


Change degree angle of rotation

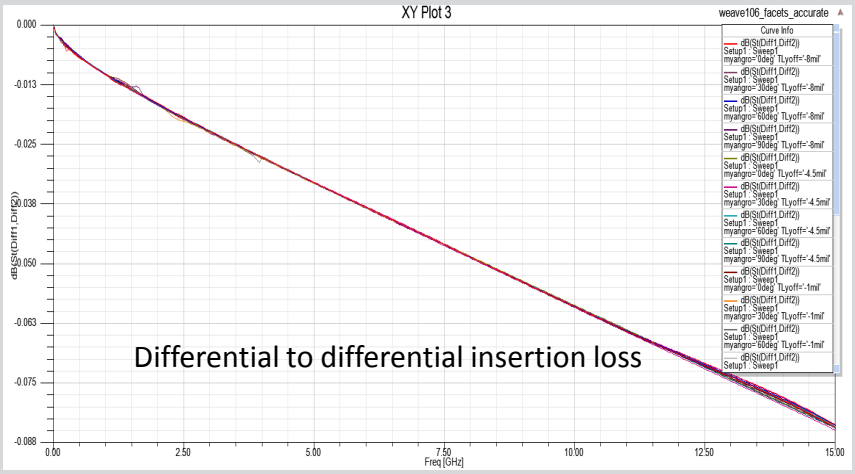
Anisotropic Substrates Variance



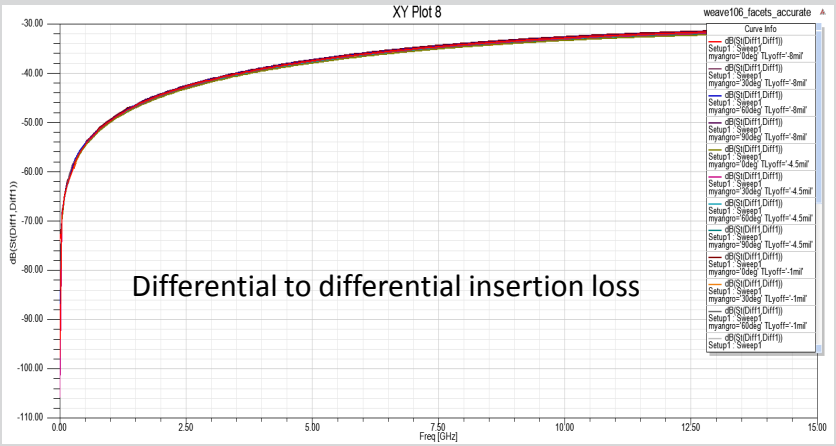
Anisotropic Substrates Variance



Anisotropic Substrates Variance



Anisotropic Substrates Variance



IBIS-AMI and statistical eye analysis

- Use the final impulse response from AMI analysis to run statistical eye analysis
- Linear modifications (AMI Init) from Tx and Rx AMI models taken into account
- AMI GetWave functionality cannot be used for statistical analysis as it is a purely time domain function

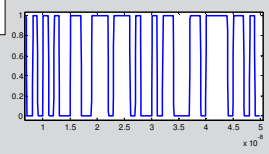
Data flow

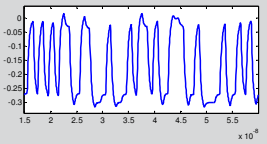
AMI Transmitter (Tx)

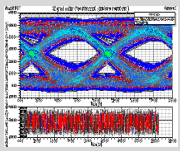
Linear Channel

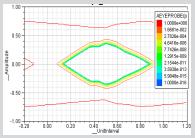
AMI Receiver (Rx)

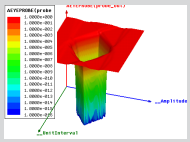
Engine post-processing











Very similar to Fast Convolution

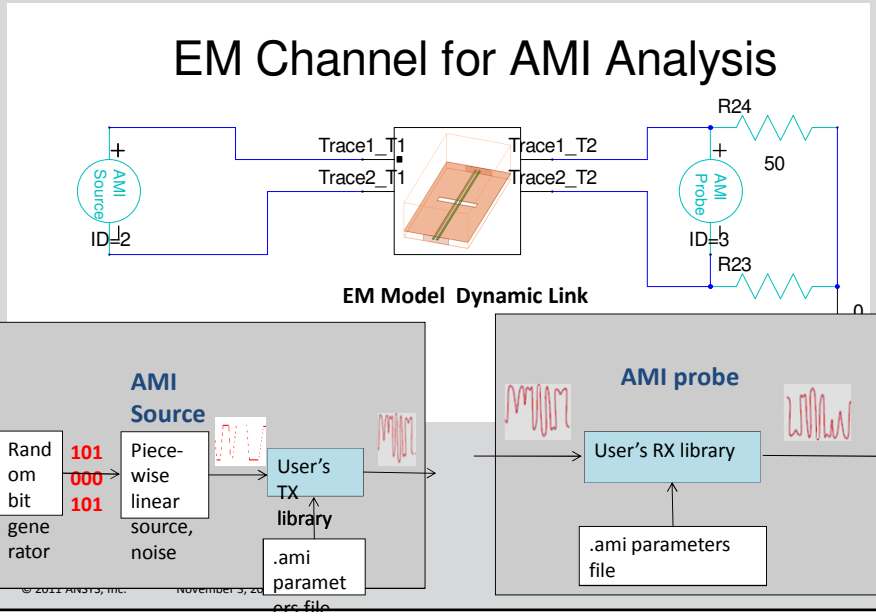
- **No backward dependency**

Transmitter and receiver are based on user supplied libraries.

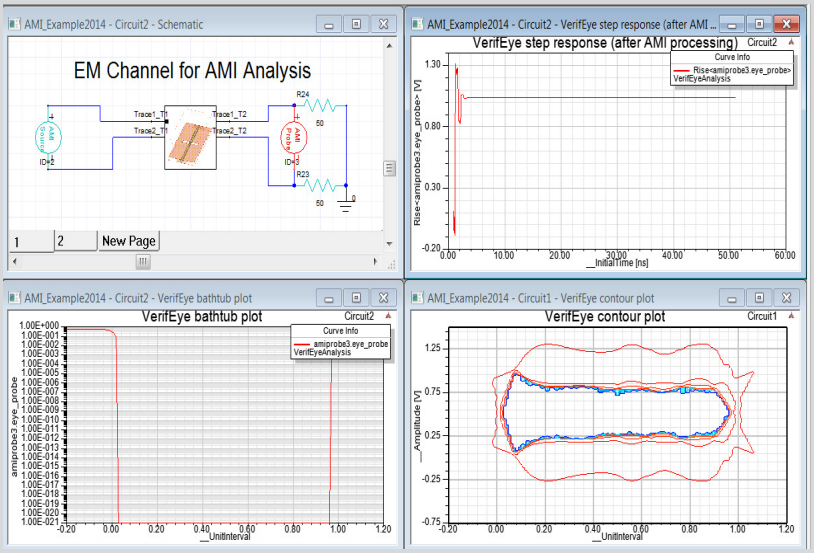
Channel is characterized with impulse response function(s)

All signals are sampled with the constant time step and handled in blocks.

EM and Circuit Co-simulation

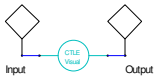


Statistical Eye Analysis Result

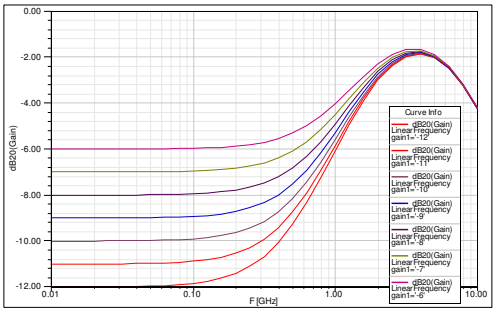


Circuit equalization techniques problem

CTLE Gain with PCIe3.0 Parameters



This example shows the response plot of a CTLE for PCIe 3.0 for different values of gain. Parameters of the CTLE component are:
1. 'p1' LF Pole = 2 GHz
2. 'p2' HF Pole = 8 GHz
3. 'z' zero frequency = 'p1' * pow(10, 'gain'/20)
4. 'gain' DC gain in dB = gain1

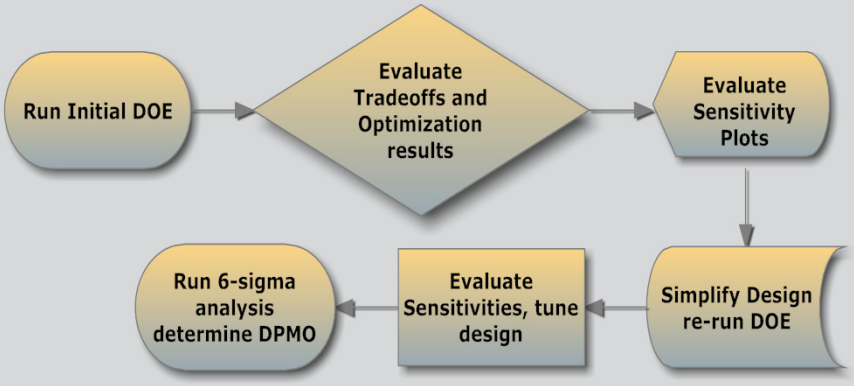


How to decide gain and pole value ??

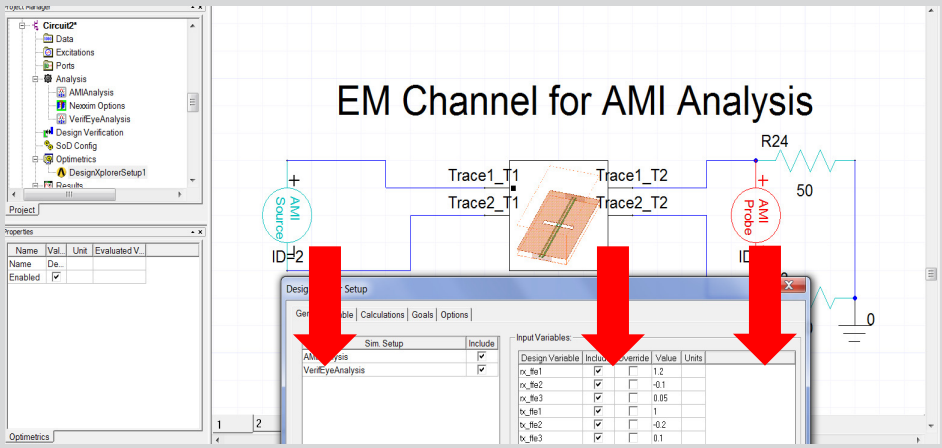
How to do that?

- Set up the DOE to sweep through the models to calculate the eye height and eye width for these cases
- The portions of the channel containing the PCB was modeled using a full-wave 3D electromagnetic extraction tool. A dynamic EM file was used to capture the channel's behavior. There are several variations of this structure that we want to include in the sensitivity analysis.
- To illustrate the results of this sensitivity analysis, we present sweeping of two of the variables: Change degree angle of rotation and equalization parameters

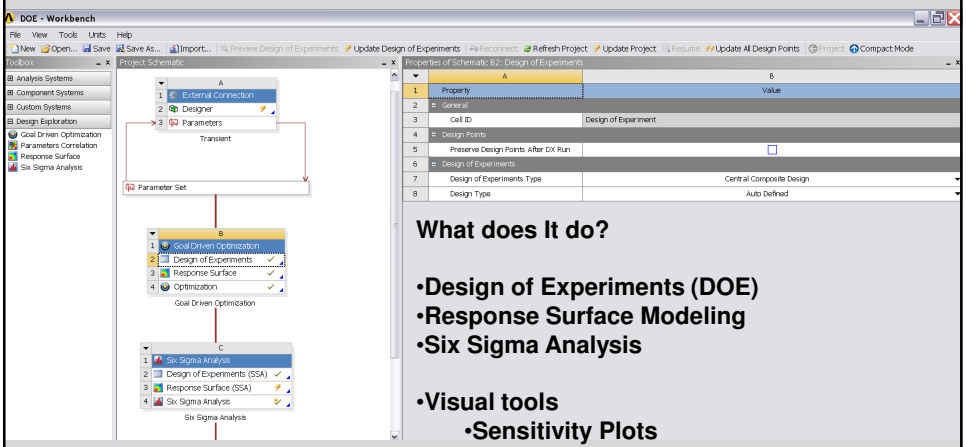
DOE Methodology



DOE setup



Any parametric analysis



What does It do?

- **Design of Experiments (DOE)**
- **Response Surface Modeling**
- **Six Sigma Analysis**

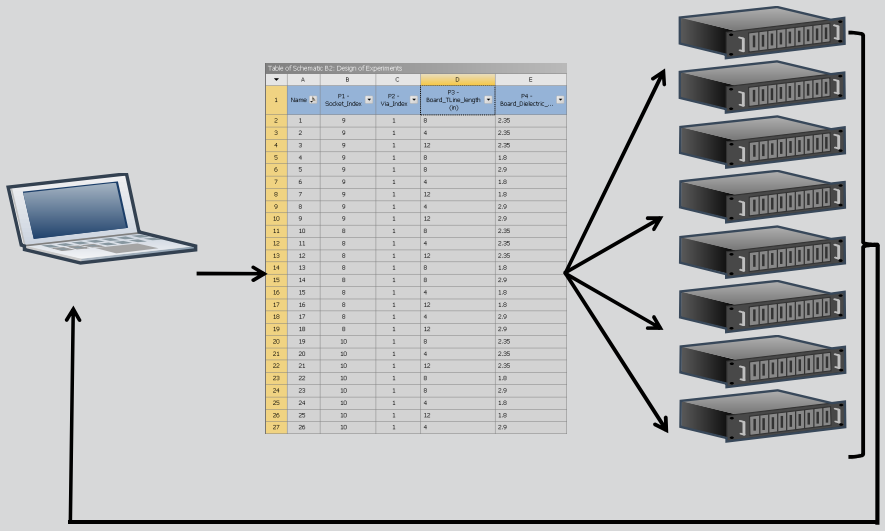
- **Visual tools**
  - **Sensitivity Plots**
  - **Correlation Matrices**
  - **Parallel charts w Pareto Front display**

Why Response Surface Modeling?

- Response Surface Modeling enables the designer to model and consider all aspects of a high speed channel design. Fit a statistical model to outputs of the design as a function of the change in input variables. A DOE table is used to select design points to solve explicitly for and the statistical model so to speak, "fills in the gaps"
- Optimized conditions and worst case scenarios are obtainable within the set of all possible design combinations within a realistic simulation timeframe.
- For example, this case, consider 8 variables or "factors", if each variable has only 5 variations or "levels" we are looking at a huge number of possible combinations in order to find optimal solutions and or worst case scenarios.

$$Combinations = Levels^{Factors} = 5^8!!!!$$

Speed Issue – HPC solution



Summary

- In this presentation, we can see the anisotropic substrates variance of PCBs, it effects phase difference between the differential pair
- Simulations on both EM dynamic models and IBIS-AMI models are applied to produce eye diagrams to check channel variance performance
- Circuit equalization techniques are applied at the Tx and Rx receiver to improve channel performance
- It is more efficient to get best channel performance by DOE and HPC solution

