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Over-Clocking model validation

Asian IBIS Summit
Yokohama, JAPAN
November 16, 2012

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Digital Products & Services Company
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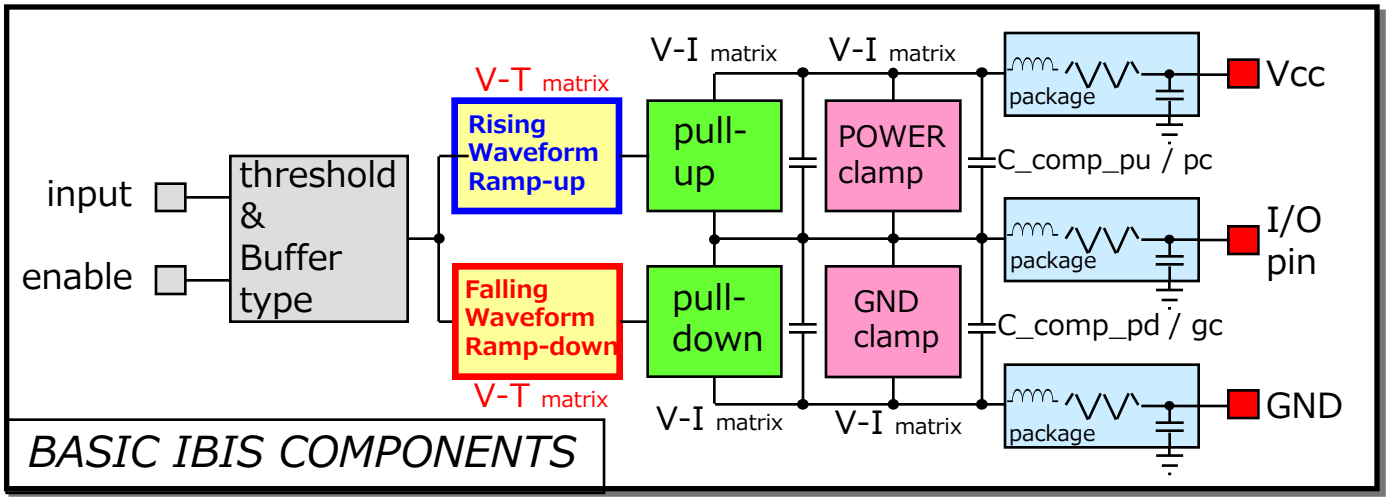
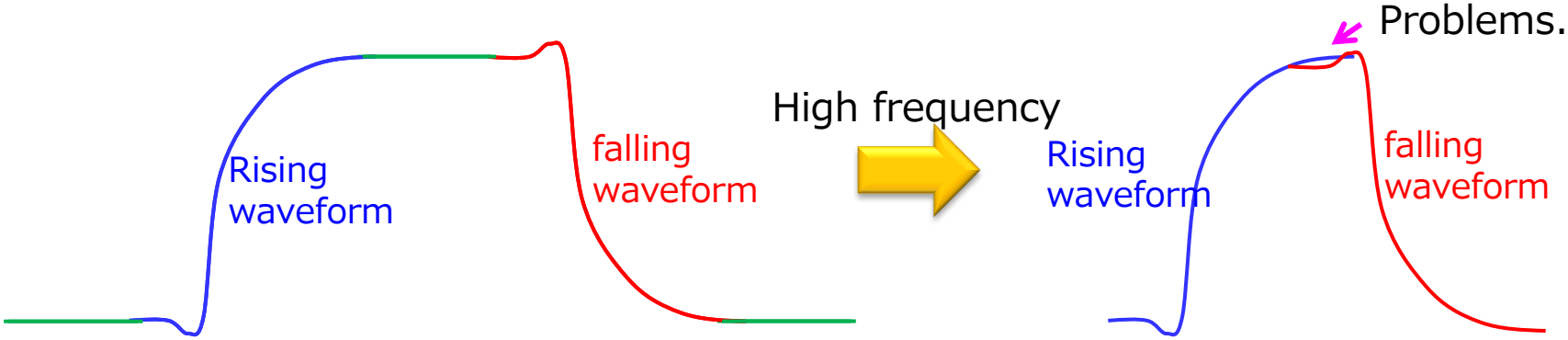
- About Over-Clocking
- Validation (Remove initial delay)
- Validation (Cut tail)
- Discussion
- Expectations for IBIS

About Over-Clocking

Over-clocking creates waveform problems.





Usual behavior
(waveform length less than 1bit length)

Overclocking
(1bit length less than waveform length)

Cookbook strongly recommends we don't use overclocking.

5.4.2 V-T Table Windowing

One procedure, which is not performed by most automated IBIS creation tools, is V-T table windowing. While there is no upper limit on the time duration of V-T tables, the transient portion of the waveforms should start and finish within the time dictated by the highest frequency of the buffer (one-half of the period).

While not an IBIS requirement, users are strongly recommended to generate V-T tables that are shorter in duration than the pulse width of the highest frequency anticipated on the interface. For example, a signal that is anticipated to drive, at maximum, 100 MHz signals should have a V-T table duration no greater than 5 ns (the period of a 100 MHz signal is 10 ns; such a signal's pulse width – longest "high time" or longest "low time" – is 5 ns).

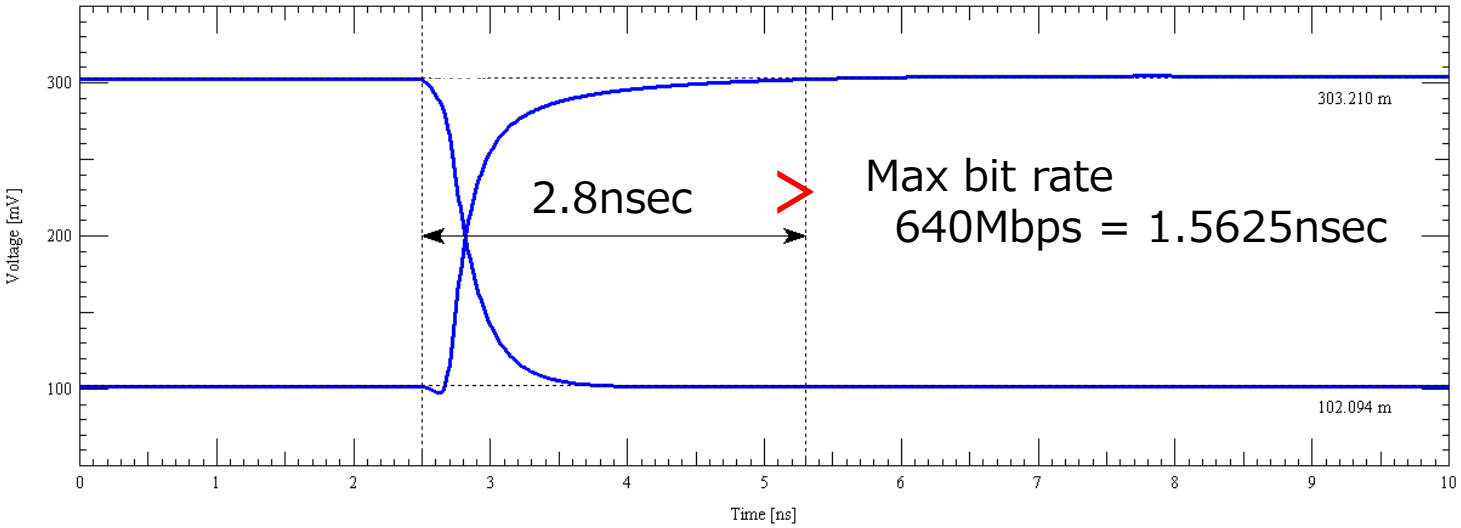
Note that this may limit the types of buffer applications appropriate for modeling under IBIS. Transistor-level models may permit switching of buffer outputs before they have completely finished a transition. However, IBIS version 4.0 assumptions do not cover this situation and buffer response for such a model may be inconsistent across EDA tools implementing IBIS.

We must create short duration waveform.

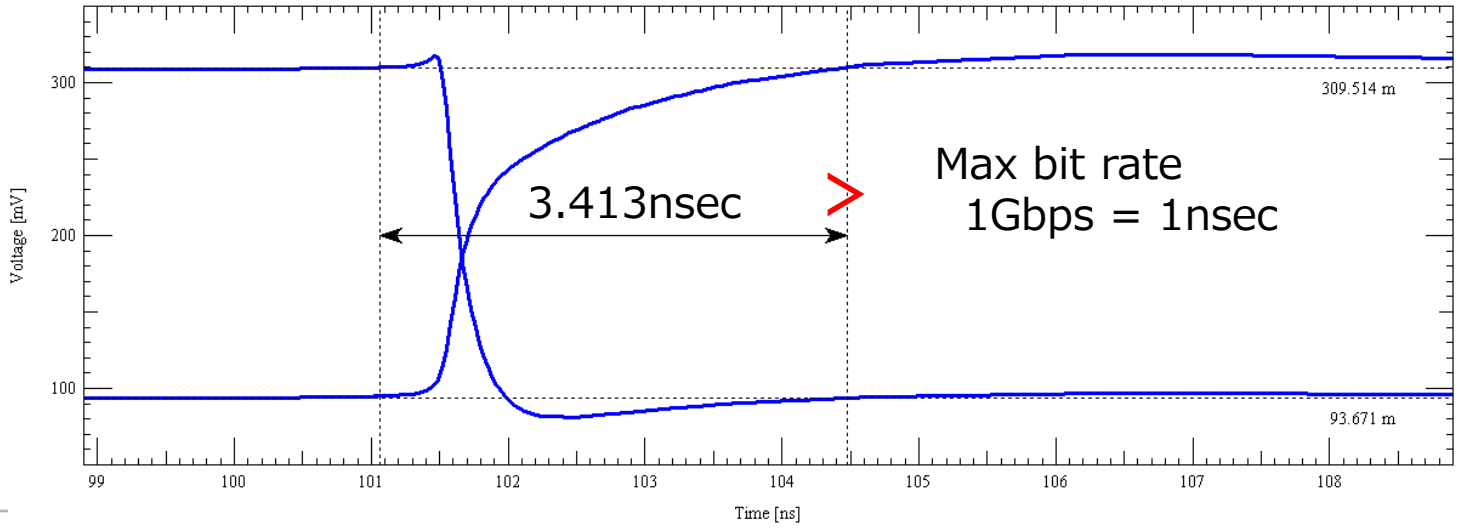
SPICE Waveform

Problem : A lot of buffer can't rise/fall within 1 bit length.

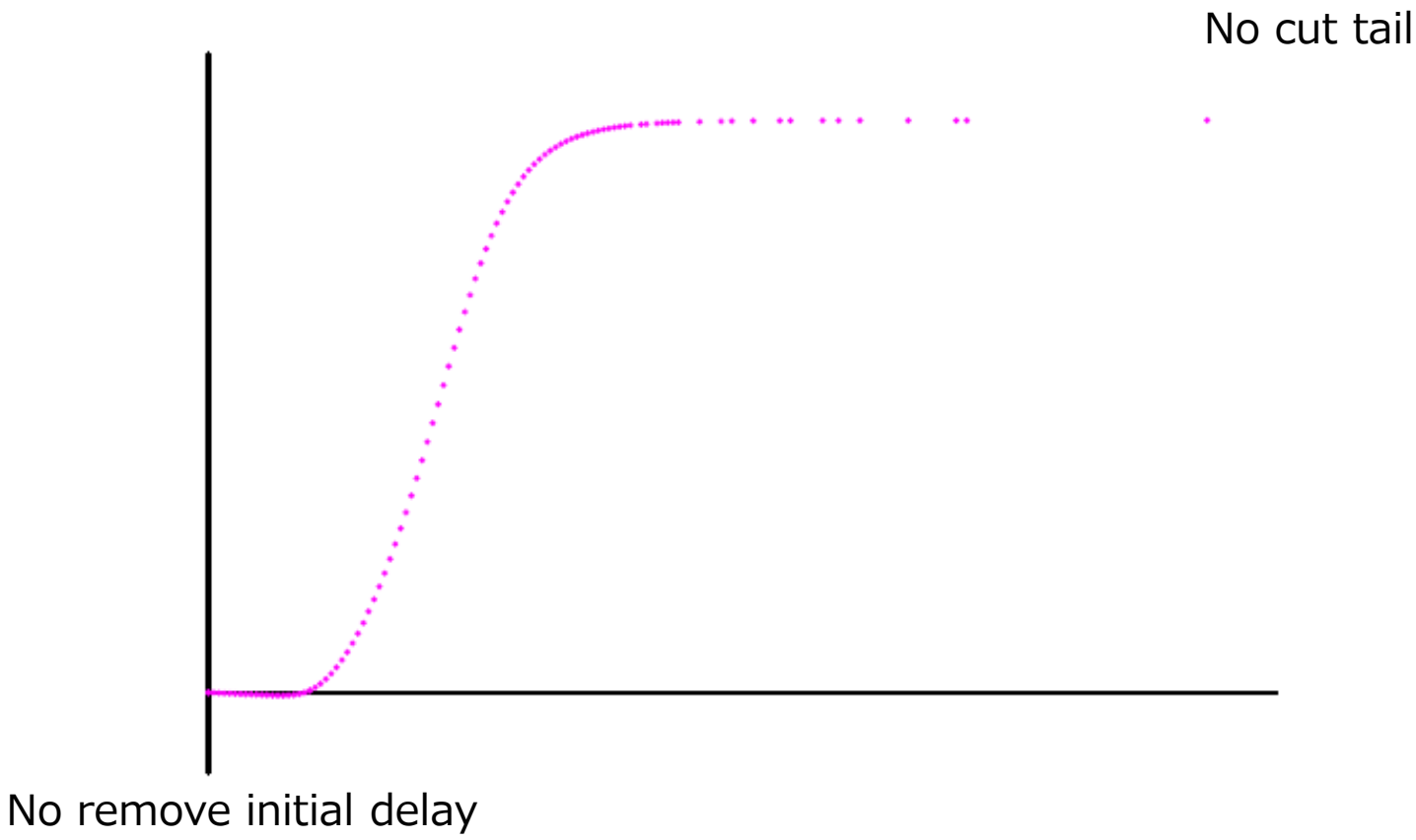
Buffer A



Buffer B

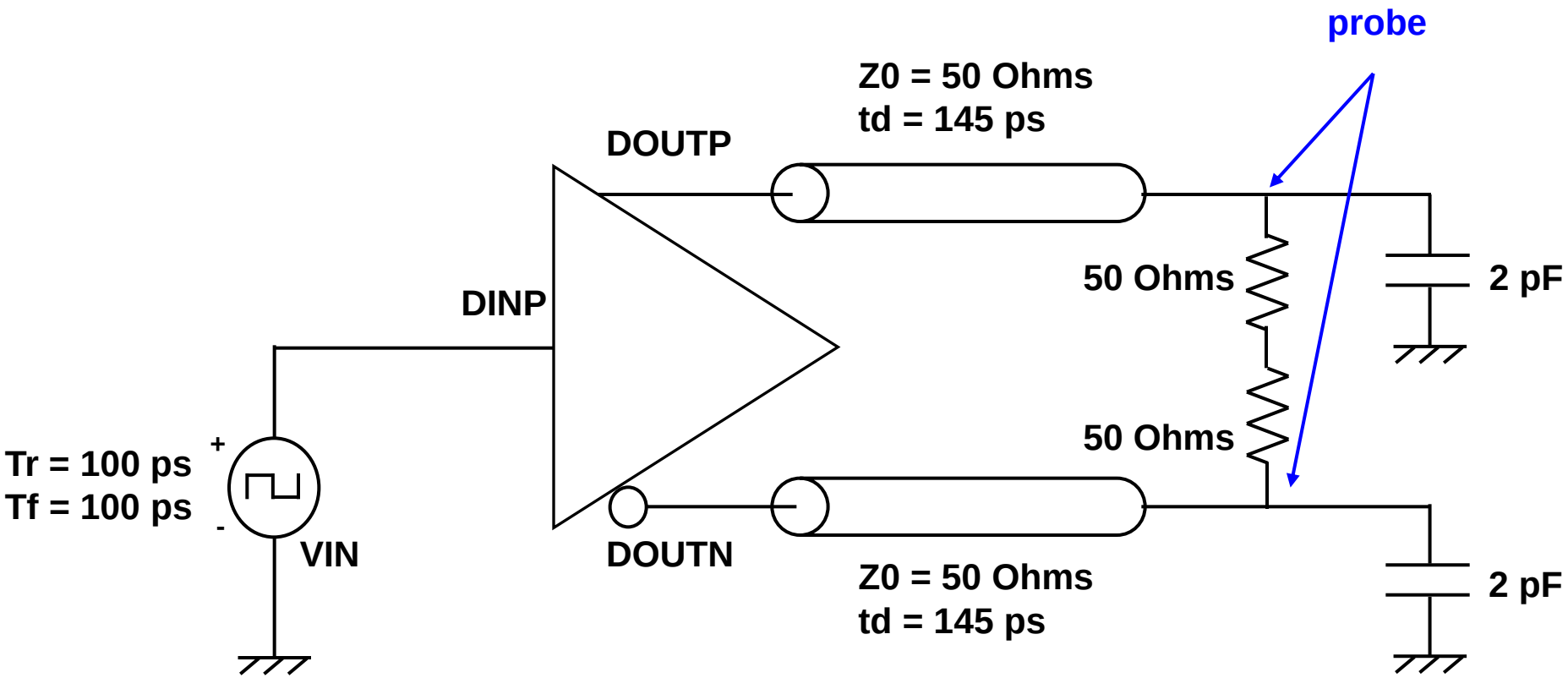


Question : really problem?



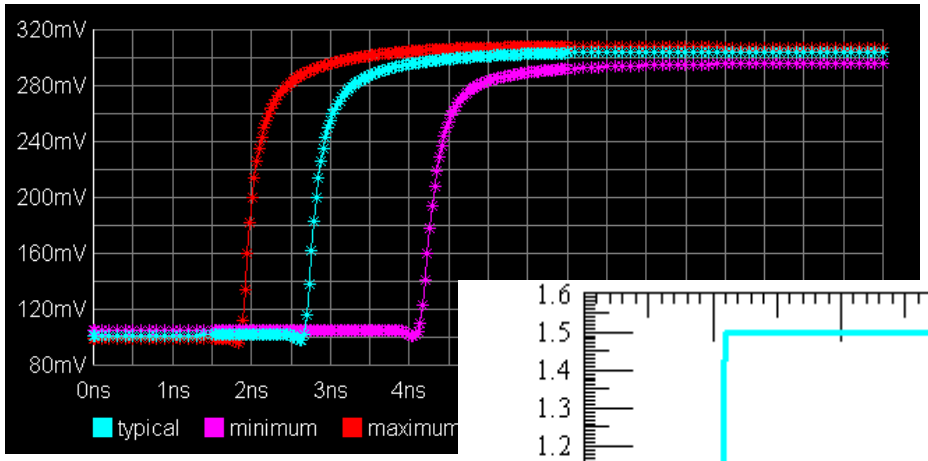
Evaluation circuit No.3

Checked using the following circuit.

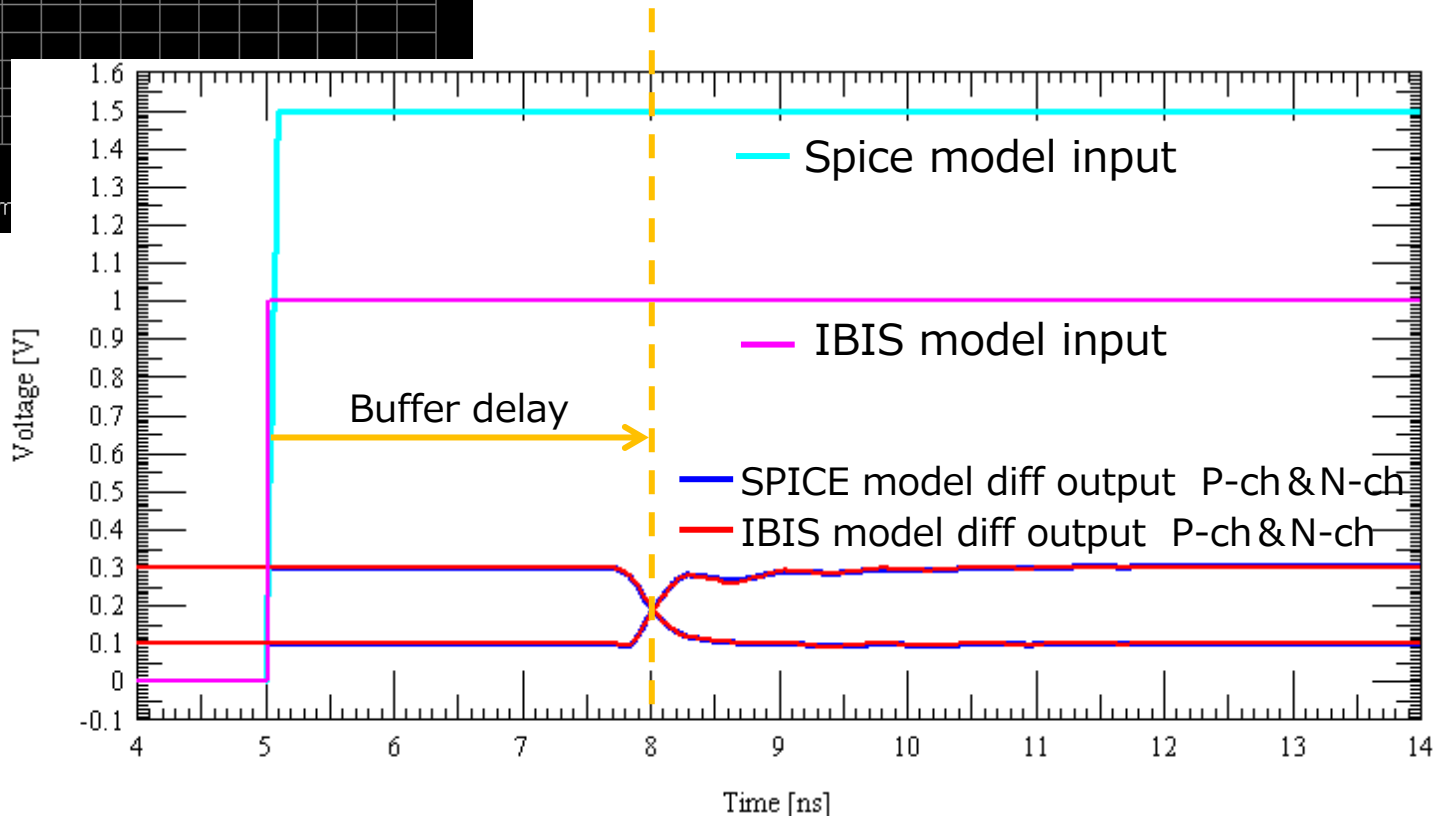


No remove initial delay model at non overclocking

Good for buffer delay at non overclocking

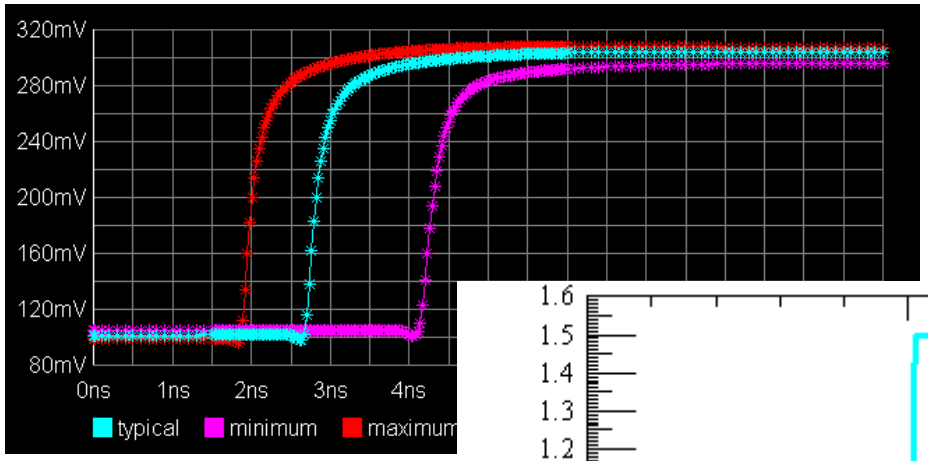


Simulator : A

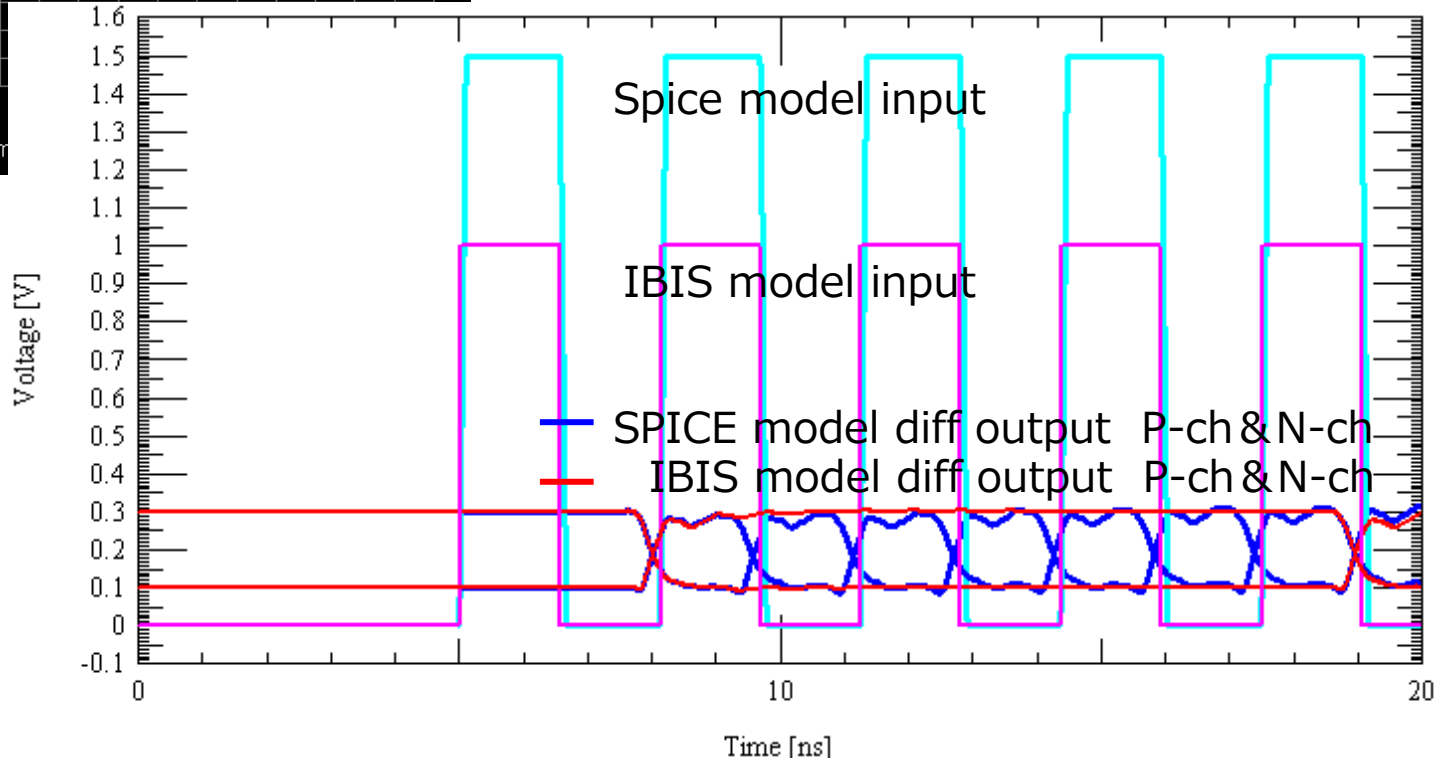


No remove initial delay model at overclocking

Doesn't work with overclocking mode

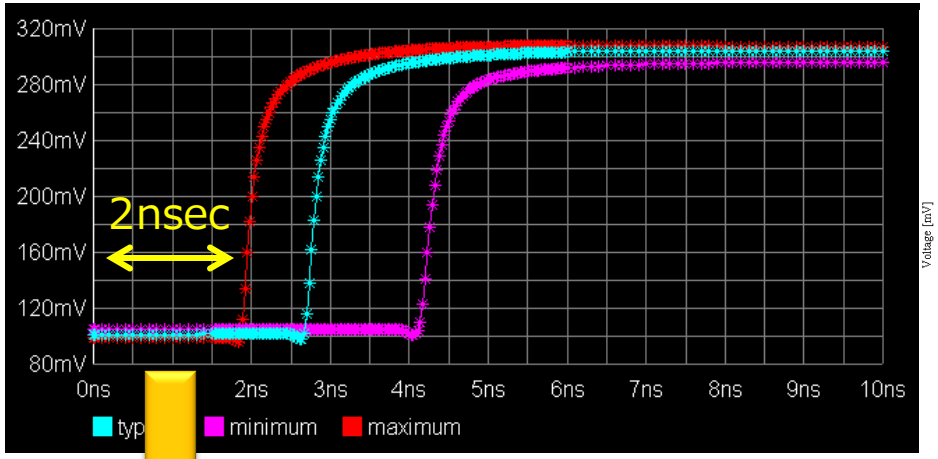


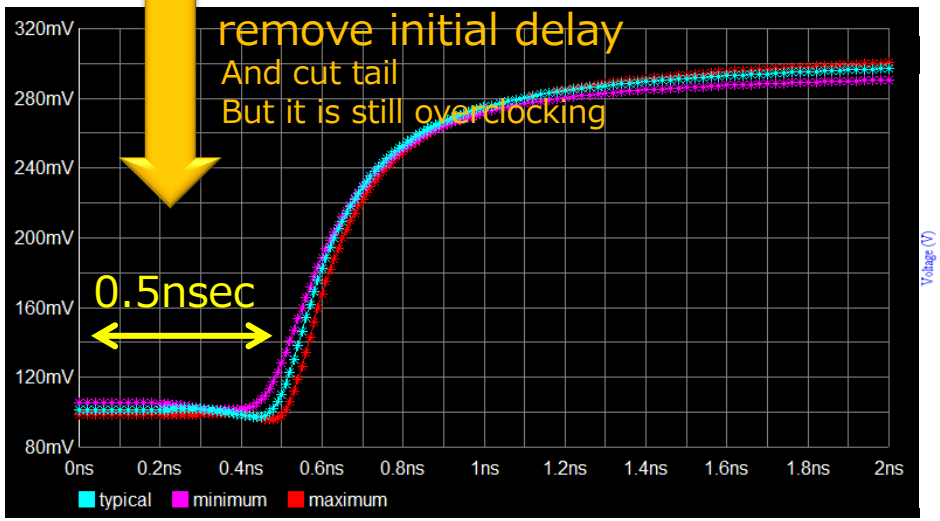
Simulator : A

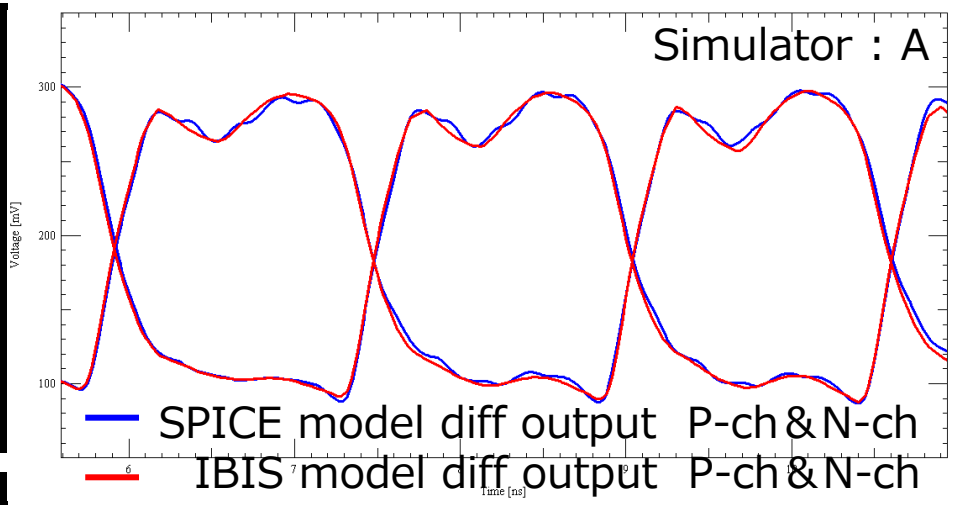


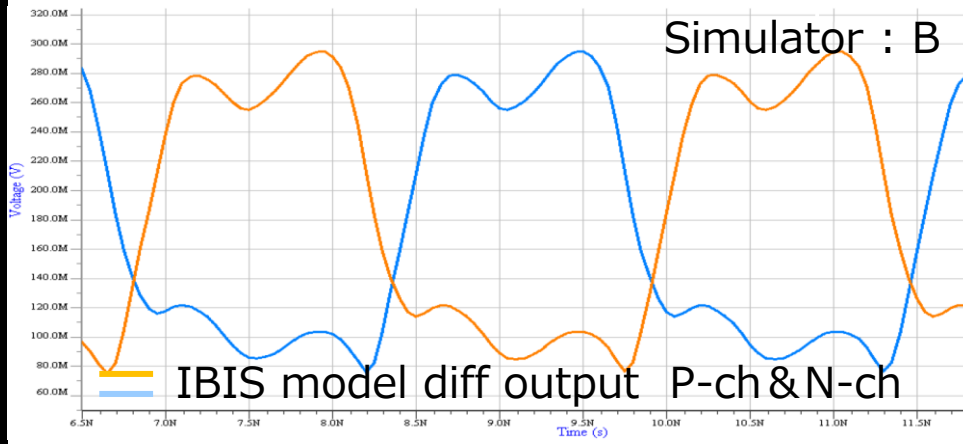
Remove initial delay

Removing initial delay is effective. But How we should do?





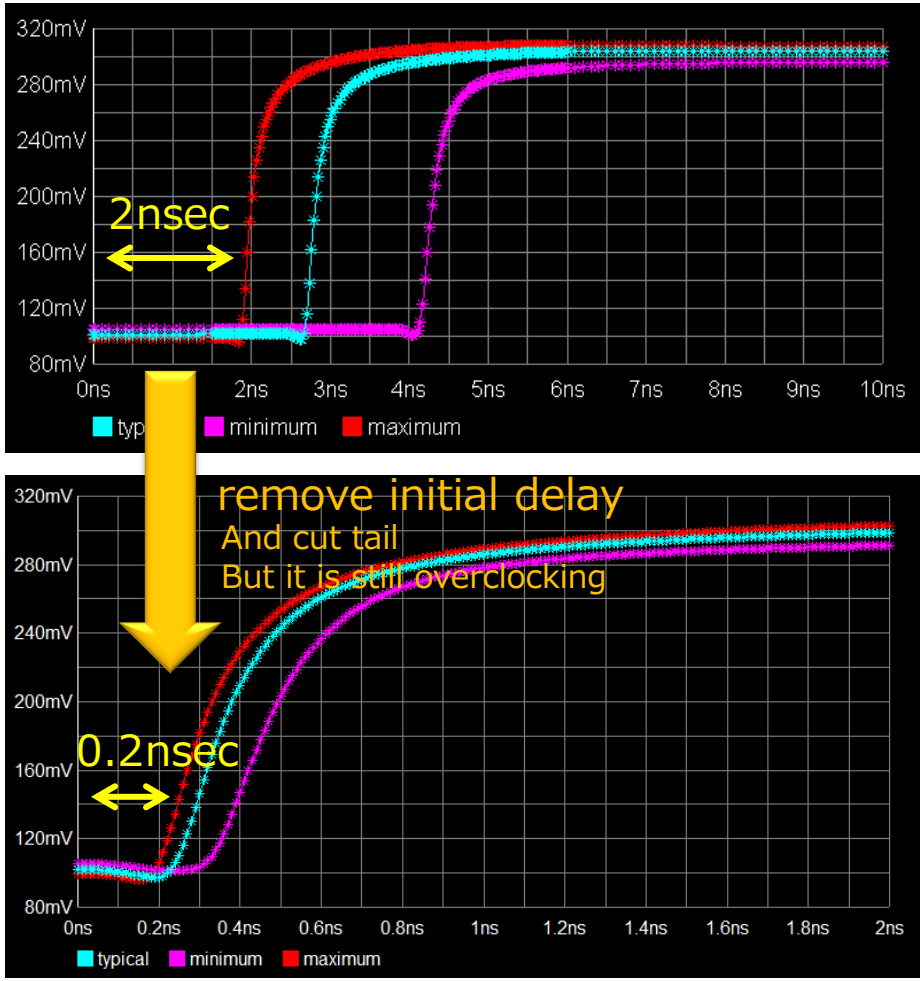


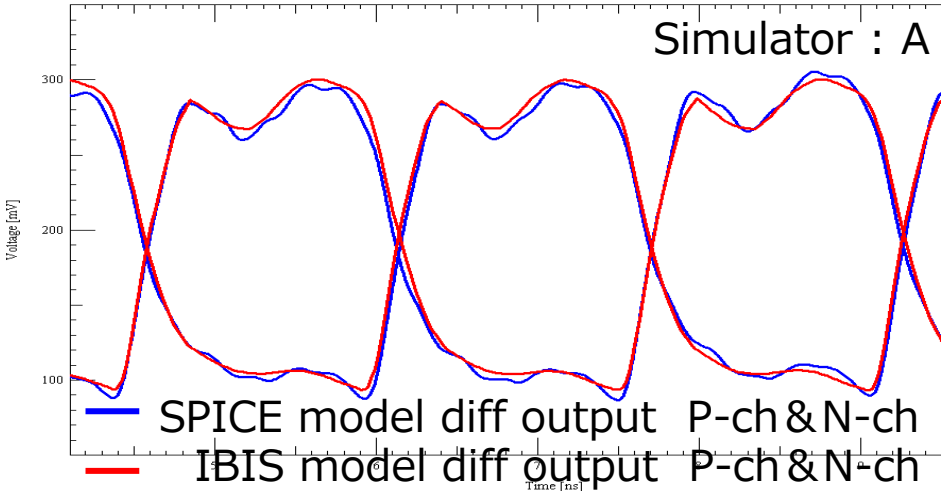


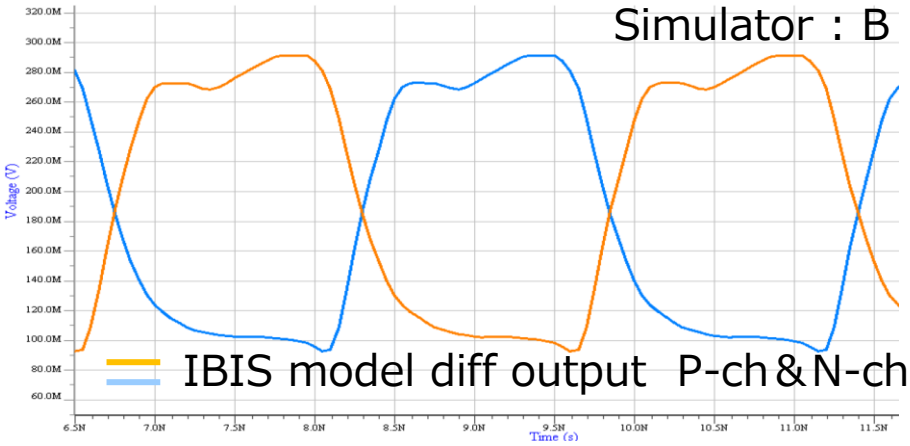
Different result simulator A and B

Remove initial delay

Removing initial delay is effective. But How we should do?



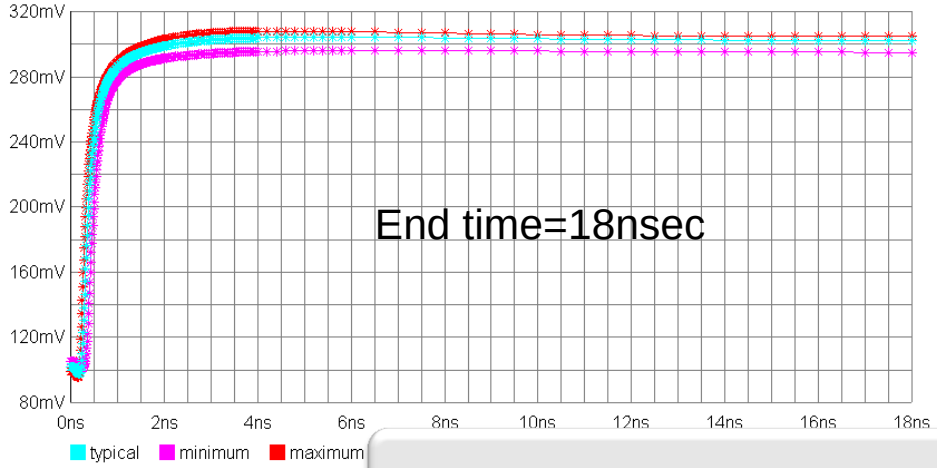


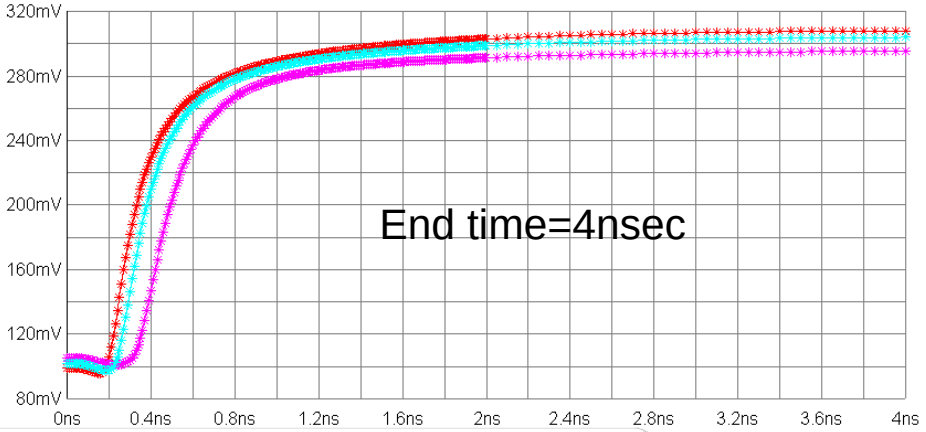


same result simulator A and B

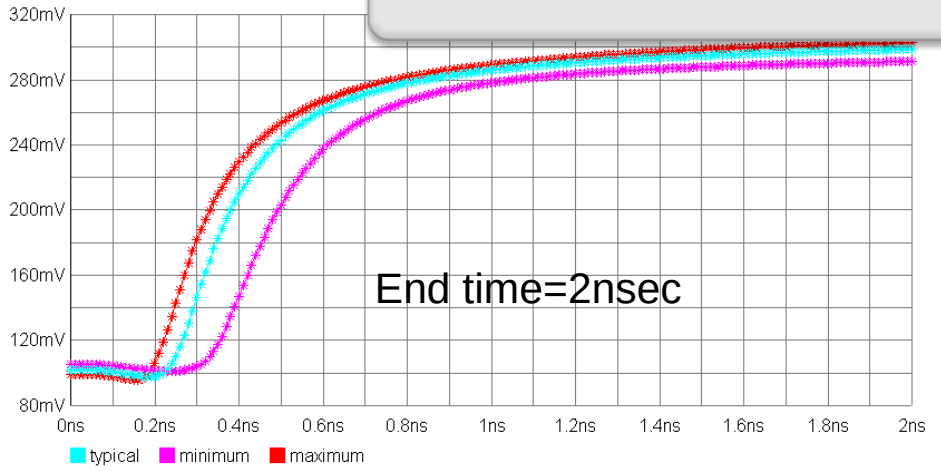
Evaluation about Cutting tail

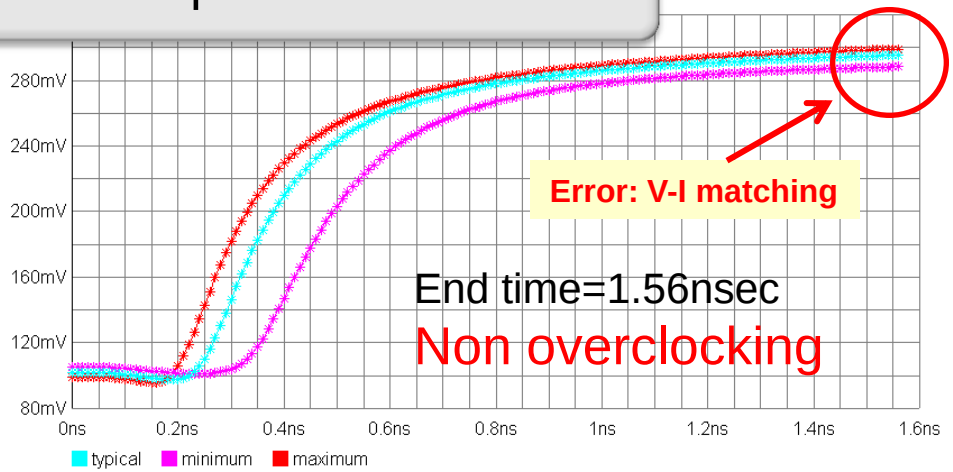
We prepared four models. All models remove initial delay.



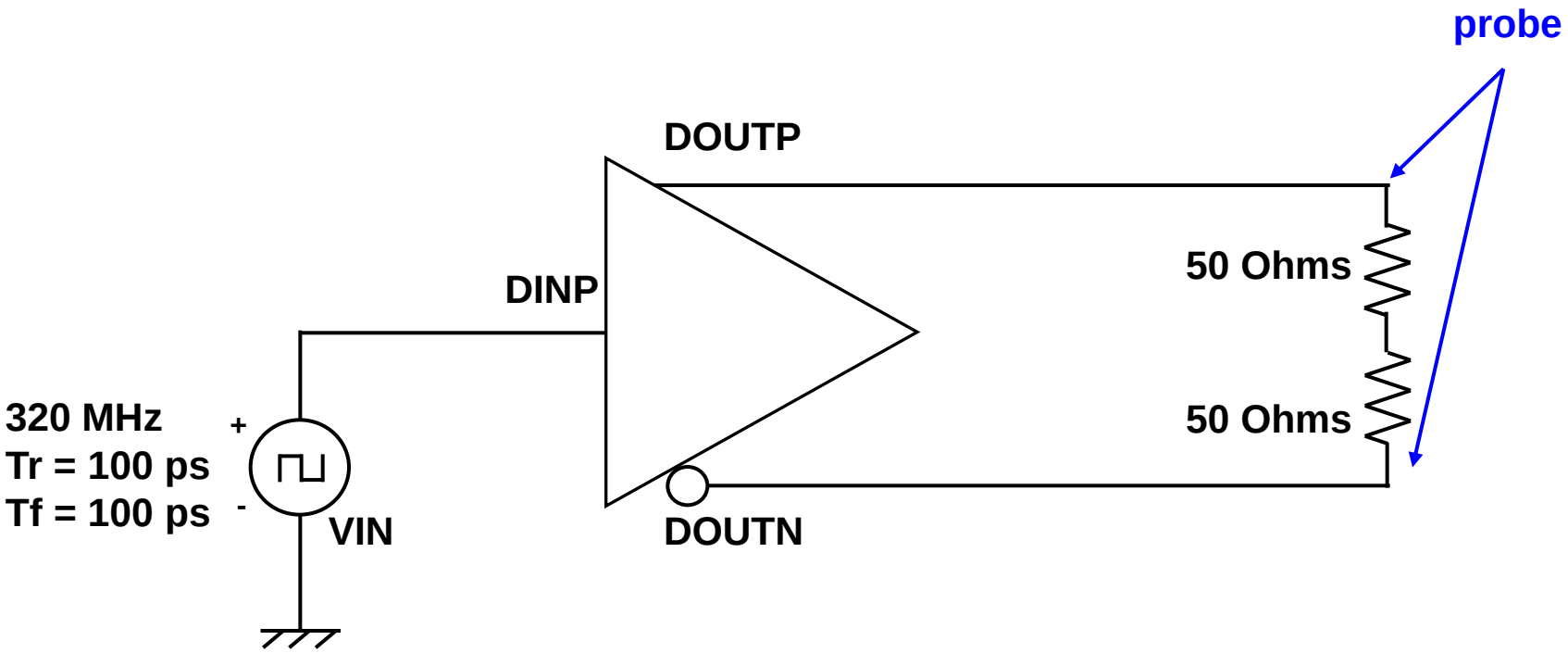


Test circuit Bitrate is 640Mbps = 1.5625nsec

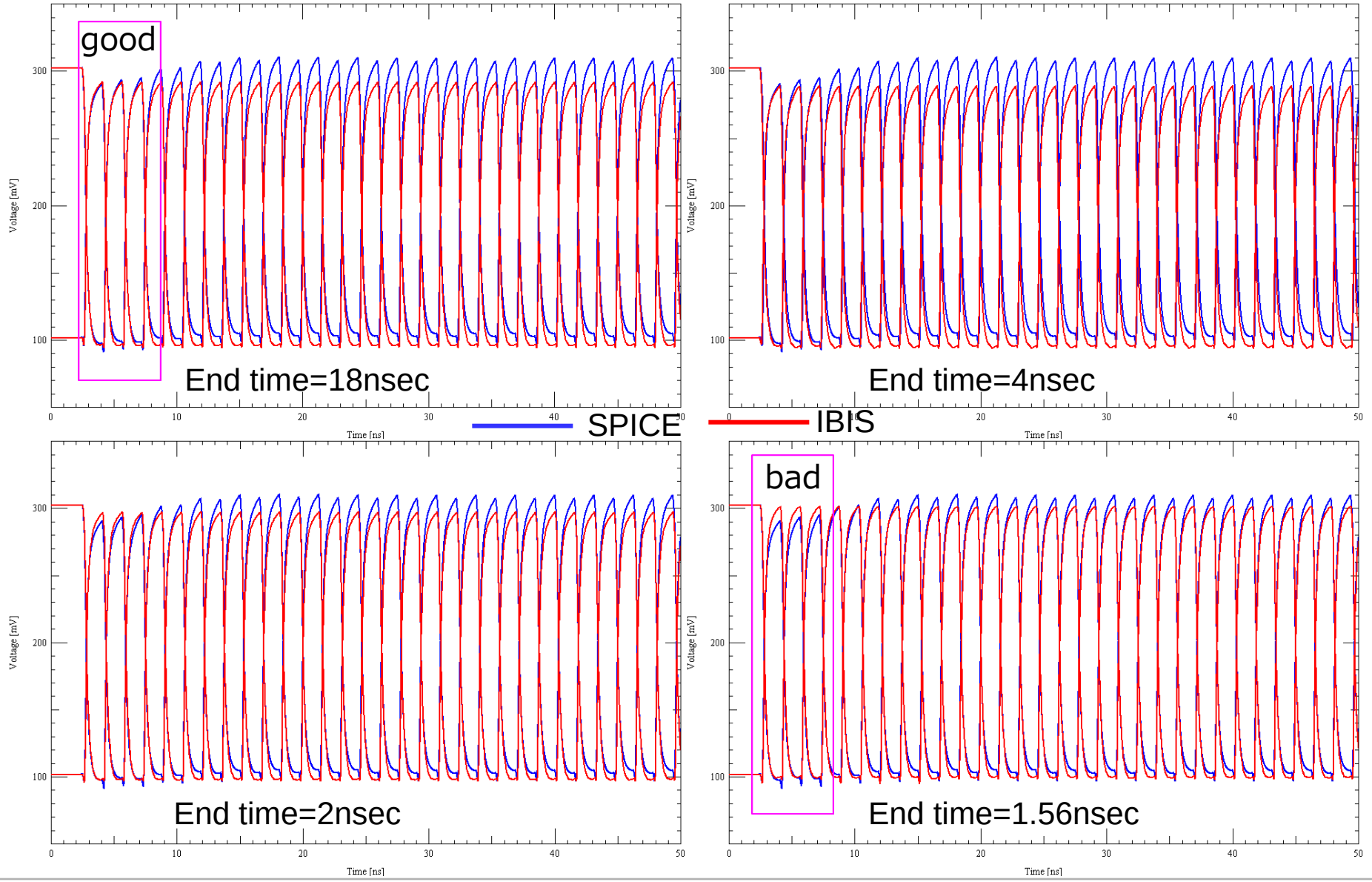




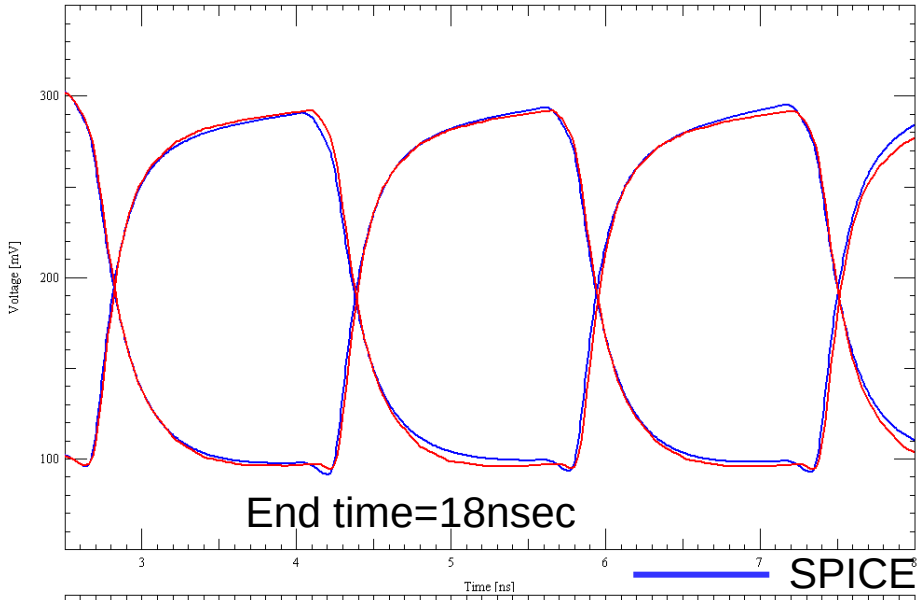
Evaluation circuit No.1

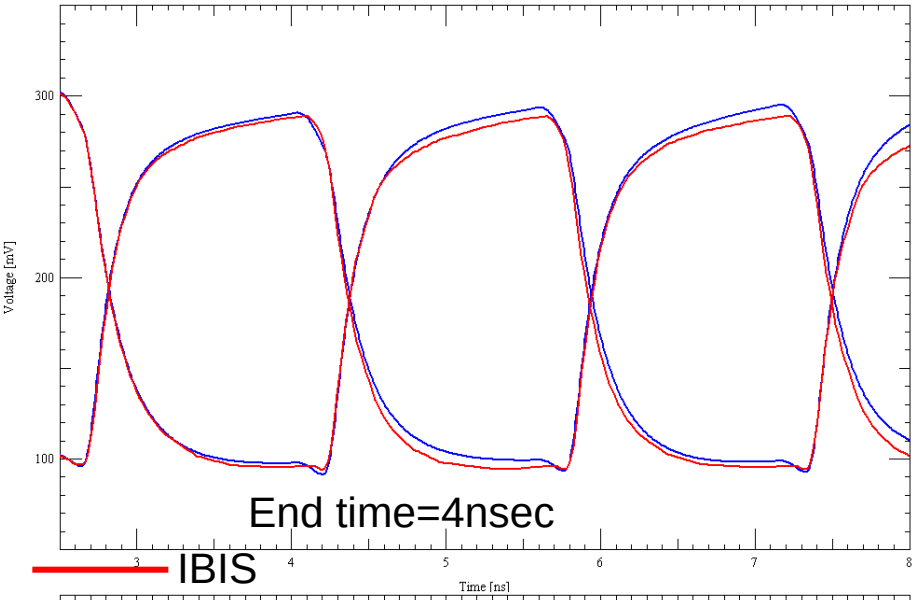


Result : Evaluation circuit No.1 (typ)

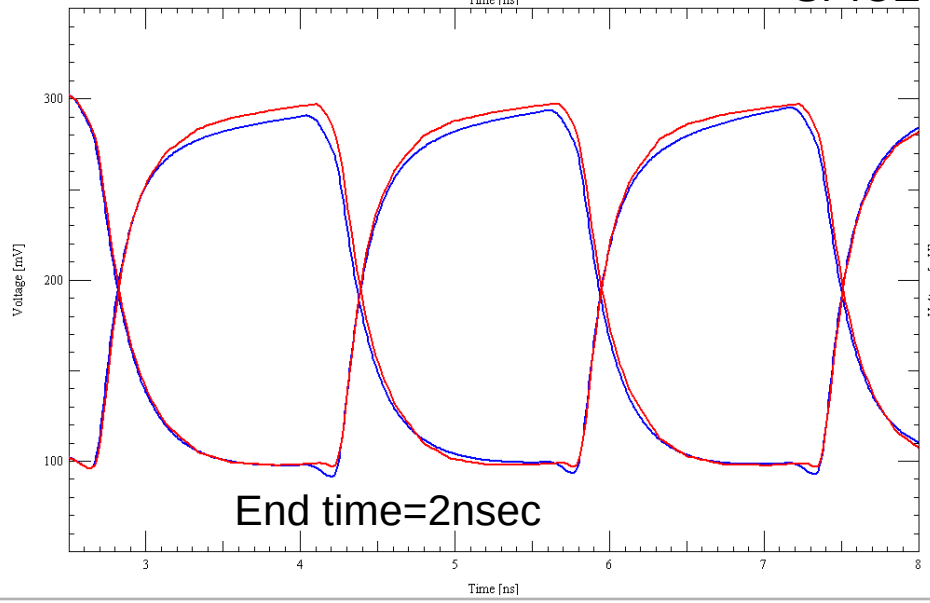


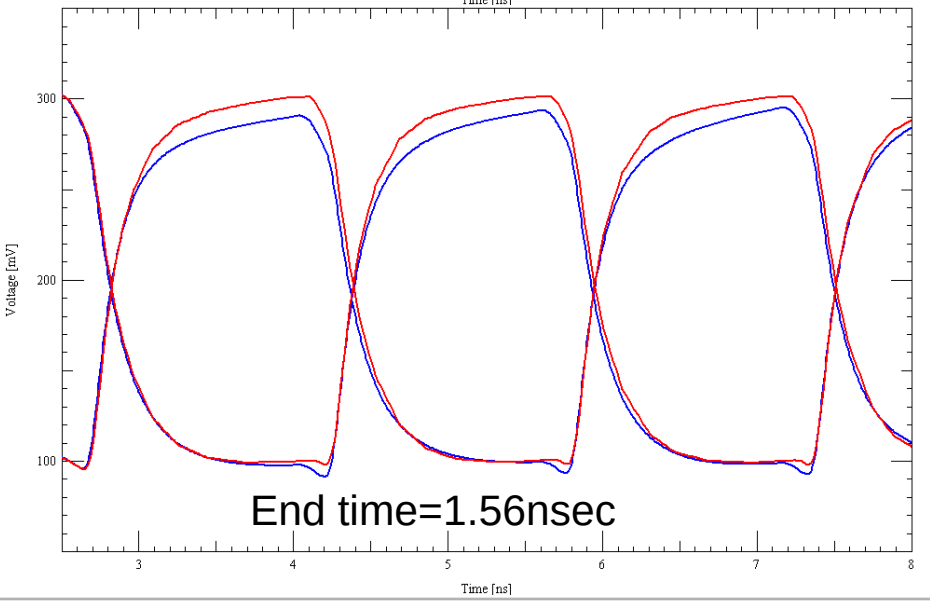
Result : Evaluation circuit No.1 （typ） Focus to first 3bits



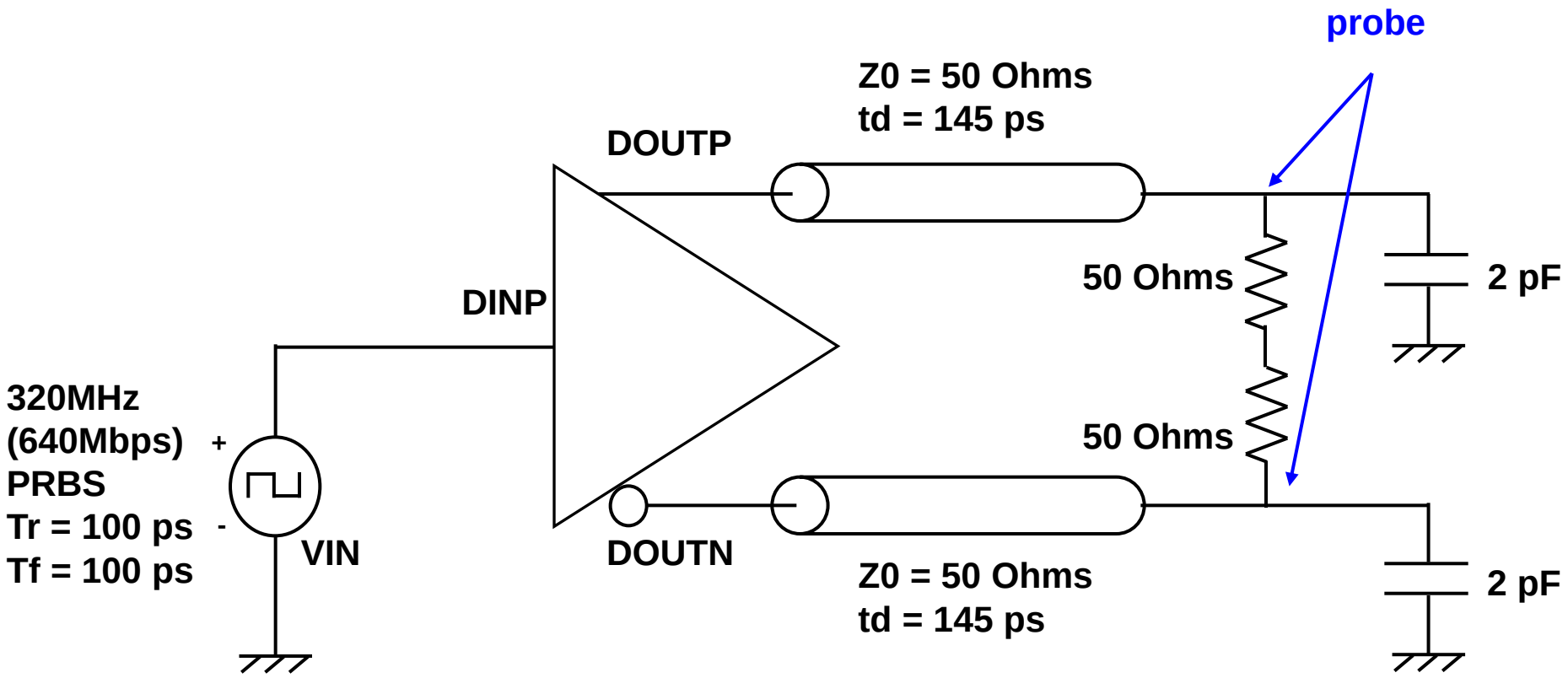


SPICE　IBIS

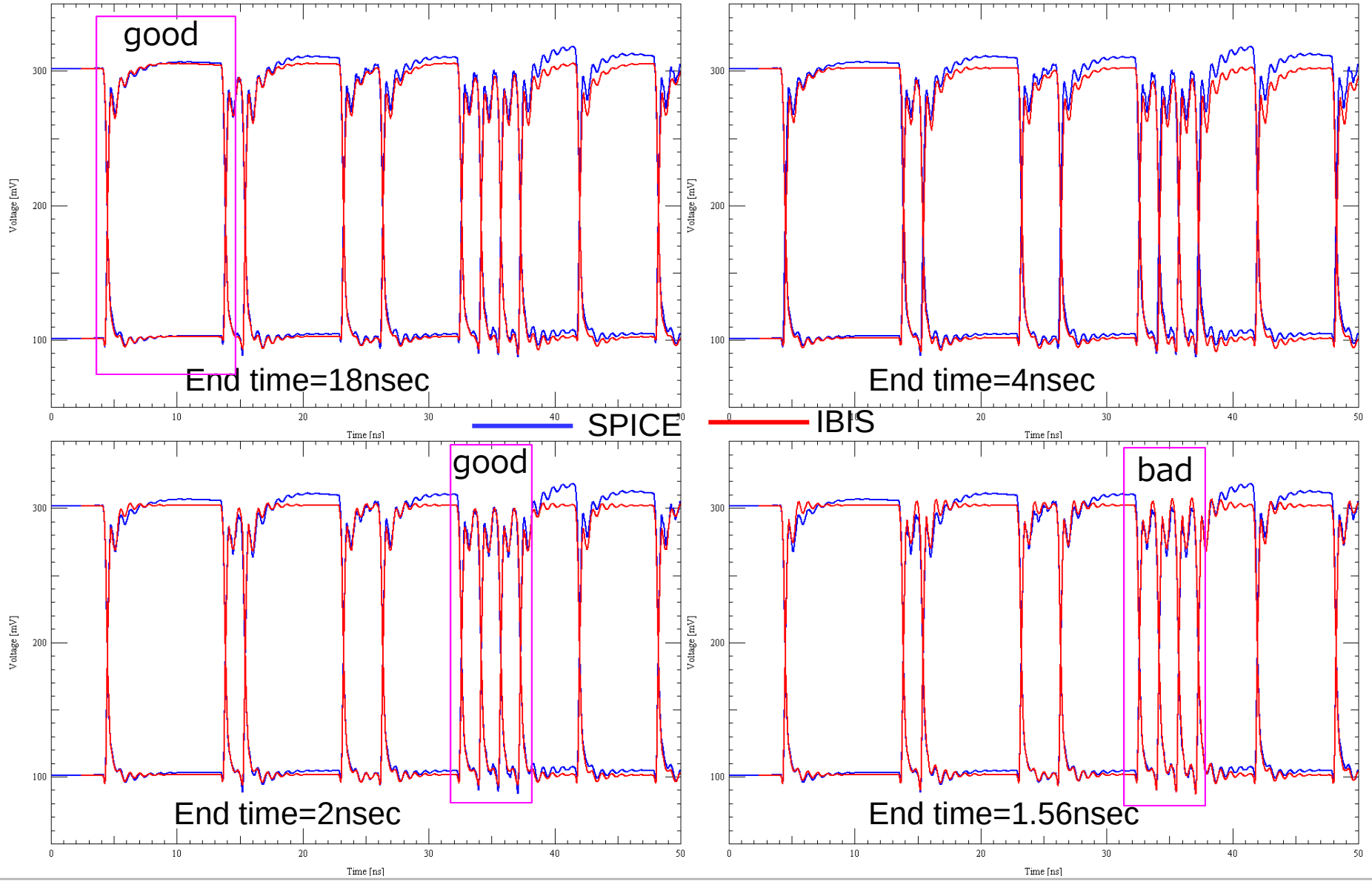




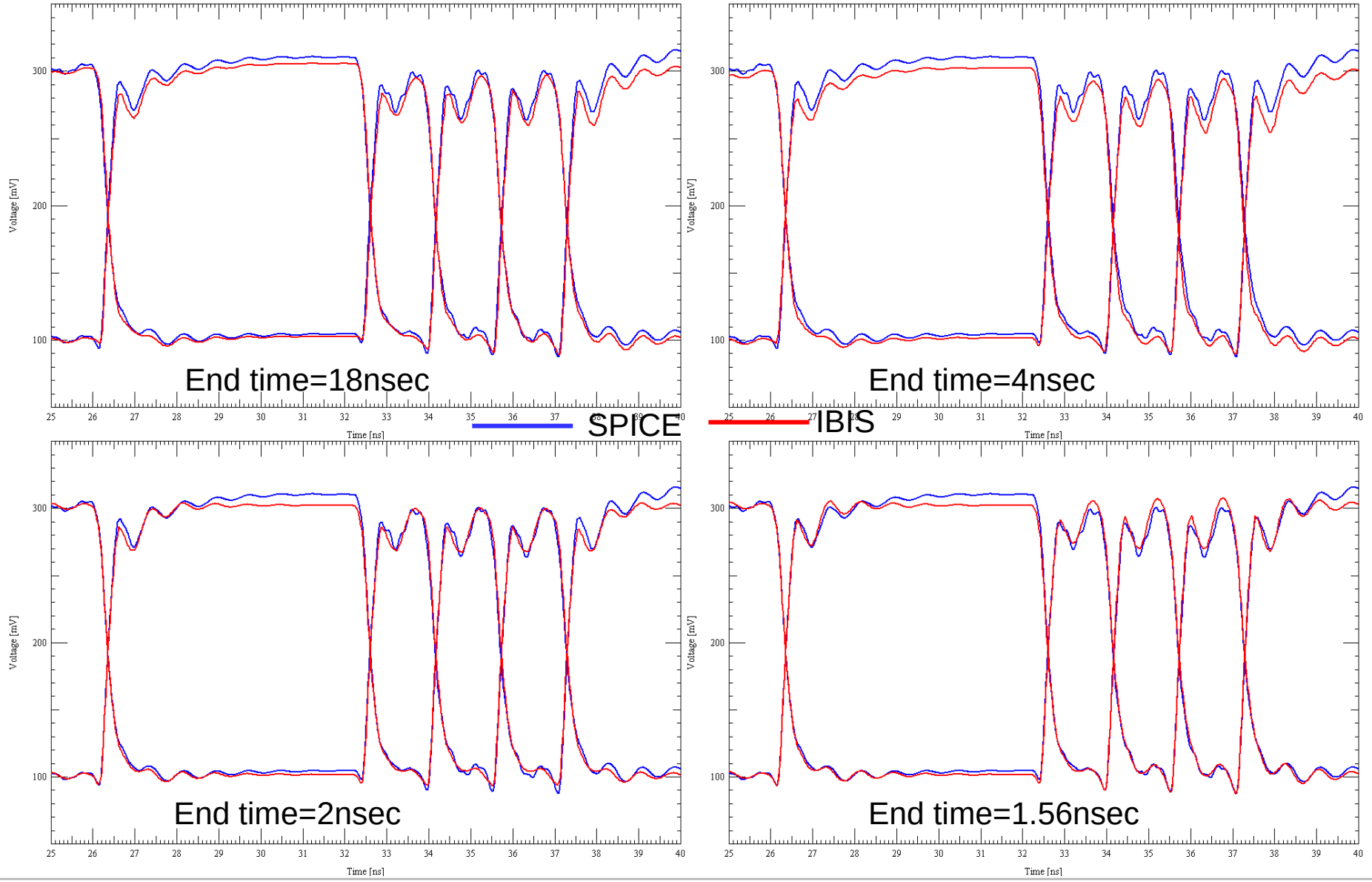
Evaluation circuit No.4



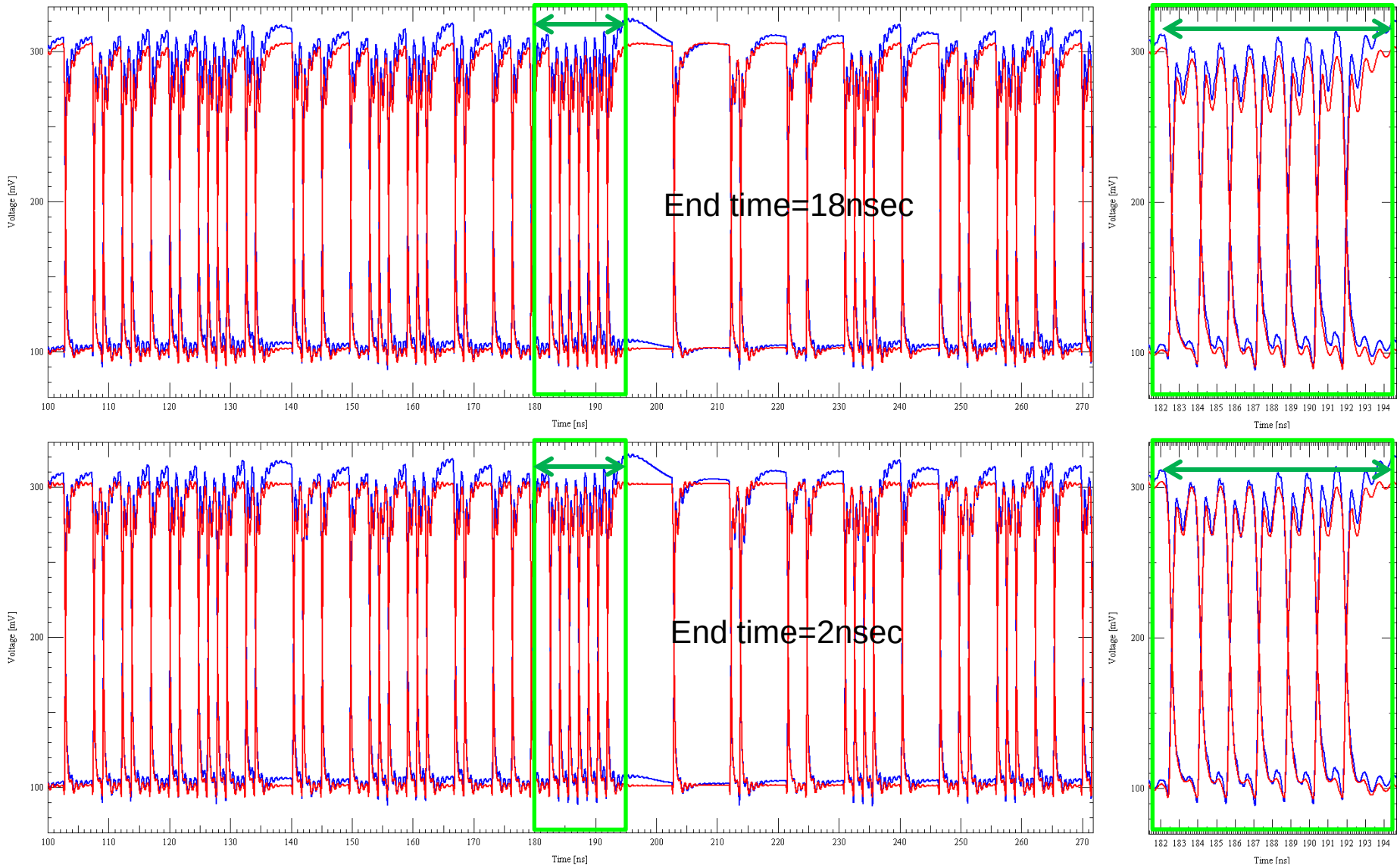
Result : Evaluation circuit No.4 (typ)



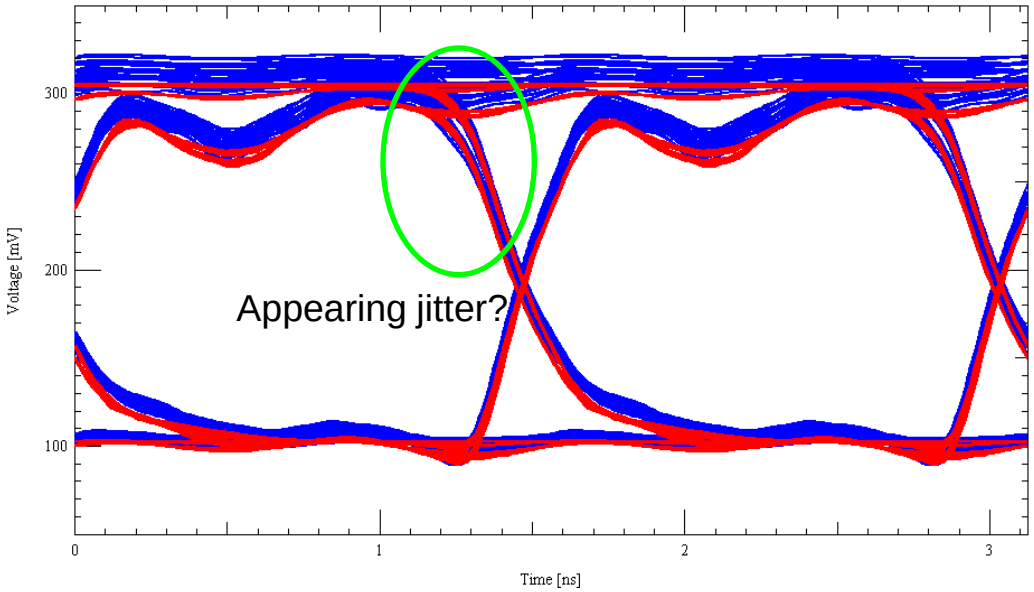
Result : Evaluation circuit No.4 (typ) Focus to fast 3bits



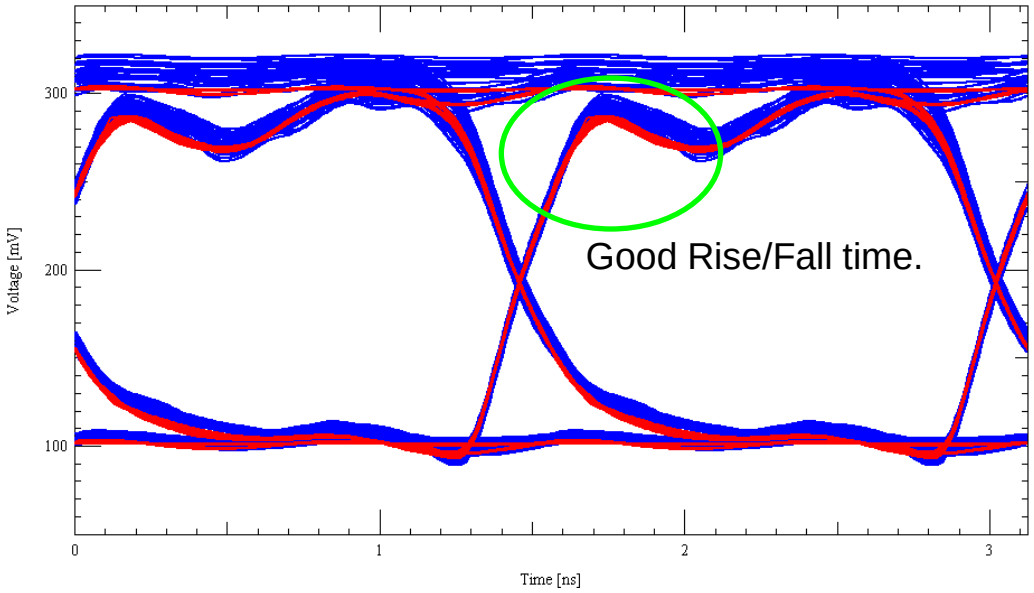
Result : Evaluation circuit No.4 （typ） long view



Result : Evaluation circuit No.4 (typ) eye-pattern



End time=18nsec



End time=2nsec

Discussion

We should improve IBIS specification.

- No-definition about shorter waveform is greatly problem.
  - → We get differential result by simulators.
    - → It is unhappy for users and creators.
      - → We should improve IBIS specification about waveform.

- By some simulators, even if it carries out neither remove initial delay nor cut tail, there are the following advantages.
  - ✓ It can express to delay of a buffer.
  - ✓ It can express to jitter of a buffer.

Suggestion

All procedure of cutting waveform should do on simulator.

- There is power supply waveform [Composite Current] in IBIS5.0.
- It is hard to create short waveform IBIS, taking time compatibility.

➢ Suggestion (as one solution)

- IBIS specification change that all procedure of cutting waveform should do on simulator.
- No-remove initial delay and no-cut tail waveform IBIS have more information than now.
- As the result does not difference between the simulator , IBIS specifications must decide the simulation method.
- This is useful also for creators also for users.

Expectations for IBIS

I want IBIS to continue to be everybody's lingua franca.

- Although the new formats such as IBIS-AMI has come out, We want IBIS to continue the environment which can do conversation.
  - A different large scale integration (LSI) maker's model can simulate in the same environment?
  - We want the viewer which can check the characteristic and a preset value.
  - Manufacturing characteristics of LSI contains really? It has not been discussed in the design value of the buffer ?

- Standards such as PCI-Express-gen3 and DDR3 is implementing a calibration value of ZQ and equalizer before communicating.
  - We hope that IBIS will automatically set the calibration value in the actual behavior.
  - We will be able to simulate more easily.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