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shaping tomorrow with you

The Application of Simulation Kit Using USB3.0 IBIS-AMI Model

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Yokohama, JAPAN
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Outline

- USB3.0 Compliance Simulation using IBIS-AMI Model
- Summary
- Expectation of IBIS-AMI

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- Expectation of IBIS-AMI

Chip-PKG-PCB Co-Design of SerDes I/F

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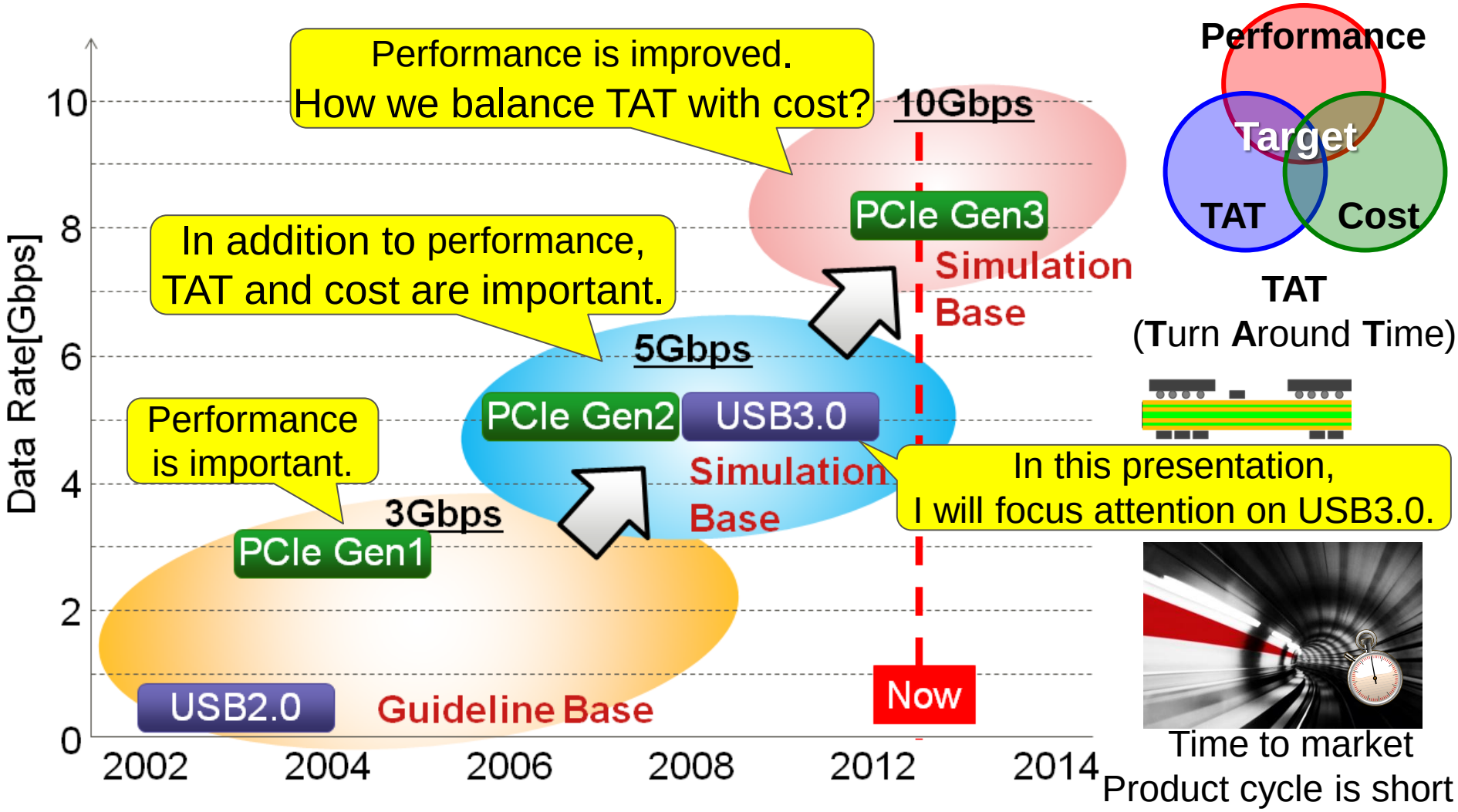
- **5Gbps SerDes I/F become prevalent, for example USB3.0.**
  - We want to bring a new product to market more quickly.



[Conclusion] : Only 0.5h for USB3.0 Analysis

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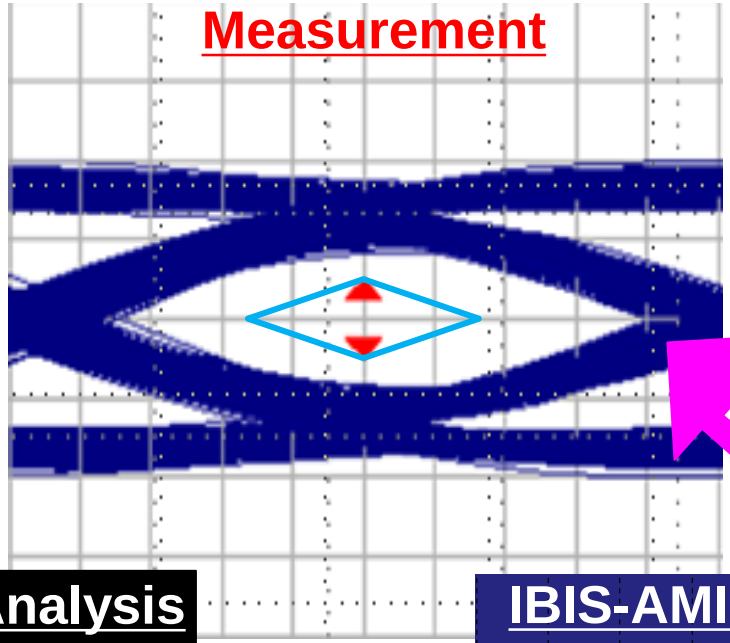
- **Measurement vs Simulation**

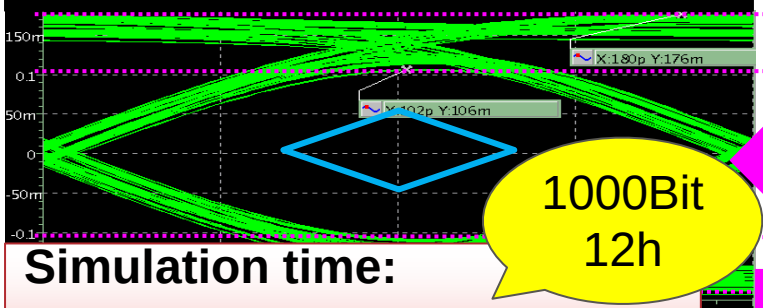
Measurement



Simulation is possible many times at the initial designing stage.

match

Spice Net Transient Analysis



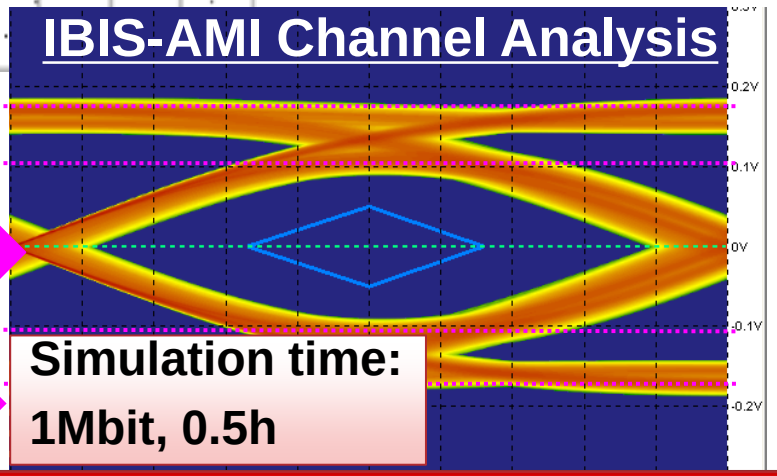
1000Bit
12h

Simulation time:
1Mbit(Conversion), 120,000h

match

1/240,000

IBIS-AMI Channel Analysis

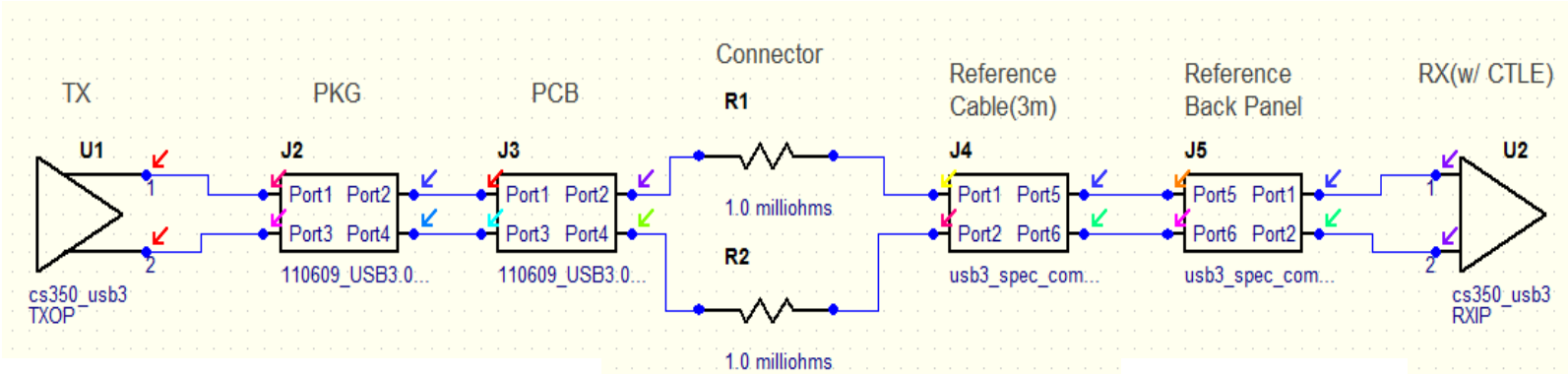


Simulation time:
1Mbit, 0.5h

IBIS-AMI enables a high accuracy and short TAT analysis.

USB3.0 Compliance Test Simulation Kit

USB3.0 Compliance Test Simulation Kit on EDA Tool



Semiconductor Vendor

(1) Simulation Kit that reflected reference design.
(4) The support of customer's difference analysis is easy.

Customer

(2) Customer can judge the quality of own design quantitatively.
(3) Customer can execute differential analysis in a short TAT. (IBIS-AMI + EDA tool)

EDA Vender

(5) EDA tool support.

Simulation Kit can prevent the troubles, for example mismatch between IBIS-AMI and EDA tool, the usage of EDA tool.

Contents of Simulation Kit

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Simulation Kit

Reference Design

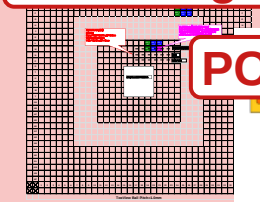
Stimulus

Bit Pattern

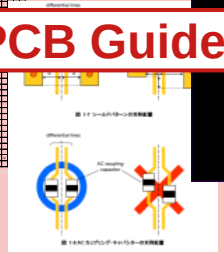
Tx Model

IBIS-AMI

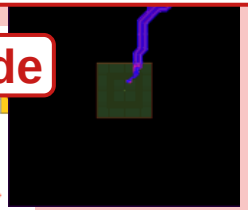
Ball Assign



PCB Guide



PCB Artwork



PKG Model

S-Para

PCB Model

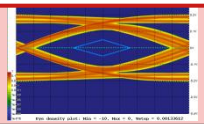
S-Para

Compliance Cable + Back Panel

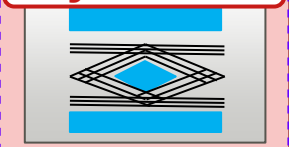
S-Para

S-Para

Sim Result



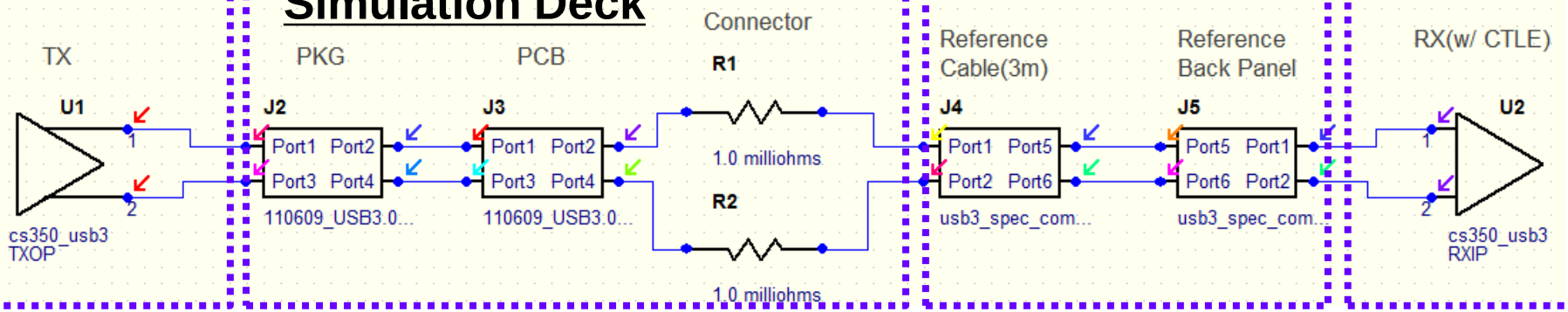
Eye Mask



Rx Model

IBIS-AMI

Simulation Deck



Compliance Test Pattern (Stimulus)

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USB3.0 Tx Compliance Test Pattern & Transmitter Eye

"Universal Serial Bus 3.0 Specification Revision 1.0"

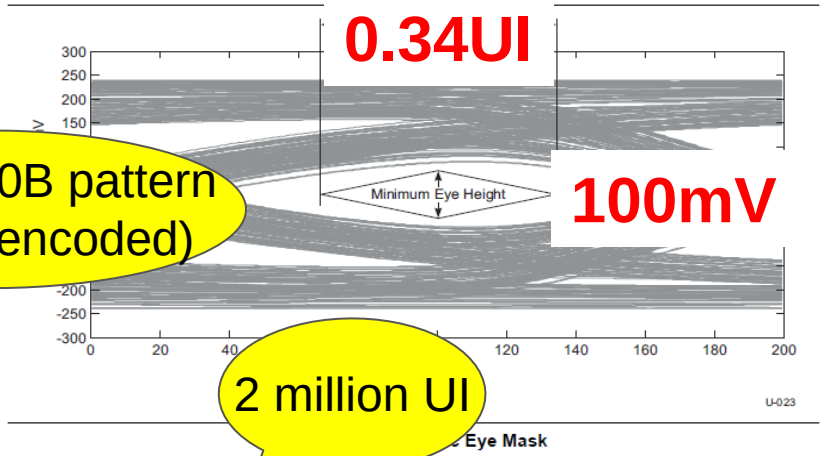
6.7.3 Transmitter Eye

The eye mask is measured using the compliance data patterns (CP0 for DJ and CP1 for RJ) as described in Section 6.4.4. Eye height is measured for 10^6 consecutive UI. Jitter is extrapolated from 10^6 UI to 10^{-12} BER.

Table 6-7. Compliance Pattern Sequences

Compliance Pattern	Value	Description
CP0	D0.0 scrambled	A pseudo-random pattern that logical idle (refer to Chapter 7) but sequences
CP1	D10.2	Nyquist frequency

CP0 : 8B/10B pattern (PRBS is encoded)



Eye Mask

2 million UI

CP1 Repeat Pattern of 0, 1

Eye Height, Jitter(10^{-12}BER) Measurement

CP0x10^6 UI + CP1x10^6 UI

about 5000 days!

Simulation time is too long in Spice Net Transient Analysis

about 0.5 hours!

Channel Analysis using IBIS-AMI

Speed up Simulation Time

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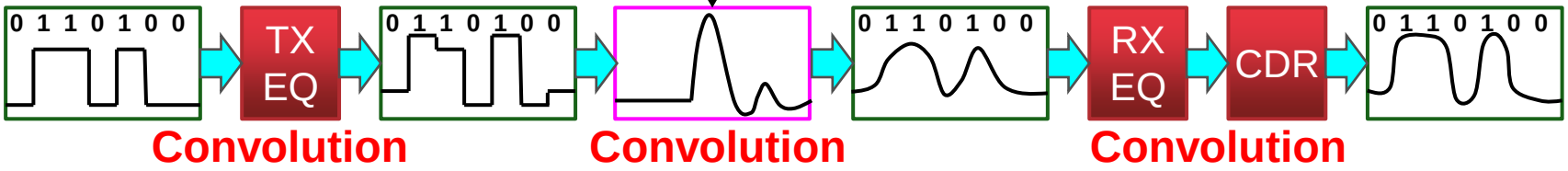
Channel Analysis

1. Analog Channel Impulse Response Process

2. Convolution Process



We can execute the analysis of 1 million bits in 0.5 hours.

Characteristic of IBIS-AMI

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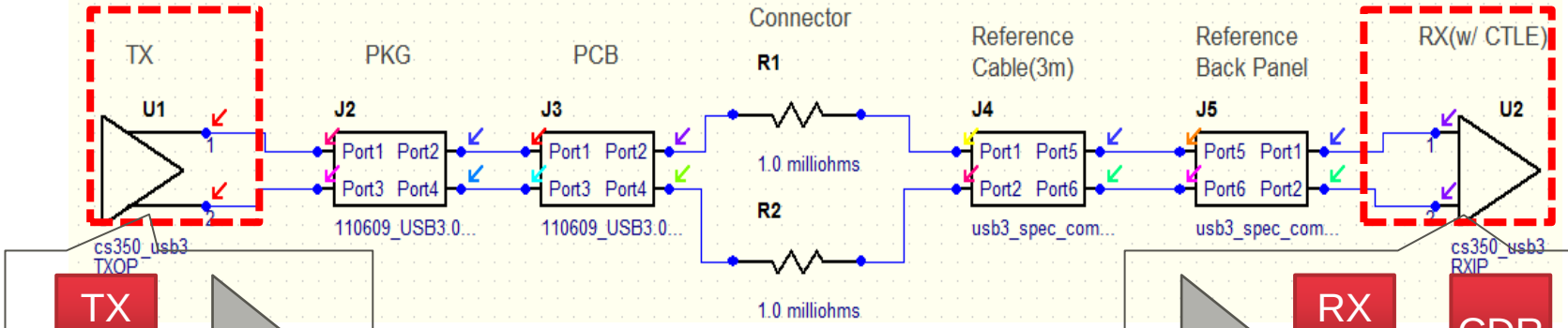
IBIS-AMI



Binary data

Binary data

[Algorithmic Model] IBIS Example
Executable Windows_VisualC_32 TX_Wx32.dll TX.ami
Executable Windows_VisualC_64 TX_Wx64.dll TX.ami
Executable Linux_gcc4.4.2_32 TX_Lx32.so TX.ami
Executable Linux_gcc4.4.2_64 TX_Lx64.so TX.ami
[End Algorithmic Model]

Windows/Linux 64bit/32bit

User can not correct IBIS-AMI, because AMI parts are black box.

Model maker should verify the quality of own IBIS-AMI.（each OS, EDA tool)

Trouble Case of IBIS-AMI Analysis (1/2)

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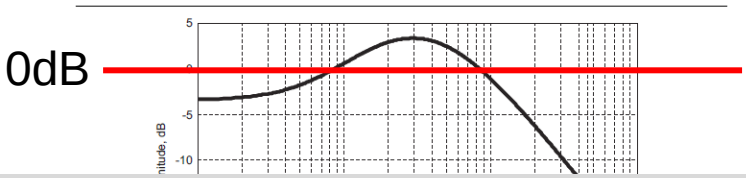
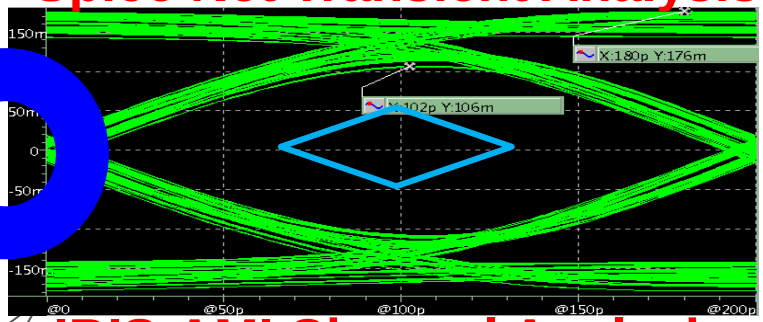
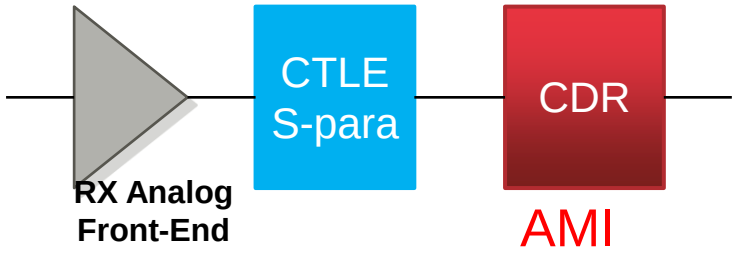
Model dependence



CTLE characteristic (Reference Equalizer)
CTLE : Continuous Time Linear Equalizer

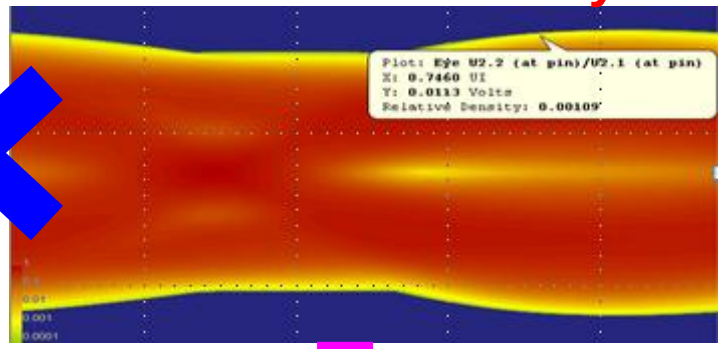
Spice Net Transient Analysis

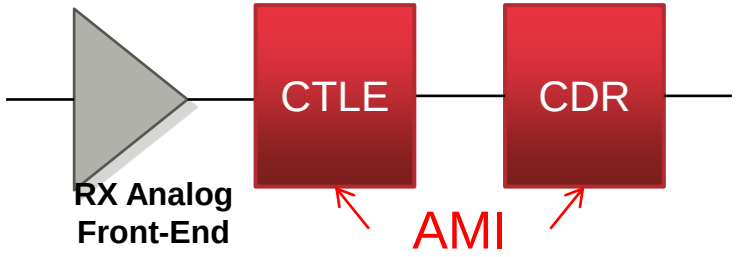




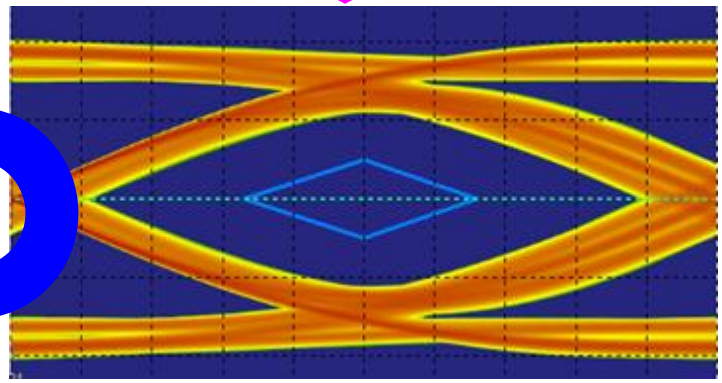
Some EDA tools are OK. Others are NG.

IBIS-AMI Channel Analysis





All EDA tools are OK.



Trouble Case of IBIS-AMI Analysis (2/2)

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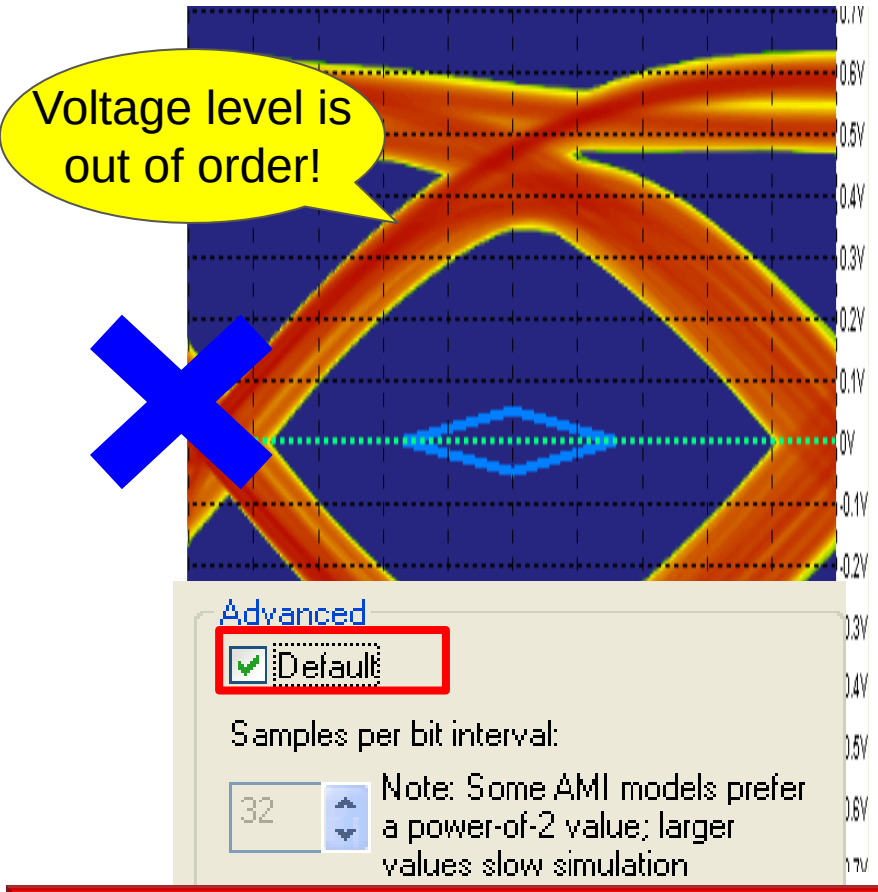
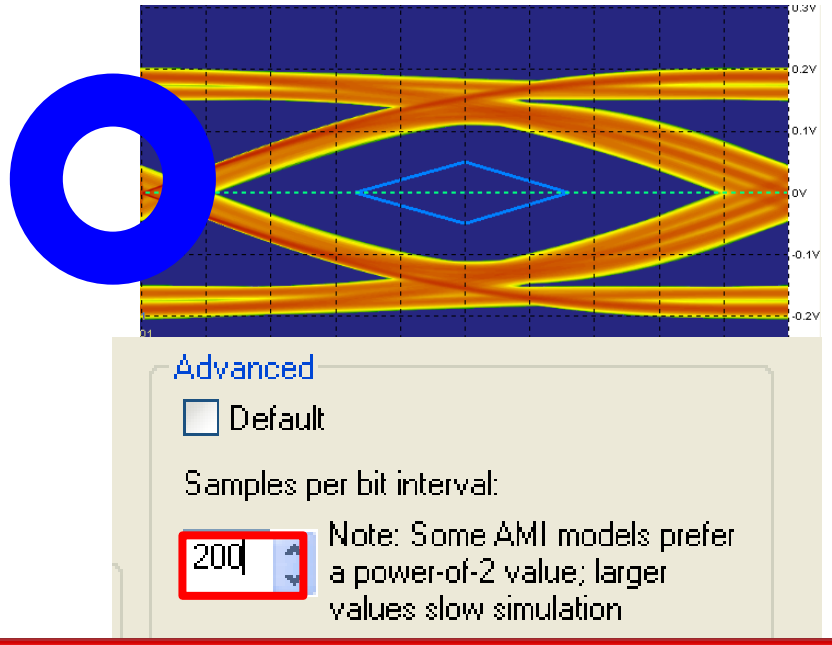
Tool dependence

Samples Per Bit Interval
=> Default Setting



Samples Per Bit Interval
=> Recommended setting

The setting value depends on modeling of IBIS-AMI.
It is necessary to use the recommended value.



It is important that IBIS-AMI model maker solve various problems of “model and tool dependence”, before model maker release it.

Reference Design (Differential Analysis)

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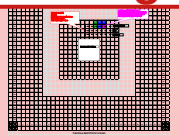
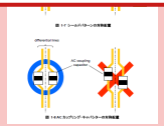
At the environment building

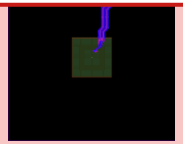
Ball Assign



PCB Guide



PCB Artwork



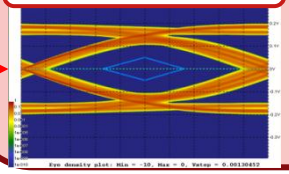
Tx/Rx Model

IBIS-AMI

Reference Cable+BP

S-Para

Sim Result



PKG Model

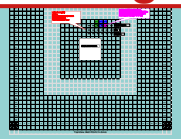
S-Para

PCB Model

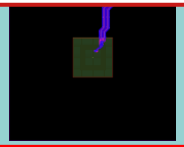
S-Para

At the actual design

Ball Assign'



PCB Artwork'



Customer Design

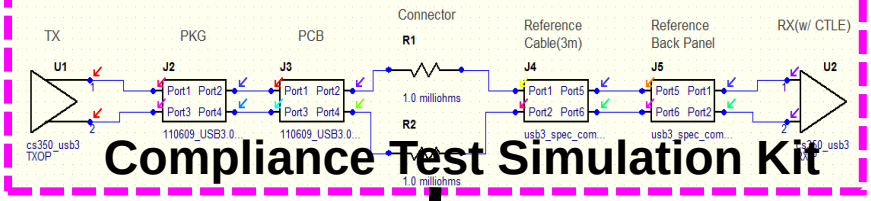
PKG Model'

S-Para

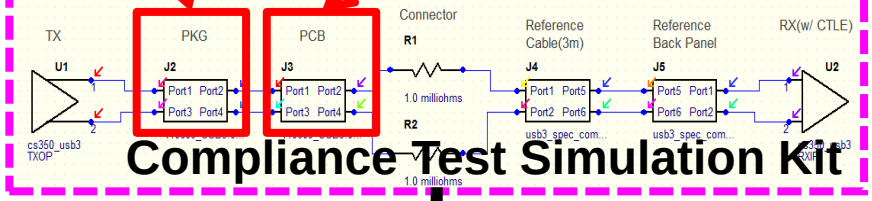
PCB Model'

S-Para

Assign

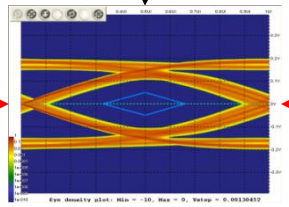


Compliance Test Simulation Kit



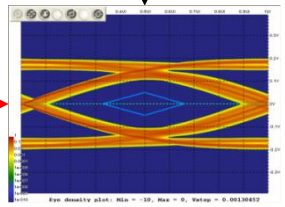
Compliance Test Simulation Kit

Compare



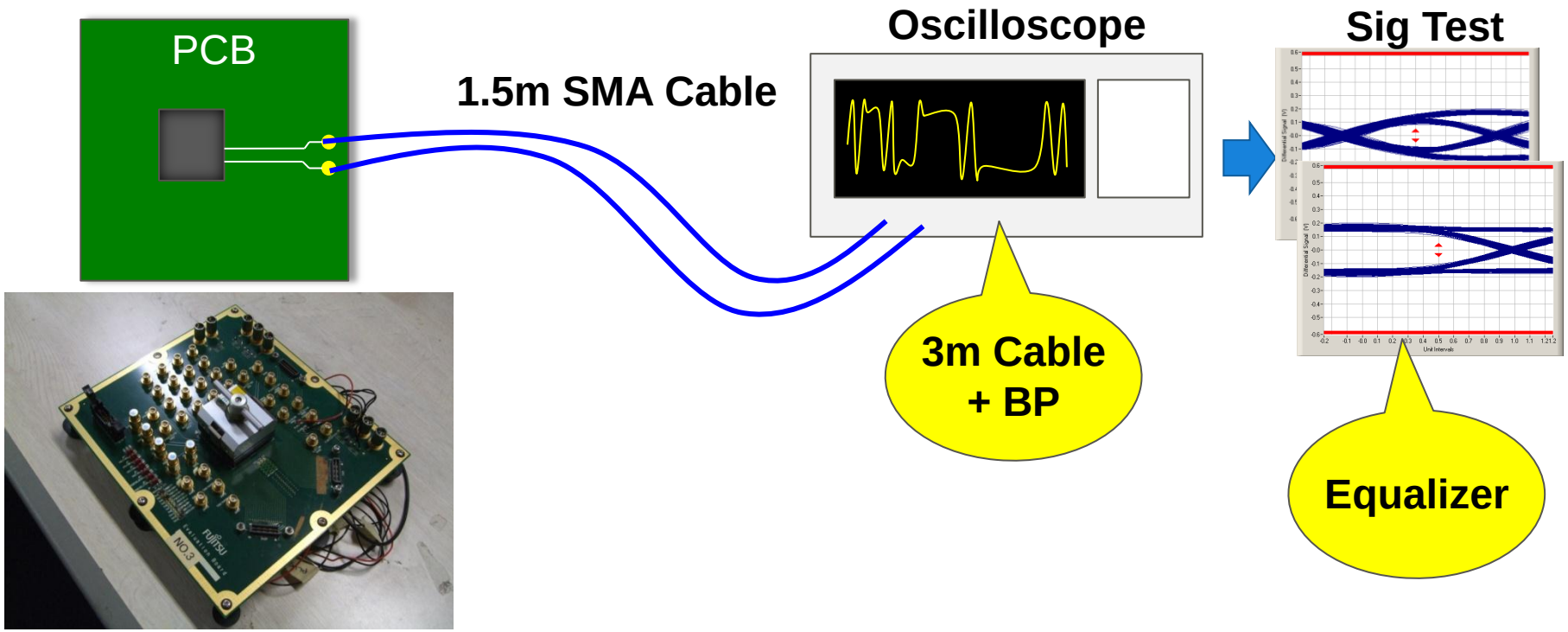
Compare

Differential Analysis



Measurement Correlation (1/2)

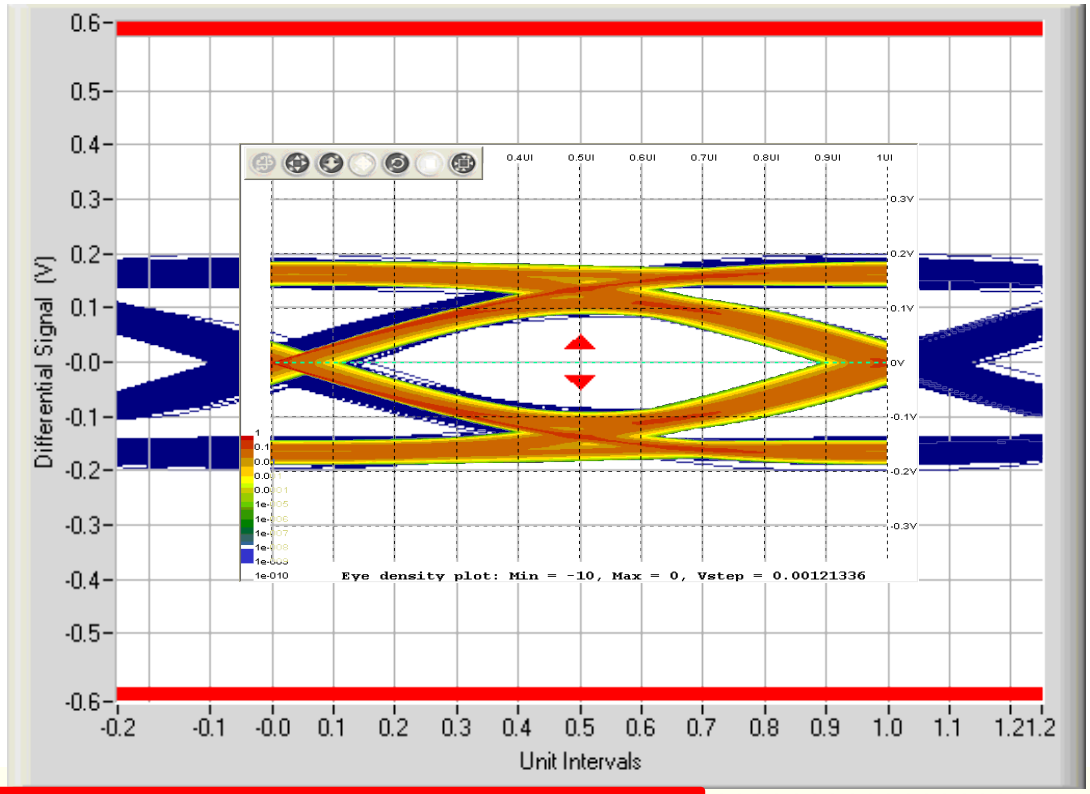
Measurement environment

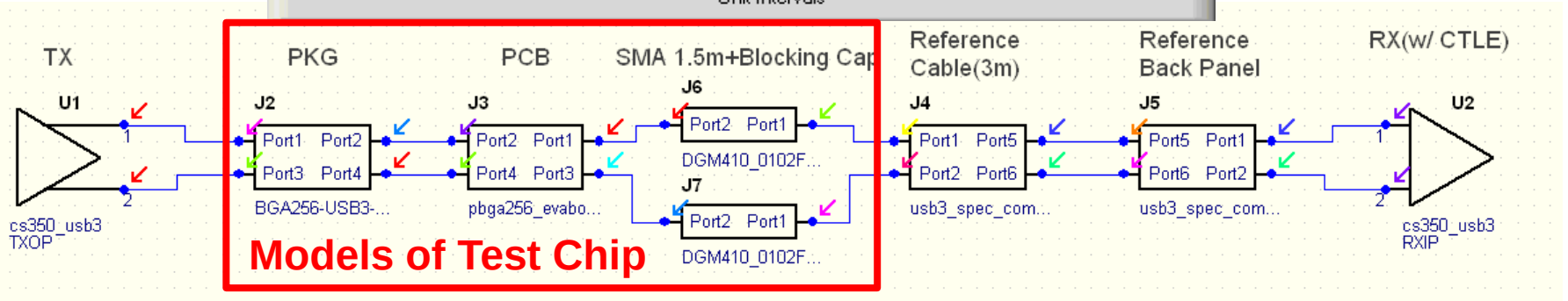


Item	Comment
CHIP	USB3.0 Test Chip
PKG	Wire Bond BGA 4layer 256ball 27mm-square
PCB	6layer
PVT	Typical

Measurement Correlation (2/2)

Measurement vs Simulation





Application：Cost Reduction Study

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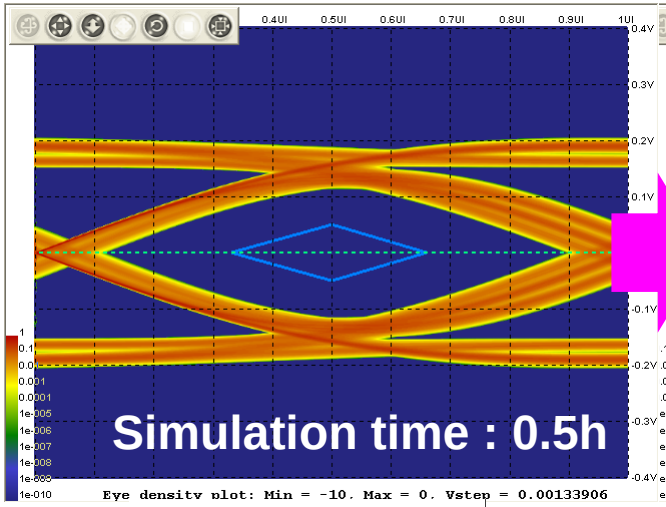
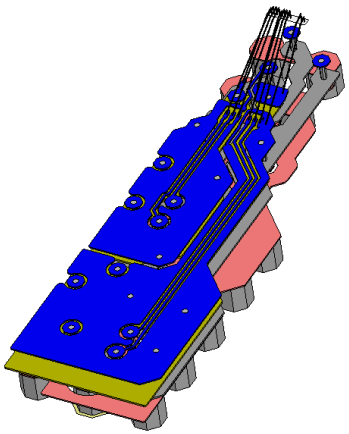
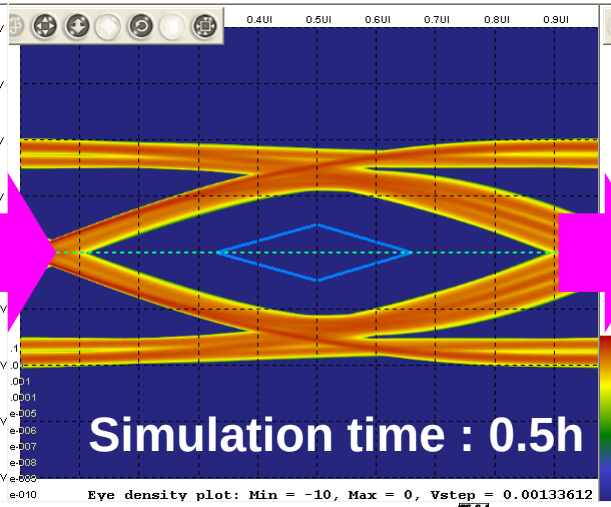
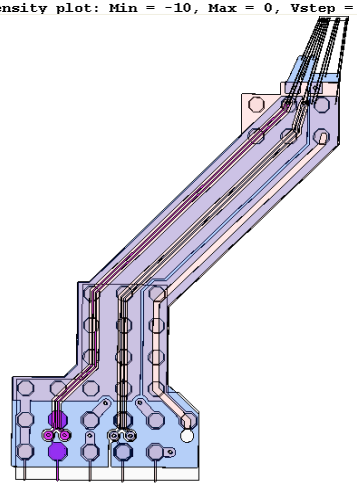
PBGA 4layer



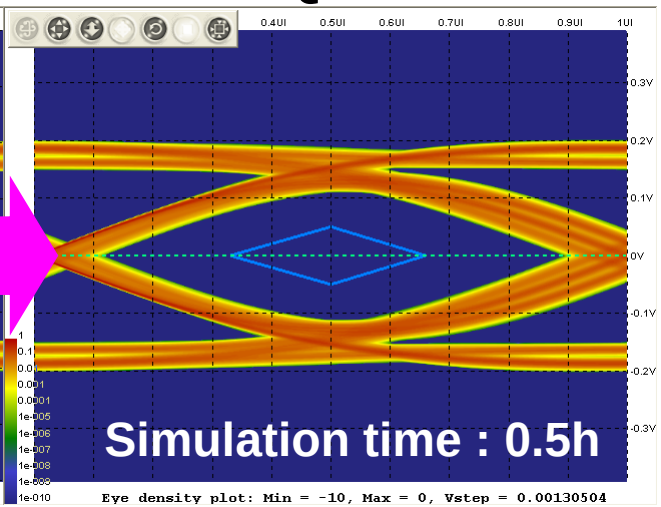


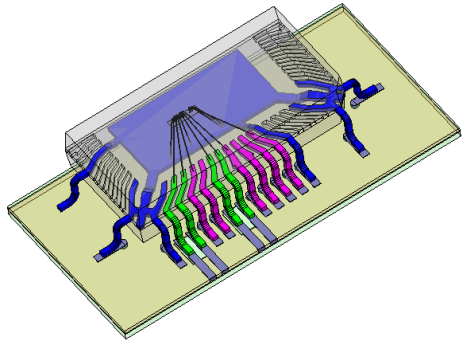
PBGA 2layer





LQFP





We can examine cost reduction of the product by using Simulation Kit in a short TAT.

Outline

- USB3.0 Compliance Simulation using IBIS-AMI Model
- Summary
- Expectation of IBIS-AMI

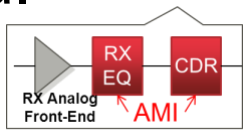
Summary

USB3.0 Compliance Simulation using IBIS-AMI Model

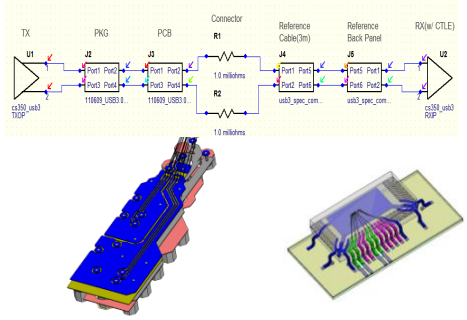
- IBIS-AMI is a key technology of 5Gbps SerDes I/F analysis.
  - High accuracy
  - Short TAT

USB3.0

- It is important that IBIS-AMI model maker solve various problems between IBIS-AMI and EDA tool beforehand.



- Simulation Kit constructed on EDA tool is able to contribute to short TAT analysis and cost reduction of the product.



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Expectation of IBIS-AMI

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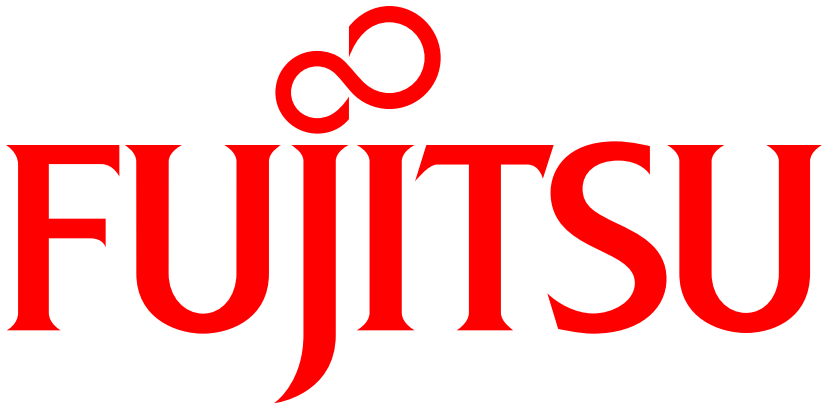
- We expect more information about IBIS-AMI.
  - Documents (IBIS-AMI Cookbook, Trouble shooting)
  - Samples (IBIS-AMI, Simulation result)
  - Visualization (EQ Characteristic)



shaping tomorrow with you