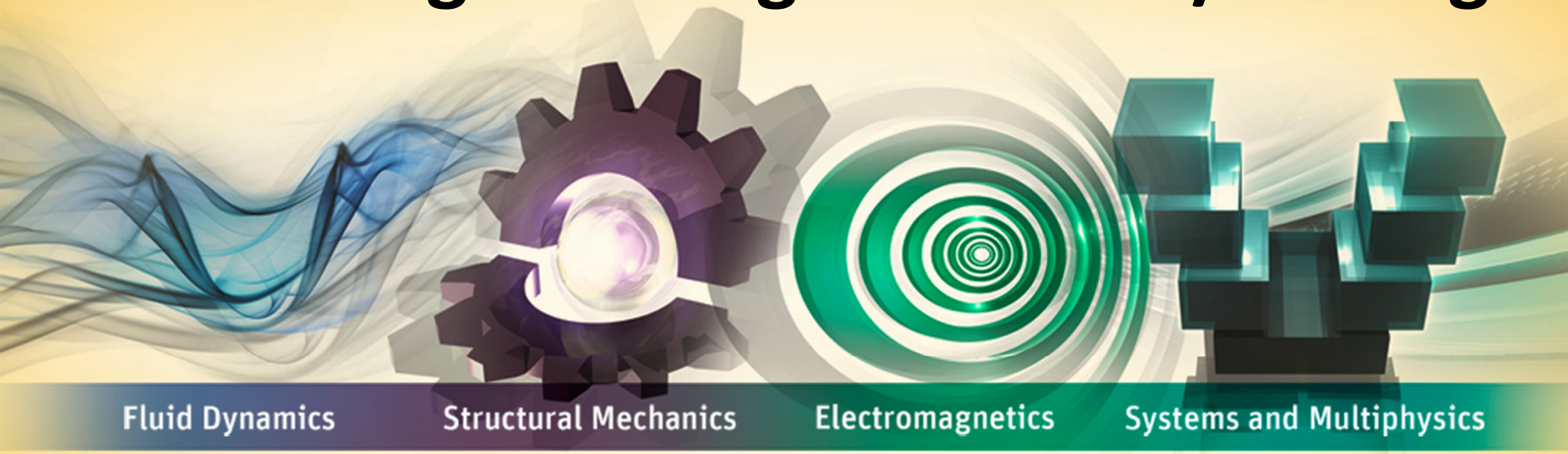
ANSYS

Realize Your Product Promise™

The Evolution of DDR Memory and Overcoming Challenges of DDR3/4 Design

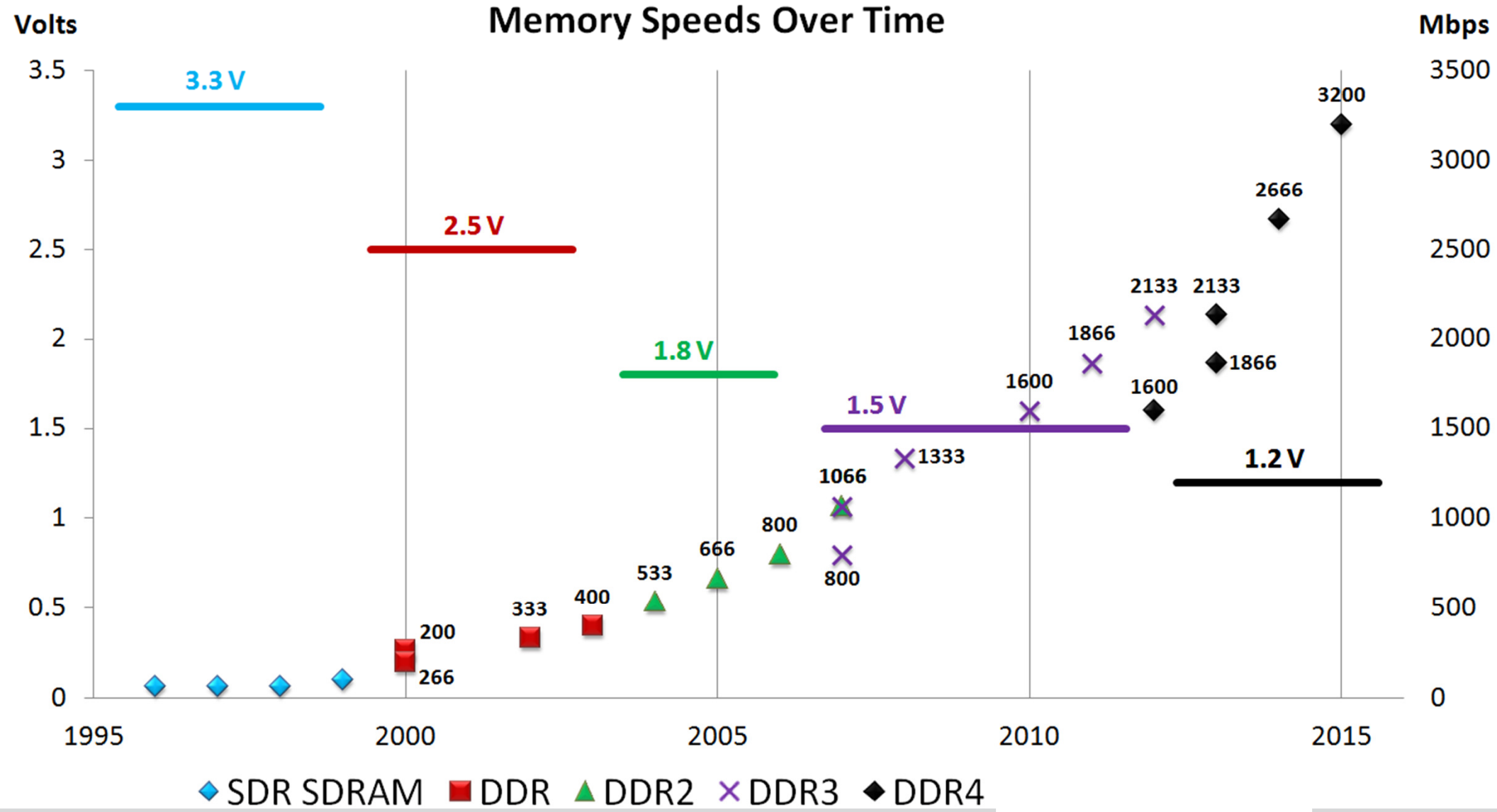


Asian IBIS Summit
Hsinchu, Taiwan
November 13, 2012

Steven G. Pytel, PhD.

SI Product Manager

Memory Speeds Over Time



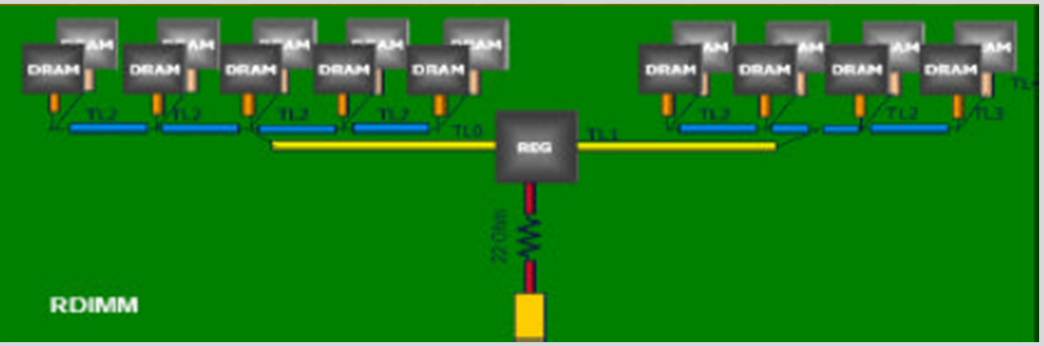
DDR4

- JEDEC recently announced the DDR4 standard
  - September 25th, 2012
  - JESD79-4

- Major Implications:
  - Point to Point Architecture
  - x4, x8, and x16 supported
  - 2GB to 16 GB SDRAMs
  - 1.2 V system
    - Vrefdq – on die reference voltage for DDR4
    - Up to 40 % reduction in power
    - Pseudo Open Drain Silicon architecture vs. push/pull
      - Pulled to Vdd thereby only drive low to zero
  - Data bus inversion
    - Limits # of SSO at a single time to improve SI and reduce power
  - Write leveling for CMD/ADD, CNTL and CLKs to control skew due to Fly-by topology
  - Server design
    - Distributed buffers for each byte lane compared to single buffer for all 64 bits
    - Point to Point topology requiring a switch between DIMMs
  - Support for Chip Stacking
    - TSV Supported architectures for SDRAMs

T-topology vs. Fly-by topology

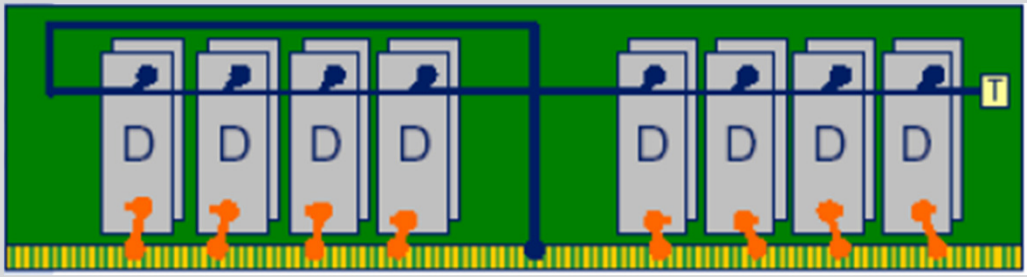
DDR2 T-topology



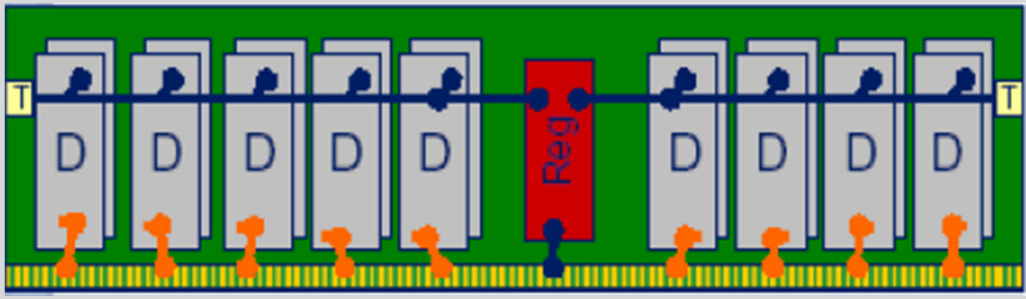
DDR2 RDIMM

Clock arriving time to all DRAMS
on a DIMM are expected to be the same

DDR3 Fly-by topology



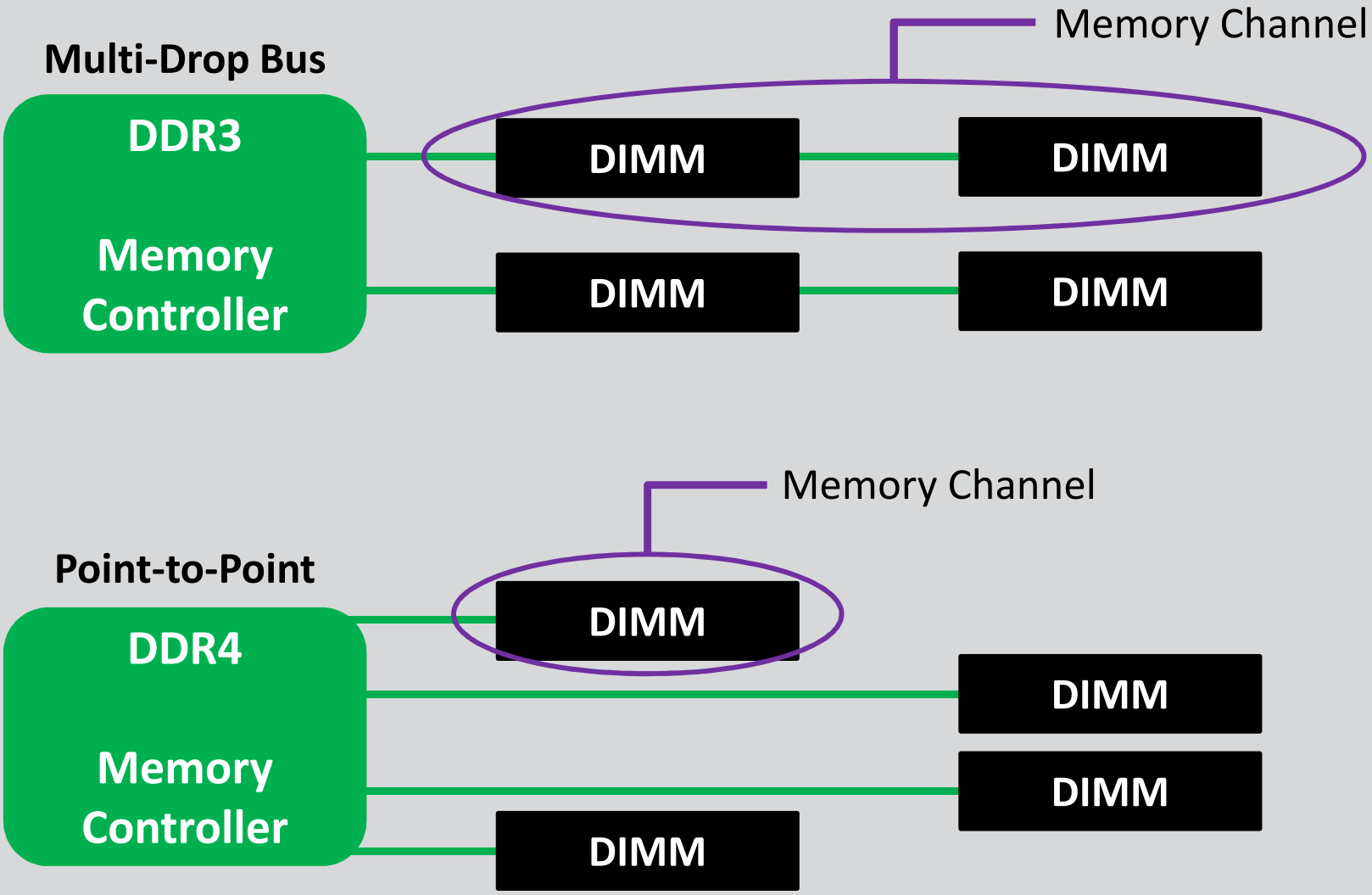
DDR3 UDIMM



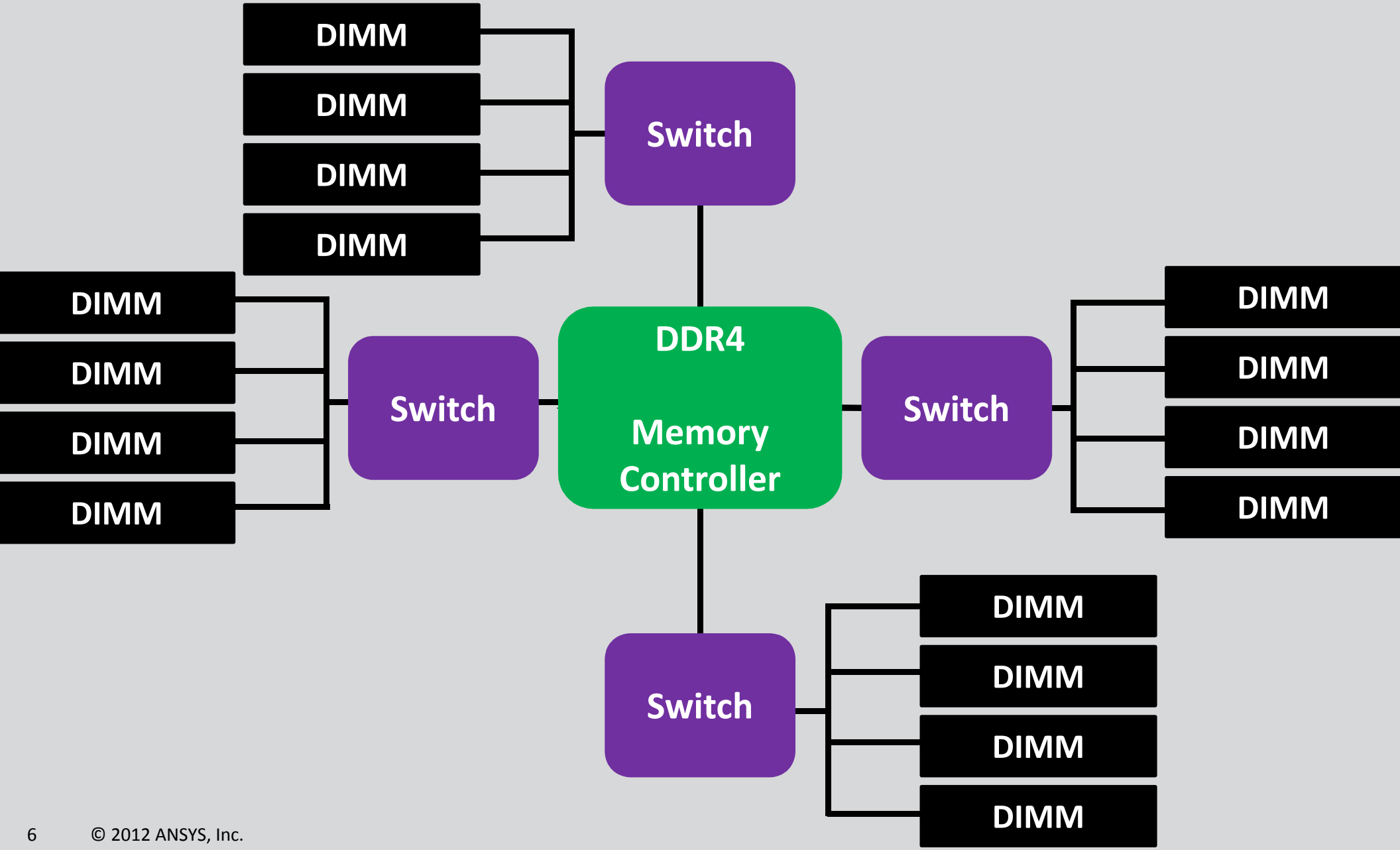
DDR3 RDIMM

Clock arriving time to each DRAM
on a DIMM are different

Point to Point vs. Multi-Drop

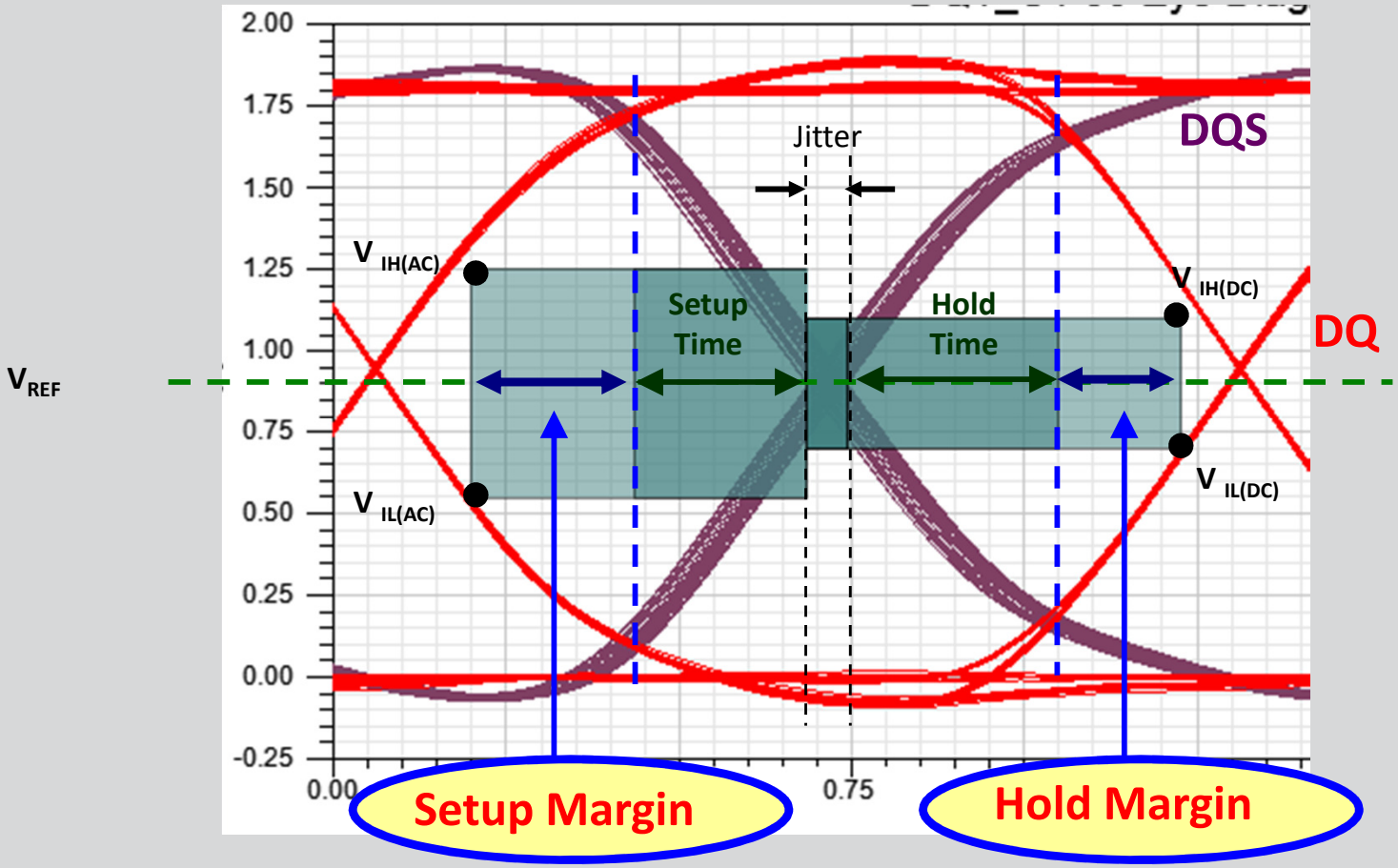


Server Architecture with Switches



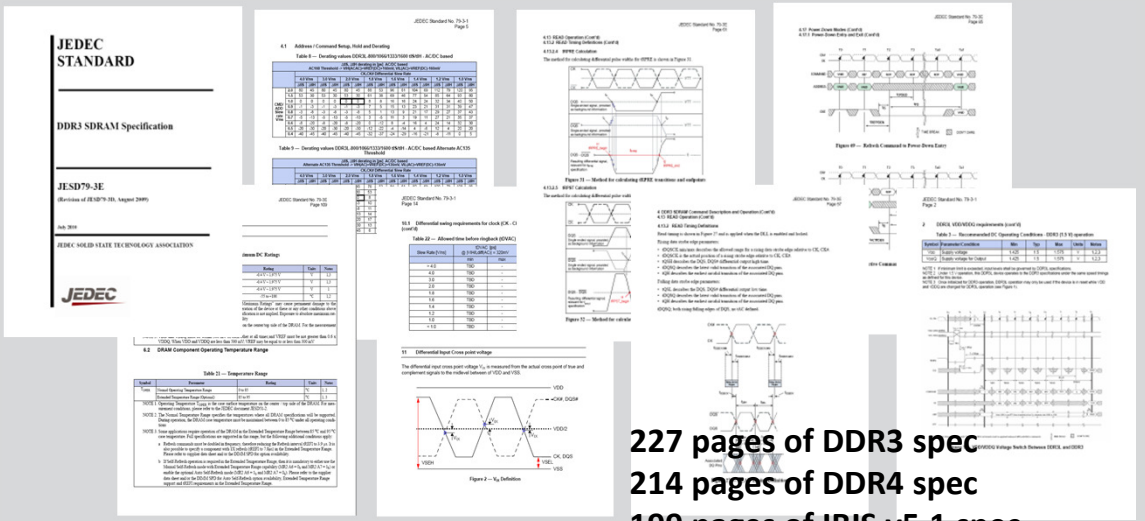
DDR 3 Key Spec

Setup Margin & Hold Margin



DDRX Technology & Challenges

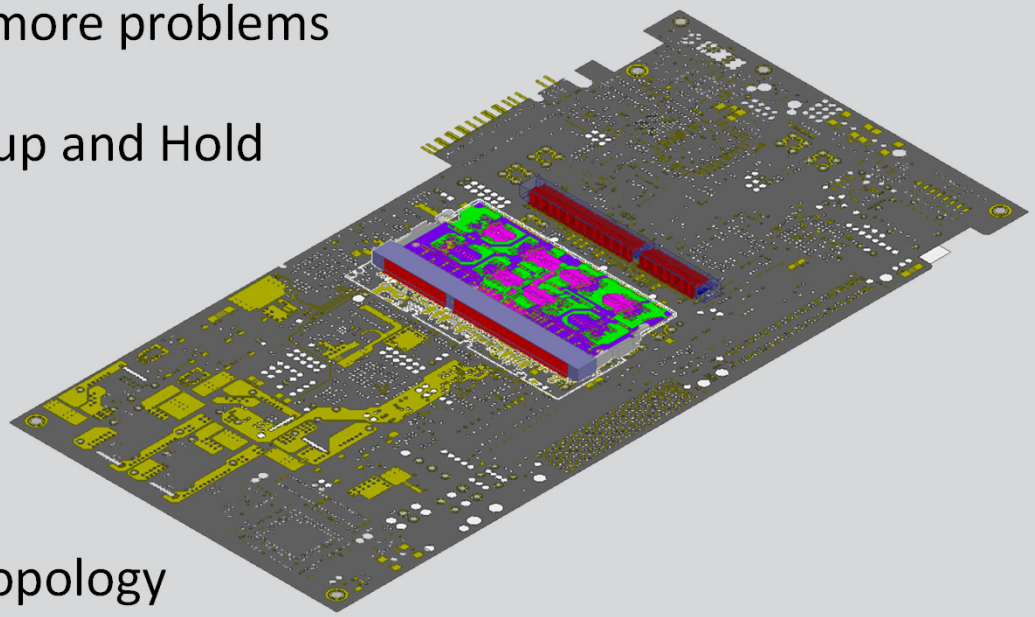
- Design challenges?
  - Validation
    - Prototype
    - Measurement
    - Interpret and implementation(calculation) of Design Spec such as DDR3/4, LPDDR2/3 and more…
    - Large amount output data report of results
  - Capacity or Complexity and Time
    - Chip to Chip or Chip to PKG
    - Chip + Package + PCB + Connector/Cable + PCB + Package + Chip
    - Full System



227 pages of DDR3 spec
214 pages of DDR4 spec
199 pages of IBIS v5.1 spec

DDRX Technology & Challenges

1. Higher Speeds
   - 66 Mbps to 3200 Mbps and beyond
   - Higher speed and edge rates cause more problems with skew, coupling, radiation, etc…
   - Timing margins become tighter; Setup and Hold timings
     - DDR 400 has a window of 2.5 ps
     - DDR4 3200 has a window of 312.5 ps



2. Changes with design topology
   - DDR2 started ODT support
   - DDR3 started Fly by topology vs. T topology
   - DDR3 uses only differential strobes
   - DDR4 architecture is point to point
     - One controller to 1 DIMM
   - DDR4 is Psuedo Open Drain vs. Push/Pull

DDRX Technology Challenges

ANSYS DDR3 Compliance Report

Table of Contents

Design Summary

Design Details

Description	
Project	byte_lane0_0912_test
Design	ODT_40
Design ID	141
Design Type	Circuit Design
Location	F:/WORK_2012/09/DDR_Tool_Kit/New_UDO_set_b
Date	9/28/2012 11:05:57 AM
Product Version	Designer 8.0.0
UDD Version	DDR3 Compliance Report, 1.0 (R14.5)
User	rmyoung

Solution Setup

Solution Details

Description	
Name	DDR3 AC-Timing 8-DQ1
UDO	C:\Program Files\AnsysEM\Designer8.0\Windows\syslib\UserDefine
Parameters	
AC DQ Level	AC150
Speed Bin	Auto (from DQS)
DQS delay	0ps
External Report	off
Probes	

Solution Setup

Solution Details

Description	
Name	DDR3 AC-Timing 8-DQ1
UDO	C:\Program Files\AnsysEM\Designer8.0\Windows
Parameters	
AC DQ Level	AC150
Speed Bin	Auto (from DQS)
DQS delay	0ps
External Report	off
Probes	
DQ0	V(DDR3SDRAM2/U27.DDR_DQ0)
DQ1	V(DDR3SDRAM2/U27.DDR_DQ1)
DQ2	V(DDR3SDRAM2/U27.DDR_DQ2)
DQ3	V(DDR3SDRAM2/U27.DDR_DQ3)
DQ4	V(DDR3SDRAM2/U27.DDR_DQ4)
DQ5	V(DDR3SDRAM2/U27.DDR_DQ5)
DQ6	V(DDR3SDRAM2/U27.DDR_DQ6)
DQ7	V(DDR3SDRAM2/U27.DDR_DQ7)
DQS	V(DDR3SDRAM2/U27.DDR_DQS0P)
DQS#	V(DDR3SDRAM2/U27.DDR_DQS0N)
VDD	V(Memory_Controller2/U3.Vprobe)

Per-Lane

AC Timing (JESD79-3E, Section 13.1)

Metric	Worst Actual	Wor
Tvb(base)	153.504	78.5
Tva(base)	212.071	112.
Tvb(derated)	64.5042	-10.
Tva(derated)	155.071	55.0

Per-DQ

Per-Lane

AC Timing (JESD79-3E, Section 13.1)

Metric	Worst Actual	Worst Margin	Spec Value	Unit	Result
Tvb(base)	153.504	78.5042	75	ps	PASS
Tva(base)	212.071	112.071	100	ps	PASS
Tvb(derated)	64.5042	-10.4958	75	ps	FAIL
Tva(derated)	155.071	55.0713	100	ps	PASS

Per-DQ

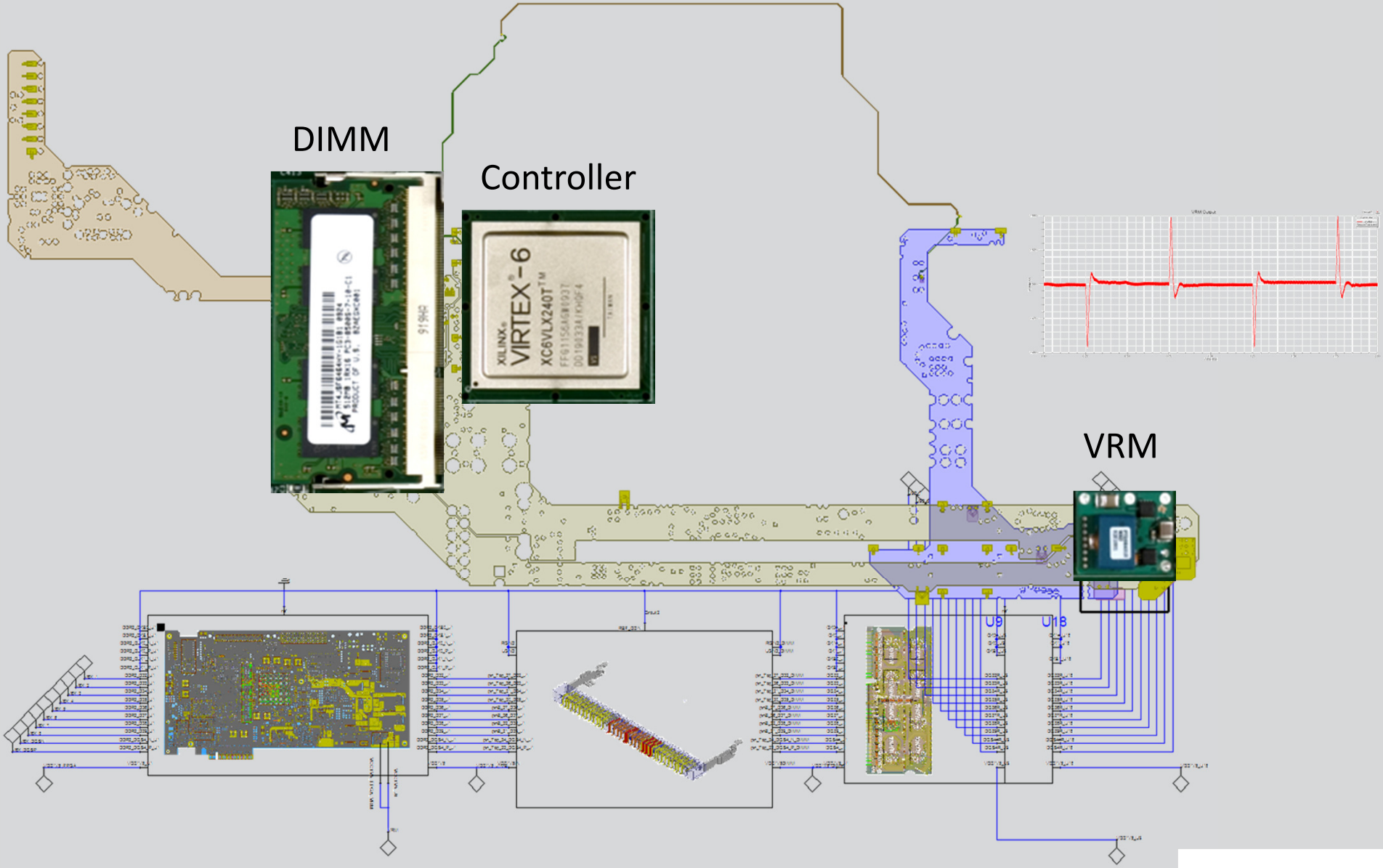
Tvb(base) - Timing Metrics

DQ	Min [ps]	Max [ps]	Mean [ps]	StdDev [ps]	t(worst) [ps]	Margin [ps]	Result
0	153.504	592.133	394.361	74.6529	826589	78.5042	PASS
1	176.383	594.543	392.969	74.6294	774061	101.383	PASS
2	160.777	595.023	383.884	74.2443	780629	85.7773	PASS
3	197.027	591.045	390.948	74.3958	167180	122.027	PASS
4	198.555	611.393	404.85	74.1993	762809	123.555	PASS
5	190.156	610.688	406.515	75.1155	774999	115.156	PASS
6	184.747	614.748	403.393	76.065	791885	109.747	PASS
7	187.724	603.508	402.726	73.5539	812520	112.724	PASS

Tva(base) - Timing Metrics

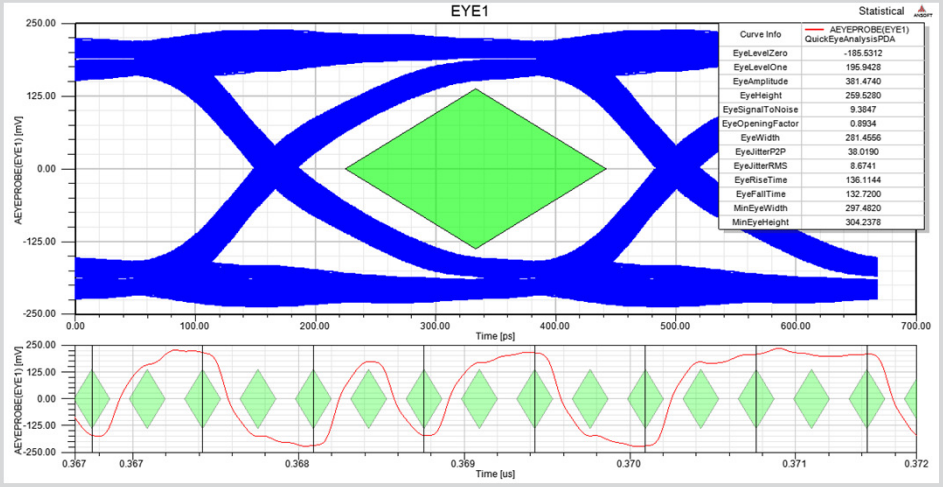
DQ	Min [ps]	Max [ps]	Mean [ps]	StdDev [ps]	t(worst) [ps]	Margin [ps]	Result
0	237.728	681.624	442.437	75.723	287239	137.728	PASS
1	234.733	662.57	442.252	75.2777	263789	134.733	PASS
2	241.428	667.318	452.396	74.2569	10530.5	141.428	PASS
3	238.837	637.559	444.067	74.8498	175625	138.837	PASS
4	224.494	637.405	431.277	75.171	254407	124.494	PASS
5	217.788	640.737	428.897	75.2974	4904.89	117.788	PASS
6	212.071	653.348	431.936	76.9848	930706	112.071	PASS
7	228.904	649.738	432.234	74.4874	189693	128.904	PASS

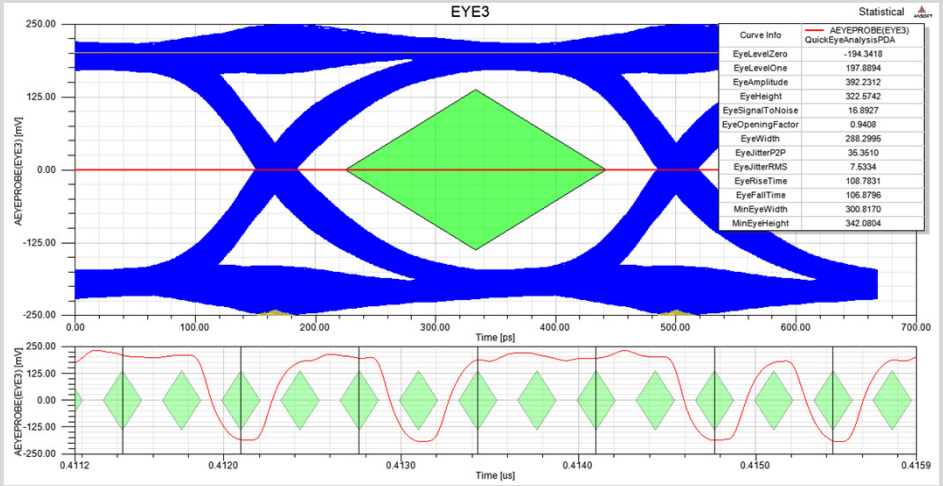
DDR3 1.5V PDN with VRM



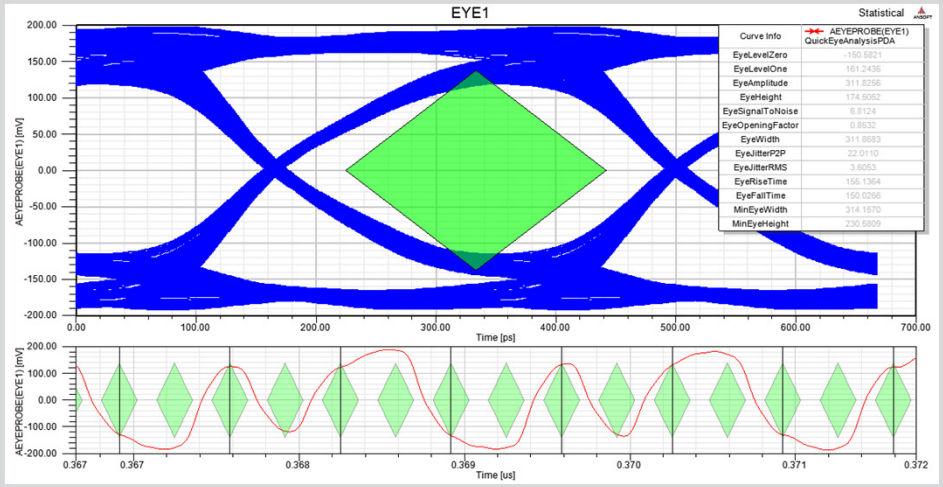
DDR3 Connector Impact (Reflections)

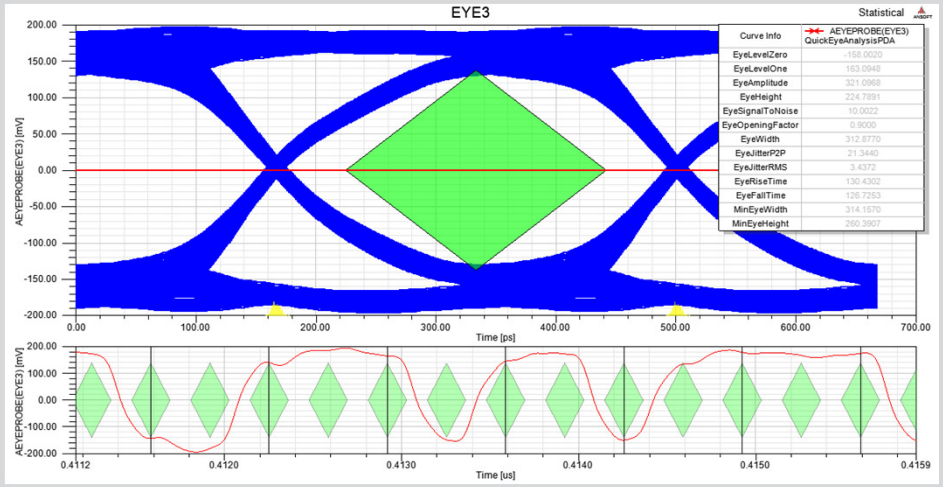
Without Connector



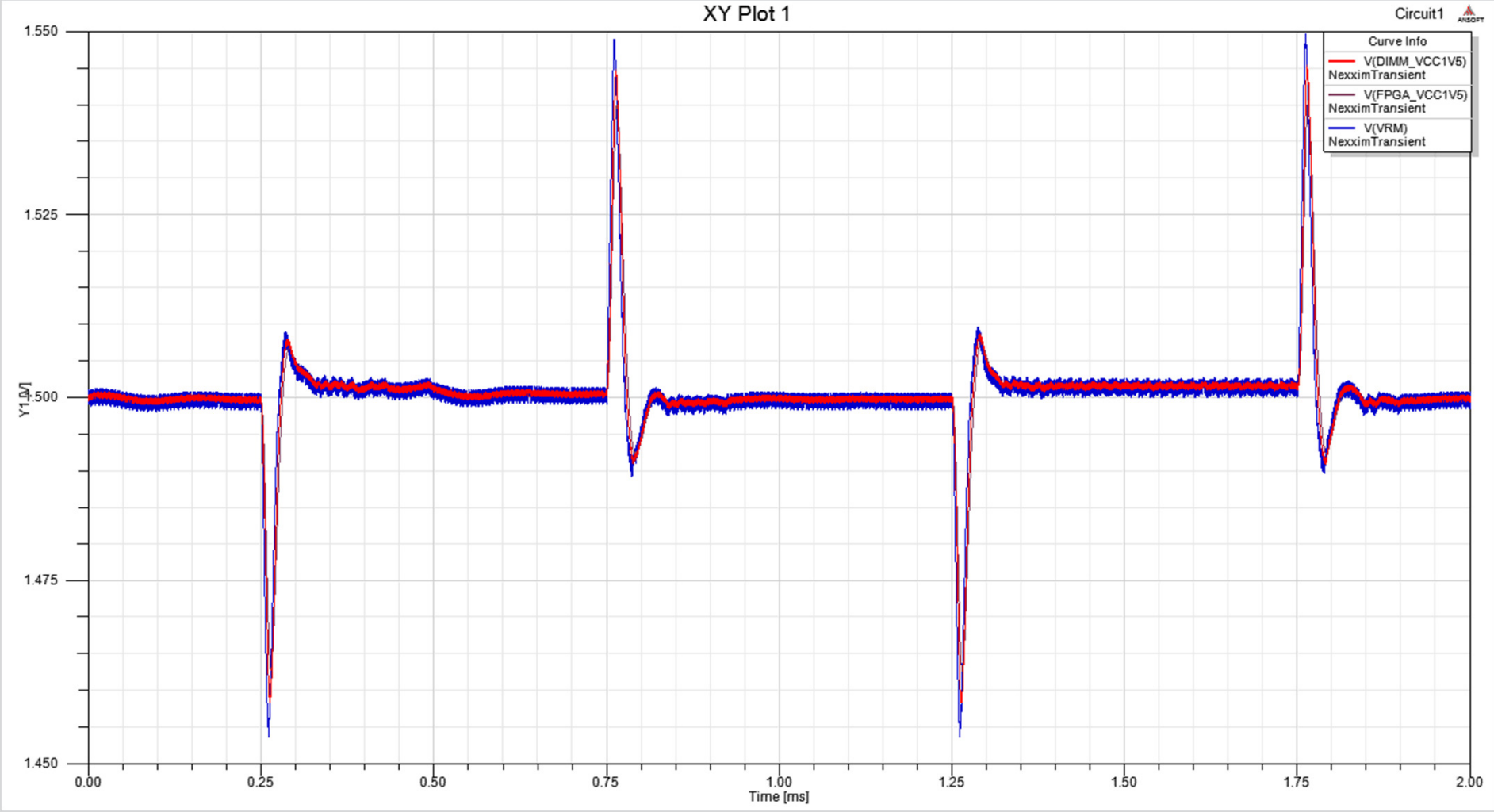


With Connector

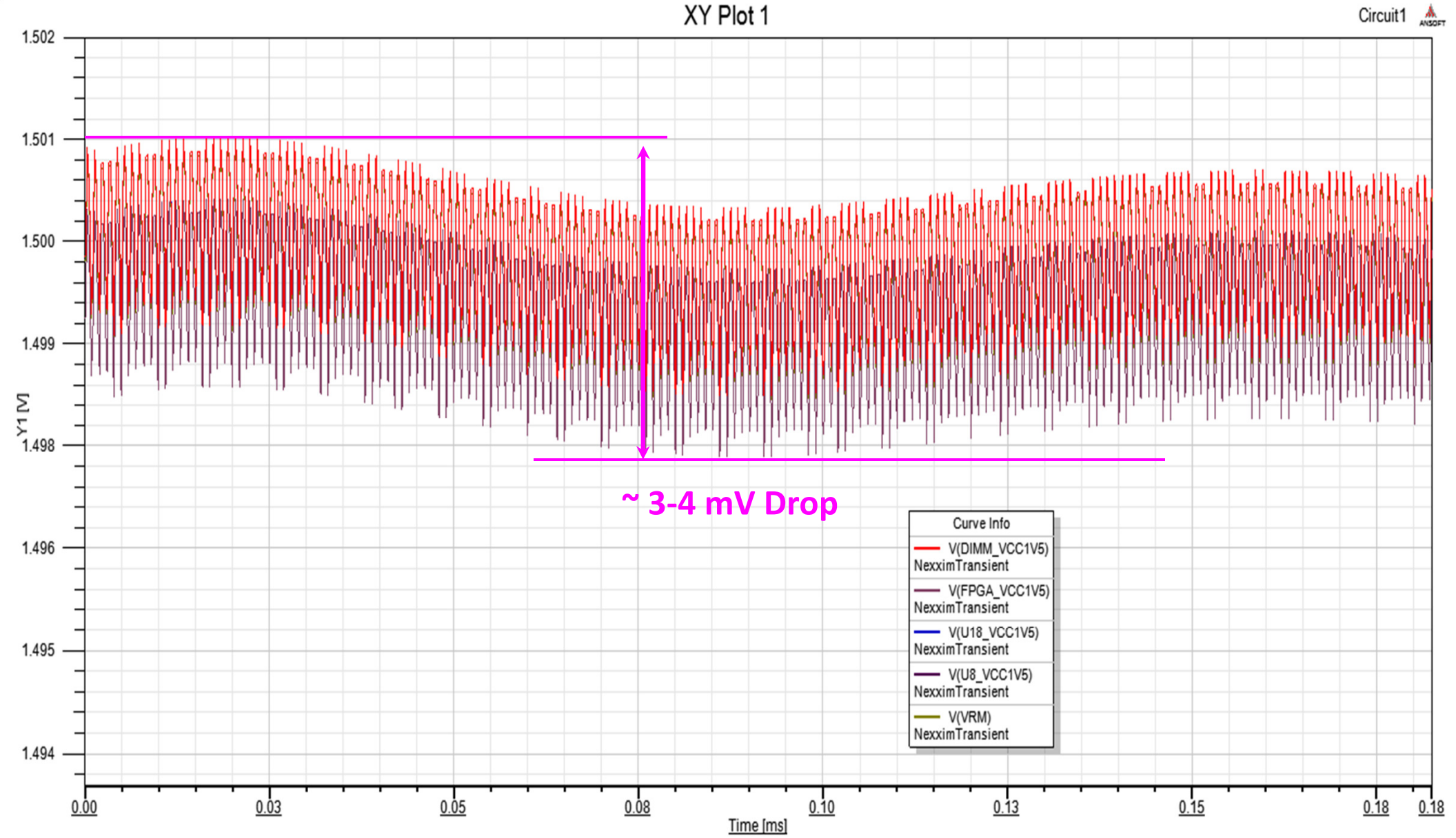




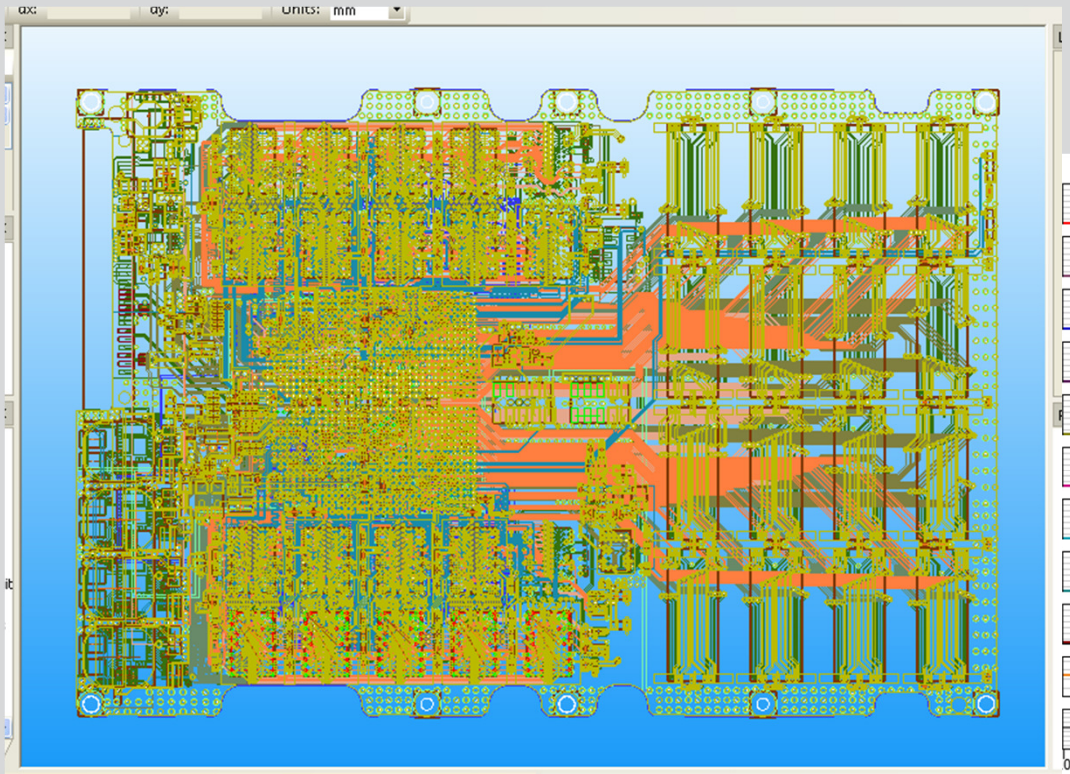
DDR3 1.5V PDN with VRM

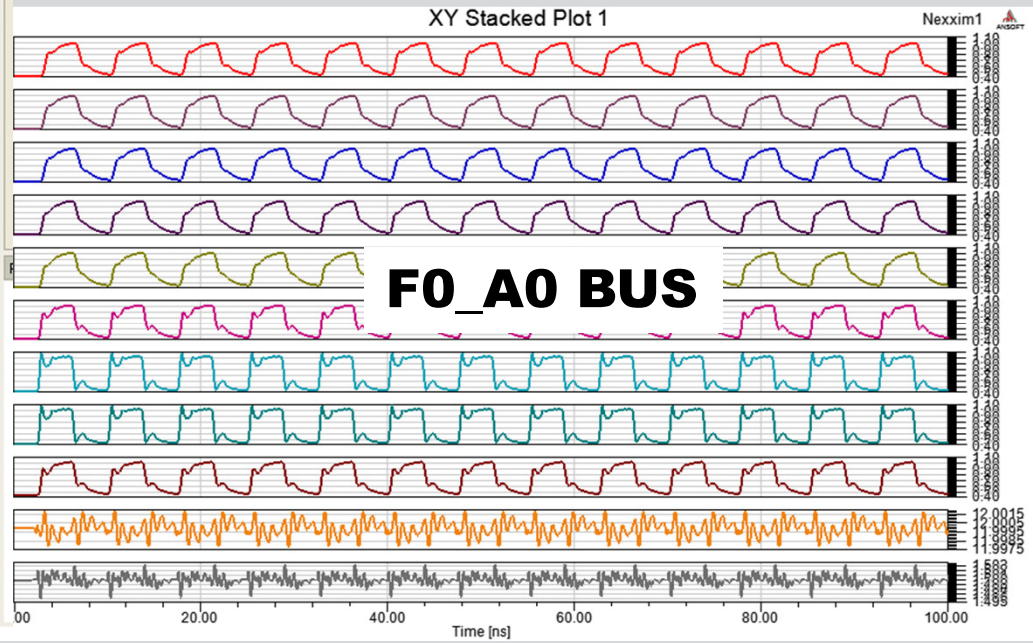


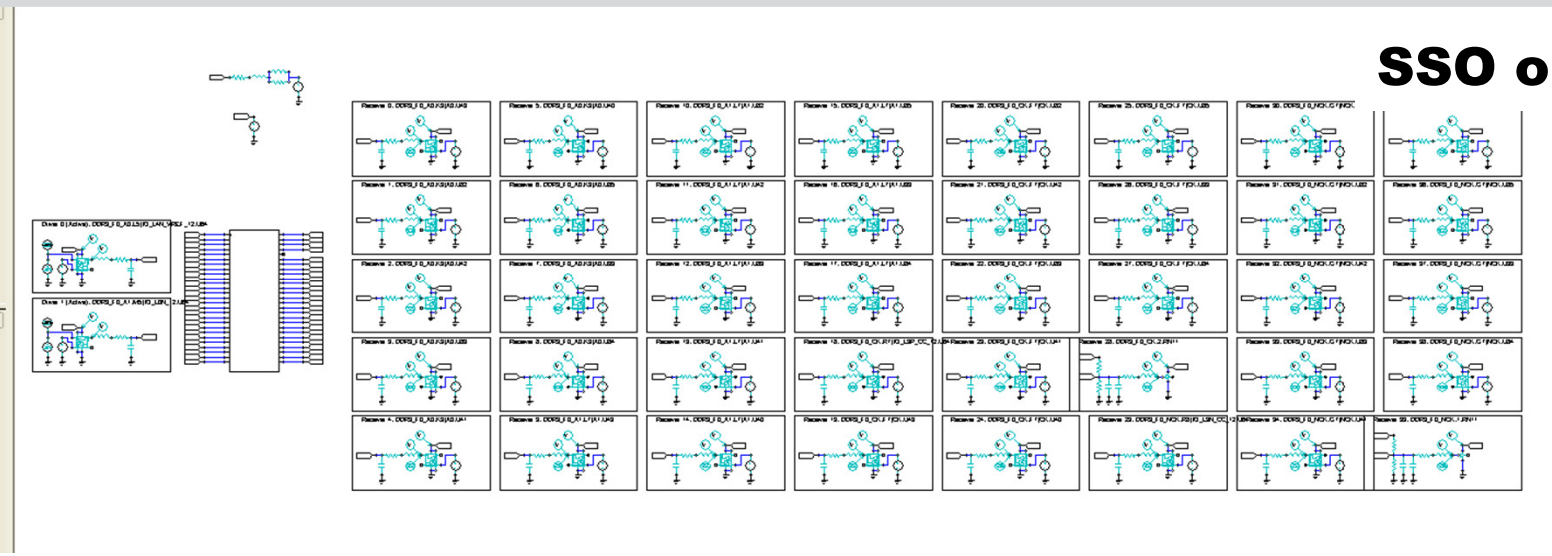
DDR3 1.5V PDN with VRM



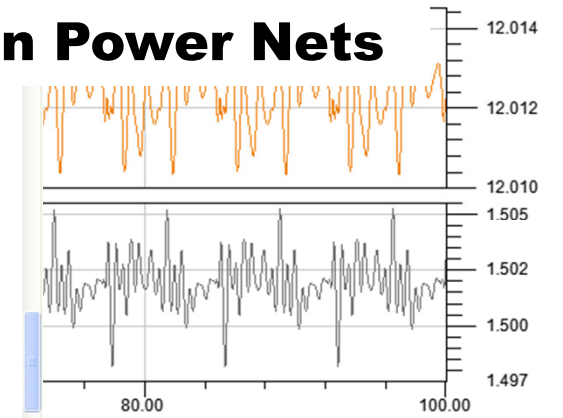
System Level Memory Analysis



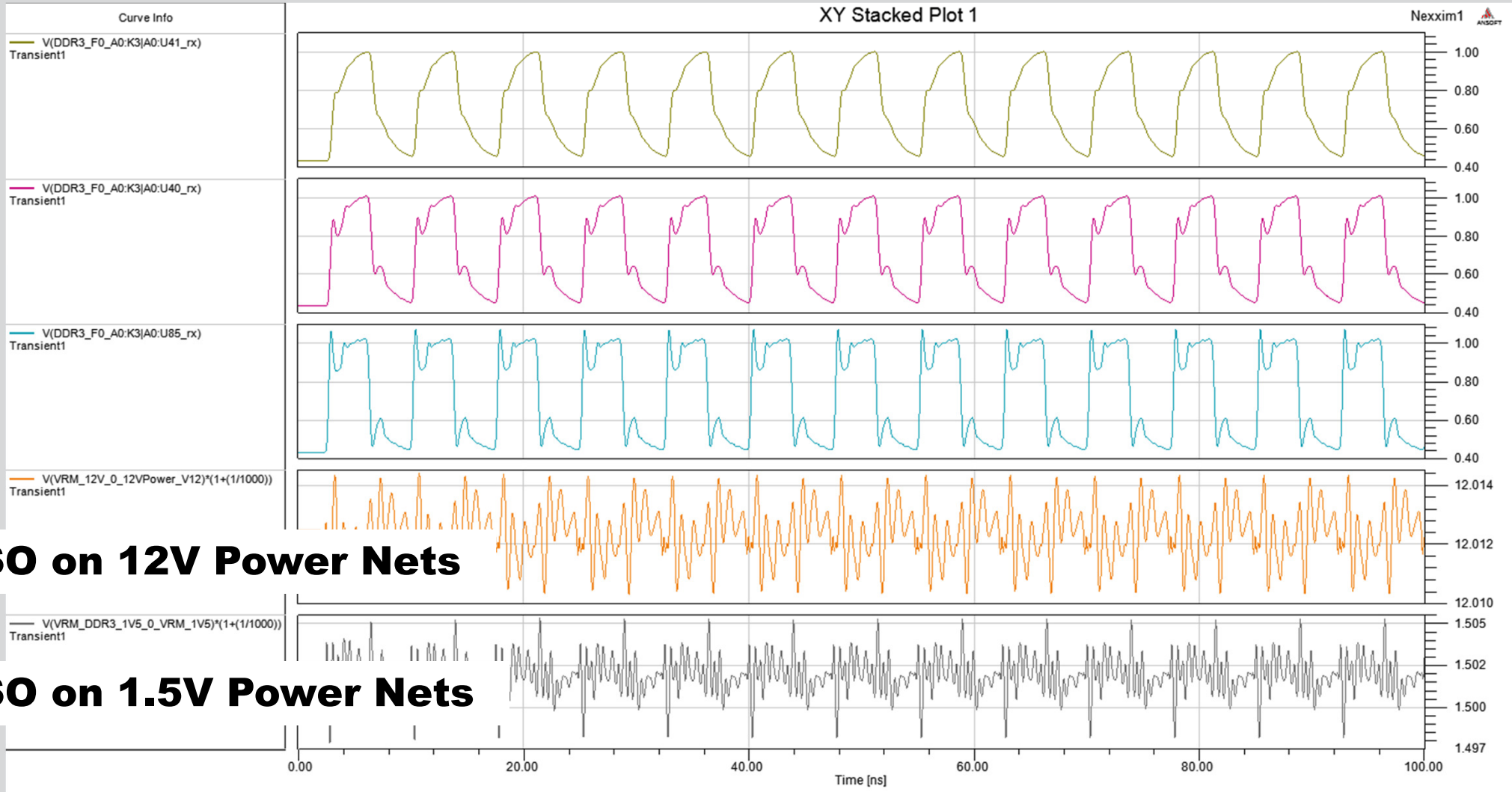




SSO on Power Nets



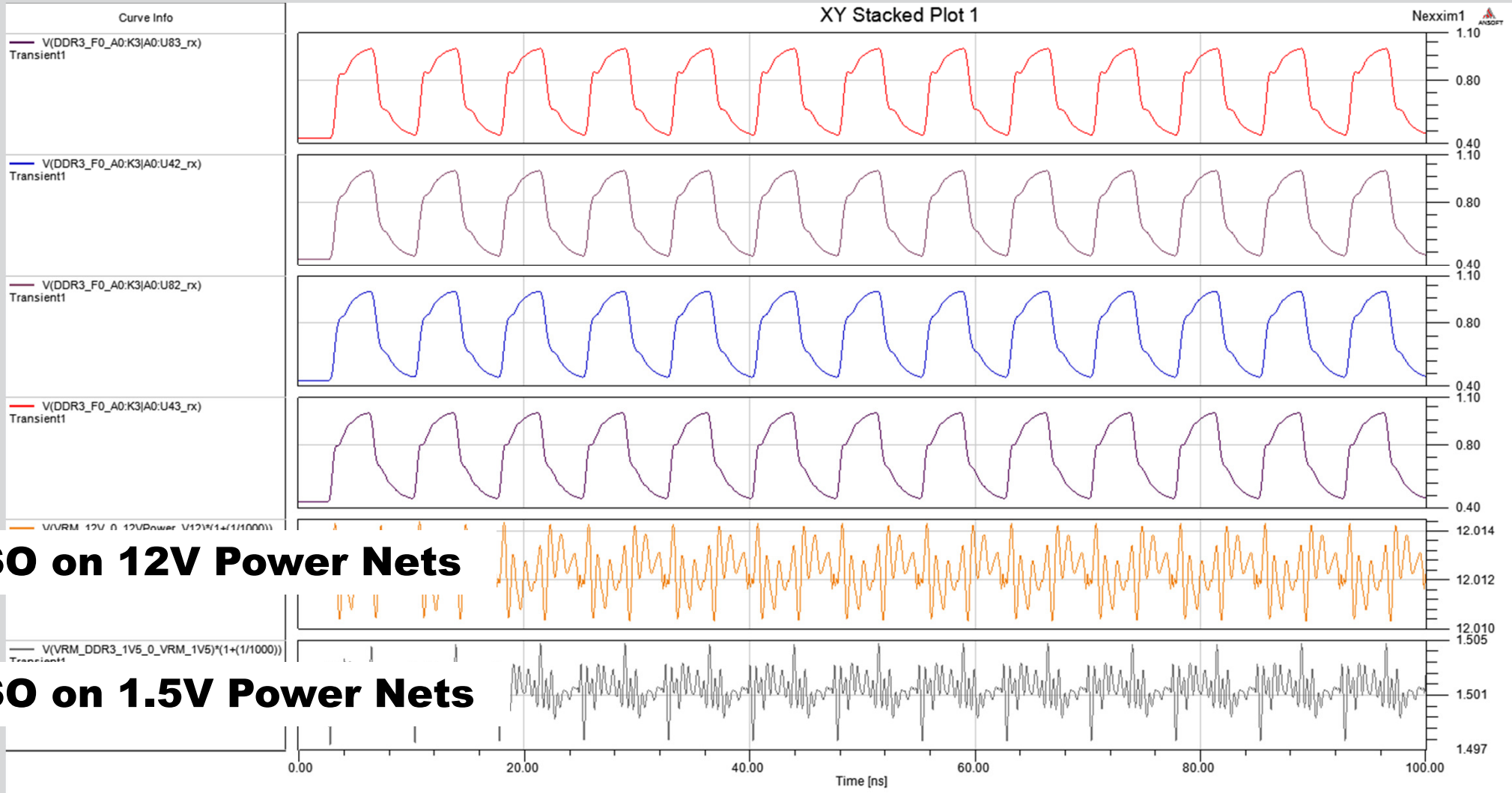
System Level Memory Analysis



SSO on 12V Power Nets

SSO on 1.5V Power Nets

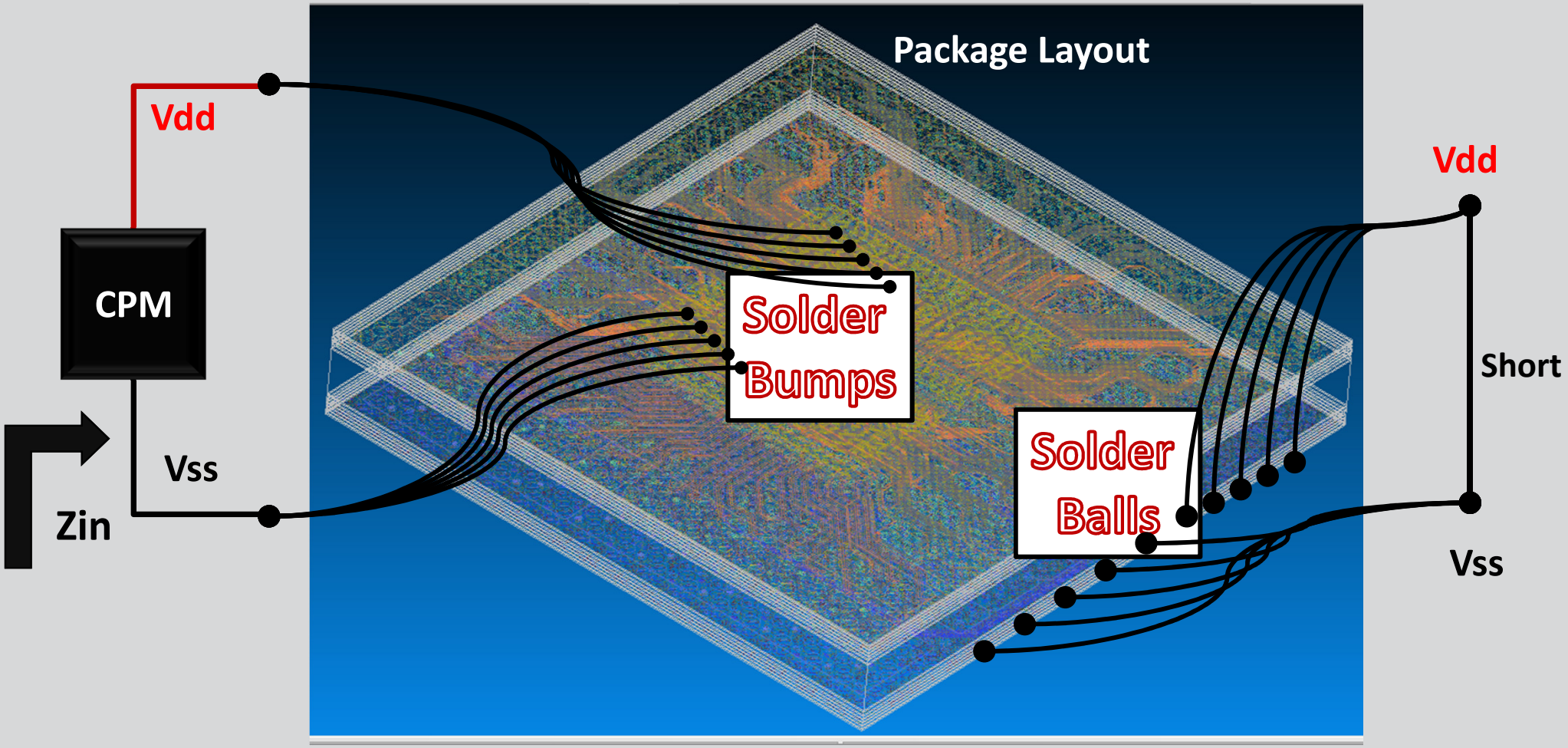
System Level Memory Analysis



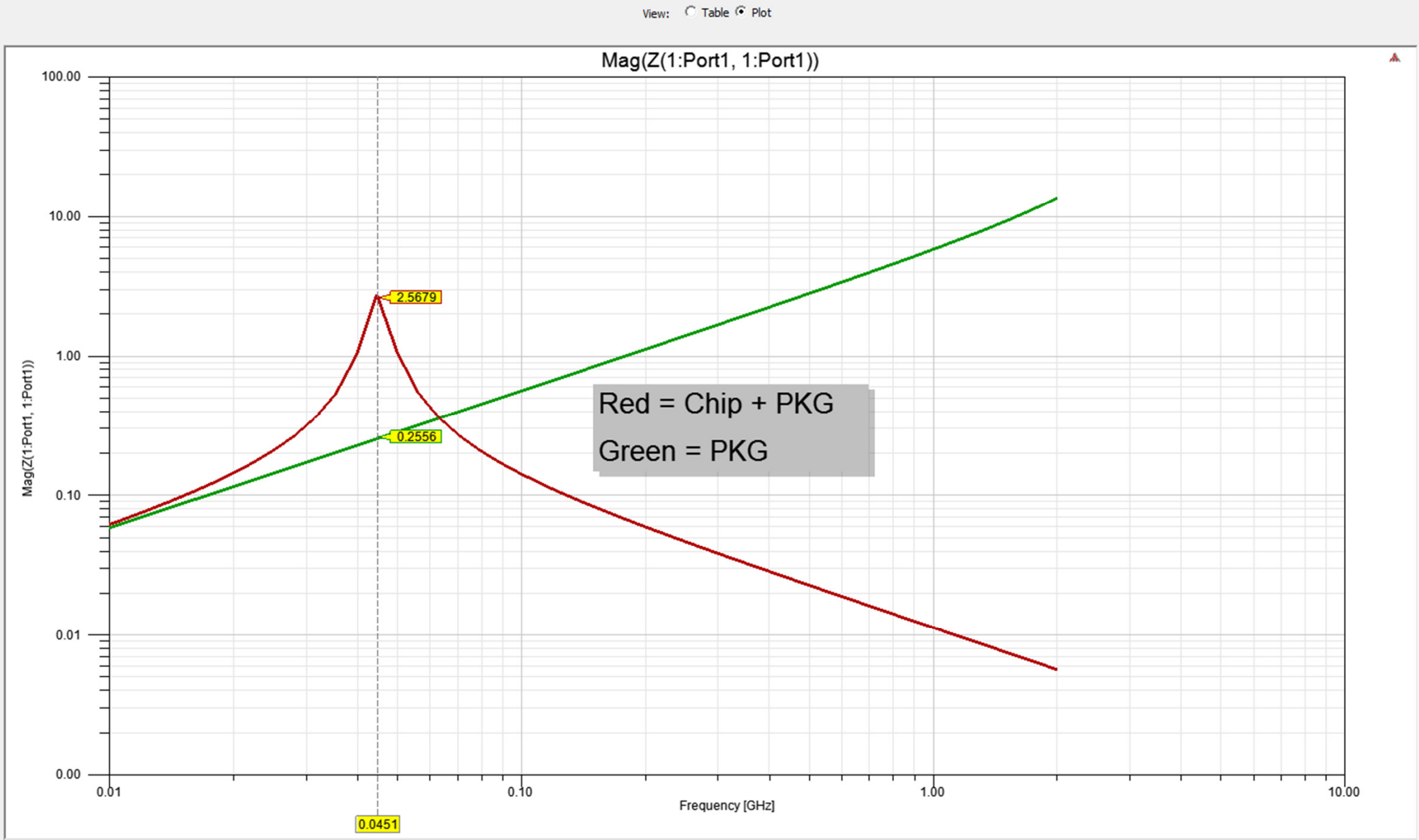
SSO on 12V Power Nets

SSO on 1.5V Power Nets

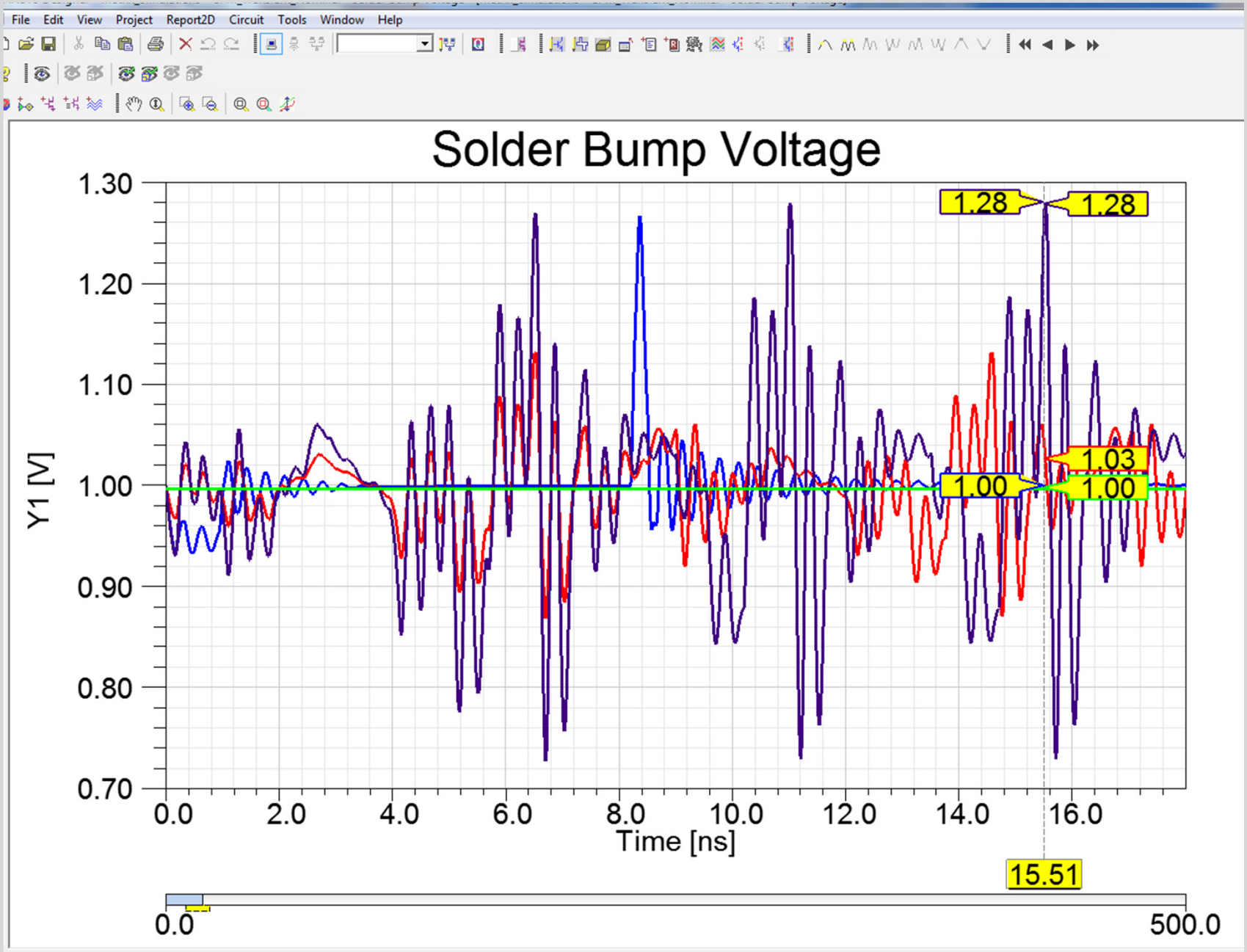
Recall Chip Impedance



Impedance Results with & without Chip



Die Solder Bump Voltage



Conclusion

- DDR4 Standard was recently released
  - Interconnect challenges due to Chip, PKG, & PCB
    - Reduced Voltage (1.2V -> 1.05V expected)
    - Increased Data Rates (1600 Mbps -> 4266 Mbps expected)
    - Future stacking of SDRAMs expected with TSV technology
- System level performance must include:
  - Accurate PKG/PCB extractions including connectors
  - Accurate Die Models: IBIS + current?