IBIS Open Forum Minutes

Meeting Date: **November 13, 2012**
Meeting Location: **Hsinchu, Taiwan**

VOTING MEMBERS AND 2012 PARTICIPANTS

Agilent	Heidi Barnes, Radek Biernacki, Yoji Sekine, Fangyi Rao, Jing-Tao Liu, Zhengpeng Zhu, Xuliang Yuan, Yi Wang, Ming-Chih Lin*, Peter C.B. Lin*, Isabella Wan*
Altera	David Banas, Hsinho Wu, Masashi Shimanouchi
ANSYS (Ansoft)	Flavio Calvano, Luis Armenta, Dan Dvorscak, Baolong Li, Kezhou Li, Daniel Chang*, Naijen Hsuan*, Steve Pytel*, Jean Wang*, Jerry Wang*, Yachin Wang*, Peishen Wei*, Jack Wu*, Tinghao Yeh*,
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ARM	(Nirav Patel)
Cadence Design Systems	Brad Griffin, Terry Jernberg, Jilin Tan, Dennis Nagle Ambrish Varma, Aileen Chen, Lanbing Chen, Li Chen Raymond Y. Chen, Jonny Fang, Zhiyu Guo, Henry He, Li Li, Xianlai Li, Lavia Liu, Peng Liu, Yabao Meng, Fang Sun, Haishan Wang, YiTong Wen, Janie Wu, Dingru Xia, Benny Yan, Jenny Zhang, Jinhui Zhang, Rong Zhang, Zhangmin Zhong, Steven Chen*, Kent Ho* Joseph Kao*, Tom Kao-Lo*, Thunder Lay*, Jack (Wei-Chang) Lin*, Paddy Wu*, Candy Yu*
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Freescale	(Jon Burnett)
Huawei Technologies	Xiaoqing Dong, Chunxing Huang, Peng Huang Hongxin Jiang, Wenjin Luo, Longfang Lv, Luya Ma, Xiao Peng, Huichao Weng, Zhengrong Xu, Juhua Yu, Fangfang Zhang
IBM	Adge Hawes, Greg Edlund
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak, Subas Bastola, Udy Shrivastava, Stewart Gilbert, Eddie Frie, Jinsong (Jason) Hu Weifeng Shu, Ming Wei, Jimmy Hsu*
IO Methodology	Lance Wang*
LSI	Brian Burdick
Maxim Integrated Products	Hassan Rafat, Mahbubul Bari
Mentor Graphics	Arpad Muranyi, Vladimir Dmitriev-Zdorov
Micron Technology	Randy Wolff, Aniello Viscardi, Francesco Madonna Antonio Prisco, Justin Butterfield

Nokia Siemens Networks GmbH	Eckhard Lenski, Evis Minga, Bruce (Zhenshui) Qin, Feiqin Shen, Yuanzhi Xu, Jieping Zhang, XiuYing (Echo) Zhou
QLogic	(James Zhou)
Signal Integrity Software	Walter Katz, Mike LaBonte, Todd Westerhoff Akalu Lentiro
Sigrity	[Raymond Chen], Yingxin Sun, Sam Chitwood Ben Franklin, Srdjen Djordjevic
Synopsys	Andy Tai, Scott Wedge, Hany Elhak, Ted Mido, Xuefeng Chen, Jinhua Huang, Huihuang Li
Teraspeed Consulting Group	Bob Ross, Tom Dagostino
Texas Instruments	Casey Morrison, Pegah Alavi, Valerie Chang Modesto Garcia, Karl Muth
Toshiba	Masatoshi Abe
Xilinx	Harry Fu
ZTE	Huifeng Chen, Xiaolin Chen, Fengling Gao, Hui Jiang, Wan Ming, Qi Ni, Anbing Sun, Lili Wei, Shunlin Zhu
Zuken	Michael Schaeder

OTHER PARTICIPANTS IN 2012

3M	Qiling Chen, Yao Li
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AMD	(Nam Nguyen)
Apache Design	Jianbo Liu, Shulong Wu, Mengfei Xu, Wei Yang
Apple Computer	(Matt Herndon)
Aruba Networks	Amir Motamedi
ASE	Alex Wang*
Avago Technologies	Sanjeev Gupta, Amolak Badesha
Avant Technology	Yi-Ching Chu, Elvis Li, Yao-Chang Chang*, Judy Huang*, Jyam Huang*, Enson Lee*
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Cavium	Johann Nittmann
Celestica	Lily Dai, Jason Liu, Ivan (Yunqiang) Meng, Harrison Xue, Lobo Zhang, Van Zhu
Ciena	Kaisheng (Klaus) Hu
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Cypress Semiconductor	Wenhe Chen
Enea Group	Xiaoliang Gao
Enterasys	Robert Haller
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Exar Corporation	Helen Nguyen
General Electric Company	Zhen Zhang
Gibabyte Technology	Eric Chien*

Granite River Labs	Jiang Xu, Johnson Tan
H3C	Longsheng Yuan
Hewlett-Packard	Ting Zhu, Rick Wu*
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Hitachi	Yutaka Uematsu
Honeywell	Chengzhi (Hunk) Hu
Huaya Microelectronics	Golden Qian
ILI Technology	Pacino Chang*, Chia-Chen (Trevor) Wu*
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Lenovo	Aiping Li
Luxshare-ICT	Alan Kinningham, Steven Wong
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Molex	Greg Fu
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NXP Semiconductors	Grace Yang
Nvidia	Eric Hsu
Pegatron Corporation	Stanley Chu*, Lawrence Ting*
Politecnico di Torino	Stefano Grivet-Talocia
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Ruijie Networks	Ye Tao
Silicon Motion Technology	Star Wang*
Sony	Kenji Yasoda
Southwest Electronics Telecommunication Technology Research Institute	Wei Hu
Spreadtrum Communications Shanghai	Steven Guo, Xianyu Meng, John Rowland
ST Microelectronics	Davide Pandini
Sunplus Technology	Forest Hsu*, Yi-Tzeng Lin*
SWIEE Electronics	Chen Gao
TechAmerica	(Chris Denham)
Teledyne LeCroy	Fachun Li, Derek Wu
Université de Brest	Mihai Telescu, Cherif Diouf
University of Illinois	Thomas Comberiate, José Schutt-Ainé
Vitesse Semiconductor	Sirius Tsang
Zhejiang United Electronic Industry	Gang Xu
Zhejiang Uniview Technologies	Sunny (Huanyang) Chen, Phil (Fei) Ye

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the

organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 16, 2012	Asian IBIS Summit - Yokohama – no telephone bridge	
November 30, 2012	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The Asian IBIS Summit took place on Tuesday, November 13, 2012 at the Ambassador Hotel in Hsinchu, Taiwan. Approximately 48 people from 18 organizations attended.

The statements below summarize the material presented. More details are available through the summit presentations posted online at:

http://www.eda.org/ibis/summits/nov12b/

Lance Wang welcomed the attendees and thanked the co-sponsors: the major sponsor ANSYS, Agilent Technologies, Cadence Design Systems, Intel Corporation, and IO Methodology. Daniel Chang of ANSYS in Taiwan also welcomed the attendees and asked Steven Pytel to provide a few remarks.

ELECTRONIC INTERCONNECT CHALLENGES

Steven Pytel (ANSYS, USA)

Steven Pytel described how chip aware system design looks at a design in both the digital and RF domains. This combines aspects of signal integrity, power integrity, EMI and thermal integrity. Power integrity analysis involves several levels including silicon, package and PCB/system. Final verification includes lab measurements and design validation. A virtual

platform for system design combines power integrity analysis at all these levels and requires detailed extractions of chip power input impedance.

Steven concluded that chip RLC parasitics and chip current signatures change system performance. Also, interconnect design must include chip-to-chip effects.

IBIS 5.1: AN OVERVIEW
Michael Mirmak (Intel Corporation, USA)
[Presented by Lance Wang (IO Methodology, USA)]

Lance announced that IBIS 5.1 was approved on August 24, 2012. It has been reformatted based on Microsoft Word for ease of editing, changes (BIRDs), readability, and cross-referencing with hyperlinks. ASCII figures and tables are replaced with graphics and actual tables. The terminology has been made more consistent. Lance showed a list of 25 BIRDs that have been incorporated to support new features and changes. The AMI parameter discussion that was in Section 6C has been moved to a new section 10A. While old AMI files will still work, there are some flow changes to support non-LTI models in TX AMI_GetWave. Use_Init_Output is deprecated for AMI_Ver 5.1 files depicted by using the AMI_Version parameter.

Lance showed some of the format changes and also announced the ibischk5 parser, Version 5.1.2 was released October 6, 2012 to support checking IBIS Version 5.1 and .ami files. The next steps for specification updates include renumbering the sections and incorporating new BIRDs written in the new format. The next major Version is 6.0, but Version 5.2 might be issued for standardization only.

A comment was made that an IBIS-AMI repeater model will be very useful in designs.

USING LATENCY INSERTION METHOD TO HANDLE IBIS MODELS
Ping Liu*#; Jilin Tan*##; and Jose Schutt-Aine** (*Cadence Design Systems, #China, ##USA; and **University of Illinois, USA)
[Presented by Joseph Kao (Cadence Design Systems, Taiwan)]

Joseph Kao indicated that the traditional way of setting up IBIS simulations is to apply Newton-Raphson techniques combined with modified nodal analysis. However, the results may be unpredictable and not even converge. A Latency Insertion Method introduced here has many advantages including no convergence issues, linear numerical complexity, speed, and no ill-conditioning problems. For large-scaled networks, a “leapfrog” scheme (current to voltage to current to voltage, etc.) is used to solve for node voltages and branch currents. Nodes must have a shunt capacitor, and branches must have a series inductor.

Joseph showed how this can be extended to the IBIS buffer simulation based on two equations, two unknowns, and Ku and Kd calculations can be reformulated using an explicit leapfrog method. The IBIS simulation converges in cases where the Newton Raphson method does not. Joseph also showed how this formulation can be extended to handle [ISSO_PU] and [ISSO_PD] tables per BIRD98. The formulation can also be used for handling composite currents described in BIRD95.

IBIS-AMI, INDUSTRY ADOPTION, AND CURRENT CHALLENGES
Naijen Hsuan and TingHao Yeh (ANSYS, Taiwan)

Naijen Hsuan described how IBIS-AMI modeling presents many challenges today. A package model standard is not finalized, so users need to manually add package parasitics to the channel model. Each IC vendor has different parameter sets, so extensive documentation is required. AMI simulations depend on accurate channel modeling, but passivity and causality issues with S-parameter models are common. There is no standard way to sweep parameters and channel corner effects. High speed serial channels are pushing the limits of simulation. Naijen presented a list of current challenges including non-liner, time variant systems.

Naijen compared several types of simulation for high speed SerDes analysis and noted that IBIS-AMI had the least disadvantages over transistor level, fast convolution and statistical methods. He noted that enforcing passivity and causality in EDA software may be necessary. Also, it can be important to combine the package and PCB to capture the transitions in 3D modeling. He showed a methodology for handling corner and manufacturing variations and introduced the concept of channel "V" design for IBIS-AMI solutions. Naijen concluded with a detailed AMI analysis flow.

EFFICIENT END-TO-END SIMULATIONS OF 25G OPTICAL LINKS
Jing-Tao Liu*#, Fangyi Rao*##, Sanjeev Gupta**, and Amolak Badesha** (*Agilent Technologies, # China, ##USA; and **Avago Technologies, USA)
[Presented by Ming-Chih Lin (Agilent Technologies, Taiwan)

Ming-Chih Lin indicated that above 25G (25 Gbps), the traditional electrical link is limited by channel losses. Optical channels have advantages including smaller loss and superior bandwidth, flawless connectivity between digital boards and backplanes, smaller footprints, and reduced EMI. Ming-Chih showed an optical link system and gave some of the challenges to model the electrical and optical portions of the link with IBIS-AMI simulation methodology. He illustrated the IBIS-AMI flow and gave advantages and disadvantages. One concern is that channels are assumed to be linear, but optical channels are strongly non-linear and noisy.

The solution is to treat the entire optical module as a mid-channel repeater and extend IBIS-AMI simulation to include the repeater. Ming-Chih showed the full channel optical link simulation flow and then gave some electrical details of the VCSEL optical model and corresponding equations. He then showed 25G optical channel simulation results (eye diagrams, bathtub curves, and optical noise effects, temperature effects, and non-linear effects, and fiber effects). Ming-Chih concluded that IBIS-AMI methodology is applied to model and simulate the optical channels and provides many advantages for end-to-end optical link analysis.

CHIP PDN MODEL FOR POWER AWARE SIGNAL INTEGRITY ANALYSIS
Jack W.C. Lin#, and Raymond Y. Chen## (Cadence Design Systems, #China, ##USA)

Jack Lin described traditional SSO analysis with traditional IBIS and showed artificially large power/ground fluctuations. On die RC decoupling capacitors reduce the fluctuations. A chip PDN helps identify mid-frequency resonance. This could add to larger power ground noise and worse digital quality. IBIS Version 5.0 is currently limited because it lacks a direct RC decoupling network.

Some chip PDN capacitance comes from the driver transistors and another part comes from outside of the transistors. For example, MIMCAPs on an interposer can contribute sizable capacitance. Jack showed how to generate a chip PDN model (as proposed earlier by Sigrity) for the driver transistors. Outside the transistors, the PDN capacitance can be extracted by I/O circuit bus groups. This can be modeled as an RC model or a distributed Spice model. Jack showed a case study using PDN in SSO analysis (with an RC model and distributed Spice model) that showed realistic power/ground noise versus artificially high noise for the case without a PDN.

Jack also illustrated a BIRD proposal that uses the [Pin Mapping] busses to map bus name to subcircuit nodes through a [Define Chip PDN Model] keyword and [External Model].

A comment was made that the chip PDN model is not easy to separate from the I/Os, therefore it is not practical.

IBIS PARSER UPDATE
Bob Ross (Teraspeed Consulting Group, USA)
[Presented by Anders Ekholm, Ericsson Sweden)]

Anders Ekholm showed the valid IBIS Version numbers through 5.1 and also the latest ibischk versions through Version 5.1.2. Specifications are upgraded to the last major version. Downward compatibility is maintained for features and syntax so that existing models remain valid.

IBIS-AMI started supporting sub-version distinctions in the .ami format. AMI_Version is required for “5.1” files and Use_Init_Output is not legal.

Anders gave a brief overview of ibischk5 Version 5.1.2 and showed its flags. There are over 1150 unique numbered error message strings. The source code package has 44 new test case files since Version 5.0.7. Ibischk Version 5.1.2 checks many more errors than the older Version 5.0.7 as a result of 23 BIRDs and 13 BUG reports that impact the parser.

Anders described briefly the tschk2 parser that checks both Touchstone Version 1.0 and Touchstone Version 2.0 files.

Anders concluded that the parsers officially check files for specification compliance and are critical to IBIS success.

IBIS VALIDATION METHOD REVIEW
Lance Wang (IO Methodology, USA)

Lance Wang described how system design engineers need validated IBIS models to analyze high speed designs. The IBIS Accuracy Specification was originally released in 1998. In 2007, the IBIS Quality task group was formed. This group has released IBIS Quality specifications and a Quality checklist. In recent years, many system companies started to ask their device vendors to supply quality control documents for their IBIS models.

The goal of IBIS validation is to correlate IBIS model simulation results with golden sources (measurements and simulations) for specific test loads. Commonly used correlation/comparison methods include the quality checklist, curve overlay or envelope metrics, threshold based metrics and differential index based metrics. Lance detailed pros and cons of each of the methods and presented several common mistakes in the validation process.

Lance concluded that validation is best done by IBIS model vendors. Comparison methods vary and must be used wisely to fit buffer model needs. IBIS users should ask their vendors for reasonable validation reports.

THE EVOLUTION OF DDR MEMORY AND OVERCOMING CHALLENGES OF DDR3/4 DESIGN

Steven Pytel (ANSYS, USA)

Steven Pytel showed a chart detailing the changes in operating voltages and memory speeds for SDR SDRAM through the most recent DDR4 SDRAM technologies. The DDR4 standard was announced in September 2012. DDR4 uses a 1.2V supply voltage and has significant changes to the operation of the data signals as compared to DDR3.

The analysis of DDRX technologies involves significant complexity including large amounts of output data in reports. Accurate system level analysis of performance must include accurate package, PCB and connector extractions. Accurate die models are needed including IBIS models plus current modeling and chip PDN modeling.

A question was asked about what kind of high speed connectors should be used in the design. Steven answered that one should go to the vendor website and get the specific connectors' S-parameter models. Then try it in the simulations to find the best one for your design.

DESIGNING DDR3 SYSTEM USING STATIC TIMING ANALYSIS IN CONJUNCTION WITH IBIS SIMULATION

Taranjit Kukal#, Zhangmin Zhong##, and Heiko Dudek### (Cadence Design Systems, #India, ##China, and ###Germany)
[Presented by Kent Ho (Cadence Design Systems, Taiwan)]

Kent Ho described how DDR3 board design requires exploration of a large solution space including timing budgets, signal quality, component selection and stack-up and layout constraints. There are multiple constraints across timing and signal integrity. Timing closure across reads, writes and address is challenging. Signal integrity (SI) also affects timing. Ad-hoc analysis and verification leads to non-optimal designs. A unified static timing analysis and SI flow produces better designs. SI simulations feedback into the static timing analysis. Kent presented several use cases. Kent concluded that DDR3 compliance requires multiple specifications to be met covering timing and SI measurements. Timing models should be able to handshake data with IBIS simulations at pre-route exploration and post-route verification stages to ensure that both SI and timing constraints are met.

A question was asked if the flow in slide 17 includes power concerns. Kent responded yes.

CONCLUDING ITEMS

Lance Wang thanked the co-sponsors, presenters and attendees for their participation and support and reminded the attendees to register. The meeting adjourned shortly at 5:00 PM.

NEXT MEETING

The Asian IBIS Summit – Yokohama will be held on Tuesday November 13, 2012. The next IBIS Open Forum teleconference will be held November 30, 2012 from 8:00 to 10:00 AM US Pacific Time.

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NOTES

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This meeting was conducted in accordance with the TechAmerica Legal Guides and TechAmerica Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda.org

In the body, for the IBIS Open Forum Reflector:
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In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda.org)
IBIS Users' Group Reflector (ibis-users@eda.org)
State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

To create an account on the TechAmerica KAVI workspace, check out:

http://workspace.techamerica.org/kwspub/join/

IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	October 5, 2012	October 26, 2012	November 9, 2012	November 13, 2012
Agilent Technologies	User	Active	X	X	X	X
Altera	Producer	Inactive	-	-	-	-
ANSYS	User	Active	-	-	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
ARM	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	X	X	X
Ericsson	Producer	Active	-	X	X	X
Foxconn Technology Group	Producer	Inactive	-	-	-	X
Freescale	Producer	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	-	X	-
IBM	Producer	Inactive	X	X	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
IO Methodology	User	Active	X	X	X	X
LSI	Producer	Inactive	X	-	-	-
Maxim Integrated Products	Producer	Inactive	-	-	-	-
Mentor Graphics	User	Inactive	X	X	-	-
Micron Technology	Producer	Inactive	X	X	-	-
Nokia Siemens Networks	Producer	Inactive	-	-	X	-
QLogic	Producer	Inactive	-	-	-	-
Signal Integrity Software	User	Inactive	X	X	-	-
Sigrity	User	Inactive	-	-	-	-
Synopsys	User	Inactive	-	-	X	-
Teraspeed Consulting	General Interest	Inactive	X	X	-	-
Texas Instruments	Producer	Inactive	-	-	-	-
Toshiba	Producer	Inactive	-	-	-	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	X	-
Zuken	User	Inactive	-	-	-	-

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH TECHAMERICA BALLOT VOTING ARE:

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