

Using Latency Insertion Method to Handle IBIS models

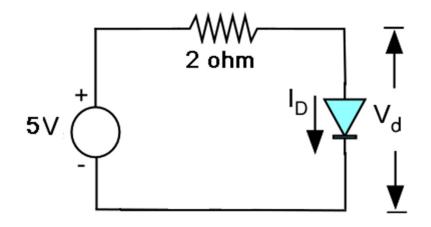
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A simple non-linear Circuit



How to solve I_D and V_d ?

Solve transcendental equations

$$I_d = 1pA \cdot \left[\exp\left(40 \cdot V_d\right) - 1 \right]$$

$$5 = V_d + 2 \cdot I_d$$



Using Newton-Raphson Method

$$X_{n+1} = X_n - \frac{f(X_n)}{f'(X_n)}$$

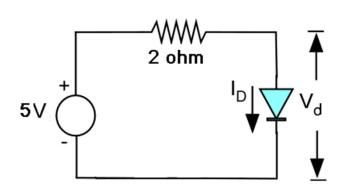
Newton-Raphson iterative process begins with an initial guess and terminates when the difference between successive guesses falls to zero.

$$I_d = 1pA \cdot \left[\exp\left(40 \cdot V_d\right) - 1 \right]$$

$$5 = V_d + 2 \cdot I_d$$

$$f(V_d) = -5 + V_d + 2pA \cdot \left[\exp\left(40 \cdot V_d\right) - 1 \right]$$

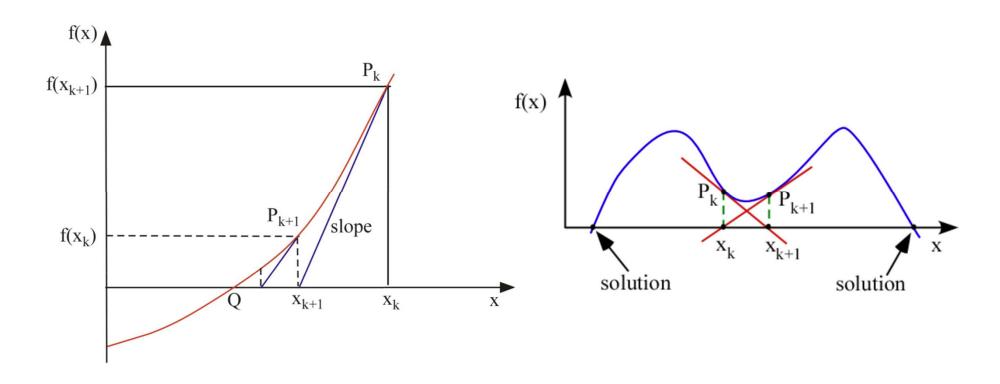
$$f'(V_d) = 0 + 1 + 80pA \cdot \exp\left(40 \cdot V_d\right)$$



$$V_d^{(n+1)} = V_d^{(n)} - \frac{-5 + V_d^{(n)} + 2 pA \cdot \left[\exp\left(40 \cdot V_d^{(n)}\right) - 1 \right]}{1 + 80 pA \cdot \exp\left(40 \cdot V_d^{(n)}\right)}$$



Newton-Raphson Method-Graphical Interpretation



Convergent

Divergent



Limitations*

- IBIS data can be unpredictable
- Transient response requires solution of nonlinear system
- Most simulators use Newton-Raphson (NR) technique combined with modified nodal analysis(MNA)
- NR may not converge
- NR may slow down simulation
 - * J. E. Schutt-Ainé, "IBIS modeling using Latency Insertion Method," European IBIS summit, Italy, May16, 2012.



Why LIM? *

- LIM does not iterate on nonlinear problems
- There is no convergence issue
- MNA has super-linear numerical complexity
- LIM has linear numerical complexity
- LIM uses no matrix formulation
- LIM has no matrix ill-conditioning problems
- LIM is much faster than MNA for large circuits

* J. E. Schutt-Ainé, "IBIS modeling using Latency Insertion Method," European IBIS summit, Italy, may16, 2012.



Latency Insertion Method**

- LIM is an efficient time-domain simulator for a large-scaled network
- Uses "leapfrog" scheme to solve node voltages and branch currents

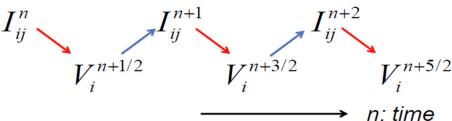
Nodes must have a shunt capacitor

$$V_i^{n+1/2} = \frac{\frac{C_i V_i^{n-1/2}}{\Delta t} + H_i^n - \sum_{k=1}^{M_i} I_{ik}^n}{\frac{C_i}{\Delta t} + G_i}$$

Branches must have an inductor

$$I_{ij}^{n+1} = I_{ij}^{n} + \frac{\Delta t}{L_{ij}} \left(V_i^{n+1/2} - V_j^{n+1/2} - R_{ij} I_{ij}^{n} + E_{ij}^{n+1/2} \right)$$

$$V_i^{n+1} = V_{ij}^{n} + \frac{\Delta t}{L_{ij}} \left(V_i^{n+1/2} - V_j^{n+1/2} - R_{ij} I_{ij}^{n} + E_{ij}^{n+1/2} \right)$$

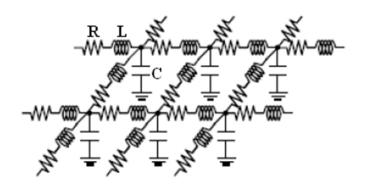


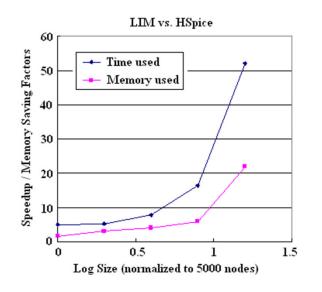
 $G_{i} \underbrace{ \begin{array}{c} C_{i} \\ \\ \end{array} } \underbrace{ \begin{array}{c} C_{i} \\ \end{array} } \underbrace{ \begin{array}{c} C_{ij} \\ \end{array} }_{H_{i}}$

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^{**} J. E. Schutt-Ainé, "Latency Insertion Method for the Fast Transient Simulation of Large Networks," IEEE Trans. Circuit Syst., vol. 48, pp. 81-89, January 2001.

LIM is fast and get faster as circuit size increases

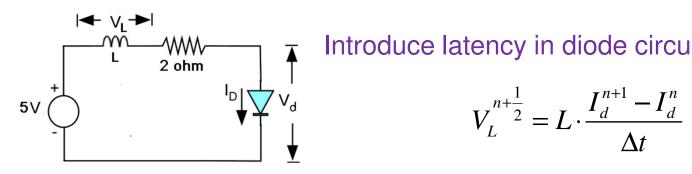




Number of Cells	HSPICE		LIM	
	Memory	Time	Memory	Time
200×200 cells	Memory overflow	abort	102M	1156 s
100×200 cells	320M	9361s	54M	573 s
100×100 cells	108M	2176s	28M	281 s
50×100 cells	53.3M	675s	16 M	132 s
50×50 cells	12.4M	244s	9M	47 s



LIM has NO Convergence Issues



Introduce latency in diode circuit through a small L

$$V_L^{n+\frac{1}{2}} = L \cdot \frac{I_d^{n+1} - I_d^n}{\Delta t}$$

Use Leapfrog:

$$V_{L}^{n+\frac{1}{2}} = L \cdot \frac{I_{d}^{n+1} - I_{d}^{n}}{\Delta t}$$

$$V_{L}^{n+\frac{1}{2}} + 2 \cdot I_{d}^{n} + V_{d}^{n+\frac{1}{2}} = 5$$

$$I_{d}^{n+1} = \frac{\Delta t}{L} \left(5 - 2 \cdot I_{d}^{n} - V_{d}^{n+\frac{1}{2}} \right) + I_{d}^{n}$$

$$V_{L}^{n+\frac{1}{2}} + 2 \cdot I_{d}^{n} + V_{d}^{n+\frac{1}{2}} = 5$$

$$V_{d}^{n+\frac{1}{2}} = \frac{1}{40} \cdot \ln \left(\frac{I_{d}^{n}}{1pA} + 1 \right)$$

Explicit!

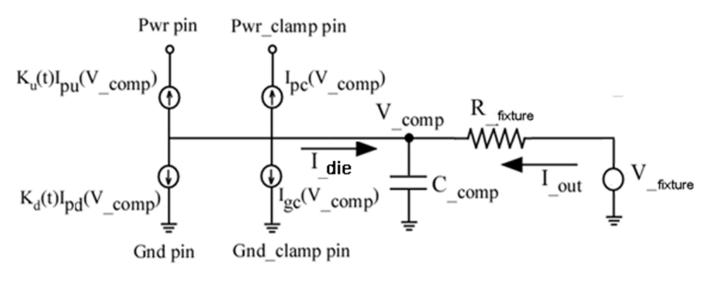
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Application LIM to IBIS

- Ku/Kd extraction
- > LIM-IBIS formulation
- > LIM-IBIS simulation results
- > Extension to Bird98
- > Extension to Bird95
- **Conclusion**



IBIS Ku/Kd Extraction



$$I_{out}^{n} = \left(V_{_fixture} - \frac{V_{_comp}^{n+\frac{1}{2}} + V_{_comp}^{n-\frac{1}{2}}}{2}\right) / R_{_fixture}$$

$$I_{_comp}^{n} = C_{_comp} \frac{V_{_comp}^{n+\frac{1}{2}} - V_{_comp}^{n-\frac{1}{2}}}{\Delta t}$$

$$I_{die}^{n} = I_{_comp}^{n} - I_{out}^{n}$$

Find closest corresponding currents in static IV data

$$V_{comp1} \rightarrow I_{pd1}, I_{pu1}, I_{gc1}$$
 and I_{pc1} $V_{comp2} \rightarrow I_{pd2}, I_{pu2}, I_{gc2}$ and I_{pc2}



IBIS Ku/Kd Extraction***

Two Equations Two Unknowns

$$-I_{die1}^{n} = K_{ur}^{n} I_{pu1}^{n} + K_{dr}^{n} I_{pd1}^{n} + I_{pc1}^{n} + I_{gc1}^{n}$$

$$-I_{die2}^{n} = K_{ur}^{n} I_{pu2}^{n} + K_{dr}^{n} I_{pd2}^{n} + I_{pc2}^{n} + I_{gc2}^{n}$$

The solution is

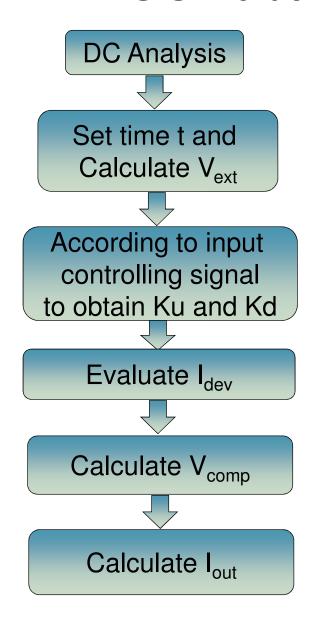
$$\begin{pmatrix} K_{ur}^{n} \\ K_{dr}^{n} \end{pmatrix} = \begin{pmatrix} I_{pu1}^{n} & I_{pd1}^{n} \\ I_{pu2}^{n} & I_{pd2}^{n} \end{pmatrix}^{-1} \begin{pmatrix} -I_{die1}^{n} - I_{pc1}^{n} - I_{gc1}^{n} \\ -I_{die2}^{n} - I_{pc2}^{n} - I_{gc2}^{n} \end{pmatrix}$$

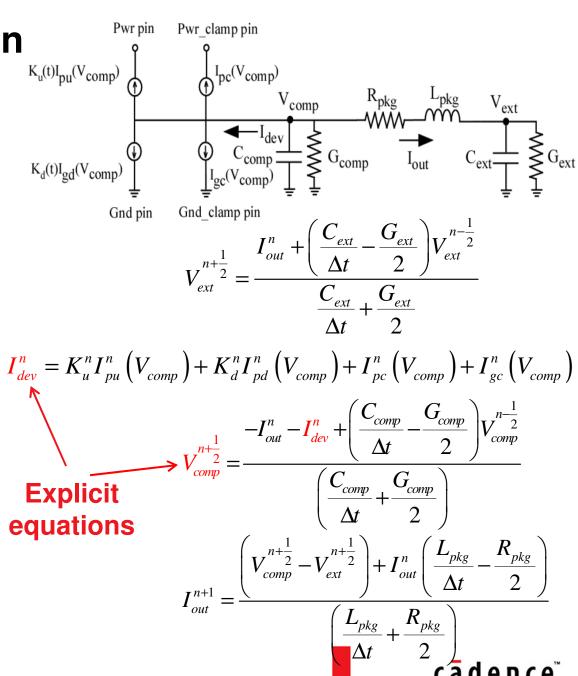
The extraction of K_{uf} and K_{df} is similar.

*** Ying Wang, Han Ngee Tan "The Development of Analog SPICE Behavioral Model Based on IBIS Model", Proceedings of the Ninth Great Lakes Symposium on VLSI, GLS '99.



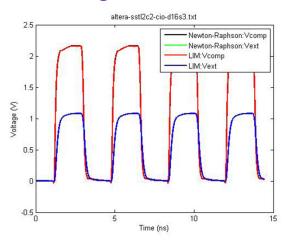
LIM-IBIS Simulation

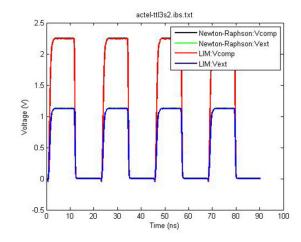




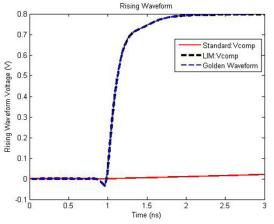
Transient Simulation Results*

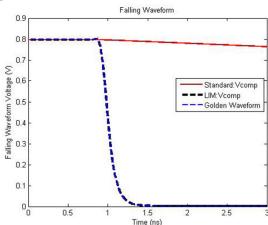
NR and LIM give the same results





In some cases NR fails to converge

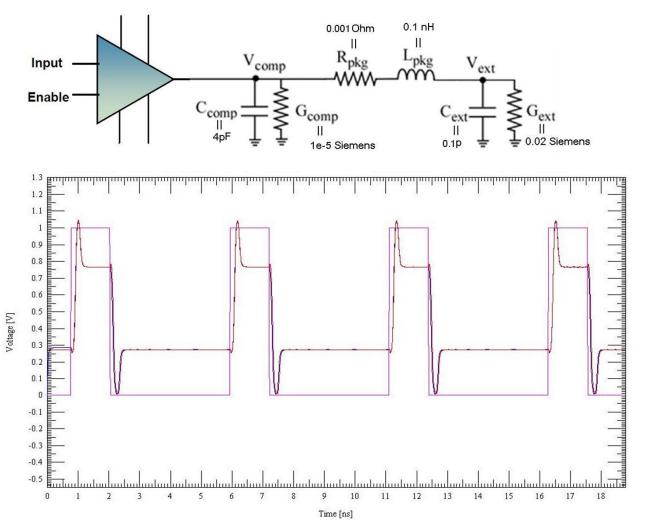




^{*} J. E. Schutt-Ainé, "IBIS modeling using Latency Insertion Method," European IBIS summit, Italy, may16, 2012.



Comparison between LIM and HSPICE





input pulse

HSpice

LIM



Extension to Bird98



LIM-IBIS formulation can **easily be modified** to handle SSN problems

Procedures:

1. use [ISSO PU] and [ISSO PD] tables (IV table) to generate Ksso_pd and Ksso_pu vectors as follows:

Ksso_pd(Vtable_pd) = Isso_pd(Vtable_pd)/Isso_pd(0) Ksso_pu(Vtable_pu) = Isso_pu(Vtable_pu)/Isso_pu(0)

2. Add Ksso_pd and Ksso_pu coefficients to the equations:

Ku(t)Ipu → Ksso_pu(Vtable_pu) *Ku(t)Ipu Kd(t)Ipd → Ksso_pd(Vtable_pd) *Ku(t)Ipd



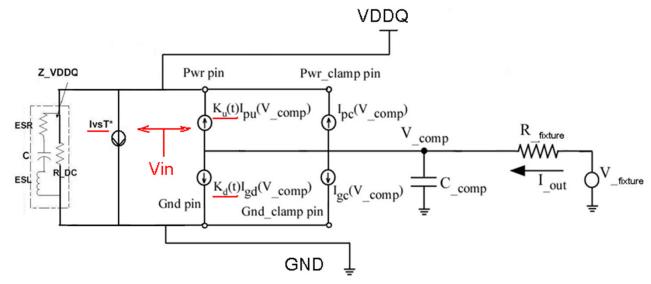
Extension to Bird95

Procedures:

- 1. Obtain composite currents **I_composite** from IBIS 5.0 file;
- 2. Obtain **I_B** from regular IBIS simulation during pre-simulation;
- 3. Obtain the pre-driver current **IvsT***, using

$$IvsT^{*}(t) = I_composite(t) - I_B(t)$$

4. Add IvsT* (t) as a voltage controlled current source (VCCS) in parallel with IBIS B element model.





Conclusions

- LIM can be used to simulate IBIS based circuits accurately;
- LIM does not suffer from convergence problems in handling nonlinear circuits;
- LIM can be extended to handle IBIS 5.0 models;
- LIM is expected to be several orders of magnitude faster for large circuits containing a multitude of IBIS models.



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