WELCOME FROM MICHAEL MIRMAK, INTEL CORPORATION

On behalf of the IBIS Open Forum, I would like to welcome you to our third Asian IBIS Summit on Taiwan. The success of our previous two summits means that we are close to establishing a "tradition" of great events with our IBIS friends and colleagues here.

We are grateful to our generous co-sponsors ANSYS, Agilent Technologies, Cadence Design Systems, Intel Corporation and IO Methodology. Their assistance makes this event possible and we hope that you will encourage them to continue their support. Our thanks also go to our presenters and to you, the attendees, for your interest.

The IBIS Summits are only a part of the regular activities of the IBIS Open Forum. You are invited to participate in all our efforts, including through e-mail discussions and by pursuing Open Forum membership.

We hope that you enjoy the Summit and find the presentations and discussions useful. We wish you luck and success!

- Michael Mirmak
  Chair, IBIS Open Forum

各位 IBIS 開放論壇的与會代表，歡迎您参加我們的第三届亞洲 IBIS 台灣峰會。前兩次峰會的成功，這意味著我們正在建立一個“傳統”，也就是我們的 IBIS 的朋友和他的同事们在這裡的一年一度的技术讨论盛会。

我們非常感謝我們慷慨的赞助商 ANSYS，安捷倫科技，Cadence 設計系統公司，英特爾公司和 IO Methodology (Avant)。他們的協助使得本次活動成为可能，我們也希望他們能繼續支持以后的会议。我們還要感謝我們的演讲人和與會者的大力支持。

IBIS 技术峰會只是 IBIS 開放論壇經常活動的一部分。我们诚邀您參與我們的一切活动，包括通過 e-mail 討論和成为開放論壇的成員。

我們希望您能享受本次會議并發現有用的發言和討論。预祝本次会议圆满。也祝你好運和成功！

马梦宽
主席，IBIS 開放論壇

WELCOME FROM DANIEL CHANG, ANSYS

Dear Experts,

On behalf of ANSYS, we would like to welcome you to join Asian IBIS Summit Taiwan and it is our pleasure can be the primary sponsor this year. We commend and thank you for taking time from your busy schedule to join us for this seminar.

Like the expectations of most of you, this seminar will help us through information on how the new technologies of IBIS improved and updated. The materials are designed to provide accurate and authoritative information. We also would like to extend a very special thanks to distinguished faculty of speakers who are experienced with the nuances and application of the IBIS models.

After a full day of new technologies and information update, we are sure that the experience of taking part in the seminar will be enriching. We eagerly await your participation in the seminar.

Thanks and regards

Daniel Chang
Regional Sales Director,
ANSYS Taiwan

尊敬的各位專家,

我仅代表 ANSYS 歡迎您参加亞洲 IBIS 台灣峰會，這是我們的榮幸能成为今年 IBIS 台灣峰會的主要贊助商。我們感謝您從百忙之中抽出時間来參加本次研討會。

和你的期望一樣，本次研討會將有助於我們通過的 IBIS 来讨论如何对新的技術进行改進和更新的信息。这些咨讯将对新的設計提供準確，權威的资料。我們特別感謝各位傑出的论文演讲者并他们在 IBIS 模型應用方面详细的經驗总结和讨论。

經過一整天的新技術和新信息的讨论，我們相信，本次研討會將给我们提供豐富的技术信息和經驗。我們熱切期待著您的參與研討會。

Daniel Chang

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

8:15 SIGN IN
- Vendor Tables Open at 8:30

9:00 **Welcome**
- Lance Wang
  (Vice-Chair IBIS Open Forum, IO Methodology, USA)
- Daniel Chang
  (ANSYS, ROC)

9:15 **Electronic Interconnect Challenges 5**
Steven Pytel (ANSYS, USA)

9:30 **IBIS 5.1: An Overview 9**
Mirmak, Michael (Intel Corporation, USA)

9:55 BREAK (Refreshments and Vendor Tables)

10:20 **Using Latency Insertion Method to Handle IBIS Models 16**
Ping Liu*#, Jilin Tan*##, and Jose Schutt-Aine**
(*Cadence Design Systems, #PRC, ##USA and
**University of Illinois, USA)

10:55 **IBIS-AMI, Industry Adoption, and Current Challenges 26**
Naijen Hsuan and TingHao Yeh (ANSYS, ROC)

11:25 **Efficient End-to-end Simulations of 25G Optical Links 37**
Jing-Tao Liu*#, Fangyi Rao*##, Sanjeev Gupta** and
Amolak Badesha** (*Technologies, #PRC, ##USA; and
**Avago Technologies, USA)

12:00 FREE BUFFET LUNCH (Hosted by Sponsors)
- Vendor Tables

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

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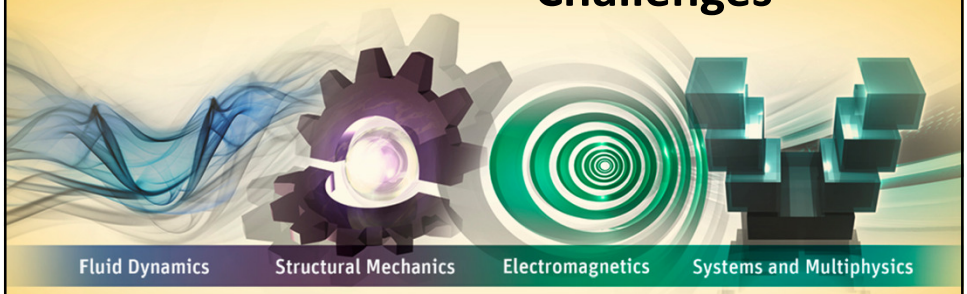
Electronic Interconnect Challenges

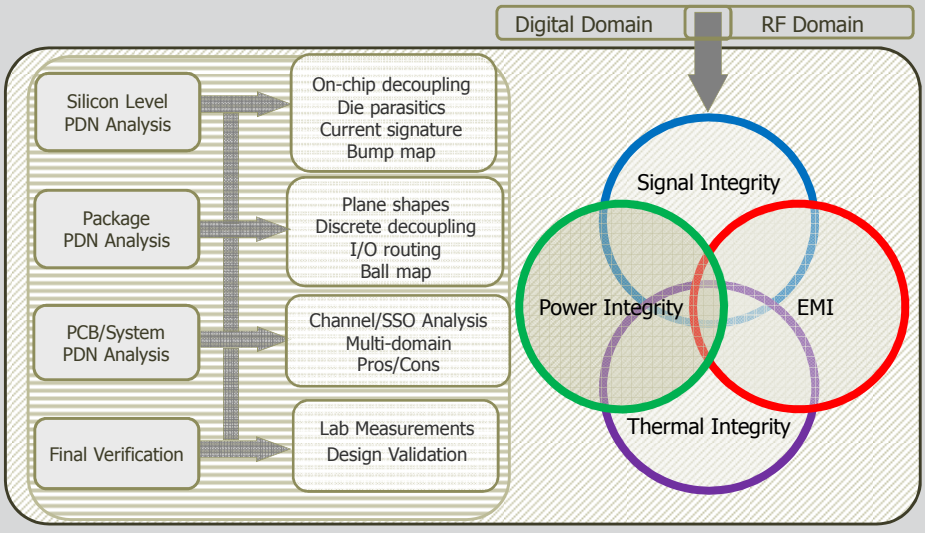


Asian IBIS Summit
Hsinchu, Taiwan
November 13, 2012

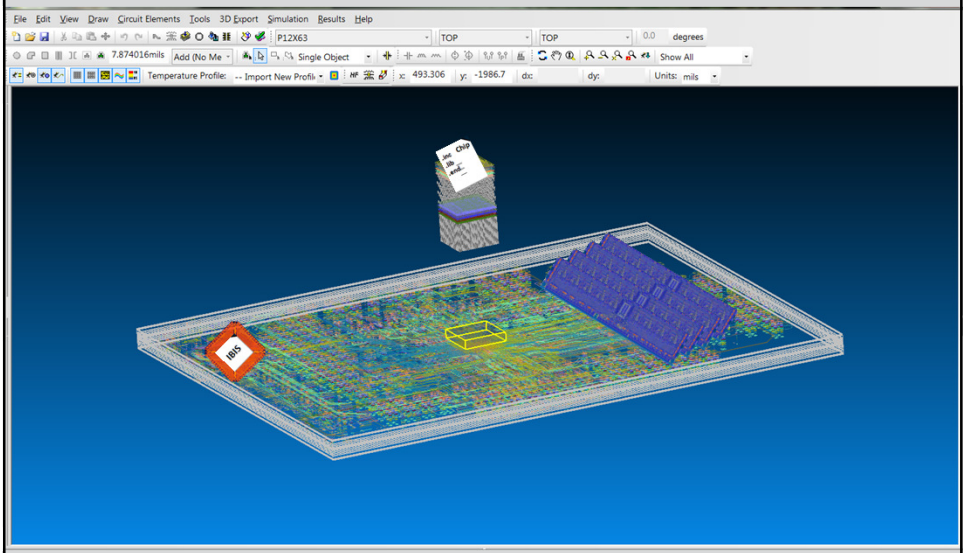
Steven G. Pytel, PhD.
SI Product Manager

ANSYS

Chip Aware System Design



Virtual Platform for System Design



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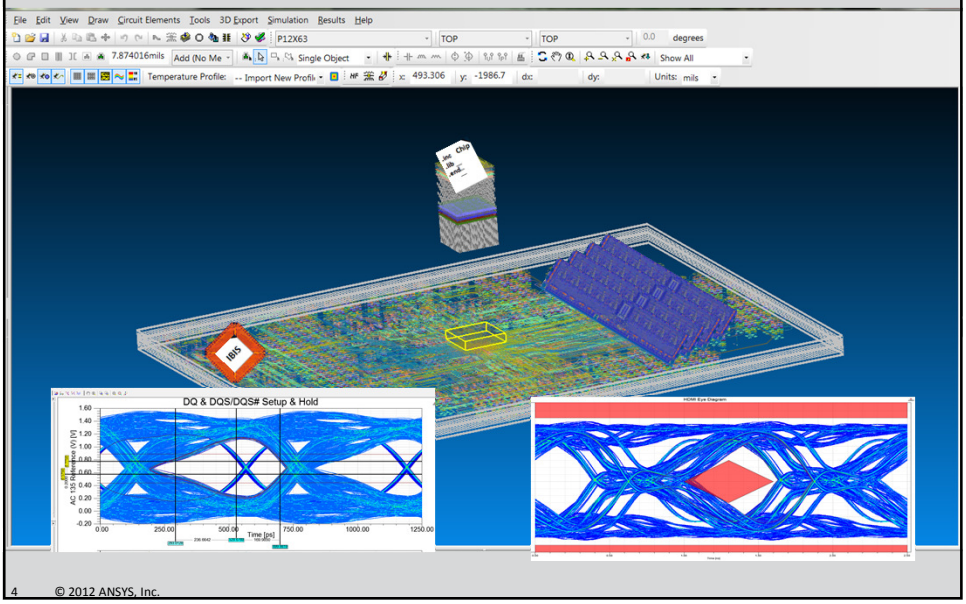
Virtual Platform for System Design



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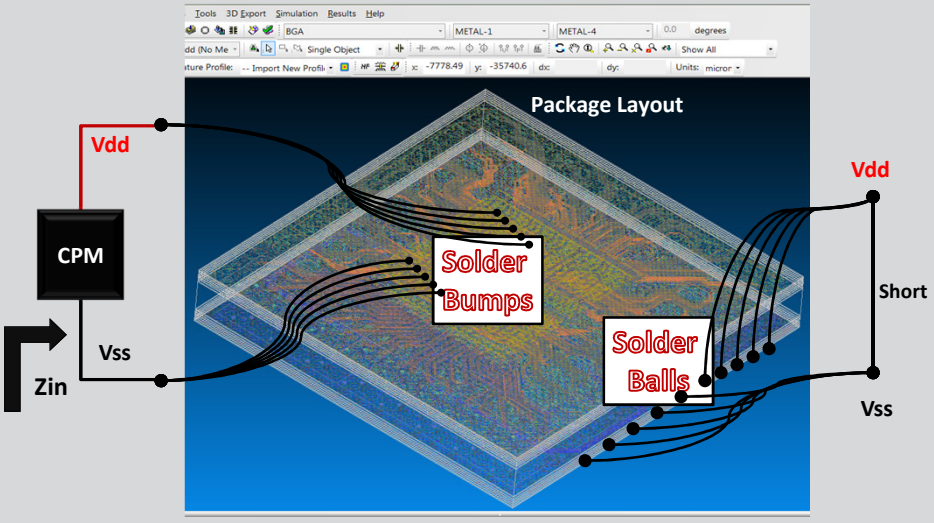
Extraction of Input Impedance



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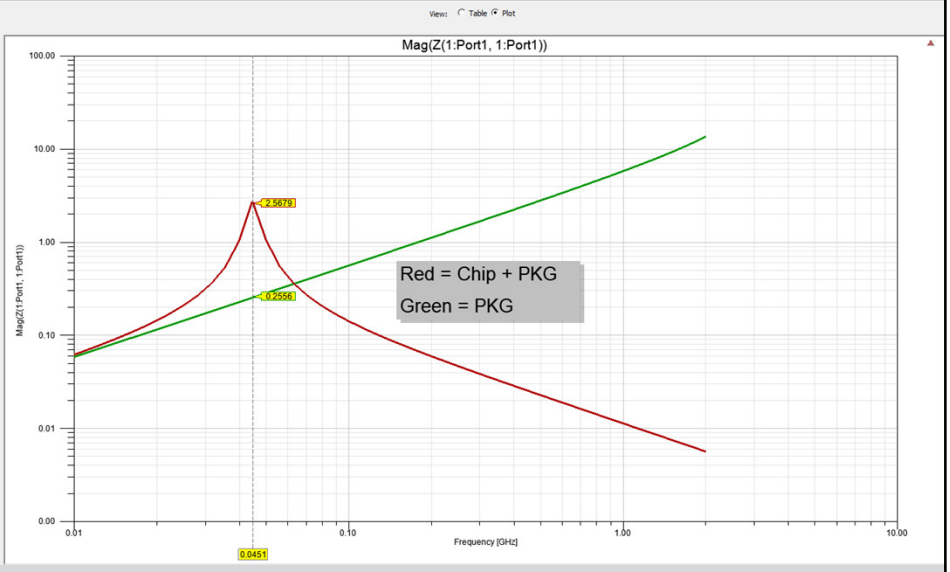
Impedance Results with & without Chip



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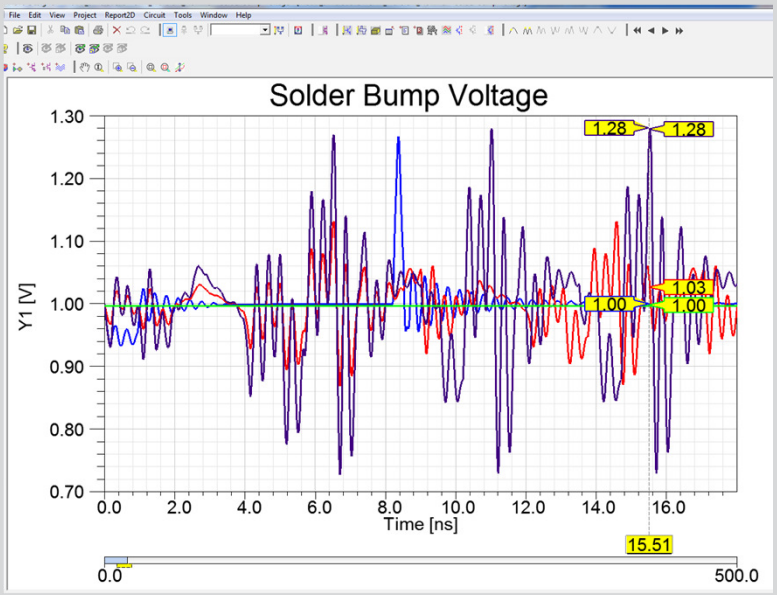
Die Solder Bump Voltage



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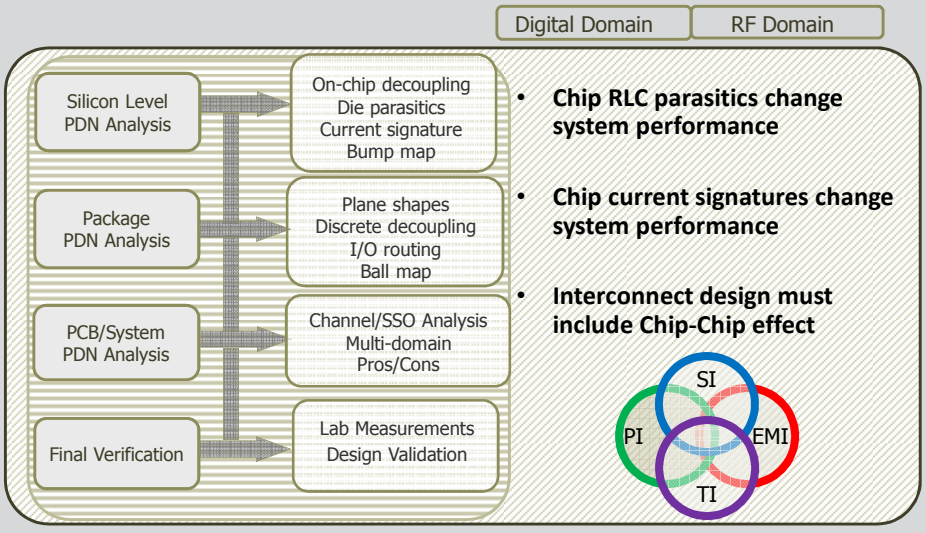
Conclusion



- **Chip RLC parasitics change system performance**
- **Chip current signatures change system performance**
- **Interconnect design must include Chip-Chip effect**

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IBIS 5.1: An Overview

Michael Mirmak (Intel Corporation)
Presented by
Lance Wang (IO Methodology)

Asian IBIS Summit
Hsinchu, Taiwan
November 13, 2012

Expanded from original presented
June 5, 2012

http://www.eda.org/ibis/

Agenda

- Why is IBIS 5.1 different?
- Major Changes
- BIRDs in IBIS 5.1
- Technical Changes
- Before and After
- Next Steps for IBIS
- Your Role: Review and Use!

IBIS 5.1 – A Reformatted Document

- IBIS 5.1 was approved Aug. 24, 2012
- IBIS 5.1 doesn't just add new features and clarifications
  - It's entirely different in appearance and format
- Rationale
  - Ease of change submissions (BIRDs)
  - Ease of editing
  - Improved readability
  - Improved usability, with cross-references & hyperlinks

Major Changes

- Clarifications for AMI and new non-AMI features
  - http://www.eda.org/ibis/birds/
- Appearance based on Microsoft Word*
  - ASCII is no longer used for figures and tables
  - Standards document style has been enforced for headers and body text
- Organization has been unified and improved
  - Terminology has been made more consistent
  - AMI flow, AMI Executable files and AMI Parameters are now more clearly explained, in separate sections (6C, 10 and 10A)

BIRDs in IBIS 5.1

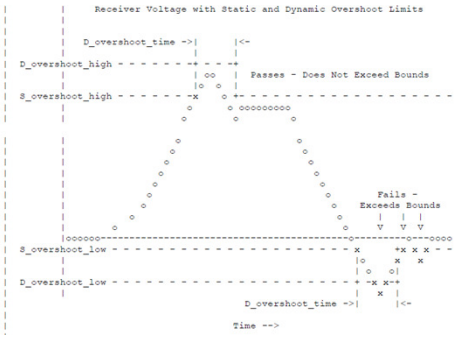
151	IBIS-AMI Modified Reserved Parameters for Jitter/Noise	9-Mar-12
149.1	Usage Out Syntax Correction	17-Feb-12
148	Allowable Model_types with IBIS-AMI	6-Jan-12
146	Clarify sample_interval for IBIS-AMI	9-Dec-11
143.1	Correcting the rules for AMI_Close	7-Oct-11
142	Clarification of [Test Data] and [Test Load] scoping	16-Sep-11
141	[Composite Current] Clarifications	16-Sep-11
140.2	Format Corner and Range Clarification for IBIS-AMI	6-Jan-12
139.2	Reserved_Parameters Order	16-Sep-11
138	IBIS-AMI Section 6c Tables Update	16-Sep-11
137.2	AMI_parameters_in, AMI_parameters_out, msg Clarifications	16-Sep-11
136	Defining Relationships between Type and Format	16-Sep-11
135.1	Add Boolean to BNF for IBIS-AMI	16-Sep-11
134	AMI Function Return Value Clarification	24-Jun-11
133.1	Model Corner C_comp	6-Jan-12
132	Clarification of the Table Format for IBIS_AMI	5-Aug-11
130	Crosstalk Clarification With Respect to AMI	24-Jun-11
127.4	IBIS-AMI Typographical Corrections	9-Dec-11
126	IBIS-AMI New Reserved Parameter AMI_Version	18-Feb-11
120.1	IBIS-AMI Flow Correction	22-Apr-11
115	Clarifying Min/Typ/Max in IBIS-AMI	22-Oct-10
114.3	IBIS-AMI Definition Clarifications	10-Dec-10
113.3	Weak tie-up or tie-down resistance and voltage	19-Nov-10
112	IBIS-AMI clock_times Clarification	11-Jun-10
111.3	Extended Usage of External Series Components in EBDs	24-Apr-09

AMI Technical Changes

- Old AMI files generally still work in IBIS 5.1
- Subtle AMI flow changes
  - Previous flow did not support non-LTI models in TX AMI_GetWave
    - For LTI models, the results should not change
  - AMI_Version identifies .ami files as specifically supporting 5.1 rather than 5.0
  - UseInitOutput has been deprecated
    - Avoids "double-counting" equalization in TX models

Before and After

- Figures and tables have been transformed



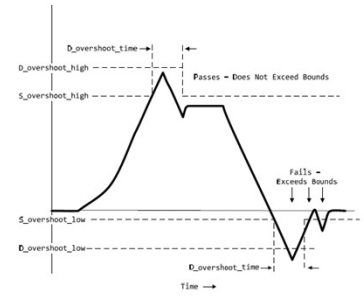


Figure 4 - Receiver Voltage with Static and Dynamic Overshoot Limits

Before…

- The presentation of AMI Parameters…

```
Tx_DCD:

Tx_DCD (Transmit Duty Cycle Distortion) can be of Usage Info
and Out.  It can be of Type Float and UI and can have Data
Format of Value, Range and Corner.  It tells the EDA platform
the maximum percentage deviation of the duration of a
transmitted pulse from the nominal pulse width.  Example of
TX_DCD declaration is:

(Tx_DCD (Usage Info)(Type Float)
        (Format Range <typ> <min> <max>))

Rx-only reserved parameters:

Rx_Clock_PDF and Rx_Receiver_Sensitivity

These reserved parameters only apply to Rx models.  These
parameters are optional; if the parameters are not specified,
the values default to "0".  If specified, they must be in the
following format:

(<parameter_name> (Usage <usage>)(Type <data_type>)
                  (Format <data format>) (Default <values>)
                  (Description <string>))
```

… and After

- The presentation of AMI Parameters…

Parameter: **Tx_DCD**
Required: No
Descriptors:
Usage: Info, Out
Type: Float, UI
Format: Value, Range, Corner, List, Increment, Steps
Default: <numeric_literal>
Description: <string_literal>
Definition: Tx_DCD (Transmit Duty Cycle Distortion) tells the EDA tool the maximum deviation of the duration of a transmitted pulse as a fraction of the nominal pulse width. Entries are assumed to be in units of seconds when declared as Type Float.
Usage Rules:
Other Notes:
Examples:

```
(Tx_DCD (Usage Info)(Type Float)
      (Range 2e-12 1e-12 3e-12))
```


5.1 Parser Now Available!

- A 5.1-compatible Golden Parser has been completed!
  - IBISCHK5, Version 5.1.2, released Oct. 6, 2012
- Free executables available
  - http://www.eda.org/ibis/ibischk5/
  - Source code available under license
- 5.1.2 checks many more .ami file features
- Numerous BUG reports addressed:
  - http://www.eda.org/ibis/bugs/ibischk/

Next Steps

- Future versions will renumber the sections to avoid names such as 10A, 6B, etc.
- Current BIRDs are being rewritten according to the new format
  - 16 BIRDs proposed for *the next IBIS version*
  - Package model improvements, repeaters and backchannel adaptive equalization are addressed
- The next major version: IBIS 6.0
  - Any IBIS 5.2 would be for standardization only

Your Role: Study and Use!

- Please create and test 5.1 models using the new specification and parser!
- Suggestions for the parser, including BUG reports, are welcome
- Review the latest BIRDs proposed for the next IBIS version
  - The schedule for IBIS specification development is accelerating

Thank you for your support of IBIS!

Q/A

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INVENTIVE

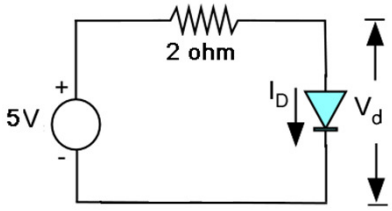
Using Latency Insertion Method to Handle IBIS models

Ping Liu, Jilin Tan
Cadence Design Systems
Presented by: Joseph Kao

José E. Schutt-Ainé
University of Illinois at Urbana-Champaign

Asian IBIS Summit
Hsinchu, Taiwan
November 13, 2012

A simple non-linear Circuit



How to solve I_D and V_d?

Solve transcendental equations

$$I_d = 1pA \cdot \left[\exp\left(40 \cdot V_d\right) - 1 \right]$$

$$5 = V_d + 2 \cdot I_d$$

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Using Newton-Raphson Method

$$X_{n+1} = X_n - \frac{f(X_n)}{f'(X_n)}$$

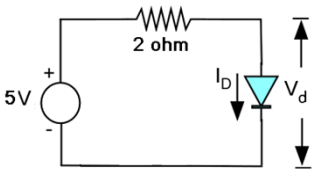
Newton-Raphson iterative process begins with an initial guess and terminates when the difference between successive guesses falls to zero.

$$I_d = 1pA \cdot \left[\exp(40 \cdot V_d) - 1\right]$$

$$5 = V_d + 2 \cdot I_d$$

$$f(V_d) = -5 + V_d + 2pA \cdot \left[\exp(40 \cdot V_d) - 1\right]$$

$$f'(V_d) = 0 + 1 + 80pA \cdot \exp(40 \cdot V_d)$$



$$V_d^{(n+1)} = V_d^{(n)} - \frac{-5 + V_d^{(n)} + 2pA \cdot \left[\exp(40 \cdot V_d^{(n)}) - 1\right]}{1 + 80pA \cdot \exp(40 \cdot V_d^{(n)})}$$

3

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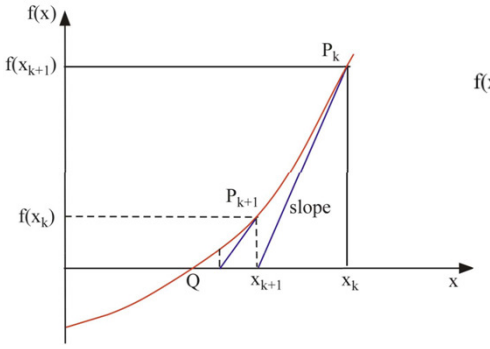
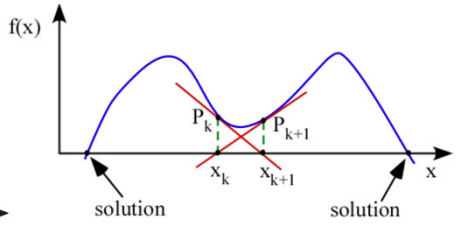
Newton-Raphson Method- Graphical Interpretation





Convergent **Divergent**

4

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Limitations*

- IBIS data can be unpredictable
- Transient response requires solution of nonlinear system
- Most simulators use Newton-Raphson (NR) technique combined with modified nodal analysis(MNA)
- NR may not converge
- NR may slow down simulation

* J. E. Schutt-Ainé, “IBIS modeling using Latency Insertion Method," European IBIS summit, Italy, May16, 2012.

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Why LIM? *

- LIM does not iterate on nonlinear problems
- There is no convergence issue
- MNA has super-linear numerical complexity
- LIM has linear numerical complexity
- LIM uses no matrix formulation
- LIM has no matrix ill-conditioning problems
- LIM is much faster than MNA for large circuits

* J. E. Schutt-Ainé, “IBIS modeling using Latency Insertion Method," European IBIS summit, Italy, may16, 2012.

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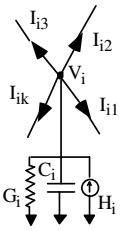
Latency Insertion Method**

- LIM is an efficient time-domain simulator for a large-scaled network
- Uses "leapfrog" scheme to solve node voltages and branch currents

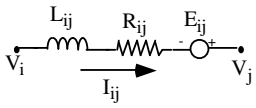
Nodes must have a shunt capacitor

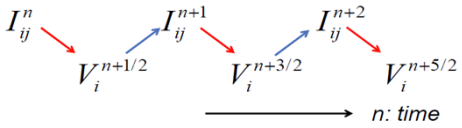
$$V_i^{n+1/2} = \frac{\frac{C_i V_i^{n-1/2}}{\Delta t} + H_i^n - \sum_{k=1}^{M_i} I_{ik}^n}{\frac{C_i}{\Delta t} + G_i}$$



Branches must have an inductor

$$I_{ij}^{n+1} = I_{ij}^n + \frac{\Delta t}{L_{ij}}\left(V_i^{n+1/2} - V_j^{n+1/2} - R_{ij} I_{ij}^n + E_{ij}^{n+1/2}\right)$$





** J. E. Schutt-Ainé, "Latency Insertion Method for the Fast Transient Simulation of Large Networks," IEEE Trans. Circuit Syst., vol. 48, pp. 81-89, January 2001.

7

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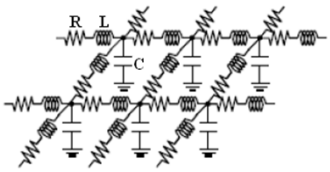
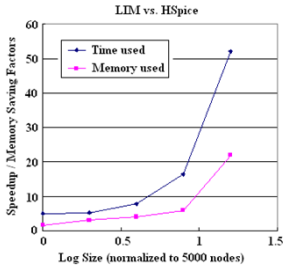
LIM is fast and get faster as circuit size increases





Number of Cells	HSPICE		LIM	
	Memory	Time	Memory	Time
200×200 cells	Memory overflow	abort	102M	1156 s
100×200 cells	320M	9361s	54M	573 s
100×100 cells	108M	2176s	28M	281 s
50×100 cells	53.3M	675s	16M	132 s
50×50 cells	12.4M	244s	9M	47 s

8

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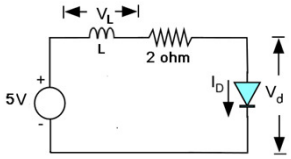
LIM has NO Convergence Issues



Introduce latency in diode circuit through a small L

$$V_L^{n+\frac{1}{2}} = L \cdot \frac{I_d^{n+1} - I_d^n}{\Delta t}$$

Use **Leapfrog:**

$$\left.\begin{aligned} V_L^{n+\frac{1}{2}} &= L \cdot \frac{I_d^{n+1} - I_d^n}{\Delta t} \\ V_L^{n+\frac{1}{2}} &+ 2 \cdot I_d^n + V_d^{n+\frac{1}{2}} = 5 \end{aligned}\right\} \Rightarrow I_d^{n+1} = \frac{\Delta t}{L}\left(5 - 2 \cdot I_d^n - V_d^{n+\frac{1}{2}}\right) + I_d^n$$

$$I_d^{n+1} = 1pA \cdot \left[\exp\left(40 \cdot V_d^{n+\frac{1}{2}}\right) - 1\right] \Rightarrow V_d^{n+\frac{1}{2}} = \frac{1}{40} \cdot \ln\left(\frac{I_d^n}{1pA} + 1\right)$$

Explicit!

9

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Application LIM to IBIS

- Ku/Kd extraction
- LIM-IBIS formulation
- LIM-IBIS simulation results
- Extension to Bird98
- Extension to Bird95
- Conclusion

10

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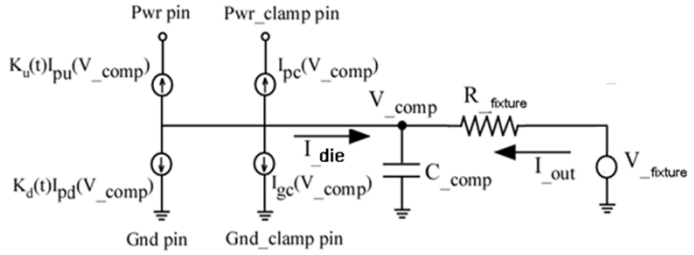
IBIS Ku/Kd Extraction



$$I^n_{out} = \left(V\_fixture - \frac{V^{n+\frac{1}{2}}\_comp + V^{n-\frac{1}{2}}\_comp}{2} \right) / R\_fixture$$

$$I^n\_comp = C\_comp \frac{V^{n+\frac{1}{2}}\_comp - V^{n-\frac{1}{2}}\_comp}{\Delta t}$$

$$I^n_{die} = I^n\_comp - I^n_{out}$$

Find closest corresponding currents in static IV data
V_comp1 -> I_{pd1}, I_{pu1}, I_{gc1} and I_{pc1}
V_comp2 -> I_{pd2}, I_{pu2}, I_{gc2} and I_{pc2}

cadence

IBIS Ku/Kd Extraction***

Two Equations Two Unknowns

$$-I^n_{die1} = K^n_{ur} I^n_{pu1} + K^n_{dr} I^n_{pd1} + I^n_{pc1} + I^n_{gc1}$$
$$-I^n_{die2} = K^n_{ur} I^n_{pu2} + K^n_{dr} I^n_{pd2} + I^n_{pc2} + I^n_{gc2}$$

The solution is

$$\begin{pmatrix} K^n_{ur} \\ K^n_{dr} \end{pmatrix} = \begin{pmatrix} I^n_{pu1} & I^n_{pd1} \\ I^n_{pu2} & I^n_{pd2} \end{pmatrix}^{-1} \begin{pmatrix} -I^n_{die1} - I^n_{pc1} - I^n_{gc1} \\ -I^n_{die2} - I^n_{pc2} - I^n_{gc2} \end{pmatrix}$$

The extraction of K_{uf} and K_{df} is similar.

*** Ying Wang, Han Ngee Tan "The Development of Analog SPICE Behavioral Model Based on IBIS Model", Proceedings of the Ninth Great Lakes Symposium on VLSI, GLS '99.

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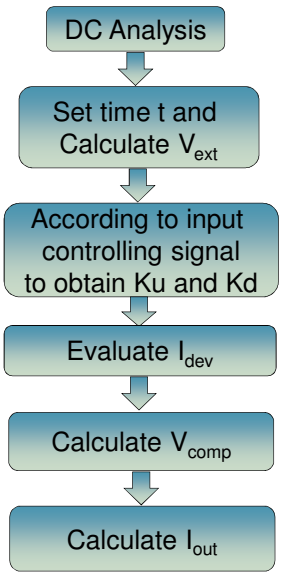
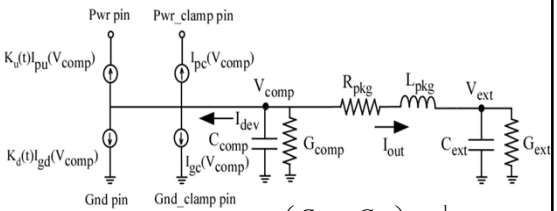
LIM-IBIS Simulation





$$V_{ext}^{n+\frac{1}{2}} = \frac{I_{out}^{n} + \left(\frac{C_{ext}}{\Delta t} - \frac{G_{ext}}{2}\right) V_{ext}^{n-\frac{1}{2}}}{\frac{C_{ext}}{\Delta t} + \frac{G_{ext}}{2}}$$

$$I_{dev}^{n} = K_u^{n} I_{pu}^{n}\left(V_{comp}\right) + K_d^{n} I_{pd}^{n}\left(V_{comp}\right) + I_{pc}^{n}\left(V_{comp}\right) + I_{gc}^{n}\left(V_{comp}\right)$$

Explicit equations

$$V_{comp}^{n+\frac{1}{2}} = \frac{-I_{out}^{n} - I_{dev}^{n} + \left(\frac{C_{comp}}{\Delta t} - \frac{G_{comp}}{2}\right) V_{comp}^{n-\frac{1}{2}}}{\left(\frac{C_{comp}}{\Delta t} + \frac{G_{comp}}{2}\right)}$$

$$I_{out}^{n+1} = \frac{\left(V_{comp}^{n+\frac{1}{2}} - V_{ext}^{n+\frac{1}{2}}\right) + I_{out}^{n}\left(\frac{L_{pkg}}{\Delta t} - \frac{R_{pkg}}{2}\right)}{\left(\frac{L_{pkg}}{\Delta t} + \frac{R_{pkg}}{2}\right)}$$

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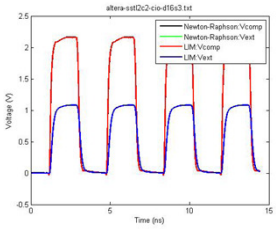
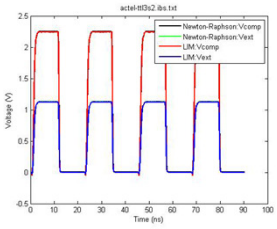
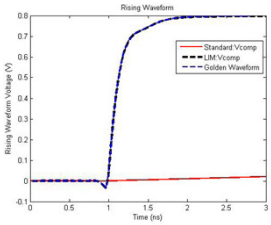
Transient Simulation Results*

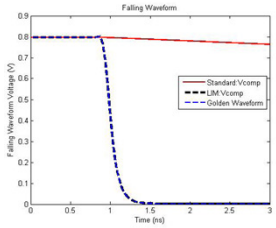
NR and LIM give the same results





In some cases NR fails to converge





* J. E. Schutt-Ainé, "IBIS modeling using Latency Insertion Method," European IBIS summit, Italy, may16, 2012.

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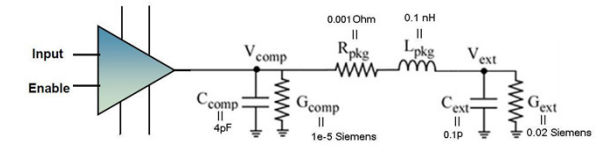
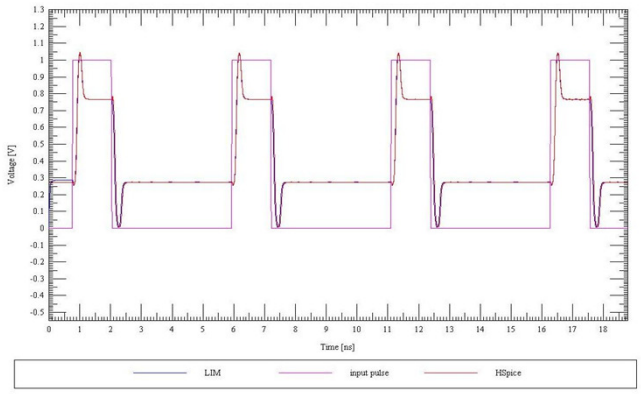
Comparison between LIM and HSPICE





AMI_TX model in ibisamiv2nodiff.ibs file

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Extension to Bird98

LIM-IBIS formulation can **easily be modified** to handle SSN problems

Procedures:

1. **use [ISSO PU] and [ISSO PD] tables (IV table) to generate Ksso_pd and Ksso_pu vectors** as follows:

   Ksso_pd(Vtable_pd) = Isso_pd(Vtable_pd)/Isso_pd(0)

   Ksso_pu(Vtable_pu) = Isso_pu(Vtable_pu)/Isso_pu(0)

2. **Add Ksso_pd and Ksso_pu coefficients to the equations**:

   *Ku(t)Ipu → Ksso_pu(Vtable_pu) *Ku(t)Ipu*

   *Kd(t)Ipd → Ksso_pd(Vtable_pd) *Ku(t)Ipd*

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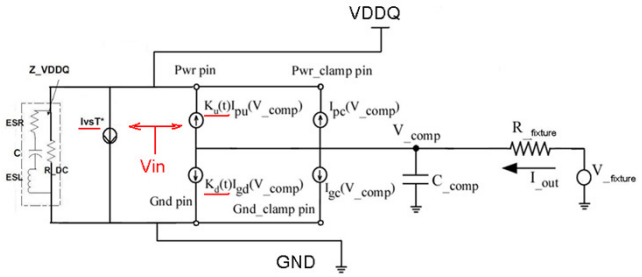
Extension to Bird95

Procedures:

1. Obtain composite currents **I_composite** from IBIS 5.0 file;
2. Obtain **I_B** from regular IBIS simulation during pre-simulation;
3. Obtain the pre-driver current **IvsT***, using

$$IvsT^*(t) = I\_composite(t) - I\_B(t)$$

4. Add **IvsT*(t)** as a voltage controlled current source (**VCCS**) in parallel with IBIS B element model.



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Conclusions

- LIM can be used to simulate **IBIS based circuits** accurately;
- LIM does not suffer from **convergence** problems in handling nonlinear circuits;
- LIM can be extended to handle **IBIS 5.0** models;
- LIM is expected to be several orders of magnitude **faster** for large circuits containing a multitude of IBIS models.

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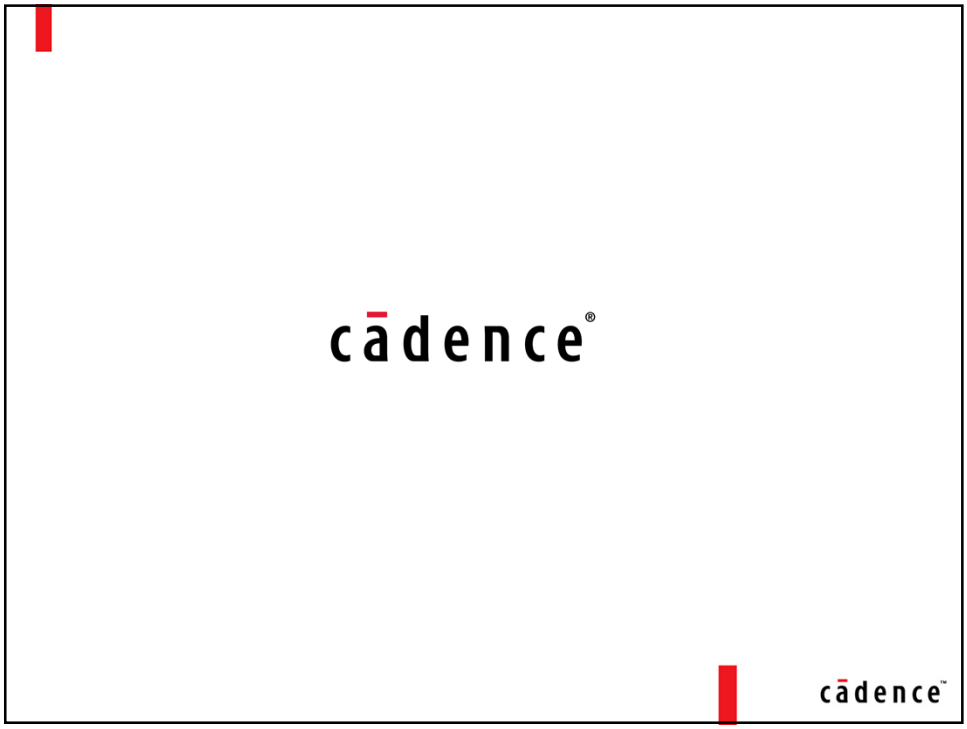
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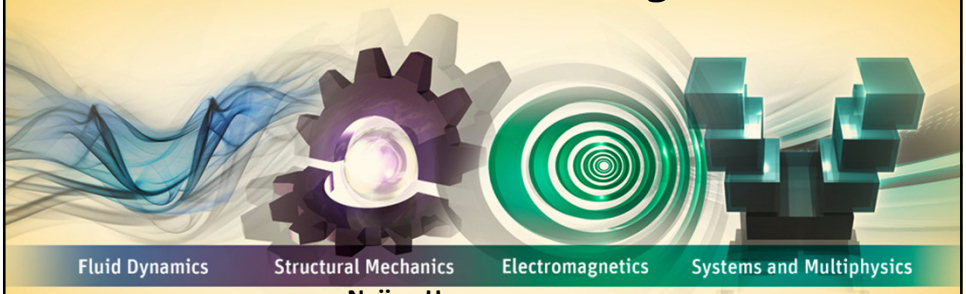
IBIS-AMI, industry adoption, and current challenges



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AMI Challenges Today

AMI models are compiled libraries and text files
- No graphical representation

Package model standard not finalized
- User needs to manually add IC/package parasitics to channel model
- Large S-parameter issue

Each IC vendor has different parameter set
- No standards set
- Each vendor must document their models

AMI simulations depend on accurate channel modeling
- Passivity and causality problem

No standard way to sweep parameters and channel corner effect
- Need to create multiple .AMI files
- EDA tools need to parse arbitrary .AMI parameters
- Six-Sigma design at one flow

SI Challenges Today

High Speed Serial channels are pushing the current limits of simulation. Models/Simulator need to handle current challenges:

- Need to accurately handle very high data rates
- Simulate large number of bits to achieve low BER
- Non-linear ,Time Variant Systems
- TX/RX equalization and vendor specific device settings
- Specific Data patterns and coding schemes
- All types of jitter: RJ, DJ, UJ, PJ, etc.
- XTLK
- Clock Data Recovery circuits
- TX and RX may come from different vendors
- Corner and Manufacturing Variations

IBIS AMI

AMI stands for Algorithmic Modeling Interface

It allows users to specify their own transmitter and receiver models as C-interface compiled libraries

- EDA tool supports Matlab as well as compiled DLLs
- faster signal processing algorithms
- intellectual property protection

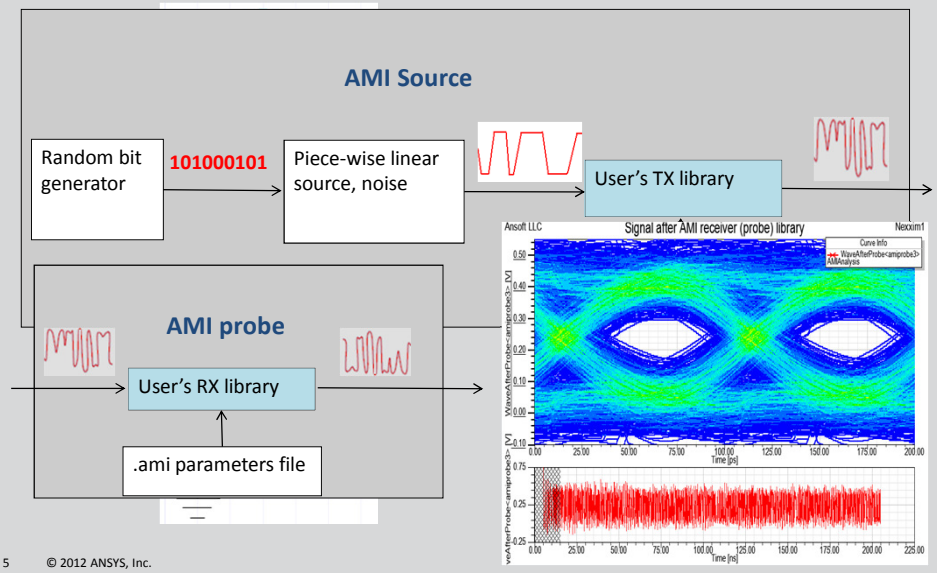
Mainly used in convolution (fast) transient engines for channel simulation

- Designed to be used with fixed time step data

Introduced in IBIS 5.0 specs

- http://eda.org/pub/ibis/ver5.0/ver5_0.txt
- IBIS stand for "I/O Buffer Information Specification"; high-level buffer specification for circuit modeling
- In these specs the library is specified inside the IBIS wrapper and the interface is called IBIS-AMI
- In fact, AMI concept is independent of IBIS

AMI Circuit Example, time domain

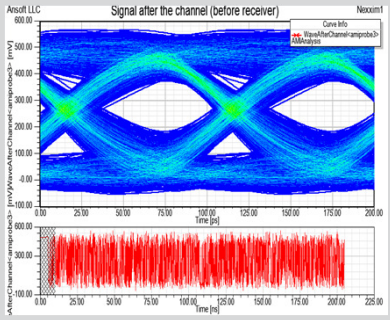


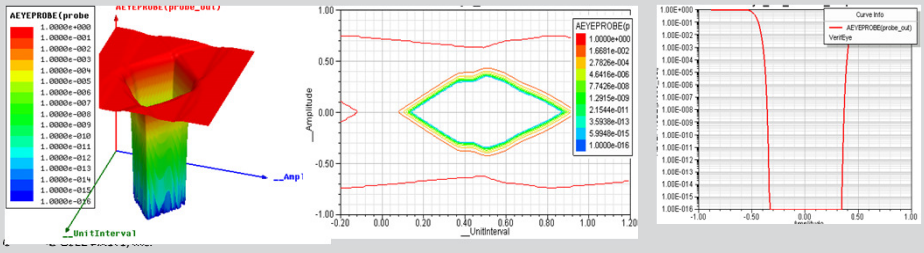
Data Processing

Impulse responses
- Before and after AMI initialization
- frequency domain is also available

Transient data

Eye diagrams
- Bathtub plots
- Contour plots
- Bit-error-rate





Comparison of Simulation Types

Method	Analysis	Advantages	Disadvantages
Traditional IBIS	Transient	Fast	Not accurate
Transistor Level	Transient	Potentially Accurate Handles Non-Linear	Very Slow No Rx Eq IP Liability Not interoperable
Fast Convolution	Quickeye	Very Fast Handles EQ Includes Bit Patterns	Not Silicon Specific LTI Assumption
Statistical	Verifeye	Very Fast Handles EQ	Not Silicon Specific No Bit Patterns LTI Assumption
IBIS-AMI	AMI	Fast Handles Vendor EQ Includes Bit Patterns Not LTI limited	Implementations vary

AMI simulations depend on accurate channel modeling

What can we do about non-passive, non-causal models?

Bypass them

- **Connect inputs to outputs directly and leave S-parameter model out of the simulation**

Leave them as-is

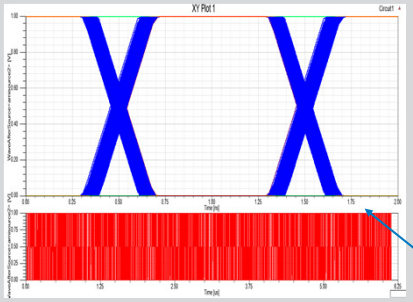
- **The source S-parameter data is non-passive, but the circuit simulation model is sufficiently passive to simulate without problems**

Enforce passivity and causality

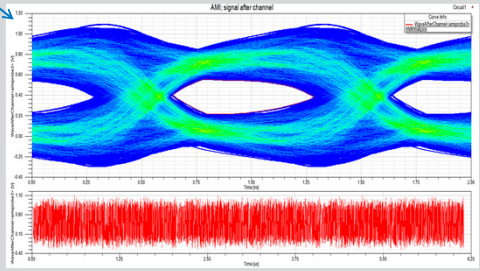
- **Built-in enforcement algorithms to generate passive and causal models**

8

AMI simulations depend on accurate channel modeling



Channel ? passivity ? causality ?



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Corner and Manufacturing Variations

- Usually SI engineers extract only the package or the pcb due to the trade-offs between capacity and simulation time
- For high speed channels, it is important to combine the package and pcb to capture the transitions in 3D
- Merging multi-layer package and pcb in 3D can be cumbersome

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Corner effect information

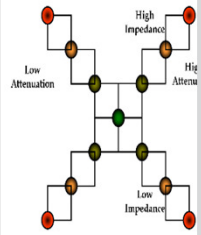
Design Data | Corner Cases Zo-Attn | Parametric | Statistical | Tabular | Queue | Utility: NMF Packer

Degrees of Freedom [Cases]
○ 3-Level Corner [5] ○ 5-Level Corner [9] ◉ 7-Level Corner [13]

Load Settings | Save Settings | Default Settings | Generate Tabular Cases

☑ Single Nominal

Materials		7 point -	5 point -	3 point -	Nominal	3 point +	5 point +	7 point +
	Dielectric Constant	0.85	0.90	0.95	1.00	1.05	1.10	1.15
	Loss Tangent	0.70	0.80	0.90	1.00	1.10	1.20	1.30
	RMS Copper Roughness	0.25	0.50	0.75	1.00	1.25	1.50	1.75
	Copper Conductivity	0.80	0.84	0.87	0.90	0.93	0.96	1.00
Stack-up								
	Copper Thickness	0.85	0.90	0.95	1.00	1.05	1.10	1.15
	Dielectric Thickness	0.85	0.90	0.95	1.00	1.05	1.10	1.15
Geometry								
	Trace Width	0.85	0.90	0.95	1.00	1.05	1.10	1.15



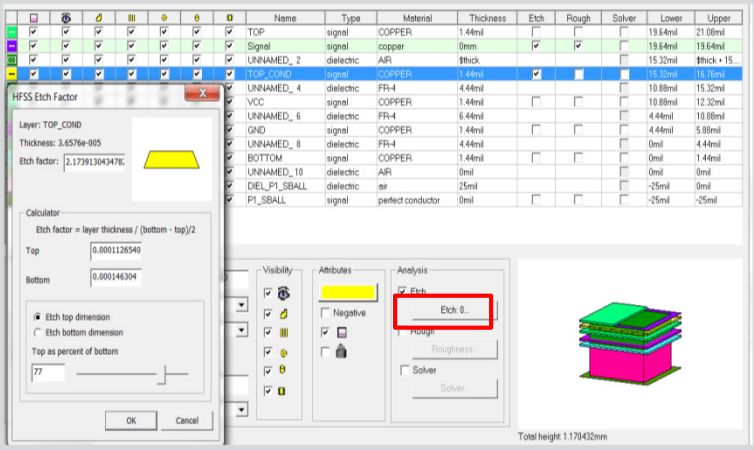
Assigning Variables – Layout Approach

- **Dielectric Thickness**

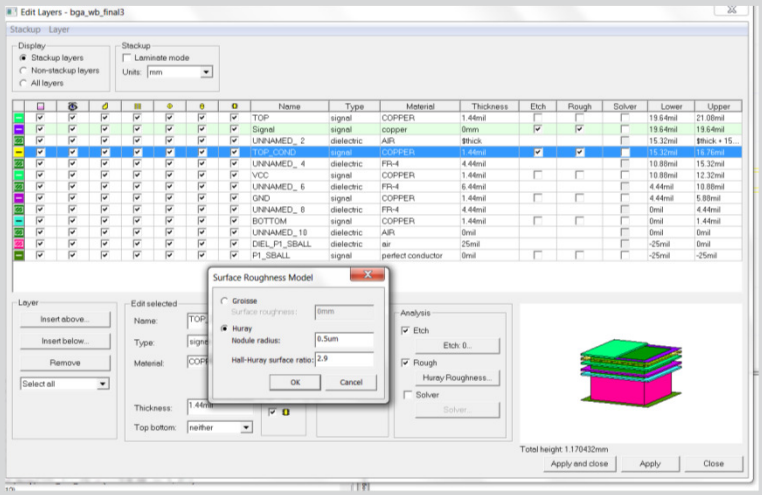
Name	Type	Material	Thickness	Etch	Rough	Solver	Lower	Upper
TOP	signal	COPPER	1.44mil				19.64mil	21.08mil
Signal	signal	copper	0mm	☑	☑		19.64mil	19.64mil
UNNAMED_2	dielectric	AIR	$thick				15.32mil	$thick + 15...
TOP_COND	signal	COPPER	1.44mil				15.32mil	16.76mil
UNNAMED_4	dielectric	FR-4	4.44mil				10.88mil	15.32mil
VCC	signal	COPPER	1.44mil				10.88mil	12.32mil
UNNAMED_6	dielectric	FR-4	6.44mil				4.44mil	10.88mil
GND	signal	COPPER	1.44mil				4.44mil	5.88mil
UNNAMED_8	dielectric	FR-4	4.44mil				0mil	4.44mil
BOTTOM	signal	COPPER	1.44mil				0mil	1.44mil
UNNAMED_10	dielectric	AIR	0mil				0mil	0mil
DIEL_PI_SBALL	dielectric	air	25mil				-25mil	0mil
PI_SBALL	signal	perfect conductor	0mil				-25mil	-25mil

Assigning Variables

- **Etching Factor**

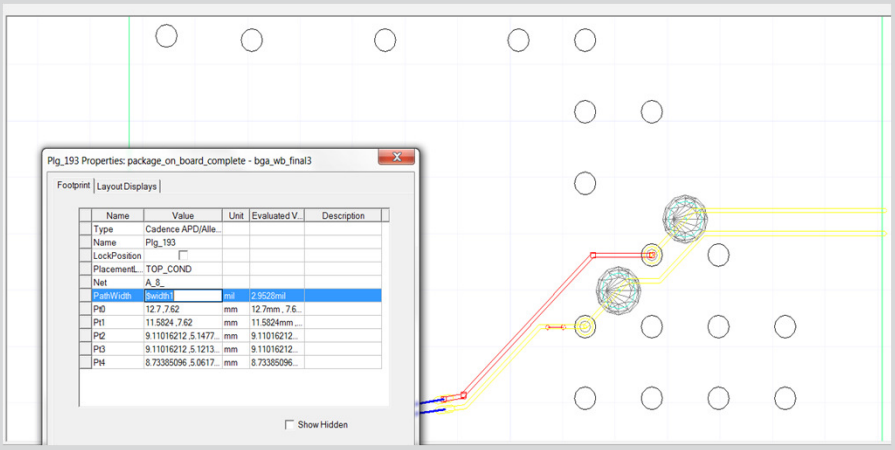


Roughness model : Huray model



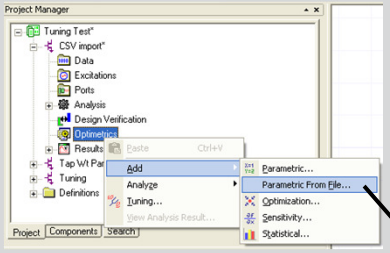
Assigning Variables

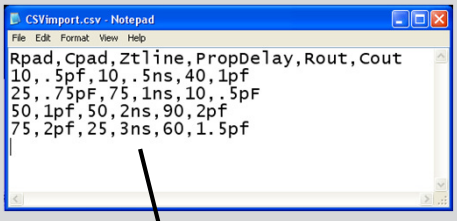
- **Trace Width**

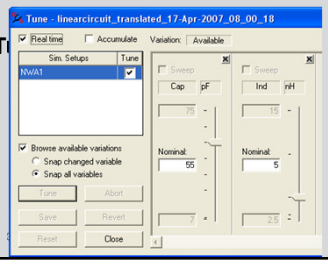


CSV Import for Parametric Analysis

Parametric Batch Mode



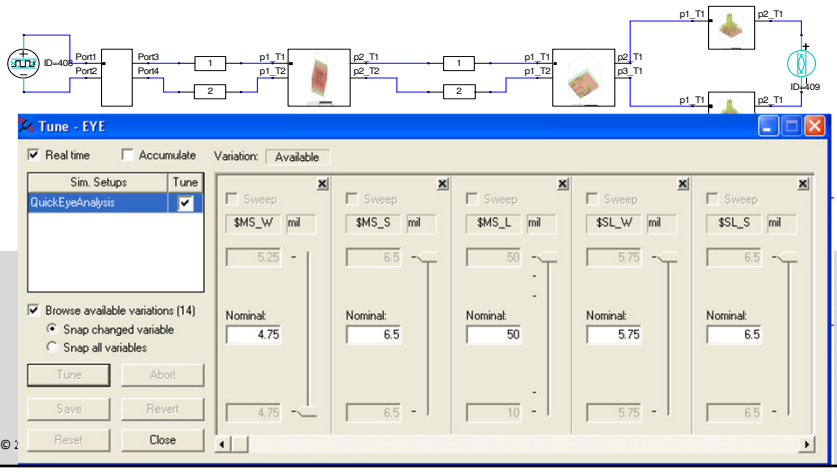




Rpad	Cpad	Ztline	PropDelay	Rout	Cout
10	.5pf	10	.5ns	40	1pf
25	.75pF	75	1ns	10	.5pF
50	1pf	50	2ns	90	2pf
75	2pf	25	3ns	60	1.5pf

Handle all of geometric project and tune for Prbs31 at Tool and Design of Experiments analysis

PRBS31



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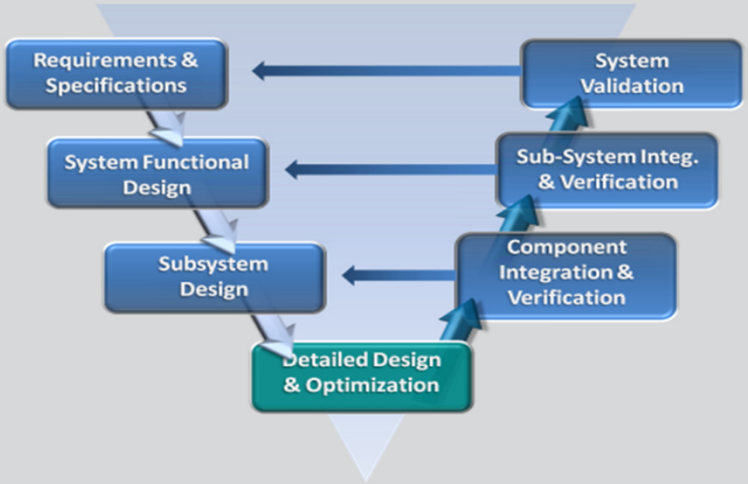
Channel "V" Design for AMI solution



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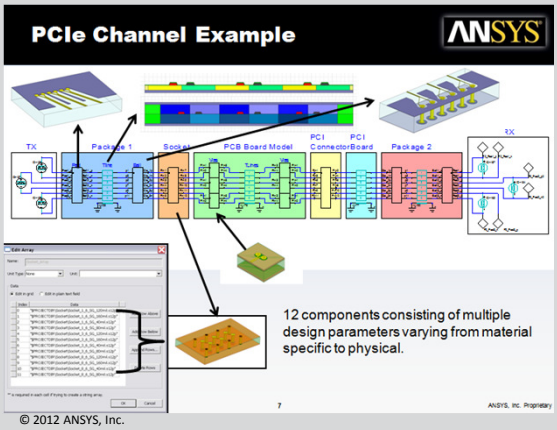
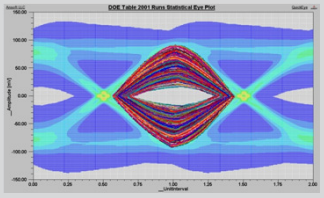
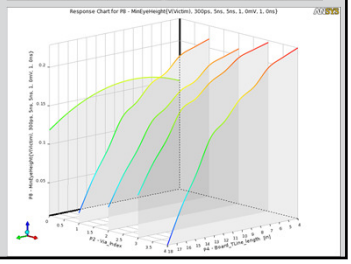
Simulation Approaches :DOE way

- we showed how we can use DOE way to investigate surface responses of a channel design with hundreds parametric variations. But we still had to break down the 3D component designs to small chunks of the board or package to keep simulation times reasonable







AMI Analysis flow

(1) Compute impulse response of the channel (as well of aggressor impulse responses)

- Regular transient analysis

(2) Initialize AMI libraries with the channel response

- Libraries can modify impulse responses

In a loop:

- Generate a block of transmitted bits
- Convert a list of bits into a piecewise-linear rise-fall signal
- Push the signal through the transmitter
- Convolve the signal with the channel
- Push the signal through the receiver
- Post-process the results (eye and bit-error-rate plots)

AMI Analysis flow

(3) Add FFE weight parameter

(4) Add Corner and Manufacturing Variations

(5)Uses the final impulse response from AMI analysis to run VerifEye (statistical eye) analysis

(6) Use DOE way to investigate surface responses of a channel design with hundreds parametric variations and find root cause with min-eye

(7) Six-Sigma Report

Conclusions

Today, It is not easy for SI engineer to take care AMI parameters and high Speed Serial channels manufacturing variations. We need to enforce passive and causal models for channel .By using channel V design , we can do large capacity simulation , and get the best solution for AMI Channel model .

Efficient End-to-end Simulations of 25G Optical Links

Co-Authors

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Fangyi Rao, Agilent Technologies
Sanjeev Gupta, Avago Technologies
Amolak Badesha, Avago Technologies

Presented by Ming-Chih Lin
Senior Application engineer

Agilent EEsof EDA

Asian IBIS Summit
Hsinchu, Taiwan

November 13, 2012

Outline

- Challenges in end-to-end optical link simulation
- AMI Modeling and Simulation Approach for Optical Channel
- Optical Models
- Simulation Results and Discussion
- Summary

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- Challenges in end-to-end optical link simulation
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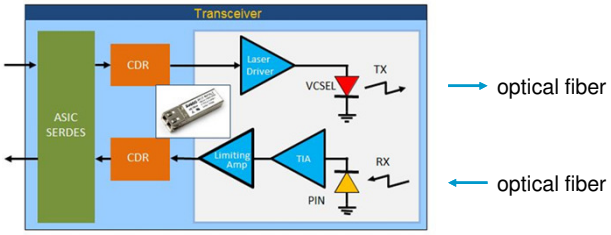
Bandwidth of traditional electrical link is increasingly limited by channel loss above 25G.

Advantages of optical channels:

- Much smaller loss and superior bandwidth
- Flawless connectivity between digital boards and backplanes
- Small footprint
- Reduced EMI
- Promising candidate to replace electrical links

Optical Link System



Inside SerDes Tx & Rx

- Equalization (FFE, CTLE & DFE)
- Clock-data recovery (CDR)

Inside optical module

- Input voltage signal drives VCSEL to emit photons
- Photons propagate along optical fiber
- Photons are converted into photocurrent in PIN
- TIA converts current into output voltage

Challenges in Full Channel Simulation

- Need to model both electrical and optical portions of the link
- Take into account SERDES equalizers and CDR
- Capture behaviors of optoelectronic devices
  - Thermal effects
  - Nonlinearity
  - Optical dispersion and loss
  - Device bandwidth
  - Laser and electrical noise
- Implementation details are proprietary for SERDES and optical Vendors
- Information typically not accessible to external simulator

Outline

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Algorithmic Modeling Interface (AMI) Overview

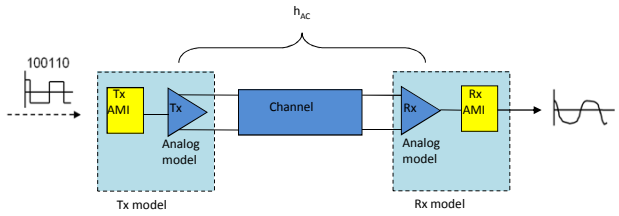
- AMI is introduced in IBIS 5.0
- Defines SERDES behavioral modeling interface
- An AMI model consists of analog model and algorithmic (AMI) block
- Analog model: regular IBIS model, represents rise/fall edge and impedance/load.
- AMI bock: SW executable, models Tx/Rx logics including gain control, equalizers and CDR
- AMI block implements three standard functions

  AMI_Init: performs model initialization and initial EQ optimization

  AMI_GetWave: takes a waveform as input, and returns a modified waveform

  AMI_Close: release model

AMI Simulation Methodology



- Assume Tx analog model, channel and Rx analog model are linear and can be represented by a combined impulse response, h_{AC}.
- Assume high impedance interface between analog model and AMI block so they are electrically decoupled.
- Simulation steps:
  1. Square wave representing bit sequence is sent into Tx AMI
  2. Tx output is convolved with h_{AC}
  3. Resulting waveform is sent into Rx AMI
  4. Rx output is used to calculate eye diagram and BER

Advantages and Limitation of AMI

Advantages of AMI

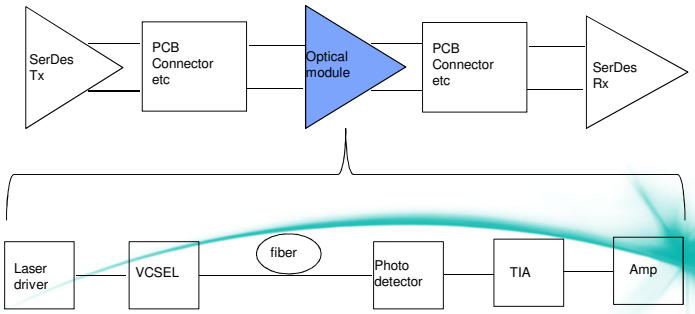
- Models capture SERDES internal functionalities
- IP protection: models are delivered as DLL or/and shared object, concealing implementation details.
- Interoperability between models from different vendors
- Highly efficient link simulation, capable to process millions of bits in minutes

Limitation

- Assumes linear channel
- Optical channel is known to be strongly nonlinear and noisy

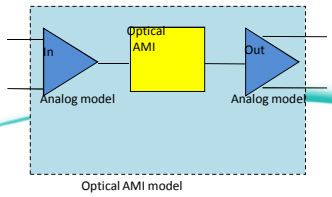
Extending AMI to Optical Channel

- Treat the entire optical module as a mid-channel repeater
- Encapsulate all optical behaviors inside the optical model
- Extend AMI simulation to include repeater



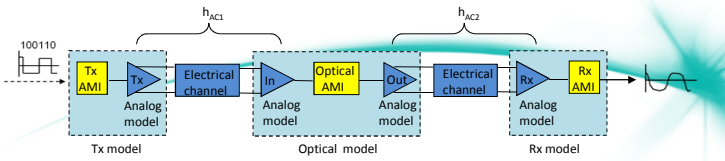
AMI Modeling for Optical Channel

- Model comprises input analog model, optical AMI block and output analog model
- Analog models represent load at input end and impedance at output end
- Optical AMI block encapsulates electrical-optical conversion and photon propagation inside the fiber.
- Optical model is defined in electrical domain. AMI_GetWave takes input voltage waveform, and returns output voltage waveform (same as regular AMI models).
- Interoperable with regular SERDES AMI models.
- Protects optical IP



Full Channel Optical Link Simulation Flow

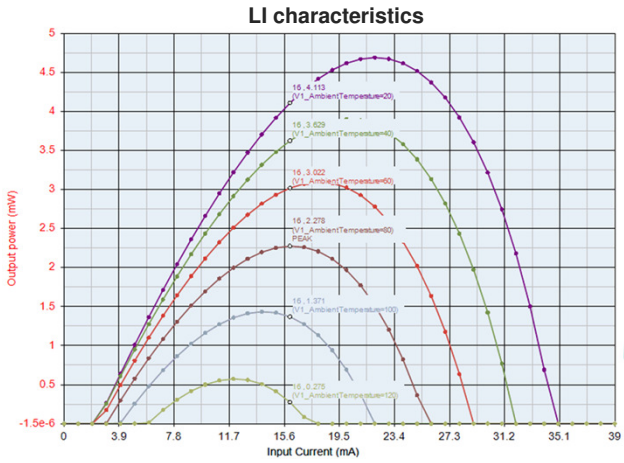
- The link includes SERDES Tx and Rx AMI models and optical AMI model.
- SERDES and optical models are connected by two electrical channels (package, PCB, connector, …)
- Tx analog model, 1st electrical channel and optical input analog model are represented by h_{AC1}
- optical input analog model, 2nd electrical channel and Rx analog model are represented by h_{AC2}
- Simulation steps:
  1. Square wave representing bit sequence is sent into Tx AMI
  2. Tx output is convolved with h_{AC1}
  3. Resulting waveform is sent into optical AMI
  4. Optical output is convolved with h_{AC2}
  5. Resulting waveform is sent into Rx AMI
  6. Rx output is used to calculate eye diagram an BER
- Both SERDES and optics are taken into account w/o exposing SERDES or optical implementation details



Outline

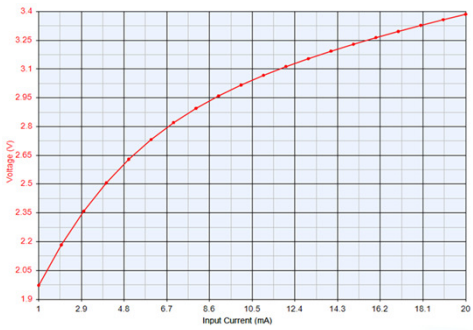
- Challenges in end-to-end optical link simulation
- AMI Modeling and Simulation Approach for Optical Channel
- Optical Models
- Simulation Results and Discussion
- Summary

VCSEL Model



- Strong thermal dependency
- Temperature dependent I_{off}
- Output power rollover

VCSEL IV Characteristics



- IV curve is temperature dependent

Laser Rate Equations

$$\frac{dN}{dt} = \frac{\eta(I - I_{off}(T))}{q} - \frac{N}{\tau_n} - \frac{G_0(N - N_0)S}{1 + \varepsilon S}$$

$$\frac{dS}{dt} = -\frac{S}{\tau_p} + \frac{\beta N}{\tau_n} + \frac{G_0(N - N_0)S}{1 + \varepsilon S}$$

Thermal Rate Equation

$$T = T_0 + (IV - P_0)R_{th} - \tau_{th}\frac{dT}{dt}$$

$$P_0 = kS$$

IV Characteristics

$$V = f(I,T)$$

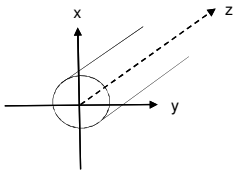
N: carrier number
S: photon number
I: injection current
I_{off}: threshold current
T: temperature
T_0: ambient temperature
P_0: optical power

- $I_{off}(T)$ and f(I,T) functions can be fitted from measured LI and IV curves
- Equations are simplified to improve simulation throughput while maintaining LI and IV characteristics.
- Spontaneous emission noise, gain compression and laser driver bandwidth are also included in the VCSEL model.

Fiber Model

Master Equation

$$\left(\nabla_\perp \frac{1}{\varepsilon(x,y)}\right) \times \left[(\nabla_\perp + ik_z\hat{z}) \times \vec{H}(x,y)\right] - \frac{1}{\varepsilon(x,y)}\nabla_\perp^2 \vec{H}(x,y) + k_z^2 \vec{H}(x,y) = \left(\frac{\omega}{c}\right)^2 \vec{H}(x,y)$$



Dispersion

- Determined by eigenvalues of $\omega(k_z)$
- Waveguide dispersion: photon confinement in fiber
- Material dispersion: frequency dependency of $\varepsilon(\omega)$
- Small pulse spectral width expansion

$$k_z(\omega_0 + \delta\omega) \approx \beta_0 + i\alpha + \beta_1\delta\omega + \frac{1}{2}\beta_2\delta\omega^2 + \cdots$$

ω_0:center frequency of laser spectrum
$k_z(\omega_0) = \beta_0 + i\alpha$

Nonlinear Schrodinger Equation of SM fiber

$$\frac{\partial A}{\partial z} + \alpha A + \beta_1\frac{\partial A}{\partial t} + \frac{i}{2}\beta_2\frac{\partial^2 A}{\partial t^2} = i\gamma|A^2|A$$

PIN Diode and TIA Models

Photon absorption in PIN creates electron-hole pairs and photocurrent

$$I_{ph} = \frac{\eta q}{\hbar \omega} \Phi$$

η:quantum efficiency
Φ: laser power

Other factors considered in the models

- Optical and electrical bandwidth
- Nonlinear transimpedance
- Thermal noise and shot noise

Outline

- Challenges in end-to-end optical link simulation
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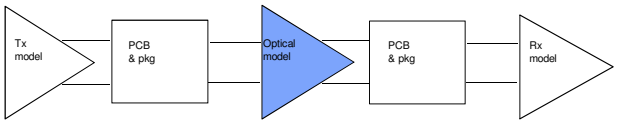
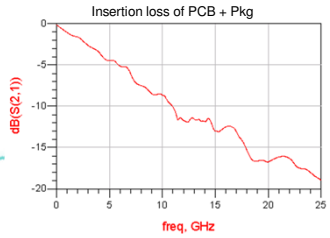
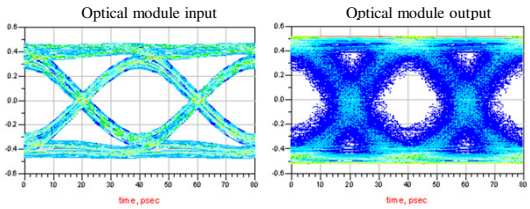
25G Optical Channel

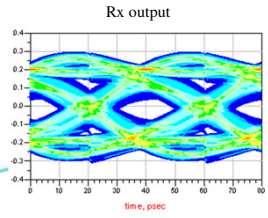


- Tx is a pass-through
- Rx implements voltage-gain control, CTLE, 5-tap DFE and CDR
- SERDES and optical module are connected by Tx/Rx package, PCB and optical package



Eye Diagrams at Room Temperature

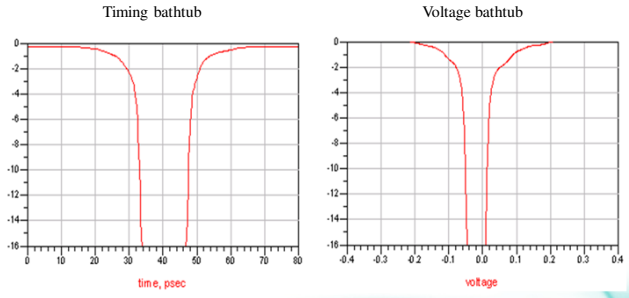




T = 27ºC
Fiber length = 50m

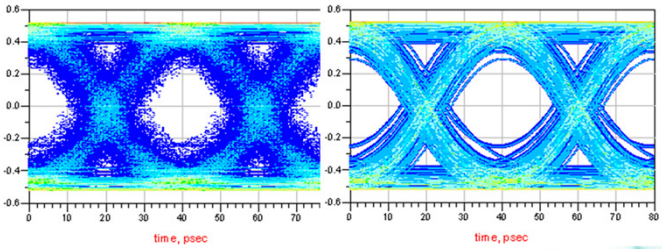
Bathtub Curves

Rx output



Optical Noise Effects

Eye at optical output

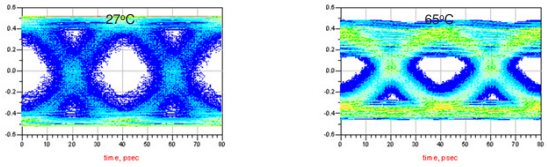


with optical noise

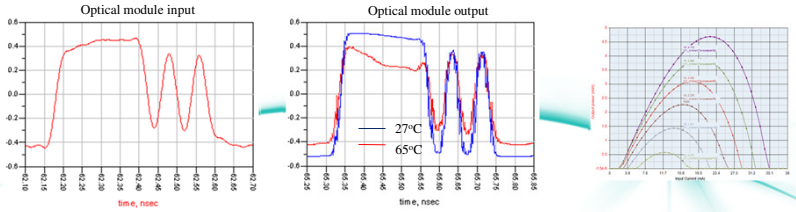
optical noise turned off

Temperature Effects

Eye at optical output

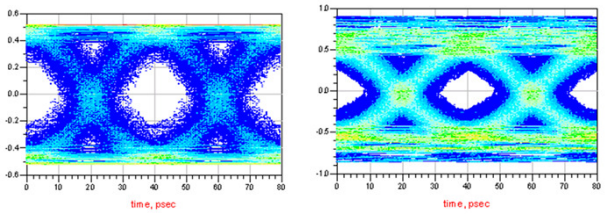


- Output level of long consecutive logic-1 sequence drops as temperature increases
- Caused by VCSEL output power rollover



Nonlinear Effects

Eye at optical output

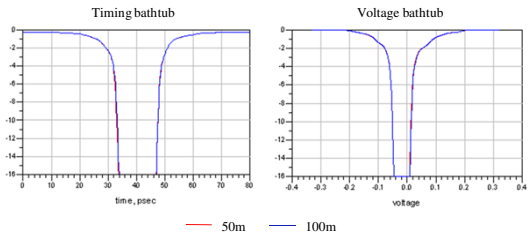


- TIA 1dB compression at 0.4V
- Output amplitude: 1V

- TIA 1dB compression at 2V
- Output amplitude: 1.8V

Fiber Length Effect

Bathtubs at Rx output



Due to low optical loss, length effect is unnoticeable.

Summary

- AMI methodology is applied to model and simulate optical channel
- IP protection to optical vendors
- Interoperable with SERDES models by supporting the same interface
- Enable co-simulation in electrical and optical domains to account for SERDES and optical effects
- Optical models are developed to describe behaviors of laser driver, VCSEL, fiber, PIN and TIA.
- Thermal effects, nonlinearity and optical noise are demonstrated in simulation results
- The approach provides a practical and efficient solution for end-to-end optical link analysis

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INVENTIVE

Chip PDN Model for Power Aware Signal Integrity Analysis

Jack W.C. Lin
Raymond Y. Chen
Presented by: Jack W.C. Lin

Asian IBIS Summit
Hsinchu, Taiwan
November 13, 2012

Outlines

- Traditional SSO analysis
- Chip PDN impact
- Limitation in current IBIS SSO simulation
- Chip PDN contribution to capacitance
- How to generate chip PDN model
- Case study—Using chip PDN in SSO analysis
- BIRD proposal to add chip PDN in IBIS

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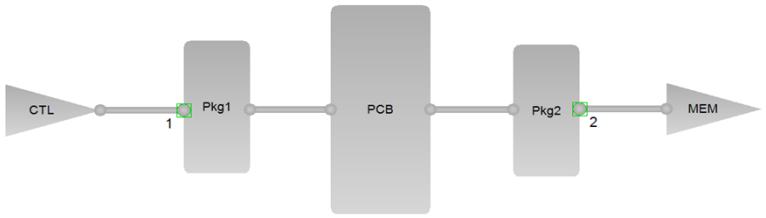
Traditional SSO analysis



- PCB/Package model is extracted by EM solver with signal and power/ground information.
- IBIS without power/ground current and package [Pin]/[Package Model] model are used.
- "Artificially large" power ground fluctuations is observed in SSO analysis due to the lack of PDN model.
- “What if “ RC on die model to mitigate power/ground noise till reasonable level.

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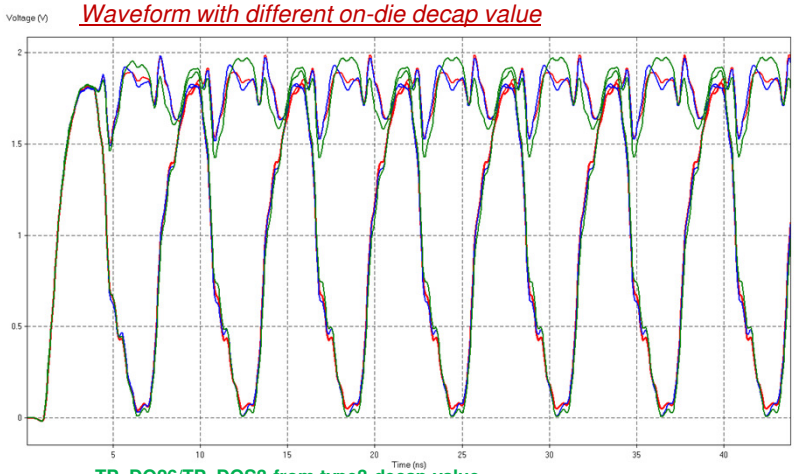
Traditional SSO analysis

1. Driver:1.3nF/0.3 ohms ; Receiver: 1.0nF/0.3 ohms
2. Driver:2nF/0.3 ohms ; Receiver: None
3. Driver:0.5nF/0.3 ohms ; Receiver: 0.5nF/0.3 ohms

Waveform with different on-die decap value



– TP_DQ26/TP_DQS3 from type3 decap value
– TP_DQ26/TP_DQS3 from type2 decap value
– TP_DQ26/TP_DQS3 from type1 decap value

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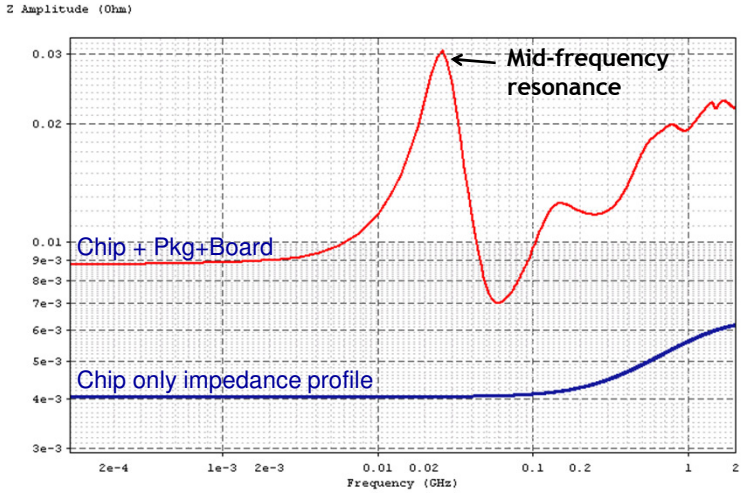
Chip PDN impact



- Chip PDN will help to identify the mid-frequency resonance of the whole system
- This will enhance the power/ground noise if working frequency meet the resonance

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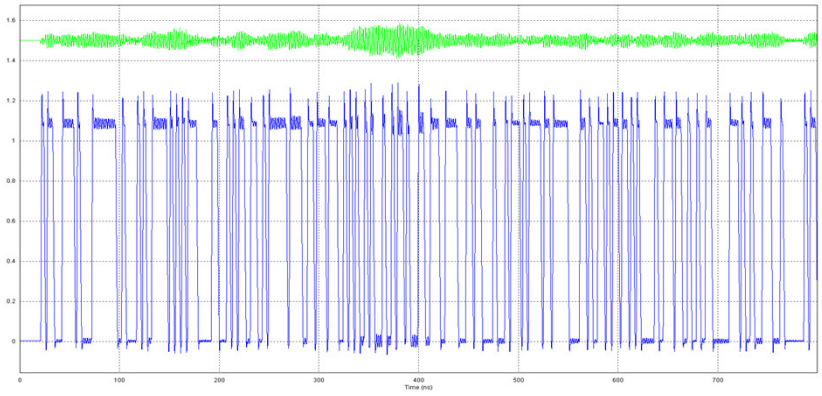
Chip PDN impact



- While performing SSO analysis with random bits pattern, lower frequency transition bits may meet the middle-frequency resonance and lead to larger power/ground noise and worse signal quality.

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Limitation in current IBIS SSO simulation

- IBIS v5.0 is more accurate to simulate the power/ground current with pre-driver/crowbar current and I-V adjusted with Vgs. But IBIS v5.0 only can't still get reasonable power/ground noise.
- Feasible on-die RC model still play a dominant role that impacts the accuracy of the SSO analysis
- On-die RC model is not available from IBIS file.
- On-die capacitance is just estimated from IC designer by how much of MOS caps they placed around I/O cells or estimated by average power dissipation (eq.1)?
- From chip point of view, what are the factors that contribute total on-die capacitance?

C: capacitance of core
P: average power dissipation
f : clock frequency
V: power supply voltage

$$C \sim \frac{P}{V^2 f} \quad \text{Eq.1}$$

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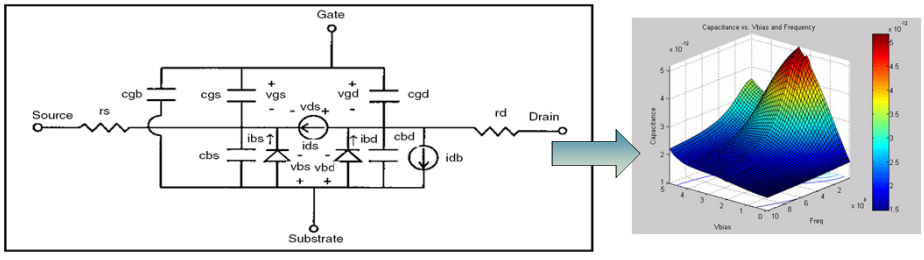
Chip PDN contribution to capacitance

- Parasitics from transistor
  - Parasitic capacitance exists between all MOSFET terminals
  - For the I/O pin, this is modeled in IBIS by C_comp
  - A new compensation capacitor is needed for the power and ground parasitics which is frequency and voltage dependency (first propose by Sigrity in DesignCon 2005)



- MOS Capacitors
  - Like n-MOS capacitors that distributed around I/O circuits

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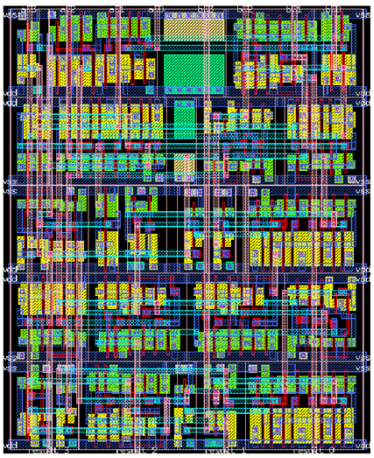
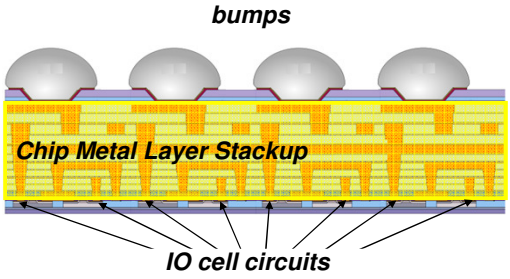
Chip PDN contribution to capacitance

- Outside of the transistors





—Power/ground metal grids outside transistors that contribute capacitance.
—Except MOS caps around I/O cell, MIM caps are distributed on interposer that contributes larger capacitance in current 2.5D IC design

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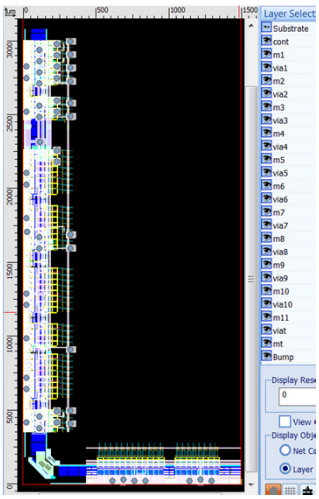
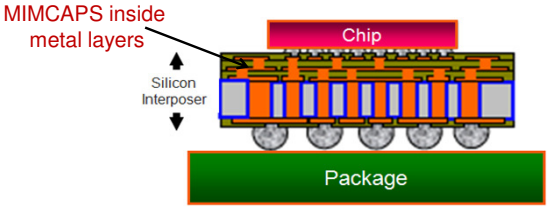
How to generate chip PDN model

- We need to categorize chip PDN model into 2 parts, one is transistor itself, the other is outside the transistor
- IBIS buffer model part only includes circuits and intrinsic parasitic.
- Chip PDN includes GDS layout and MOS capacitors of I/O region.
- Silicon interposer chip design becomes popular and MIMCAPs on interposer contribute sizable capacitance which need to be consider in chip PDN extraction





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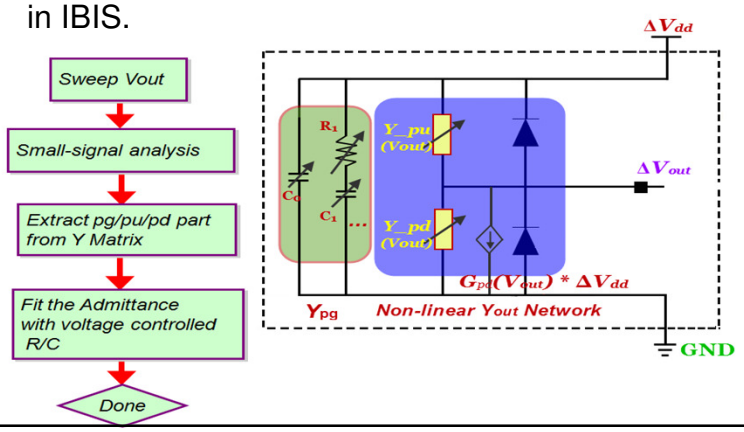
How to generate chip PDN model—transistor

- The IBIS Plus model proposed by Sigrity that dynamic capacitance is included while performing Y admittance extraction between power and ground.
- The equivalent circuit is extracted and added to power/ground pins through [External Model] circuit call in IBIS.



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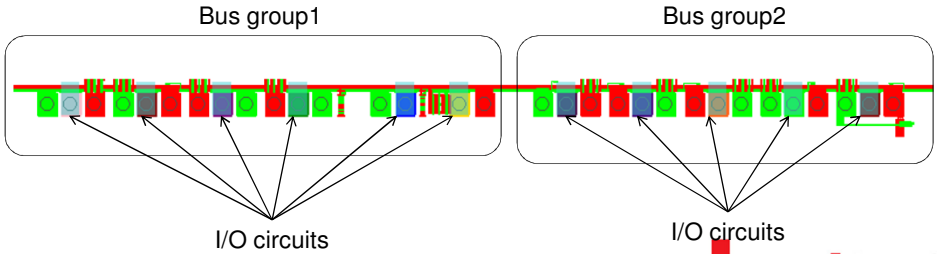
How to generate chip PDN model—outside transistor

- To extract chip PDN by I/O bus group. Same bus group share the same PDN model.
- To set power to ground ports on bumps by different bus group for model extraction
- Capacitance outside the transistor with MOS capacitors can be extracted through chip level extractor.
- The model can be lumped as simple RC value or distributed as SPICE circuit by the concern of frequency bandwidth.



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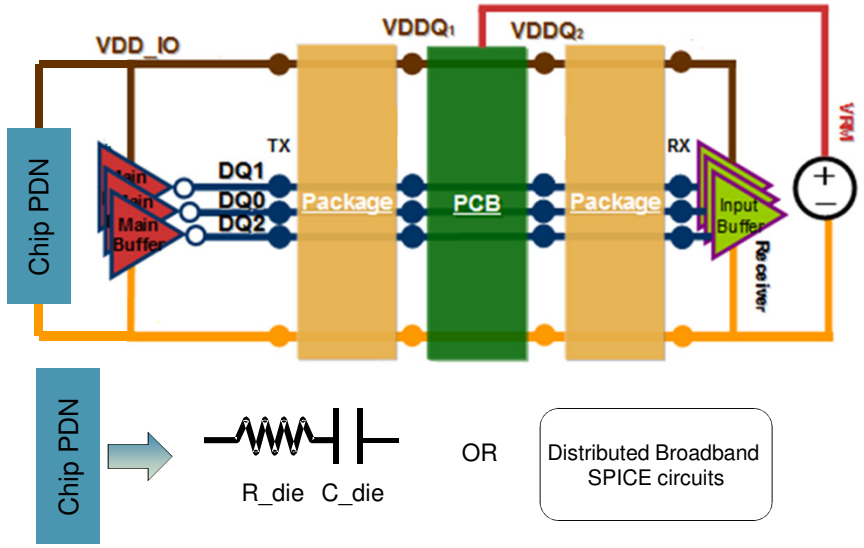
Case study—Using chip PDN in SSO analysis



- Lump RC and distributed broadband model will be applied for SSO analysis with PRBS patterns

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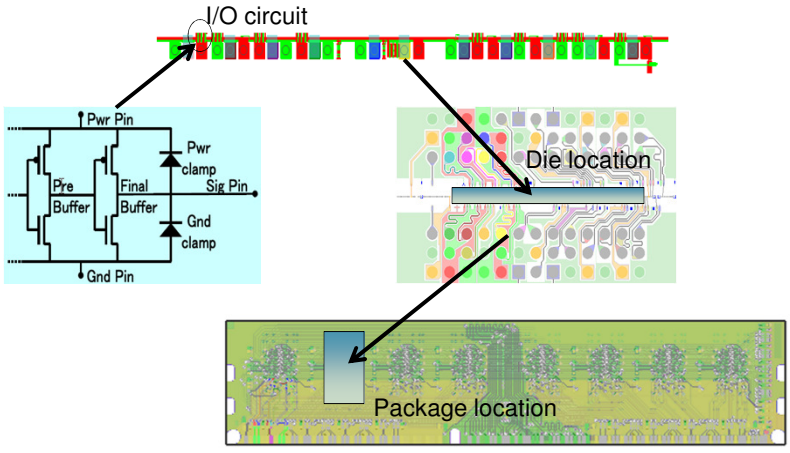
Case study—Using chip PDN in SSO analysis



- I/O circuit is converted into IBIS/IBIS plus model
- Chip is extracted by chip level extractor which include RLCK elements.
- PCB and package are extracted by EM solver and converted into broadband SPICE.
- Only 1 group DDR data is considered for this test

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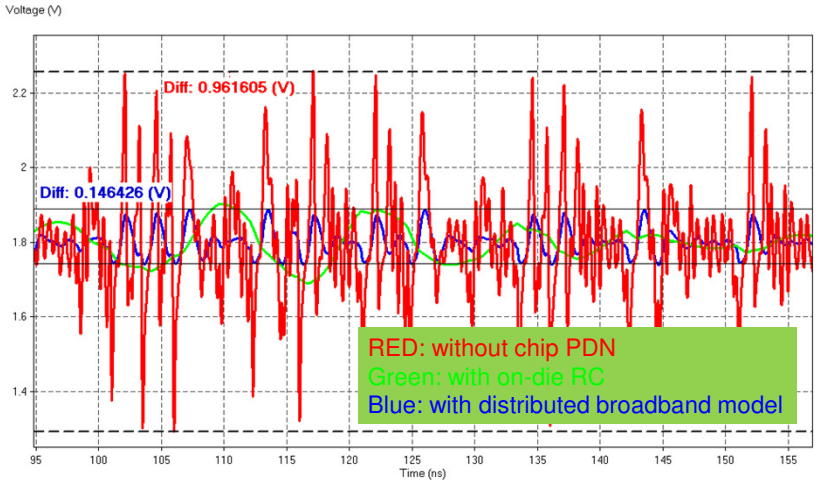
Case study—Using chip PDN in SSO analysis



- On-die RC or better distributed chip PDN model can yield realistic power/ground noise analysis.
- Chip PDN is responsible to filter high frequency noise

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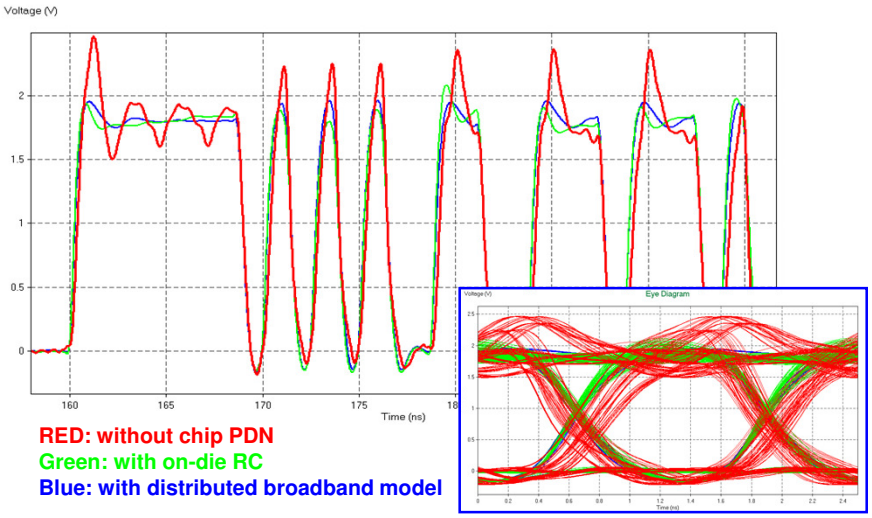
Case study—Using chip PDN in SSO analysis



- Without Chip PDN model, artificially large power/ground noise impact the signal waveform significantly

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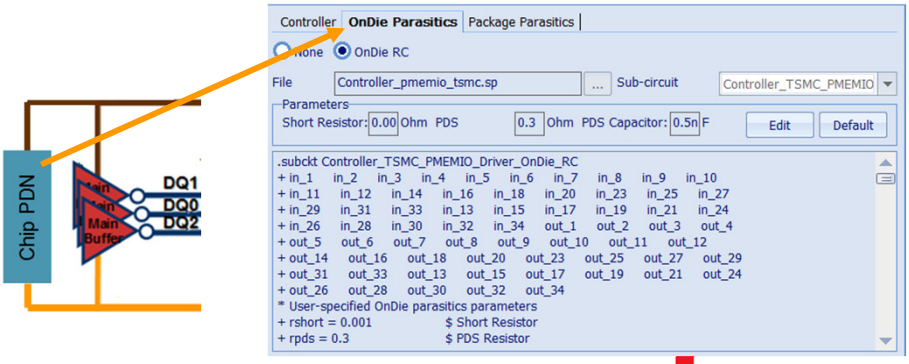
BIRD proposal to add chip PDN in IBIS

- Chip PDN model can be lump RC or SPICE distributed model.
- The chip distributed model is generated by different bus group.
- The bus group is mapping to the bus group in [Pin Mapping] section.
- [Chip PDN Model] can be included in IBIS by [External Model] call



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BIRD proposal to add chip PDN in IBIS

```
[Package Model] DDR3_WBGA_PKG
[Chip PDN Model] DDR_Chip
[Manufacturer]  Cadence
[Package]
.........
[Pin]
.........
[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
B2      GNDBUS2   NC
B3      GNDBUS2   PWRBUS2   GNDBUS2   PWRBUS2
B7      GNDBUS2   PWRBUS2   GNDBUS2   PWRBUS2
B8      GNDBUS2   NC
B9      NC        PWRBUS2
C2      GNDBUS2   PWRBUS2   GNDBUS2   PWRBUS2 |GNDBUS2 is VSSQ
C3      GNDBUS2   PWRBUS2   GNDBUS2   PWRBUS2 |PWRBUS2 is VDDQ
[Define Chip PDN Model]
[Manufacturer] Cadence
[Description]   3mmx3mm Flip-Chip
[External Model]
Language SPICE
|
| Corner  corner_name  file_name  circuit_name
Corner   Typ        chip_PDN.ckt   vddq_pdn
|
| Ports List of port names (in same order as in SPICE)
Ports A_puref A_pdref
```

bus name is mapping to sub-circuit nodes

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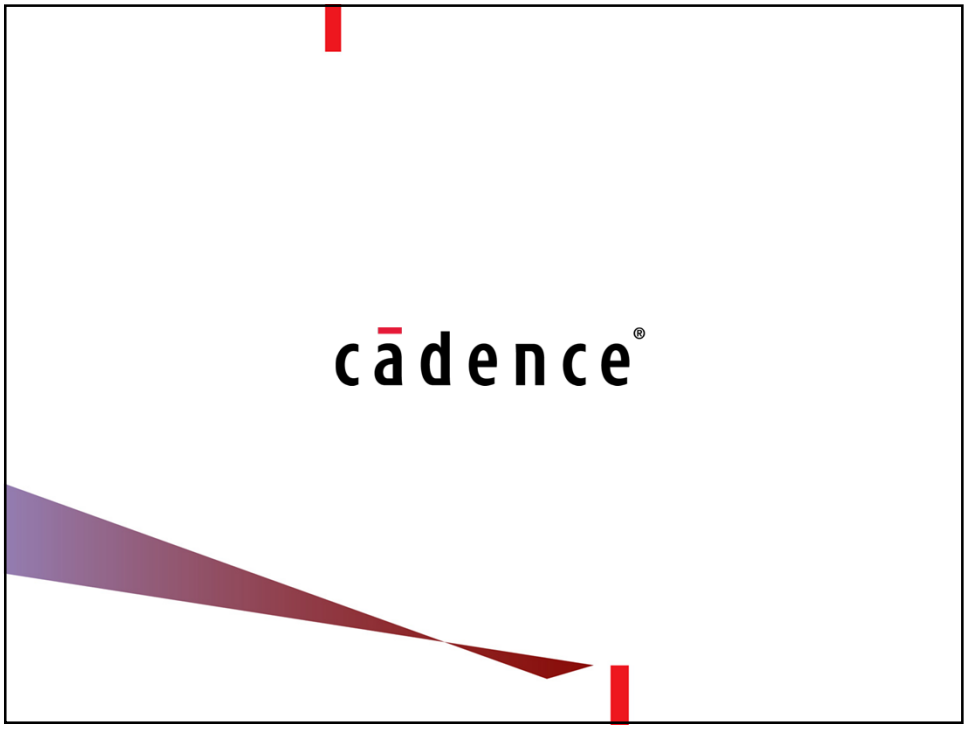
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IBIS Parser Update

Bob Ross
Asian IBIS Summit
Hsinchu, Taiwan
November 13, 2012
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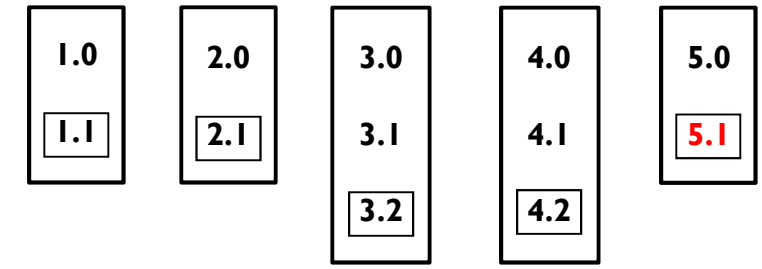
(presented by Anders Ekholm, Ericsson)

Outline, Specifications and Parsers

- IBIS through Version 5.1
  - ibischk5
- Touchstone Version 2.0
  - tschk2
- Conclusions

Valid IBIS Versions and Latest ibischk Versions



ibis_chk	ibischk2	ibischk3	ibischk4	ibischk5
V1.1a	V2.1.17	V3.2.9	V4.2.2	**V5.1.2**

IBIS Parser Major Version Logic

- Subversions upgraded to **last** major version
  - **V5.1** upgrades V5.0
  - **V4.2** upgraded V4.0 and V4.1
  - **V3.2** upgraded V3.0 and V3.1
  - **V2.1** upgraded V2.0
  - **V1.1** upgraded V1.0
- **V5.1** checks **V1.1**, **V2.1**, **V3.2**, **V4.2**, and **V5.1** levels for features and corrections

Downward Compatibility

- Current IBIS **downward compatible** with all earlier features and syntax
  - Prior EDA implementations supported
  - Existing models remain valid
  - Specification includes all features
  - Earlier specification mistakes corrected
- Specification well tested and corrected

IBIS-AMI Version Exception

- IBIS-AMI subversions supported by the **.ami** format
- **AMI_Version** required for "**5.1**" files and **later**
  - First Reserved Parameter
  - Use_Init_Output **not legal**
- **Omission** of **AMI_Version implies** "5.0" level
  - Use_Init_Output **legal**
  - **All other AMI_Version "5.1" rules apply**
- Later AMI_Version levels will have more features and possible deprecation at the subversion level
- Later Specification will track all subversion changes

"ibischk5" Parser

- Ibischk5, Version 5.1.2
  - Free executables: http://www.eda.org/ibis/ibischk5/
  - Bug reports: http://www.eda.org/ibis/bugs/ibischk/
- Checks all [IBIS Ver]s of IBIS files
- Over $117,000 of contracted work since 1993
- Supports .ibs, .pkg, .ebd, and .ami formats
  - directly or through higher level linkages

Flags in ibischk5

```
Usage: ibischk5       <IBS filename>
     : ibischk5  -ebd <EBD filename>
     : ibischk5  -pkg <PKG filename>
     : ibischk5  -ami <AMI filename>
Usage: ibischk5  -caution -numbered      <IBS filename>
     : ibischk5  -caution -numbered -ebd <EBD filename>
     : ibischk5  -caution -numbered -pkg <PKG filename>
     : ibischk5  -caution -numbered -ami <AMI filename>
The flags prior to the file name can be in any order,
and the -caution and/or -numbered flags are optional.
```

- **–ami** for <file_name>.ami (algorithmic model interface control file)
- **–numbered** for numbered **E**rror, **W**arning, **N**otes and **C**aution messages

ibischk5 {–numbered} –ami file4.ami

```
Checking file4.ami for IBIS 5.0 Compatibility...

ERROR - Illegal Usage value A specified for Param1
ERROR - Illegal Type value B specified for Param1
ERROR - Illegal Format value C specified for Param1
ERROR - No Reserved_Parameters found

Errors  : 4

File Failed
```

```
Checking file4.ami for IBIS 5.0 Compatibility...

E4627 - Illegal Usage value A specified for Param1
E4627 - Illegal Type value B specified for Param1
E4627 - Illegal Format value C specified for Param1
E4622 - No Reserved_Parameters found

Errors  : 4

File Failed
```


Message Number File Being Updated (Over 1150 unique message strings)

Number	Symbol in Code	Message string	Parameters	Comment	Category	Clasification
100	MDL_ERR_0	Unable to Allocate Memory: %s %d	filename, line number	The code failed to allocate memory in <filename> at <linenumber>	Internal Error	E
101	MDL_ERR_1	Unable to get IBIS structure		Program data structures are corrupt	Internal Error	E
102	MDL_ERR_2	Orphan Model keyword.		Model keyword found but not within a Model declaration	Error with IBIS file Line number	E
103	MDL_ERR_3	Illegal Digital Port <%s> (not allowed in SPICE Ports section)	portname	Improper use of Digital port <portname>	Error with IBIS file Line number	E
104	MDL_ERR_4	D_switch not allowed with (D_drive,D_receive,or D_enable) in		Improper use of D_switch	Error with IBIS file Line number	E
105	MDL_ERR_5	%s not allowed with D_switch in Ports/A2D/D2A Section			Error with IBIS file Line number	E
106	MDL_ERR_6	Reserved Digital Port <%s> used as	portname	Improper use of Reserved Digital port <portname>	Error with IBIS file Line number	E
107	MDL_ERR_7	Orphan data line keyword.		A Model related data line was found where none was expected	Error with IBIS file Line number	E
108	MDL_ERR_8	TTgnd Typical value should be > 0		Improper TTgnd typical value	Error with IBIS file Line number	E
109	MDL_ERR_9	TTgnd Min value should be > 0		Improper TTgnd minimum value	Error with IBIS file Line number	E
110	MDL_ERR_10	TTgnd Max value should be > 0		Improper TTgnd maximum value	Error with IBIS file Line number	E
111	MDL_ERR_11	TTgnd typ value is not in between		Improper range for TTgnd	Warning	W
112	MDL_ERR_12	TTpower Typical value should be > 0		Improper TTpower typical value	Error with IBIS file Line number	E
113	MDL_ERR_13	TTpower Min value should be > 0		Improper TTpower minimum value	Error with IBIS file Line number	E
114	MDL_ERR_14	TTpower Max value should be > 0		Improper TTPower maximum value	Error with IBIS file Line number	E
115	MDL_ERR_15	TTpower typ value is not in between		Improper range for TTPower	Warning	W
116	MDL_ERR_16	[Model Spec] should be specified immediately after all the subparameters of a model and		Improper positioning of [Model Spec]	Error with IBIS file Line number	
117	MDL_ERR_17	[Receiver Thresholds] should not be specified for model type %s	modeltype	Receiver thresholds are not allowed for a <modeltype> which is not an Input or I/O model type	Warning with IBIS file Line number	W
118	MDL_ERR_18	[Add Submodel] should be specified before other keywords for a model		Improper positioning of [Ad Submodel]	Error with IBIS file Line number	E
119	MDL_ERR_19	%s Already Defined For Model '%s'	sub parameter/keyword, modelname	A model <sub-parameter or keyword> was already defined for <modelname>	Error with IBIS file Line number	E
120	MDL_ERR_20	[Receiver Thresholds] should be specified immediately after all the subparameters of a model and before the other keywords of a		Improper positioning of [Receiver Thresholds] keyword	Error with IBIS file Line number	E
121	MDL_ERR_21	Expecting Keyword. Invalid Line		An invalid line was found where a keyword was expected	Error with IBIS file Line number	E

Recent ibischk5 Version 5.1.2

- Major IBIS-AMI syntax implementation
  - IBIS Version 5.1 – rules clarified and CHECKED
  - Table-syntax defined and now parsed
  - **Major Errors now detected** (versus not being checked in the older Version 5.0.7)
- 23 BIRDs on IBIS and IBIS-AMI syntax
- 13 BUG reports on file testing for specification compliance closed through BUG138
- Source code checked with 44 new test files since V5.0.7
- Unfortunately, some new BUGs may be discovered with more usage

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"tschk2" Parser

- Checks Touchstone Version 1.0 (TS1) and Version 2.0 (TS2)
  - Error and Warning numbers
  - Free executables: http://www.eda.org/ibis/tschk2/
- Converts TS1 to TS2, TS2 to TS1 where practical with **-canonical*** flags
- Provides comment headers and real, imaginary format (RI) with **-describe** flag
- Source code package includes 440+ test cases
- C++, well documented
- Only one mixed mode BUG found so far

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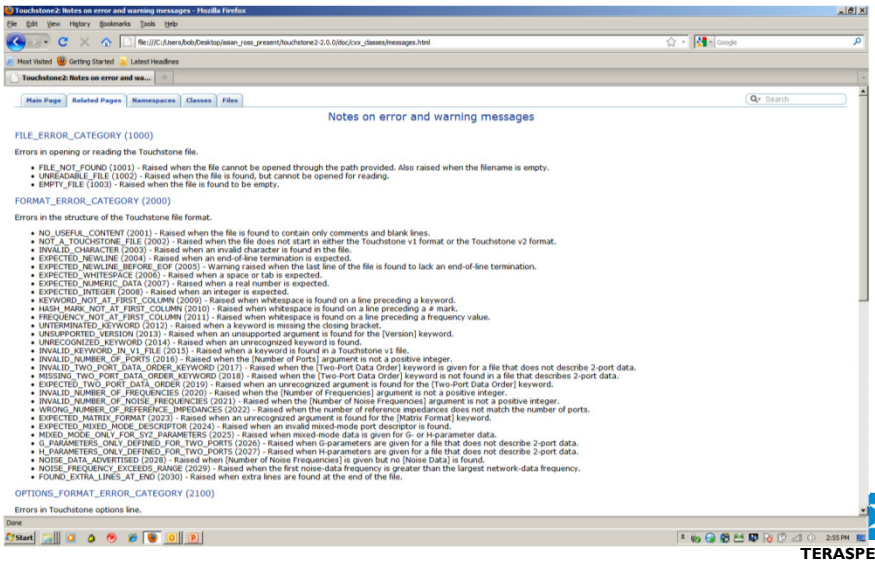
tschk2 {-canonical*} FILE

- **{-canonical | -canonical-v2}**
  - **TS1, TS2 → TS2**
  - Provides number of ports, frequencies and other information
  - Un-normalizes TS1 Y-, Z-, G- and H-parameters and effective noise resistance
- **{-canonical-v1}**
  - **TS1, TS2 → TS1** where practical
  - Applies column formatting rules and 2-port 21_12 ordering
  - Normalizes TS2 Y-, Z-, G- and H-parameters and effective noise resistance
  - No mixed mode or selectable reference resistance processing

71 tschk2 Messages



Conclusions

- ibischk5 and tschk2 parsers - **officially** check files for specification compliance
- Parsers helps test specification rules for clarity and accuracy
- BUG process continues to improve the parsers and eliminate mistakes

- **Parsers are critical to IBIS success**

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Useful Links Under IBIS Home Page: www.eda.org/ibis/

ver5.1/	**IBIS Version 5.1** (August 24, 2012)
ibischk5/	**ibischk5 Version 5.1.2** (October 2012)
touchstone_ver2.0/	**Touchstone Version 2.0** (April 24. 2009)
tschk2/	**tschk2 Version 2.0.0** (December 2009)
quality_ver2.0/	**IBIS Quality Specification** (Oct. 30, 2009)
ibis-iss_ver1.0/	**Interconnect SPICE Subcircuit Specification Version 1.0** (October 7, 2011)
editorial_wip/	**Editorial Task Group** (wip)
interconnect_wip/	**Interconnect Task Group** (wip)
macromodel_wip/	**Advanced Technology Task Group** (wip)
quality_wip/	**Quality Task Group** (wip)

(wip: work in progress)

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IBIS Model Validation Review

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Outlines

- Motivation
- History
- Method Review
- Common Mistakes
- Conclusion

Motivation

- Why model validation is the MUST?
  - Models are artificial representations of the real devices. This applies to all the models including our SI simulation models
  - System design engineers need the validated models to analyze their High-Speed system designs through simulations
  - “Garbage in, Garbage out” is true for all the simulations
- Proper IBIS model validation method is required
  - IBIS is the behavioral model which is no way to verify internal structures or monitor internal signals
- Common mistakes for IBIS validation and correction methods

Note: this presentation is focusing on “traditional” IBIS buffer model validation methods only.

History

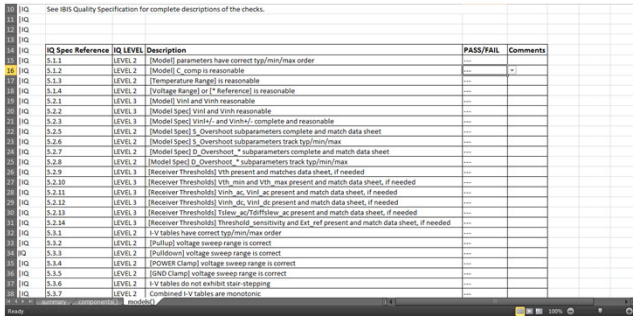
- 1997 – the IBIS Accuracy Subcommittee (IAS) was established
  - 1998 - IAS release their initial version of the IBIS Accuracy Specification, which later becomes the I/O Buffer Accuracy Handbook.
- 2007 - the IBIS Quality Task Group (IQTG) was formed
  - It is still ON in the regular teleconference basis
  - Several IBIS Quality Specifications have been released as the IBIS Standard Specification documents
  - A Quality Checklist also has been release from IQTG
- In the past few years, many system companies start to ask their device vendors to have their specific IBIS model quality control documents to be filled before the devices used in their high-speed designs

Method Review

- IBIS Validation Goal
  - Correlate IBIS model simulation results with the desired Golden sources (measurements and simulations) for specific test loads
- Common Used Correlation/Comparison Methods
  - From IQTG
    - Quality Checklist
  - From the Accuracy Handbook
    - Curve Overlay Metric
    - Curve Envelop Metric
  - From Xilinx and Huawei
    - Threshold based Metric
  - From IO Methodology
    - Differential Index based Metric

Quality Checklist from IQTG

- Great start! A lot of good suggestions
- Simply follow the list for the check items
- Too many items asking for “reasonable” and “visual” checking
- Not easy to implement by using a computer program
- Incomplete especially for correlations



See IBIS Quality Specification for complete descriptions of the checks.

IQ Spec Reference	IQ LEVEL	Description	PASS/FAIL	Comments
5.1.1	LEVEL 2	[Model] parameters have correct typ/min/max order	---	
5.1.2	LEVEL 2	[Model] C_comp is reasonable	---	
5.1.3	LEVEL 2	[Temperature Range] is reasonable	---	
5.1.4	LEVEL 2	[Voltage Range] or [* Reference] is reasonable	---	
5.2.1	LEVEL 3	[Model] Vinl and Vinh reasonable	---	
5.2.2	LEVEL 3	[Model Spec] Vinl and Vinh reasonable	---	
5.2.3	LEVEL 3	[Model Spec] Vinh+/- and Vinh+/- complete and reasonable	---	
5.2.5	LEVEL 2	[Model Spec] S_Overshoot subparameters complete and match data sheet	---	
5.2.6	LEVEL 2	[Model Spec] S_Overshoot subparameters track typ/min/max	---	
5.2.7	LEVEL 2	[Model Spec] D_Overshoot_* subparameters complete and match data sheet	---	
5.2.8	LEVEL 2	[Model Spec] D_Overshoot_* subparameters track typ/min/max	---	
5.2.9	LEVEL 3	[Receiver Thresholds] Vth present and matches data sheet, if needed	---	
5.2.10	LEVEL 3	[Receiver Thresholds] Vth_min and Vth_max present and match data sheet, if needed	---	
5.2.11	LEVEL 3	[Receiver Thresholds] Vinh_ac, Vinl_ac present and match data sheet, if needed	---	
5.2.12	LEVEL 3	[Receiver Thresholds] Vinh_dc, Vinl_dc present and match data sheet, if needed	---	
5.2.13	LEVEL 3	[Receiver Thresholds] Tslew_ac/Tdiffslew_ac present and match data sheet, if needed	---	
5.2.14	LEVEL 3	[Receiver Thresholds] Threshold_sensitivity and Ext_ref present and match data sheet, if needed	---	
5.3.1	LEVEL 2	I-V tables have correct typ/min/max order	---	
5.3.2	LEVEL 2	[Pullup] voltage sweep range is correct	---	
5.3.3	LEVEL 2	[Pulldown] voltage sweep range is correct	---	
5.3.4	LEVEL 2	[POWER Clamp] voltage sweep range is correct	---	
5.3.5	LEVEL 2	[GND Clamp] voltage sweep range is correct	---	
5.3.6	LEVEL 2	I-V tables do not exhibit stair-stepping	---	
5.3.7	LEVEL 2	Combined I-V tables are monotonic	---	

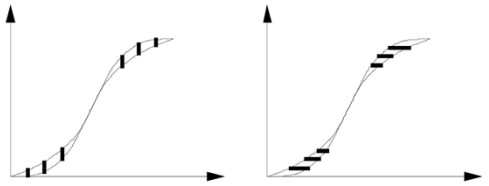
Curve Overlay Metric

- Relatively simply method
- Easy to implement by using a computer program
- Large error occurs when the most points are not perfectly aligned up even visual check seems to be good
- Do not count the error due to waveform shifting
- Not a great reference for automation purposes

4.3 Curve Overlay Metric

The Curve Overlay Metric applies to cases in which the measured and simulated data should theoretically lie directly on top of each other. For example, a structural simulation of a 50 Ω load and a behavioral simulation of the same load should theoretically yield identical results. Another example is the measurement of a known-typical sample component and a structural simulation of the same network under identical process-voltage-temperature conditions. The Curve Overlay Metric measures how well the two curves or waveforms match each other by summing the absolute value of the x-axis (or y-axis) differences between the two data points, weighing the sum against the range of data points along that axis, and dividing by the number of data points.

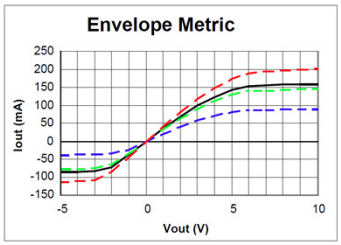
$$FOM = 100 \cdot \left[1 - \frac{\sum_{i=1}^{N} |X_i(golden) - X_i(DUT)|}{\Delta X \cdot N} \right]$$



Curve Envelop Metric

4.4 Curve Envelope Metric

The Curve Overlay Metric applies to cases in which the measured data are, in theory, bounded by two curves (or waveforms) that represent process-voltage-temperature extremes. In general, this metric is useful when the processing conditions of the sample component are unknown. The Curve Overlay Metric returns a yes/no value depending on whether or not every one of the data points falls within the envelope boundaries defined by the min and max curves. The plot below demonstrates a lab pull-down curve (solid line) that is slightly stronger than the typical curve (middle dashed line) and lies well within the (outer dashed lines).



The Curve Envelope Metric presents a difficulty in the case of unterminated transmission line loads. Because these waveforms overshoot normal logic levels and ring back, the min and max waveforms intersect each other and do not define an envelope. Therefore, the Curve Envelope Metric may not be applied to the Open Transmission Line load or the Transmission Line and Receiver load.

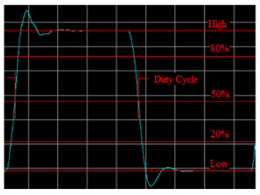
- Good to be used for measurement correlation cases
- Applies a good estimate for unknown/hard_to_ control operation conditions
- No result that indicates how accurate the model is

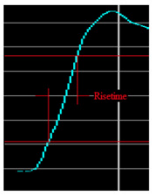
Threshold based Metric from Xilinx

- Uses 5 the most important thresholds to measure the correlation result
- Simple and easy to use a computer program for the results
- Ignores some transition effects
- Difficulty to be used for some abnormal waveform correlations

5 Metrics Defined

- We propose the following 5 metrics/features for waveform comparison:
  - high level, low level, rise time, fall time, and duty cycle

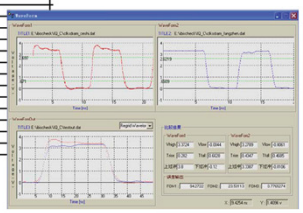




IBIS-to-Spice Correlation 10 Xilinx

Threshold based Metric from Huawei

验证项	检查要素
统计量化验证	1.1 FOM1
	1.2 FOM2
电气指标验证	2.1 高电平稳定电压（V）
	2.2 低电平稳定电压（V）
	2.3 高电平过冲(V)
	2.4 低电平过冲(V)
	2.5 高电平有效位宽(ns)
	2.6 低电平有效位宽(ns)
	2.7 上升时间(ns)
	2.8 下降时间(ns)
	2.9 边沿单调性
辅助验证项	3.1 高电平回冲
	3.2 低电平回冲
	3.3 眼宽
	3.4 眼高



FOM:

$$FOM1 = 100 \cdot \left[1 - \frac{\sum_{i=1}^{N} |Y1_i - Y2_i|}{YW \cdot N}\right]$$

$$FOM2 = 100 \cdot \left[\frac{\max|Y1_i - Y2_i|}{YW}\right]$$

$$FOM3 = \max|Y1_i - Y2_i|$$

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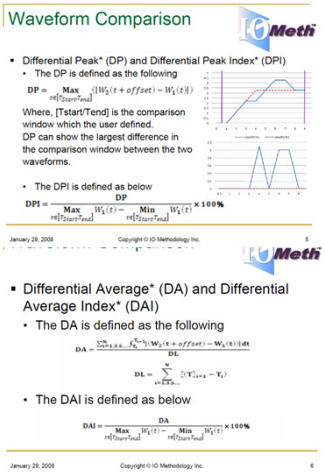
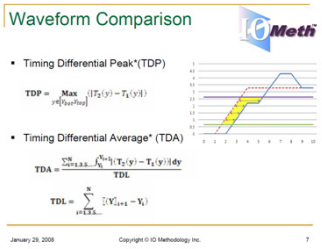
- Uses more thresholds to measure the correlation result including overshoots, monotonicity and eye measurements, etc. Plus FOM and customized FOMs
- Getting more difficult to use a computer program for the results but kind of manageable
- Still difficulty to be used for some abnormal waveform correlations

Differential Index based Metric from IO Methodology





- Brings 3 differential indexes (peek, average and timing) measuring together for the result (generic waveform comparison approach)
- Close to human visual predictions
- No dependency for threshold settings
- Works find even for abnormal waveforms
- Must use a computer program to calculate

Common Mistakes

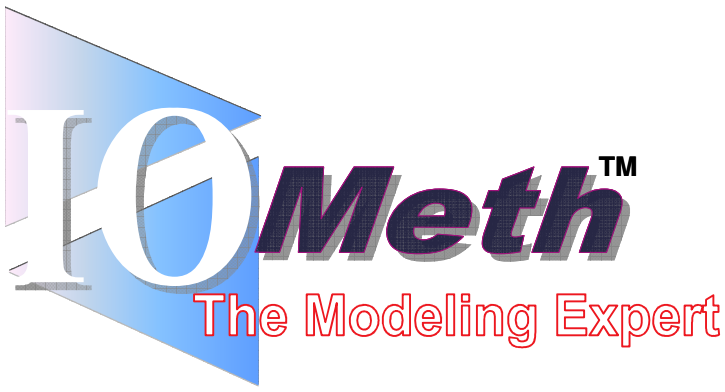
- Syntax Check
  - IBIS Golden Parser is a good first-pass tool for legal IBIS syntax check
  - The most of simulators will stop if your IBIS file contains syntax errors
  - No error and warning doesn't mean it is a good IBIS model for simulations
  - With warning messages, the IBIS model might still produce the accurate results against golden sources
- Test Circuit
  - Proper test circuit is important to get meaningful validation results
    - ➢ Your IBIS model might not be operable for certain conditions. It might heavily depend on your extraction conditions
  - Use application level test circuit for your correlations

Common Mistakes (continue)

- I-V / V-T Curves
  - Individual I-V might not within your expectations. Need to check the combined curves instead
  - IBIS Spec only accepts 100 data points for I-V curves
    - A number of system vendors asked for 1000 I-V points
  - Do not always use/ask 2 sets of V-T curves with 50 ohm + V_fixture=VCC/GND
    - Some buffers are only working properly for high-impedance load
    - Some buffers will produce a straight line for V_fixture=VCC or GND. e.g. OPEN type buffers
    - For some differential buffers, you might have to set V_fixture=Common_mode_voltage
  - Be careful about I-V / V-T mismatch error/warning
    - The most of times, this mismatch indicates your IBIS extraction settings are improper or inconsistent
    - Be aware of fixing
      - Don't fix it if it is not just a numerical error. It might have to be extracted again

Conclusion

- Validation is better to be done by IBIS model vendors
- Comparison methods are vary. Use them wisely to fit your buffer model needs
- IBIS user should ask for the vendor for reasonable validation report and/or test bench files
  - I/O buffers are vary. Be sure the contents you asked are reasonable
  - The different simulators could give out different IBIS simulation results



http://www.iometh.com

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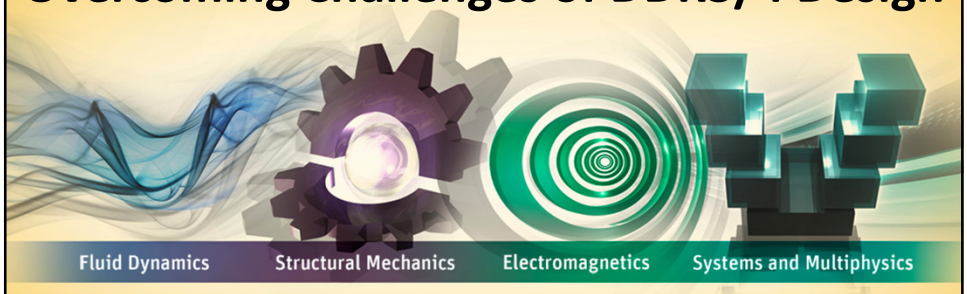
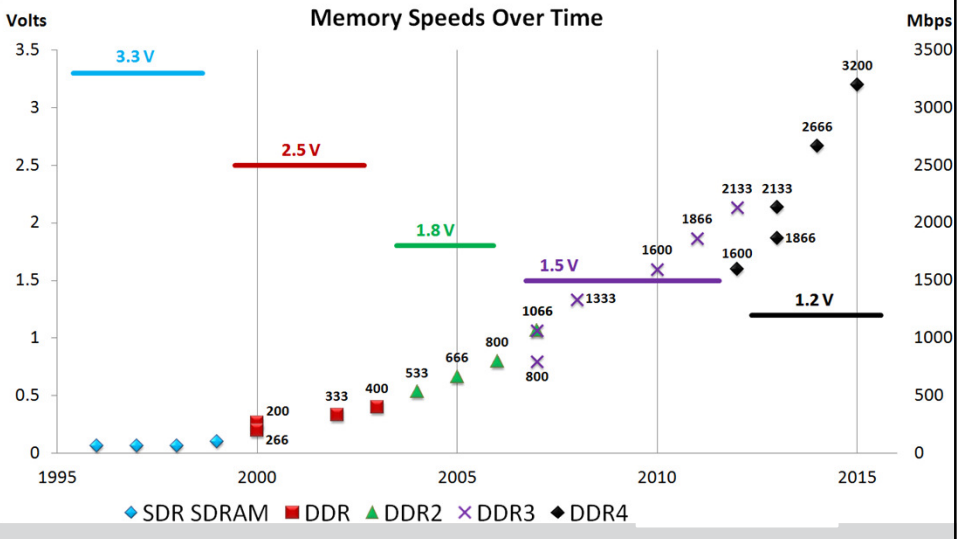


Asian IBIS Summit
Hsinchu, Taiwan
November 13, 2012

Steven G. Pytel, PhD.
SI Product Manager

ANSYS

Memory Speeds Over Time



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DDR4

- JEDEC recently announced the DDR4 standard
  - September 25th, 2012
  - JESD79-4
- Major Implications:
  - Point to Point Architecture
  - x4, x8, and x16 supported
  - 2GB to 16 GB SDRAMs
  - 1.2 V system
    - Vrefdq – on die reference voltage for DDR4
    - Up to 40 % reduction in power
    - Pseudo Open Drain Silicon architecture vs. push/pull
      - Pulled to Vdd thereby only drive low to zero
  - Data bus inversion
    - Limits # of SSO at a single time to improve SI and reduce power
  - Write leveling for CMD/ADD, CNTL and CLKs to control skew due to Fly-by topology
  - Server design
    - Distributed buffers for each byte lane compared to single buffer for all 64 bits
    - Point to Point topology requiring a switch between DIMMs
  - Support for Chip Stacking
    - TSV Supported architectures for SDRAMs

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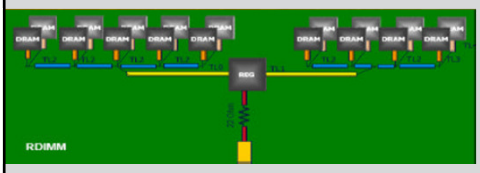
T-topology vs. Fly-by topology

DDR2 T-topology

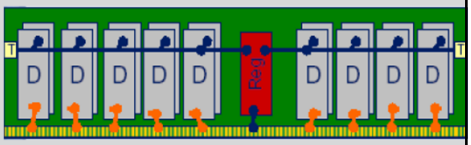


DDR2 RDIMM

Clock arriving time to all DRAMS
on a DIMM are expected to be the same

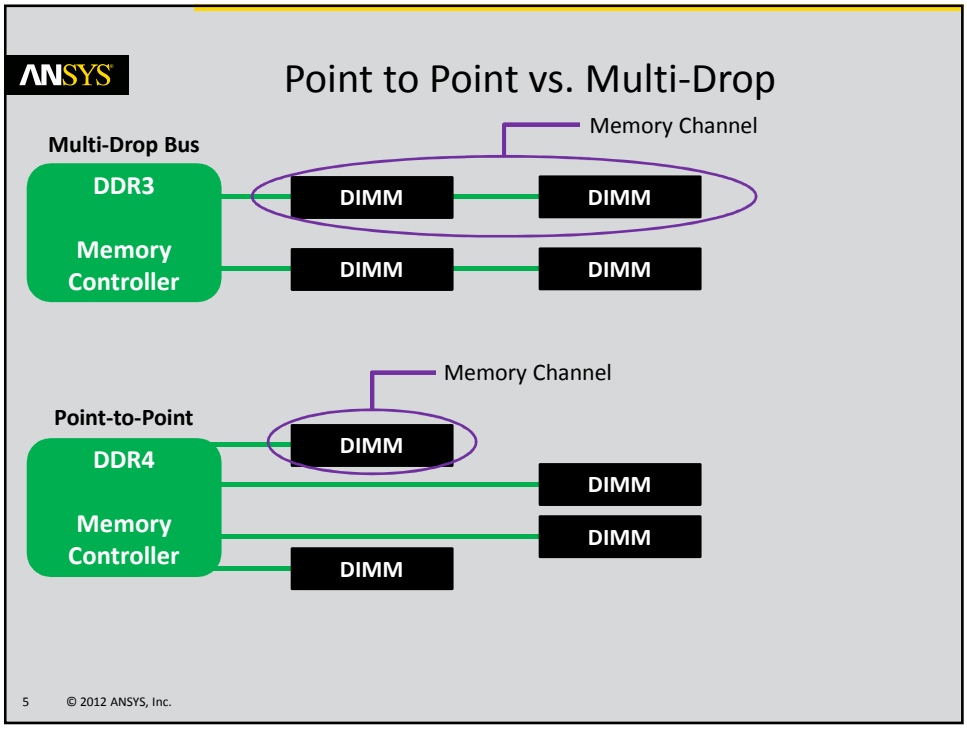
DDR3 Fly-by topology

DDR3 UDIMM



DDR3 RDIMM

Clock arriving time to each DRAM
on a DIMM are different


ANSYS
Point to Point vs. Multi-Drop
Multi-Drop Bus
DDR3
Memory Controller
Memory Channel
DIMM
DIMM
DIMM
DIMM
Point-to-Point
DDR4
Memory Controller
Memory Channel
DIMM
DIMM
DIMM
DIMM
5
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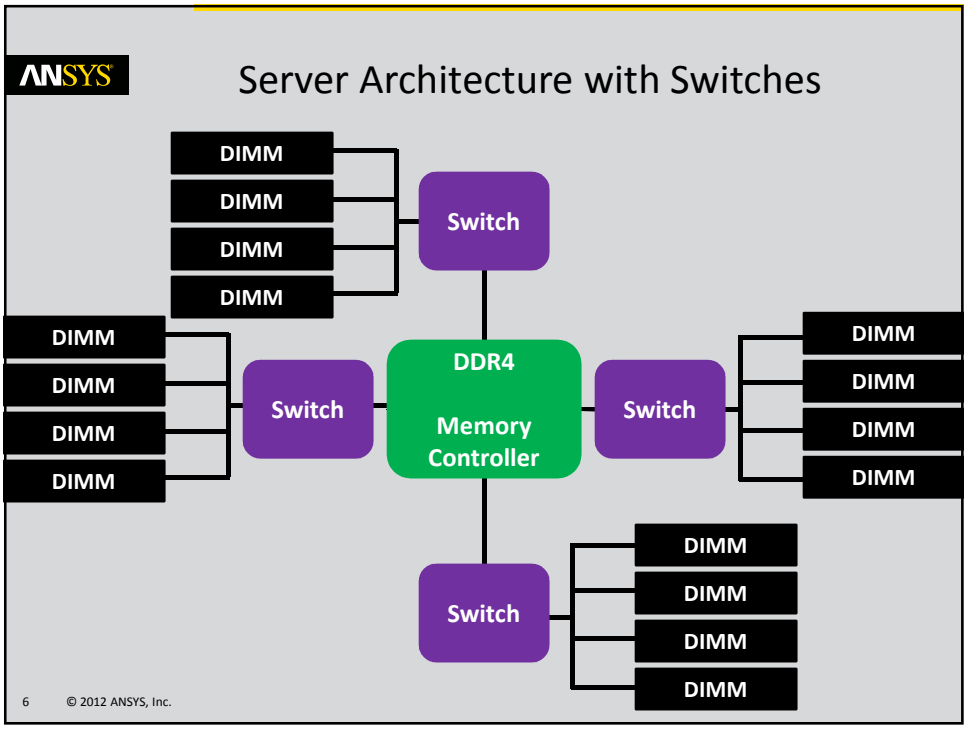
ANSYS
Server Architecture with Switches
DIMM
DIMM
DIMM
DIMM
Switch
DIMM
DIMM
DIMM
DIMM
Switch
DDR4
Memory Controller
Switch
DIMM
DIMM
DIMM
DIMM
Switch
DIMM
DIMM
DIMM
DIMM
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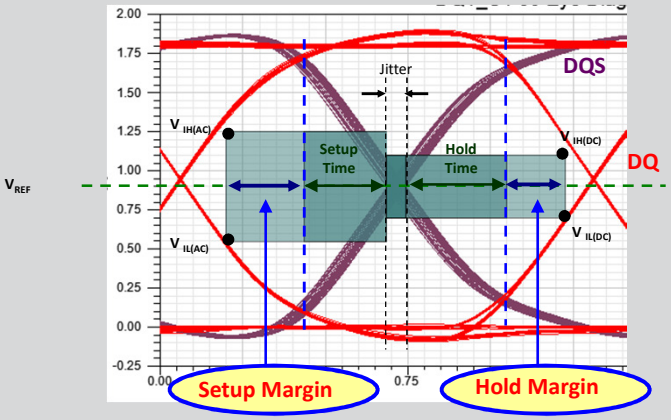
DDR 3 Key Spec

Setup Margin & Hold Margin



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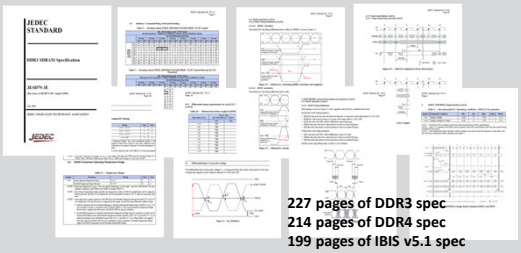
DDRX Technology & Challenges

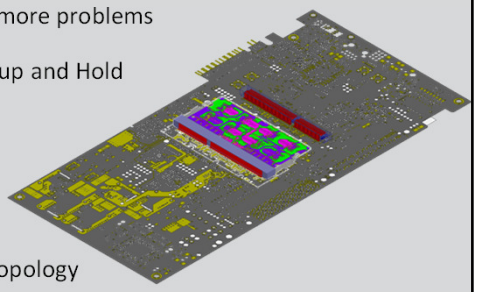
- Design challenges?
  - Validation
    - Prototype
    - Measurement
    - Interpret and implementation(calculation) of Design Spec such as DDR3/4, LPDDR2/3 and more…
    - Large amount output data report of results
  - Capacity or Complexity and Time
    - Chip to Chip or Chip to PKG
    - Chip + Package + PCB + Connector/Cable + PCB + Package + Chip
    - Full System



227 pages of DDR3 spec
214 pages of DDR4 spec
199 pages of IBIS v5.1 spec

DDRX Technology & Challenges

1. Higher Speeds
   - 66 Mbps to 3200 Mbps and beyond
   - Higher speed and edge rates cause more problems with skew, coupling, radiation, etc…
   - Timing margins become tighter; Setup and Hold timings
     - DDR 400 has a window of 2.5 ps
     - DDR4 3200 has a window of 312.5 ps



2. Changes with design topology
   - DDR2 started ODT support
   - DDR3 started Fly by topology vs. T topology
   - DDR3 uses only differential strobes
   - DDR4 architecture is point to point
     - One controller to 1 DIMM
   - DDR4 is Psuedo Open Drain vs. Push/Pull

DDRX Technology Challenges

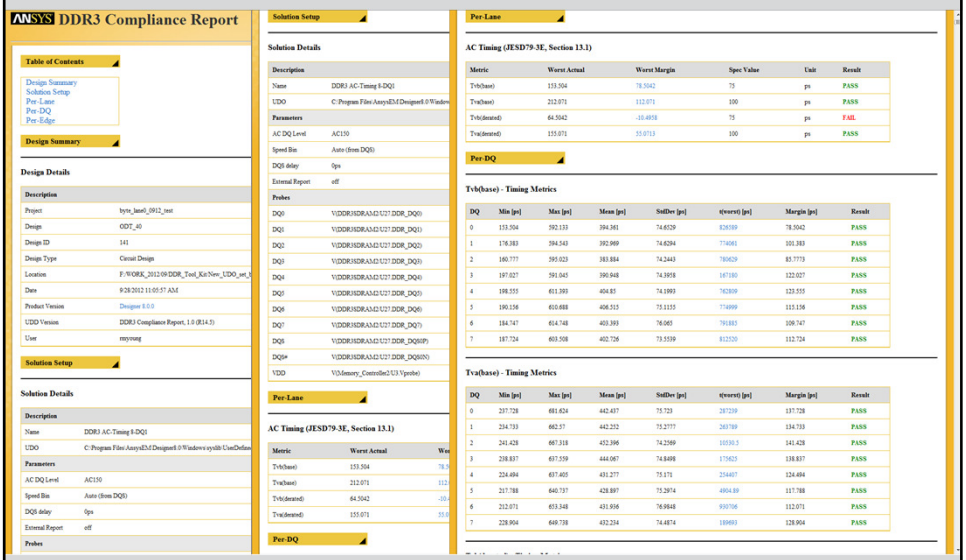

ANSYS DDR3 Compliance Report

Table of Contents
Design Summary
Solution Setup
Per-Lane
Per-DQ
Per-Edge

Design Summary

Design Details

Description	
Project	byte_lane0_0912_test
Design	ODT_40
Design ID	141
Design Type	Circuit Design
Location	F:/WORK_2012/09/DDR_Tool_Kit/New_UDO_set_3
Date	9/28/2012 11:05:57 AM
Product Version	Designer 8.0.0
UDD Version	DDR3 Compliance Report, 1.0 (R14.5)
User	rmyoung

Solution Setup

Solution Details

Description	
Name	DDR3 AC-Timing 8-DQ1
UDO	C:\Program Files\AnsysEM\Designer8.0\Windows\sysdir\UserDefinedComponents\DDR3_AC_Timing_8_DQ1.udo
Parameters	
AC DQ Level	AC150
Speed Bin	Auto (from DQS)
DQS delay	0ps
External Report	off
Probes	

Solution Setup

Solution Details

Description	
Name	DDR3 AC-Timing 8-DQ1
UDO	C:\Program Files\AnsysEM\Designer8.0\Windows\sysdir\UserDefinedComponents\DDR3_AC_Timing_8_DQ1.udo
Parameters	
AC DQ Level	AC150
Speed Bin	Auto (from DQS)
DQS delay	0ps
External Report	off
Probes	
DQ0	V(DDR3SDRAM2/U27.DDR_DQ0)
DQ1	V(DDR3SDRAM2/U27.DDR_DQ1)
DQ2	V(DDR3SDRAM2/U27.DDR_DQ2)
DQ3	V(DDR3SDRAM2/U27.DDR_DQ3)
DQ4	V(DDR3SDRAM2/U27.DDR_DQ4)
DQ5	V(DDR3SDRAM2/U27.DDR_DQ5)
DQ6	V(DDR3SDRAM2/U27.DDR_DQ6)
DQ7	V(DDR3SDRAM2/U27.DDR_DQ7)
DQS	V(DDR3SDRAM2/U27.DDR_DQS0P)
DQS#	V(DDR3SDRAM2/U27.DDR_DQS0N)
VDD	V(/Memory_Controller2/U3/Vprobe)

Per-Lane

AC Timing (JESD79-3E, Section 13.1)

Metric	Worst Actual	Worst Margin	Spec Value	Unit	Result
Tvb(base)	153.504	78.5042	75	ps	PASS
Tva(base)	212.071	112.071	100	ps	PASS
Tvb(derated)	64.5042	-10.4958	75	ps	FAIL
Tva(derated)	155.071	55.0713	100	ps	PASS

Per-DQ

Tvb(base) - Timing Metrics

DQ	Min [ps]	Max [ps]	Mean [ps]	StdDev [ps]	t(worst) [ps]	Margin [ps]	Result
0	153.504	592.133	394.361	74.6529	826589	78.5042	PASS
1	176.383	594.543	392.969	74.6294	774061	101.383	PASS
2	160.777	595.023	383.884	74.2443	780629	85.7773	PASS
3	197.027	591.045	390.948	74.3958	687180	122.027	PASS
4	198.555	611.393	404.85	74.1993	762809	123.555	PASS
5	190.156	610.688	406.515	75.1155	774999	115.156	PASS
6	184.747	614.748	403.393	76.065	791885	109.747	PASS
7	187.724	603.508	402.726	73.5539	812520	112.724	PASS

Tva(base) - Timing Metrics

DQ	Min [ps]	Max [ps]	Mean [ps]	StdDev [ps]	t(worst) [ps]	Margin [ps]	Result
0	237.728	681.624	442.437	75.723	287239	137.728	PASS
1	234.733	662.57	442.252	75.2777	263789	134.733	PASS
2	241.428	667.318	452.396	74.2569	10530.3	141.428	PASS
3	238.837	637.559	444.067	74.8498	175625	138.837	PASS
4	224.494	637.405	431.277	75.171	254407	124.494	PASS
5	217.788	640.737	428.897	75.2974	4904.89	117.788	PASS
6	212.071	653.348	431.936	76.9848	930706	112.071	PASS
7	228.904	649.738	432.234	74.4874	189693	128.904	PASS

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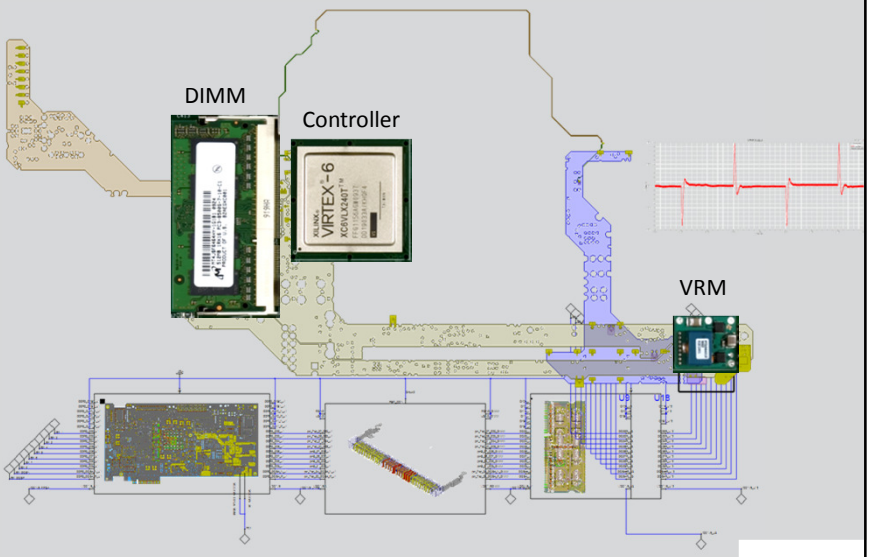
DDR3 1.5V PDN with VRM



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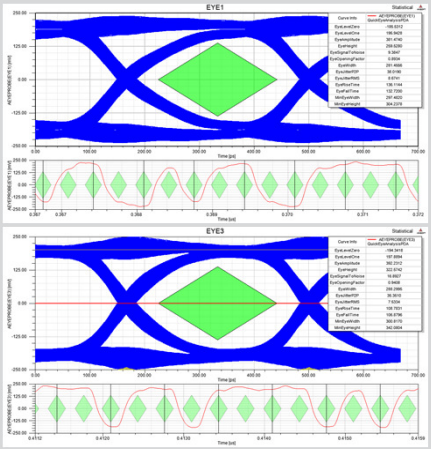
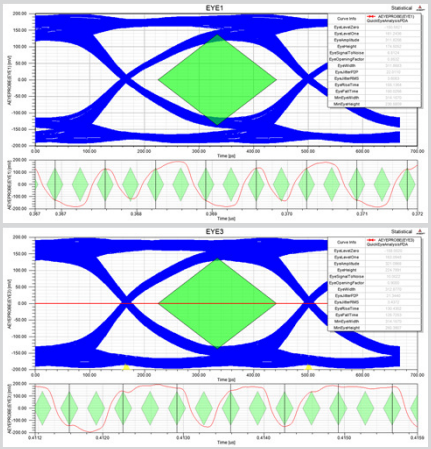
DDR3 Connector Impact (Reflections)

Without Connector



With Connector



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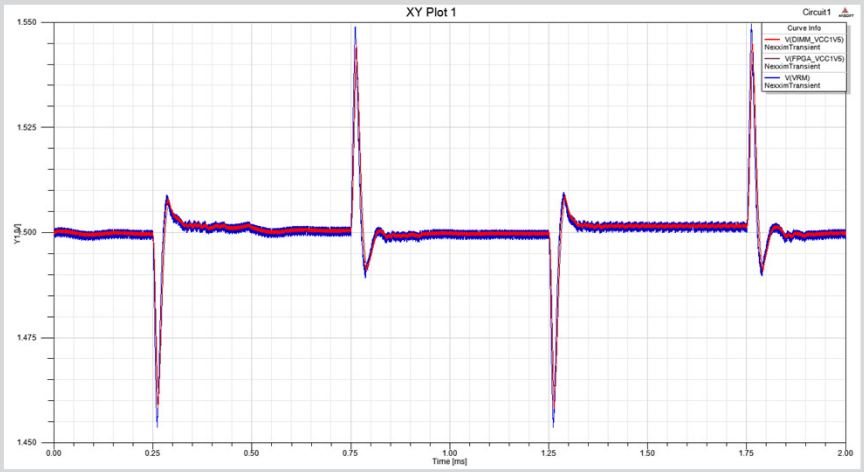
DDR3 1.5V PDN with VRM



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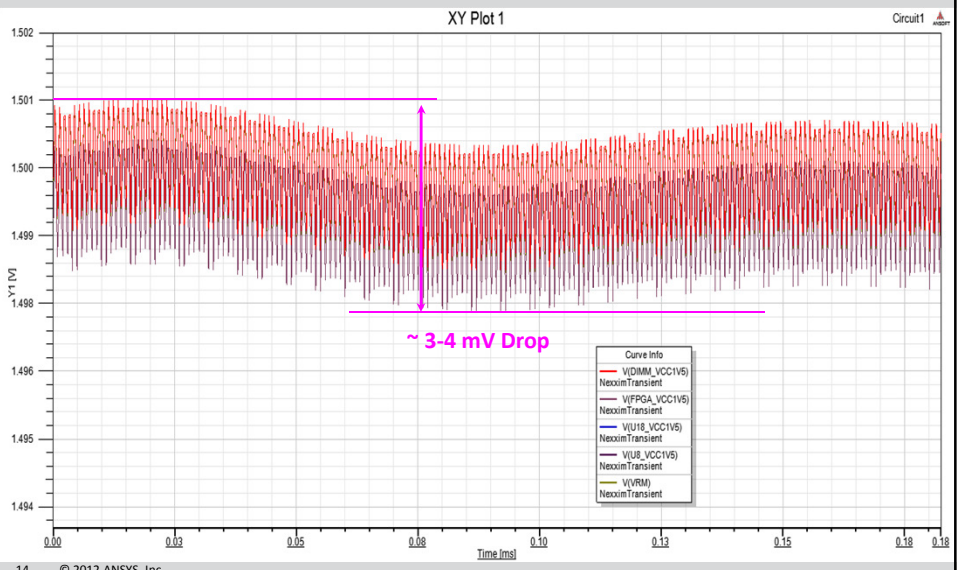
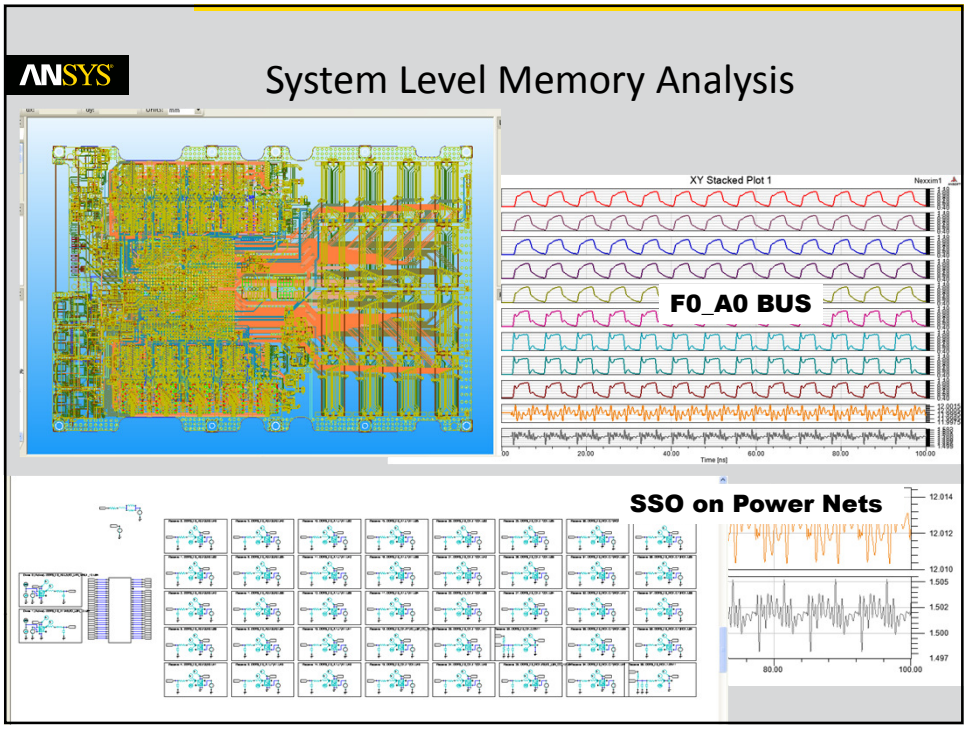
DDR3 1.5V PDN with VRM

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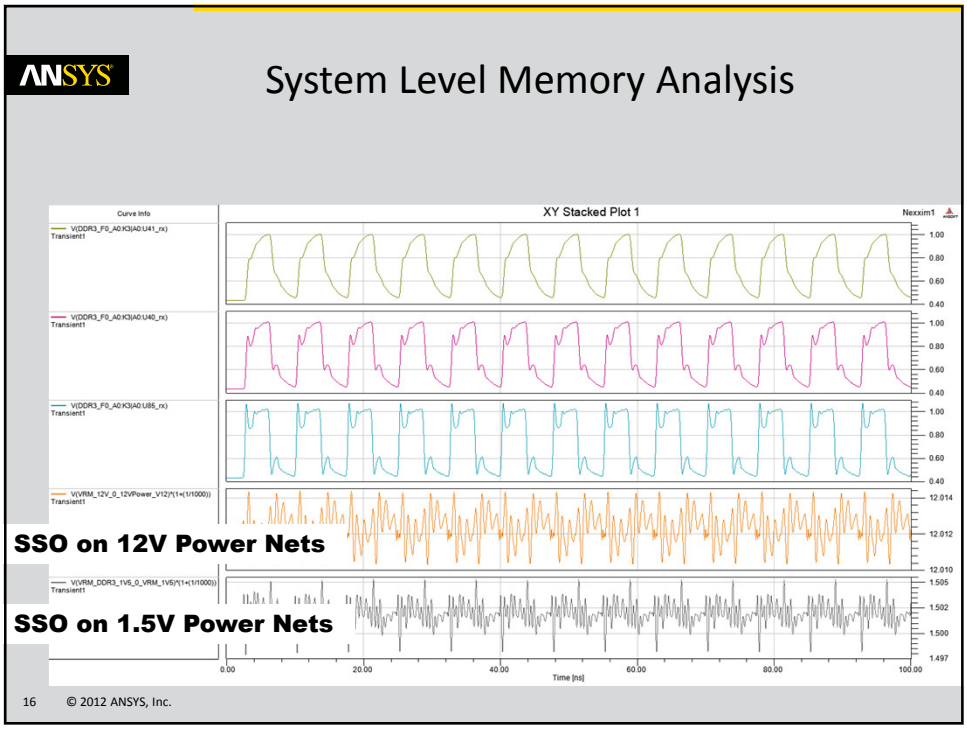
System Level Memory Analysis
XY Stacked Plot 1
Nexxim1
F0_A0 BUS
SSO on Power Nets
Time [ns]


ANSYS
System Level Memory Analysis
XY Stacked Plot 1
Nexxim1
Curve Info
SSO on 12V Power Nets
SSO on 1.5V Power Nets
Time [ns]
16
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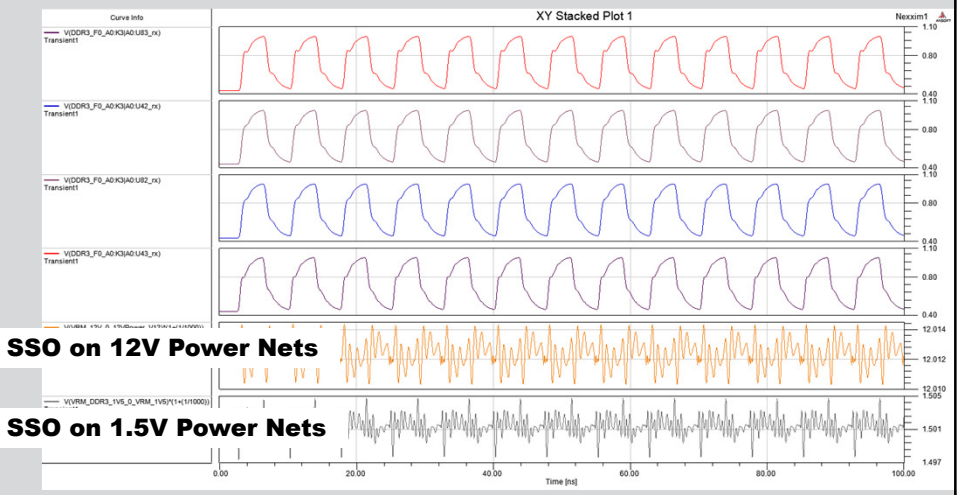
System Level Memory Analysis



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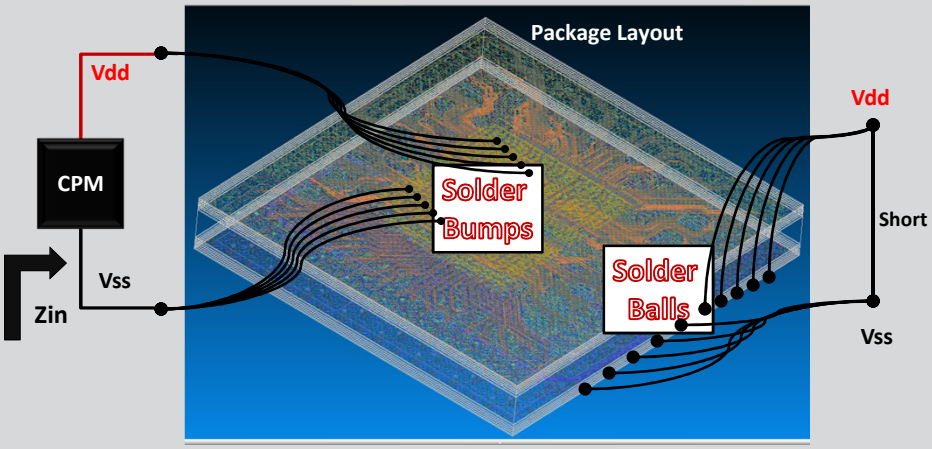
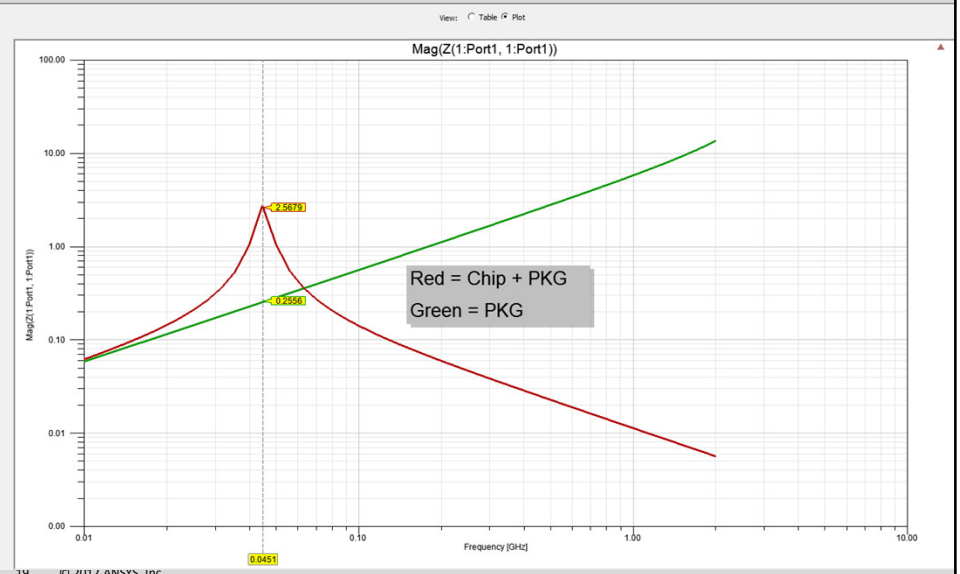
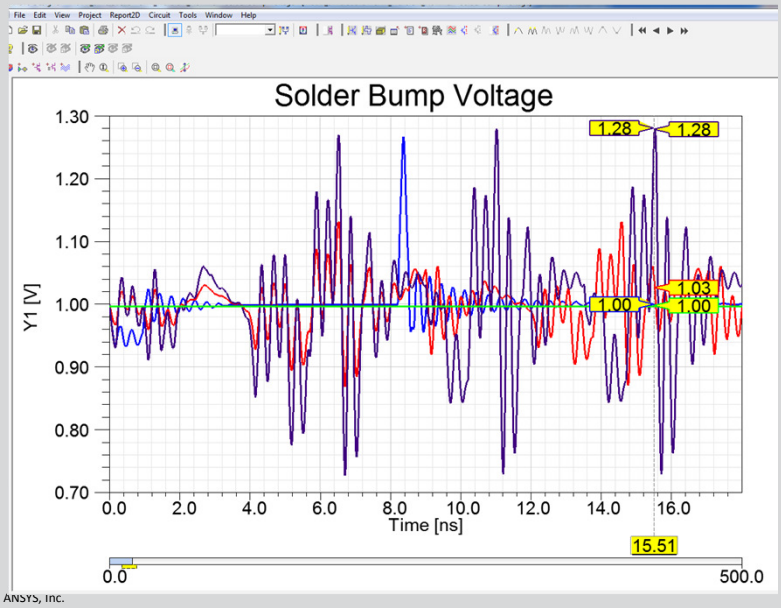
Recall Chip Impedance



Impedance Results with & without Chip



Die Solder Bump Voltage



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Conclusion

- DDR4 Standard was recently released
  - Interconnect challenges due to Chip, PKG, & PCB
    - Reduced Voltage (1.2V -> 1.05V expected)
    - Increased Data Rates (1600 Mbps -> 4266 Mbps expected)
    - Future stacking of SDRAMs expected with TSV technology
- System level performance must include:
  - Accurate PKG/PCB extractions including connectors
  - Accurate Die Models: IBIS + current?

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INVENTIVE

Designing DDR3 system using Static Timing Analysis in conjunction with IBIS simulations

Taranjit Kukal, Zhangmin Zhong, Heiko Dudek
Cadence Design Systems, Inc.
Presented by: Kent Ho

Asian IBIS Summit
Hsinchu, Taiwan
November 13, 2012

Agenda

- Key Design Challenges
  - DDR3 Timing and SI specifications
- Problem Statement
  - Piecemeal simulations do not guarantee optimal design
- Solution
  - Static Timing Analysis in conjunction with IBIS simulations
- Use-cases
  - Step-by-step method to optimally use EDA flows
- Summary

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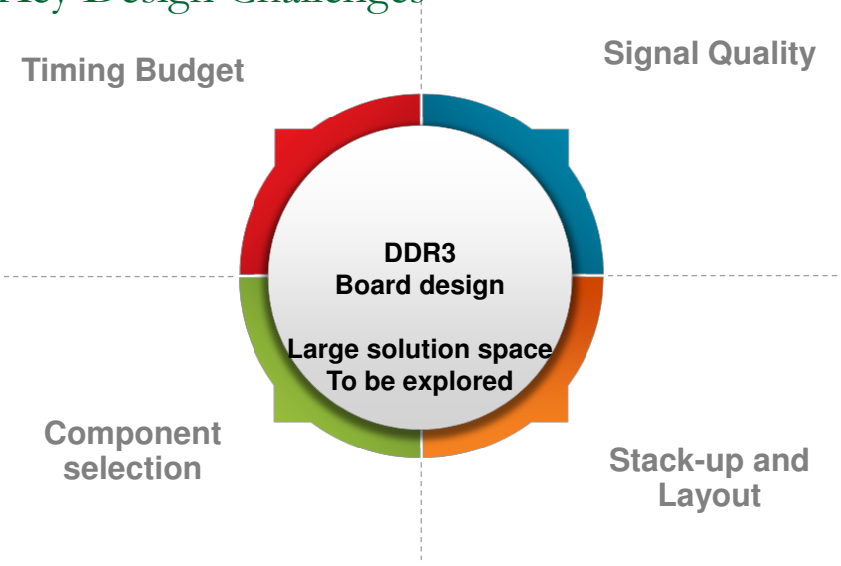
Key Design Challenges



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Key Design Challenges: Timing Budget

- Set-up / Hold Times
  - Data write w.r.t strobe
  - Data read w.r.t strobe
  - Addressing w.r.t clock
- Strobe w.r.t clock
  - Data w.r.t Address
- Account for
  - Clock/Strobe Jitters and Interconnect Jitters
  - Slew-rates and hence derating of setup/hold

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Key Design Challenges: Signal Quality

- Thresholds
  - DC and AC
  - Noise-Margins
- Overshoots/Undershoots
  - Magnitude
  - Area
- tVac
  - Minimum time for signal to stay above threshold
- Eye
  - Data-Valid Window after accounting Jitter
- Slews that in-turn affect timing
  - Rise/Fall times

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Key Design Challenges: Component Selection

- Memory-Buffers
  - Trade-off between read-write cycles
- Controller Driver strength
  - Trade-off between read-write cycles
- Connector
  - Insertion loss
- Strobe/Clock differential buffers
  - Should satisfy tDVac and overshoot/undershoot area requirements

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Key Design Challenges: Layout Constraints

- Trace-lengths
  - Relational Propagation-delays Data-Strobe for balanced setup/hold
  - Relational Propagation-delays Address-Clock for balance setup/hold
  - Relational Propagation-delays Strobe-Clock for successful write-leveling
- Topology schedules
  - Point to Point for Data
  - FlyBy for Address
- Trace Impedance
  - Example: Lead-in section (45 ohm) to Load-in section (60 ohm) through neck-down (~5 to 10 mm) for clock
  - Percentage variation that can be tolerated
- Differential matching (CLK, STROBE)
  - Maximum unparallel length

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Agenda

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Problem Statement: Multiple constraints across Timing / SI

- DDR3 has several SI and Timing constraints and getting all of them to meet is a big solution-space to explore.
- Designer tries to fix a few; and in the process puts other measurements-of -interest out of specifications.

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Problem Statement: Timing Closure across read/write/address

- Timing-Closure is time-consuming as there are too many constraints to be met
  - Etch delays needed for timing-closure during Read cycle may not work during Write cycle.
  - It is not enough to get just positive Setup/Hold margins; optimal design needs setup and hold margins that equally distributed.
- Requirement of relative delays between Data (Strobe) vs Address (Clock) brings additional challenge.
- It is also important to budget for signal and interconnect jitters on various signals.
  - What may look to be meeting the constraint is likely to fail due to jitter causing uncertainty in the signal.

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Problem Statement: SI affects timing

- Slew-rates affect Setup/Hold time-constraints.
  - SI simulations provide slew-rates of signals that in-turn need to be considered for timing constraints. For example, hold-time constraint could be 160pS for slew-rate of 1V/ns while it could be 200pS when the signal slew-rate is 2V/ns
- Eye-shape could indicate a need for different relative etch-lengths for equal setup/hold margins.
  - While Static Timing Calculations would provide one set of readings for etch-delays, the eye-shape (that could be narrow on one side) may force the designer to refine the relative delays for balanced setup/hold times.
- Stack-up variation and Cross-talk causes interconnect jitter that needs to be accounted for in the timing-checks.
  - It is important that such jitter is estimated through SI simulations and then annotated to the Timing-models for timing closure.

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Problem Statement (Current approach): Ad-hoc analysis and verification (Leading to Non-optimal design)

- Timing-checks are done using hand-calculations at times and then the focus is to do post-layout verification using SI simulations to ensure correctness.
- Limitations:
  - Goal is to just meet constraints as against optimal design with enough margins on all constraints.
  - Manual timing-budget calculations are time-consuming and inefficient
  - No way to include SI effects into timing-calculations

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Problem Statement (Current approach) : Ad-hoc analysis and verification (Leading to Non-optimal design)

- Designers use layout rules provided by device manufacturers
- Limitation:
  - Limits flexibility. PCB designers refrain from trying variations in terms of component selection from different vendors and in trying different board dimensions and circuit configurations.
  - Over-design at times as layout guidelines are usually on the stricter side to ensure working of system

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Problem Statement (Current approach) : Ad-hoc analysis and verification (Leading to Non-optimal design)

- SI simulations are usually done as audit at verification step following a piecemeal approach
- Limitations:
  - Use of real-time simulations to do exhaustive timing-verification is too time-consuming and difficult.
  - It is very difficult to manage optimal parameter selection across constraints spread across read/write and address cycles.

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Agenda

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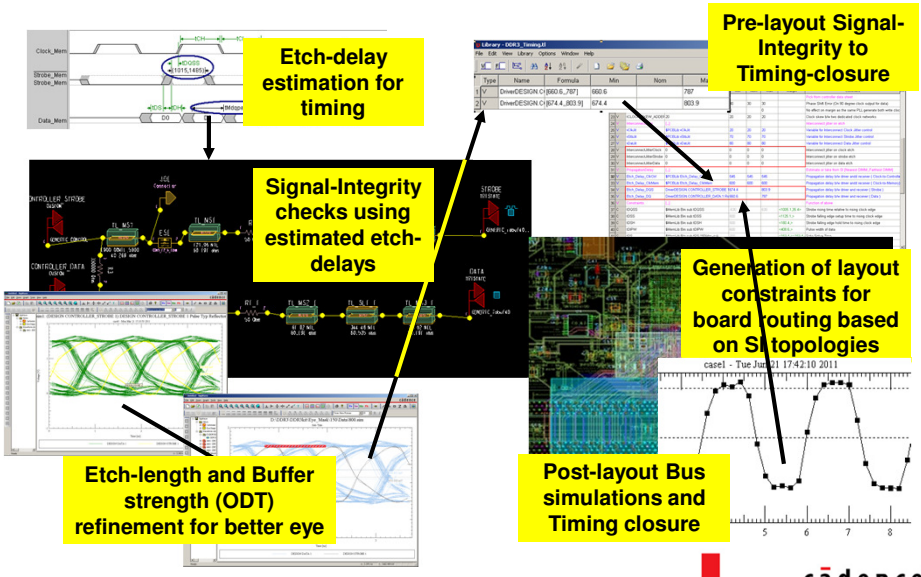
Unified SI/STA flow for DDR3



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Solution: Static Timing analysis

- Static Timing exploration independent of time-expensive SI simulations can provide seed for etch estimation.
- Automatic update of constraint limits based on data-rate, slew-rate of signals, threshold-values selected for design can make easy computation.
- Automatic calculation of relative etch-delays for balanced setup/hold times while accounting for uncertainty in signals due to jitter can save multiple iterations.

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Solution: Timing analysis feeds SI simulations

- Results of STA feed into SI simulations.
  - Estimated etch-delays (flight-time) of data, strobe, address, clock map to interconnect flight-times
  - Estimated jitter becomes constraint for cross-talk (interconnect and data-dependent)
- SI Simulations with IBIS buffers
  - Building on interconnect details (vias, trace-lengths, stack-up) keeping the flight-time constraint from STA
  - Improving on interconnect topologies to meet SI constraints and better centering of strobe w.r.t data

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Solution: SI simulations that feedback STA

- Feed-back updated flight-times (switch-delays), worst-jitter and slew-rates from real-time SI simulations to timing-models to close timing-constraints.
- Generation of layout constraints from interconnect topologies
  - Routing the board based on layout constraints
- Post-route SI simulations followed by timing-closure.

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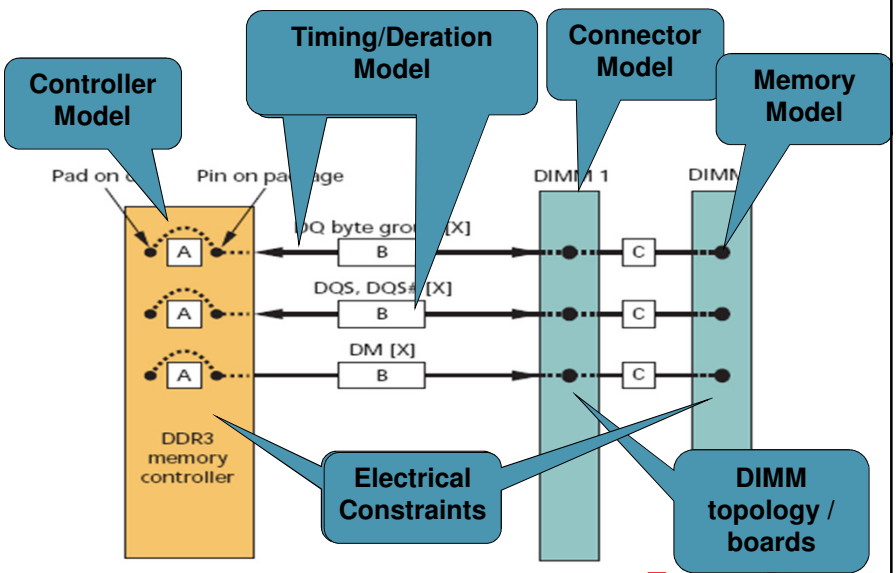
cadence

Use-case



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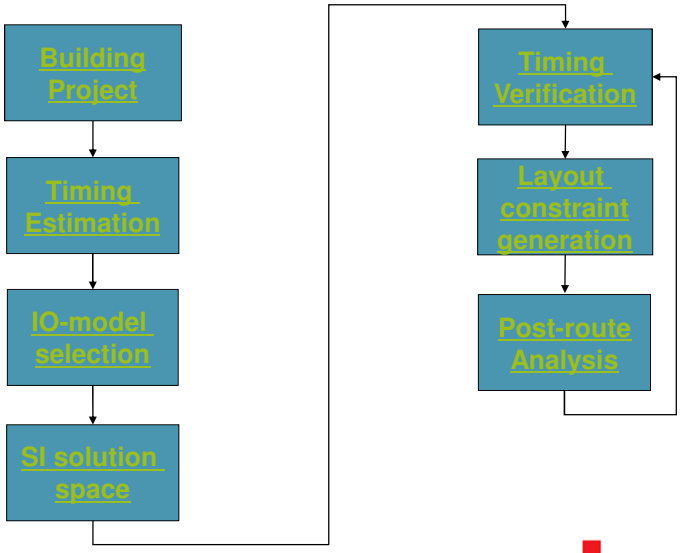
Use-case



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Building Project

- Frequency of operation and AC threshold levels
  - *Configures TD models*
  - *Configures custom measurements*
- Address (1T / 2T)
  - *Configures TD models*
- New DIMMs (Or On-board) vs Existing DIMMs
  - Pre-created Topologies vs Extracted DIMM topologies
- DIMM Card Type
  - *Configures topologies and ECSets*

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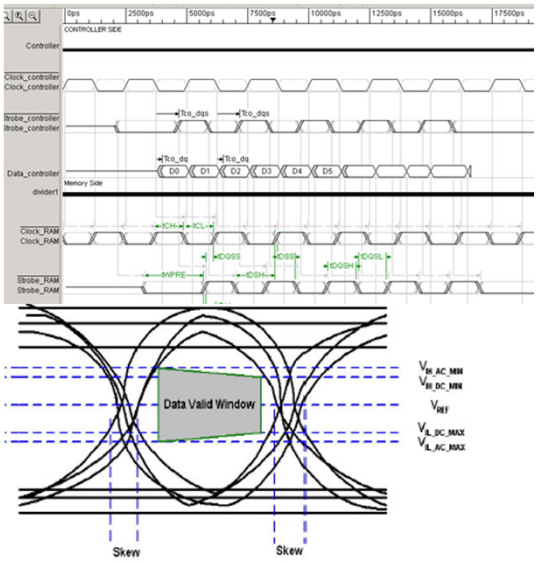
Timing estimation

- Data-Strobe
  - Write
  - Read
- Address-Clock (1T or 2T)
- Decide etch-delays that can meet timing specifications



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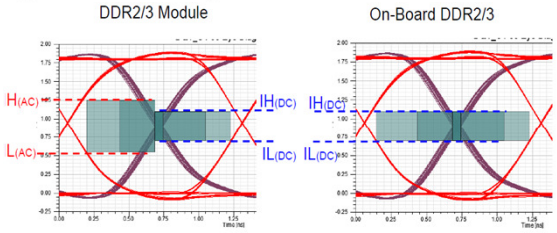
IO-model selection/Exploration

- For best noise-margins and Eye for read/write

- Controller Model
  - Impedance
- Memory Model
  - ODT
- Connector Model
- Strobe
  - tvac, shoot-area



Configuration		Write To	DRAM Controller	Slot 1		Slot 2	
Slot 1 (DIMM 1)	Slot 2 (DIMM 2)			Rank 1	Rank 2	Rank 1	Rank 2
Dual rank	Dual rank	Slot 1	ODT off	120Ω	ODT off	ODT off	30Ω
		Slot 2	ODT off	ODT off	30Ω	120Ω	ODT off
Dual rank	Single rank	Slot 1	ODT off	120Ω	ODT off	20Ω	n/a
		Slot 2	ODT off	ODT off	20Ω	120Ω[1]	n/a
Single rank	Dual rank	Slot 1	ODT off	120Ω[1]	n/a	ODT off	20Ω
		Slot 2	ODT off	20Ω	n/a	120Ω	ODT off
Single rank	Single rank	Slot 1	ODT off	120Ω[1]	n/a	30Ω	n/a
		Slot 2	ODT off	30Ω	n/a	120Ω[1]	n/a
Dual rank	Empty	Slot 1	ODT off	40Ω	ODT off	n/a	n/a
Empty	Dual rank	Slot 2	ODT off	n/a	n/a	40Ω	ODT off
Single rank	Empty	Slot 1	ODT off	40Ω	n/a	n/a	n/a
Empty	Single rank	Slot 2	ODT off	n/a	n/a	40Ω	n/a

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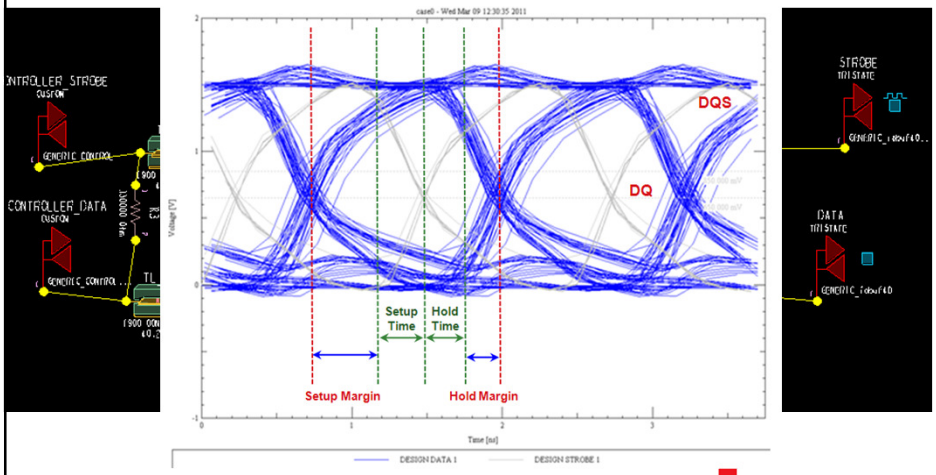
SI Solution Space for Relational Topologies - Explore data w.r.t strobe; address w.r.t clock



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Timing Verification after SI-annotation

- Re-verify timing after import of flight delays and jitter from SI simulations

Name	Formula	Min	Nom	Max	Margin	Comment
JitterSpecifications	[...]					Pick from controller data sheet
tPLL_PSERR	30	30	30	30		Phase Shift Error (On 90 degree clock output for data)
tPLL_Jitter	0	0		0		No effect on margin as the same PLL generate both write clo
tCLOCK_SKEW_ADDER	20	20	20	20		Clock skew b/w two dedicated clock networks
InterconnectJitter	[...]					Interconnect jitter on etch
vClkJit	$PCBLib:vClkJit	20	20	20		Variable for Interconnect Clock Jitter control
vStbJit	$PCBLib:vStbJit	70	70	70		Variable for Interconnect Strobe Jitter control
vDatJit	$PCBLib:vDatJit	80	80	80		Variable for Interconnect Data Jitter control
InterconnectJitterClock	0	0	0	0		Interconnect jitter on clock etch
InterconnectJitterStrobe	0	0	0	0		Interconnect jitter on strobe etch
InterconnectJitterData	0	0	0	0		Interconnect jitter on data etch
PropagationDelay	[...]					Estimate or take from SI [Nearest DIMM_Farthest DIMM]
Etch_Delay_ClkCtrl	$PCBLib:Etch_Delay_ClkCtrl	545	545	545		Propagation delay b/w driver andd receiver (Clock-to-Controll
Etch_Delay_ClkMem	$PCBLib:Etch_Delay_ClkMem	600	600	600		Propagation delay b/w driver andd receiver (Clock-to-Memory
Etch_Delay_DQS	DriverDESIGN.CONTROLLER_STROBE.1	674.4		803.9		Propagation delay b/w driver and receiver (Strobe)
Etch_Delay_DQ	DriverDESIGN.CONTROLLER_DATA.1:Re	660.6		787		Propagation delay b/w driver and receiver (Data)
Constraints	[...]					Function of above
tDQSS	$MemLib:Bin:sub:tDQSS	-630		630	<1005.1,35.4>	Strobe rising time relative to rising clock edge
tDSS	$MemLib:Bin:sub:tDSS	500			<1125.1,>	Strobe falling edge setup time to rising clock edge
tDSH	$MemLib:Bin:sub:tDSH	500			<180.4,>	Strobe falling edge hold time to rising clock edge
tDIPW	$MemLib:Bin:sub:tDIPW	600			<408.6,>	Pulse width of data
tDS	$MemLib:Bin:sub:tDS:150(der_su)	200			<163.4,><163.4,	Data Setup Time
tDH	$MemLib:Bin:sub:tDH(der_hl)	200			<275.7,><275.7,	Data Hold Time

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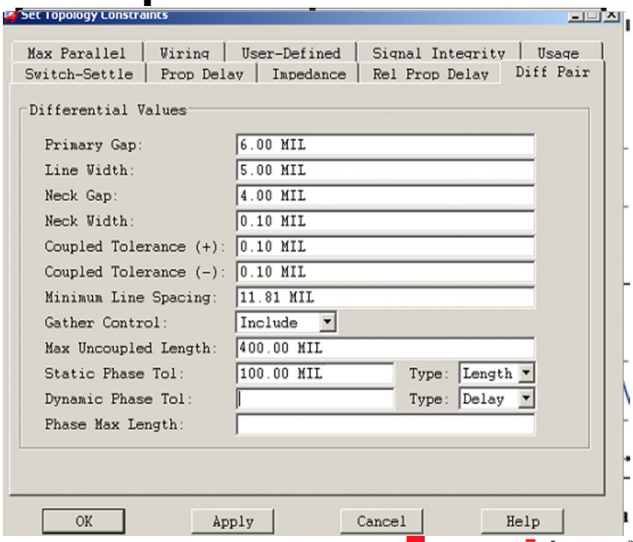
Setting up Layout constraints depending on SI exploration

- Propagation Delays
- Impedance
- Relative Propagation delays
- Max Parallel



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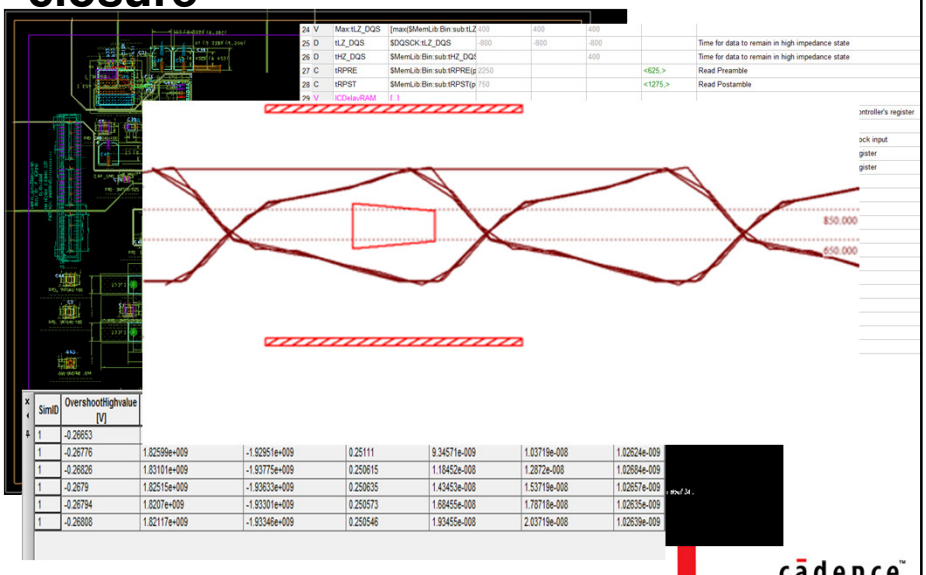
Post-layout verification and Timing closure



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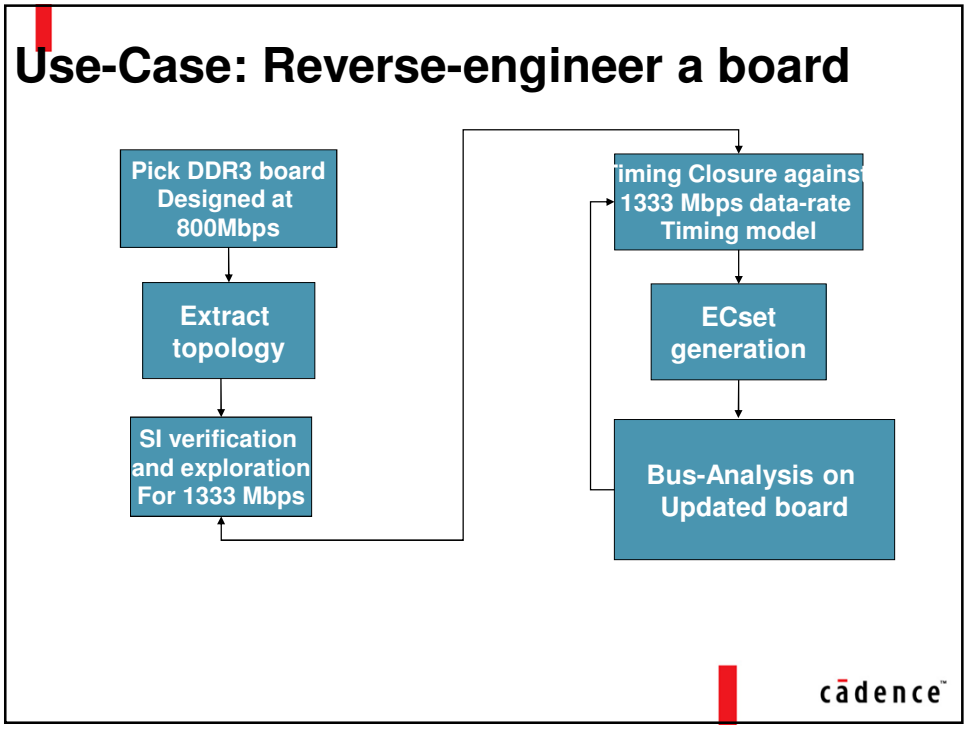
Use-Case: Reverse-engineer a board
Pick DDR3 board Designed at 800Mbps
Extract topology
SI verification and exploration For 1333 Mbps
Timing Closure against 1333 Mbps data-rate Timing model
ECset generation
Bus-Analysis on Updated board
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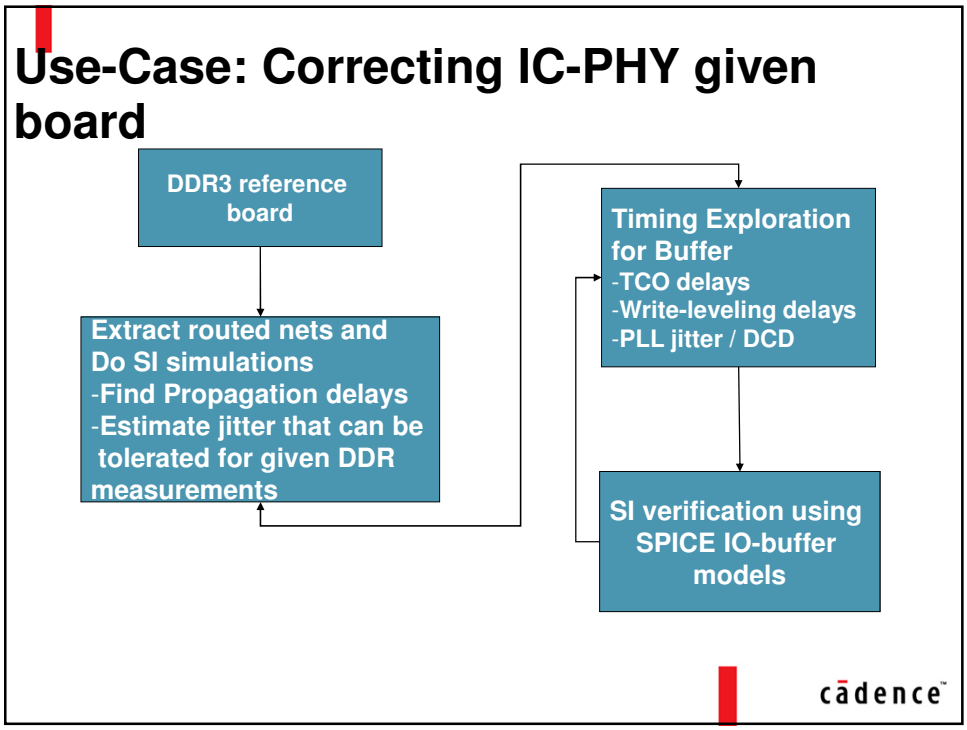
Use-Case: Correcting IC-PHY given board
DDR3 reference board
Extract routed nets and Do SI simulations
-Find Propagation delays
-Estimate jitter that can be tolerated for given DDR measurements
Timing Exploration for Buffer
-TCO delays
-Write-leveling delays
-PLL jitter / DCD
SI verification using SPICE IO-buffer models
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Agenda

- Key Design Challenges
  - DDR3 Timing and SI specifications
- Problem Statement
  - Piecemeal simulations do not guarantee optimal design
- Solution
  - Static Timing Analysis in conjunction with IBIS simulations
- Use-cases
  - Step-by-step method to optimally use EDA flows
- Summary

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Summary

- DDR3 compliance requires multiple specifications to be met, covering timing and signal-integrity measurements.
- Just using SI simulations to meet all specifications and explore solution space is difficult.
- Use of tools in a piecemeal approach can validate specifications but may not result in the most optimal IC/package/board design

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Summary

- Use of STA in conjunction with SI simulations in a methodical manner is needed to achieve optimal design.
- Timing models should be able to handshake data with IBIS simulations at pre-route exploration and post-route verification stages to ensure that both SI and Timing constraints are met.

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