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INVENTIVE

Chip PDN Model for Power Aware Signal Integrity Analysis

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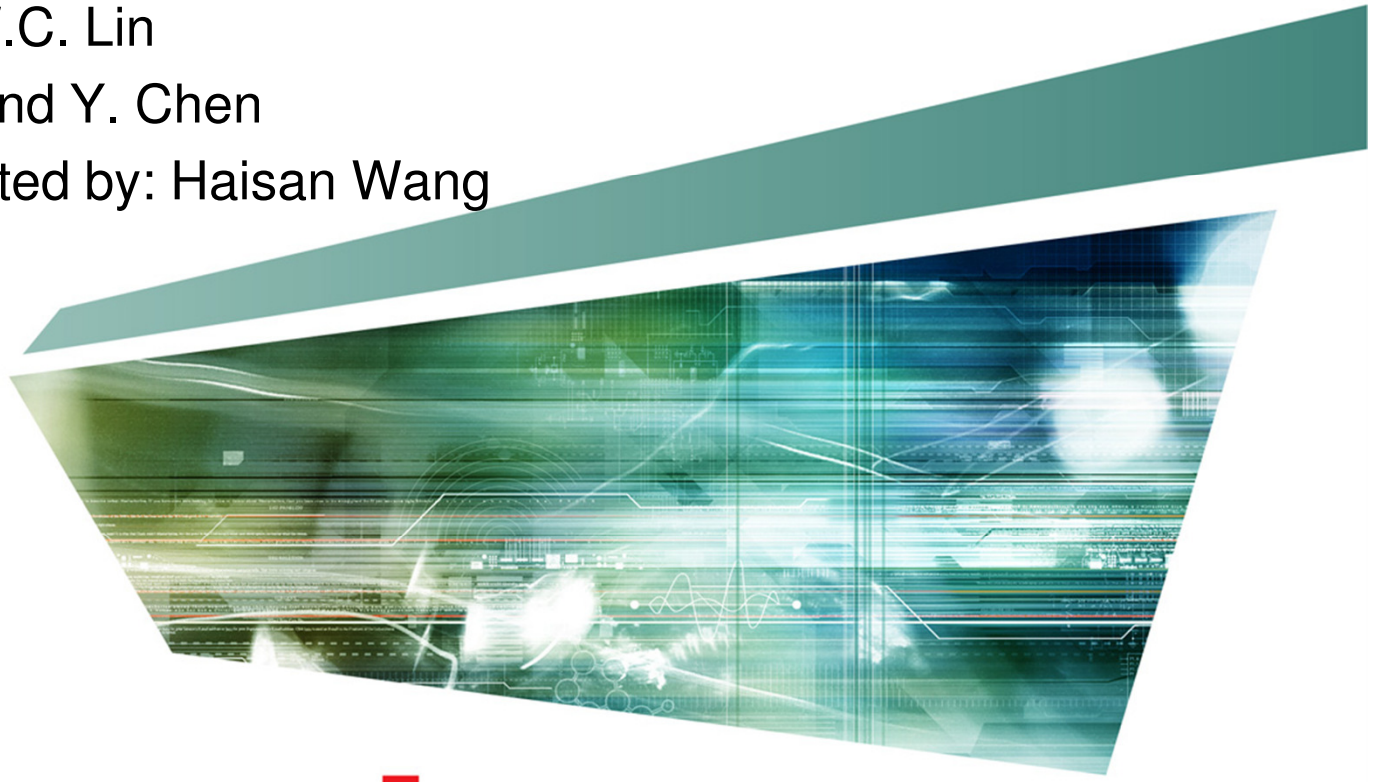

Asian IBIS Summit
Shanghai, China
November 9, 2012

Outlines

- Traditional SSO analysis
- Chip PDN impact
- Limitation in current IBIS SSO simulation
- Chip PDN contribution to capacitance
- How to generate chip PDN model
- Case study—Using chip PDN in SSO analysis
- BIRD proposal to add chip PDN in IBIS

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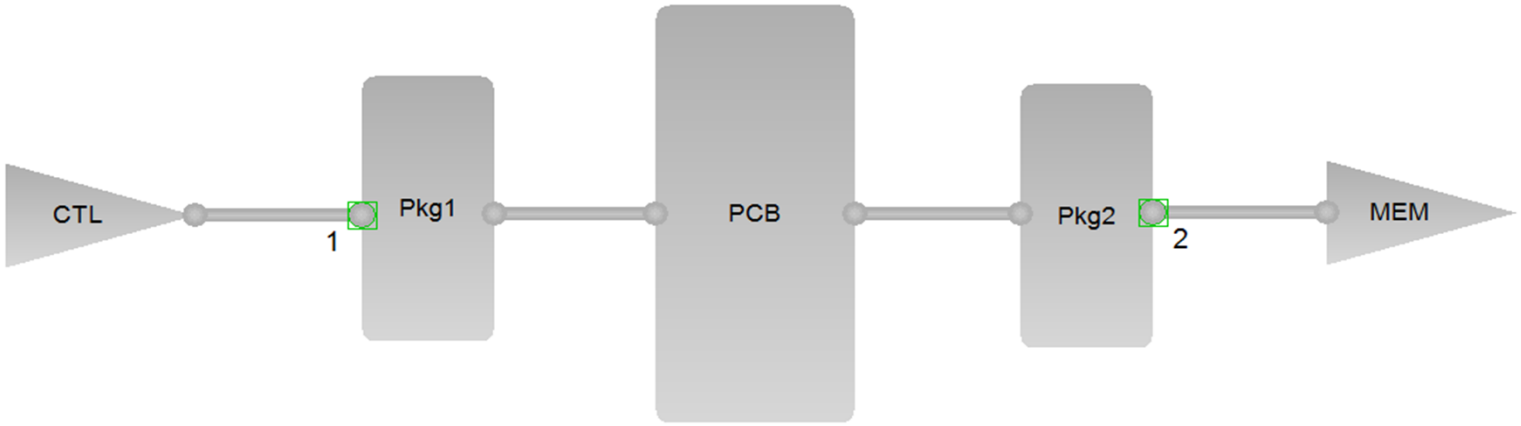
Traditional SSO analysis



- PCB/Package model is extracted by EM solver with signal and power/ground information.
- IBIS without power/ground current and package [Pin]/[Package Model] model are used.
- "Artificially large" power ground fluctuations is observed in SSO analysis due to the lack of PDN model.
- “What if “ RC on die model to mitigate power/ground noise till reasonable level.

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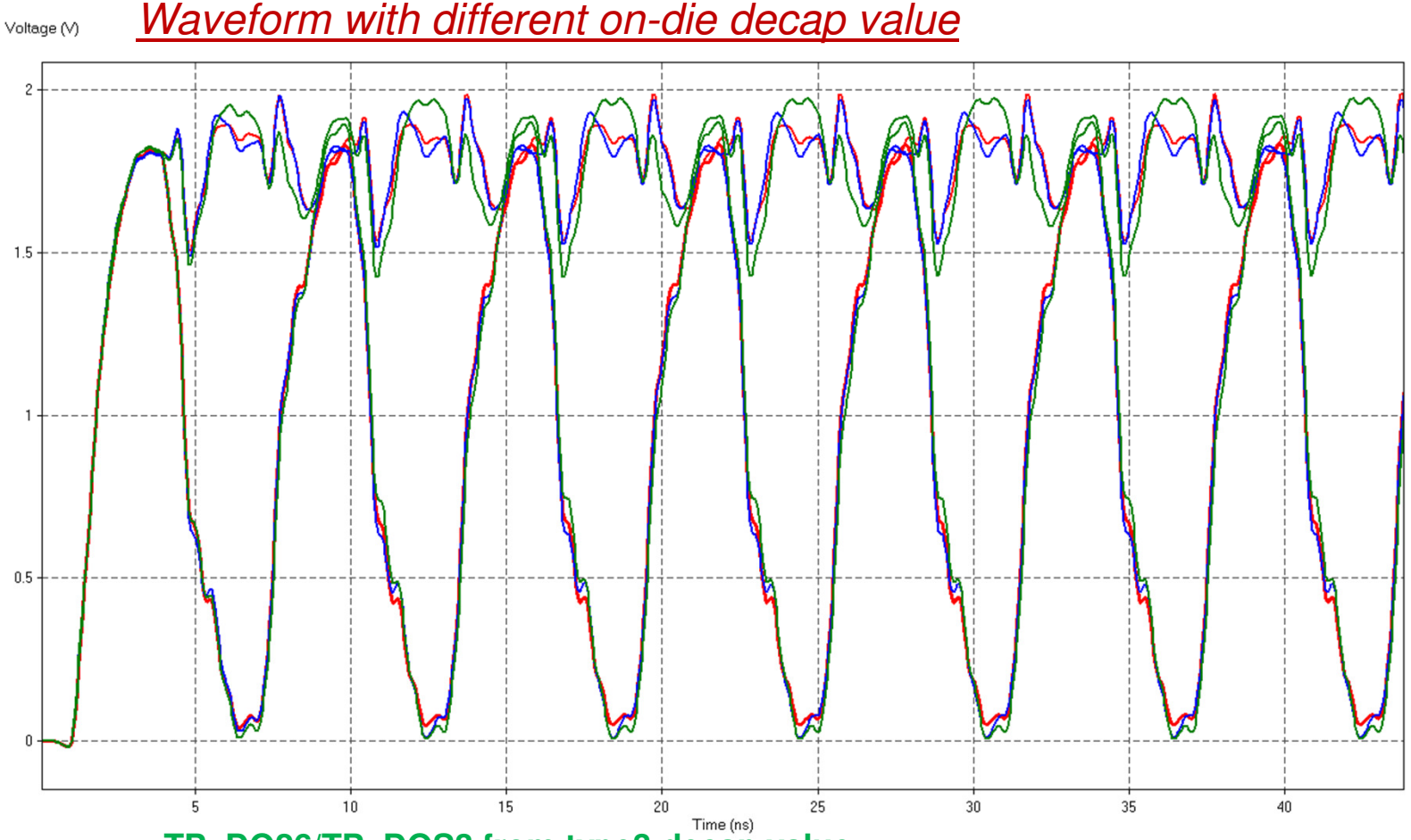
Traditional SSO analysis

1. Driver:1.3nF/0.3 ohms ; Receiver: 1.0nF/0.3 ohms
2. Driver:2nF/0.3 ohms ; Receiver: None
3. Driver:0.5nF/0.3 ohms ; Receiver: 0.5nF/0.3 ohms

Waveform with different on-die decap value



– TP_DQ26/TP_DQS3 from type3 decap value
– TP_DQ26/TP_DQS3 from type2 decap value
– TP_DQ26/TP_DQS3 from type1 decap value

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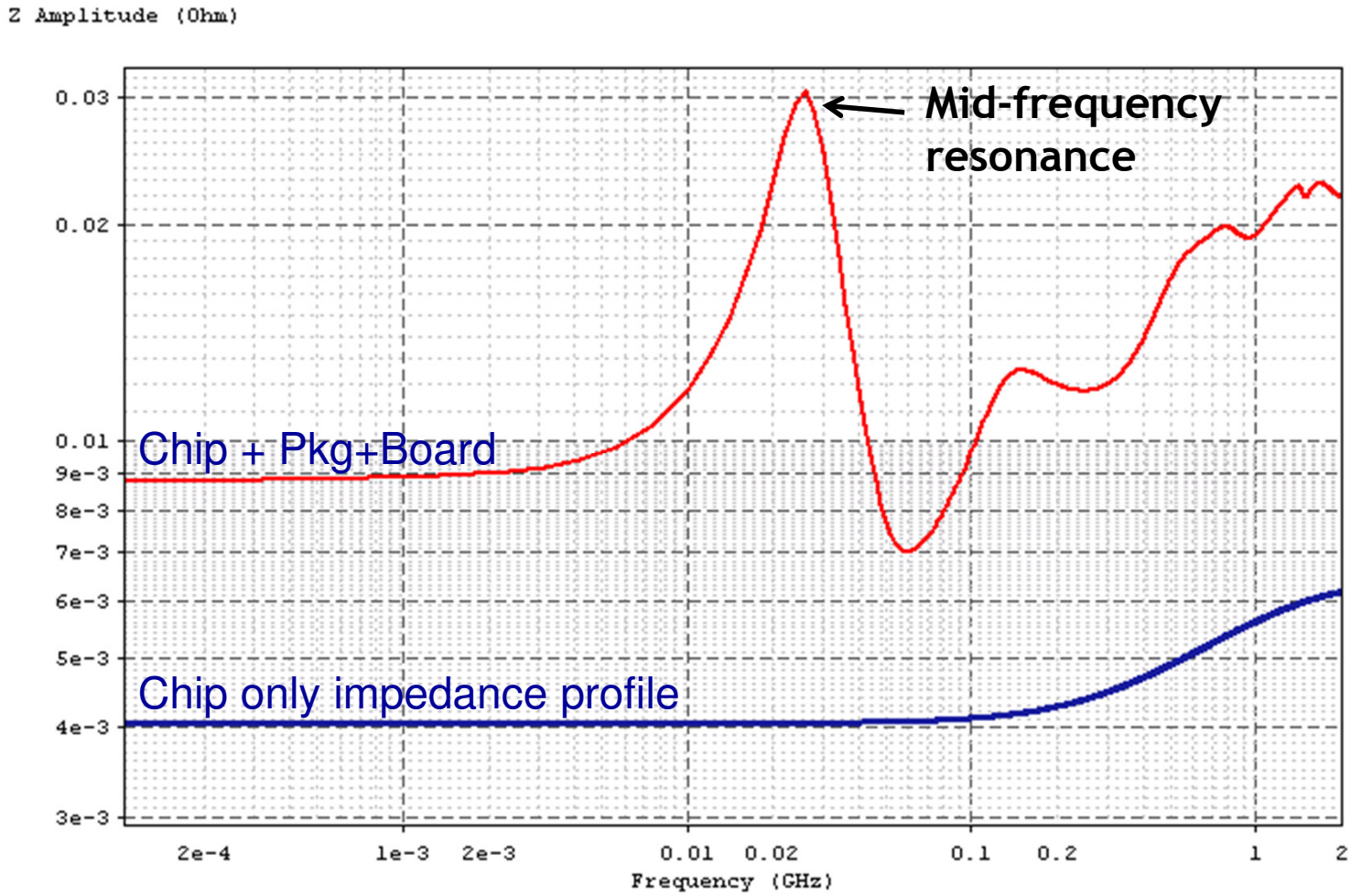
Chip PDN impact



- Chip PDN will help to identify the mid-frequency resonance of the whole system
- This will enhance the power/ground noise if working frequency meet the resonance

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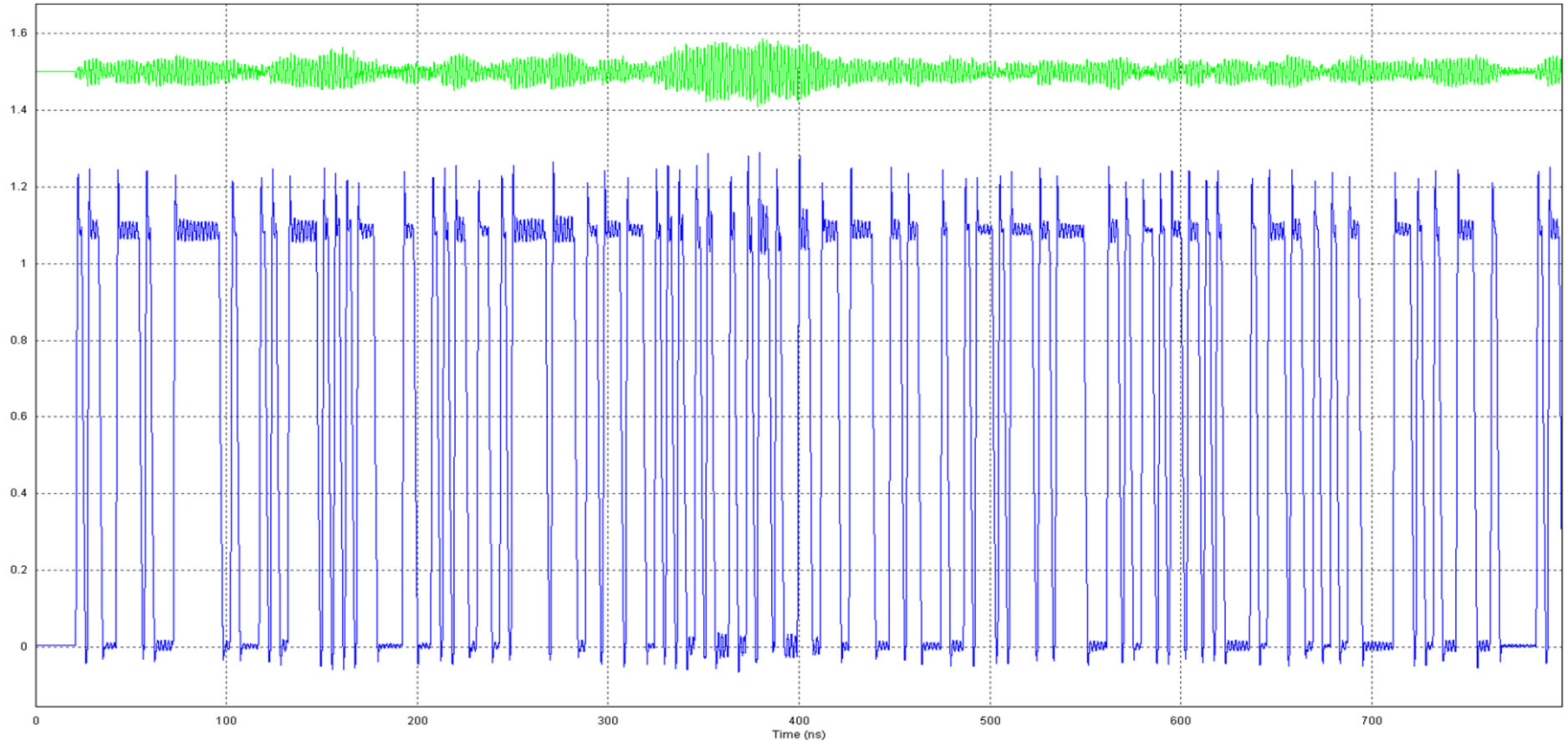
Chip PDN impact



- While performing SSO analysis with random bits pattern, lower frequency transition bits may meet the middle-frequency resonance and lead to larger power/ground noise and worse signal quality.

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Limitation in current IBIS SSO simulation

- IBIS v5.0 is more accurate to simulate the power/ground current with pre-driver/crowbar current and I-V adjusted with Vgs. But IBIS v5.0 only can't still get reasonable power/ground noise.
- Feasible on-die RC model still play a dominant role that impacts the accuracy of the SSO analysis
- On-die RC model is not available from IBIS file.
- On-die capacitance is just estimated from IC designer by how much of MOS caps they placed around I/O cells or estimated by average power dissipation (eq.1)?
- From chip point of view, what are the factors that contribute total on-die capacitance?

C: capacitance of core
P: average power dissipation
f : clock frequency
V: power supply voltage

$$C \sim \frac{P}{V^2 f} \qquad \text{Eq.1}$$

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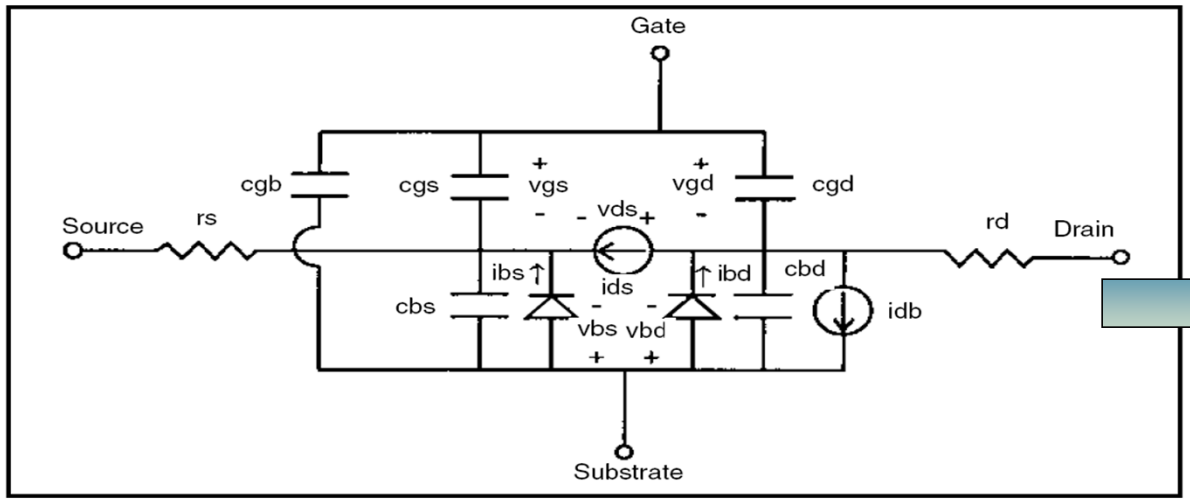
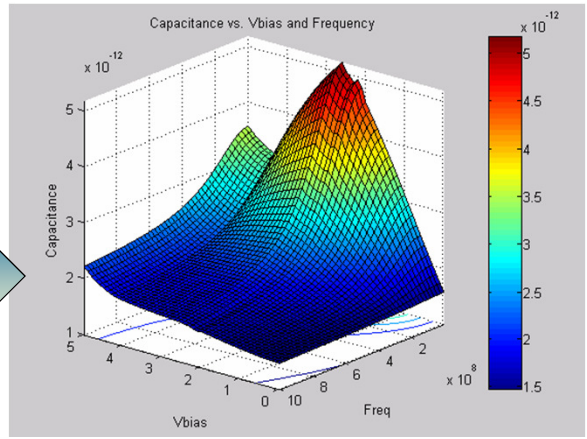
Chip PDN contribution to capacitance

- Parasitics from transistor
  - Parasitic capacitance exists between all MOSFET terminals
  - For the I/O pin, this is modeled in IBIS by C_comp
  - A new compensation capacitor is needed for the power and ground parasitics which is frequency and voltage dependency (first propose by Sigrity in DesignCon 2005)





- MOS Capacitors
  - Like n-MOS capacitors that distributed around I/O circuits

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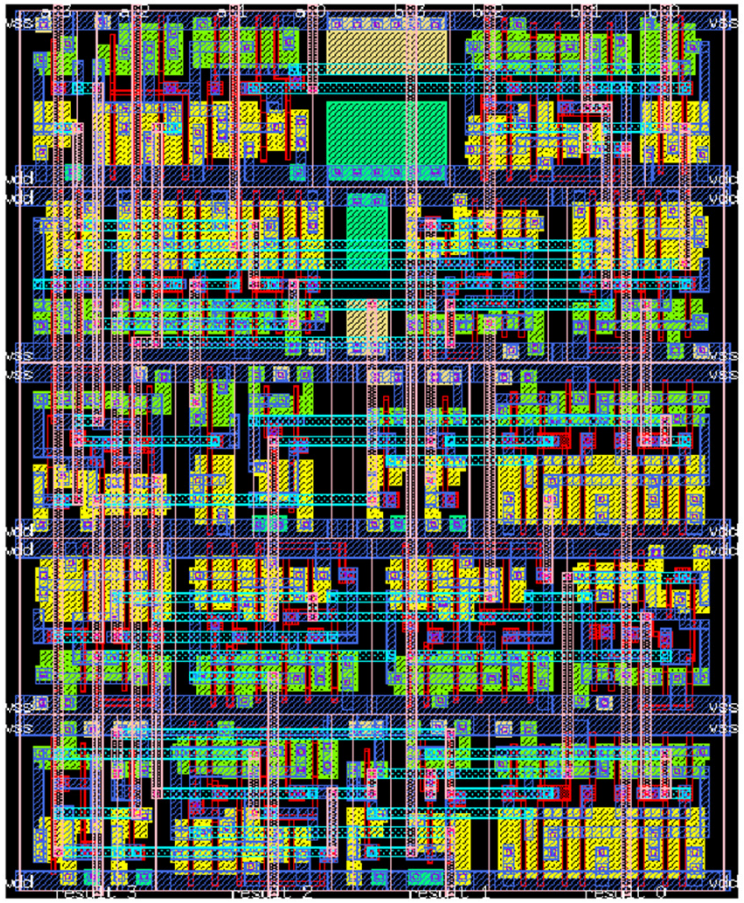
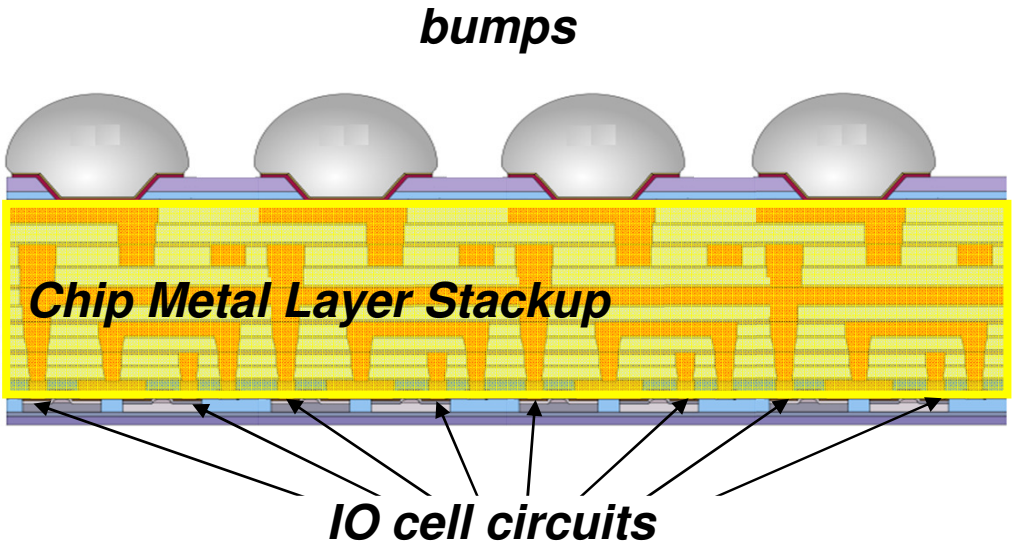
Chip PDN contribution to capacitance

- Outside of the transistors





—Power/ground metal grids outside transistors that contribute capacitance.

—Except MOS caps around I/O cell, MIM caps are distributed on interposer that contributes larger capacitance in current 2.5D IC design

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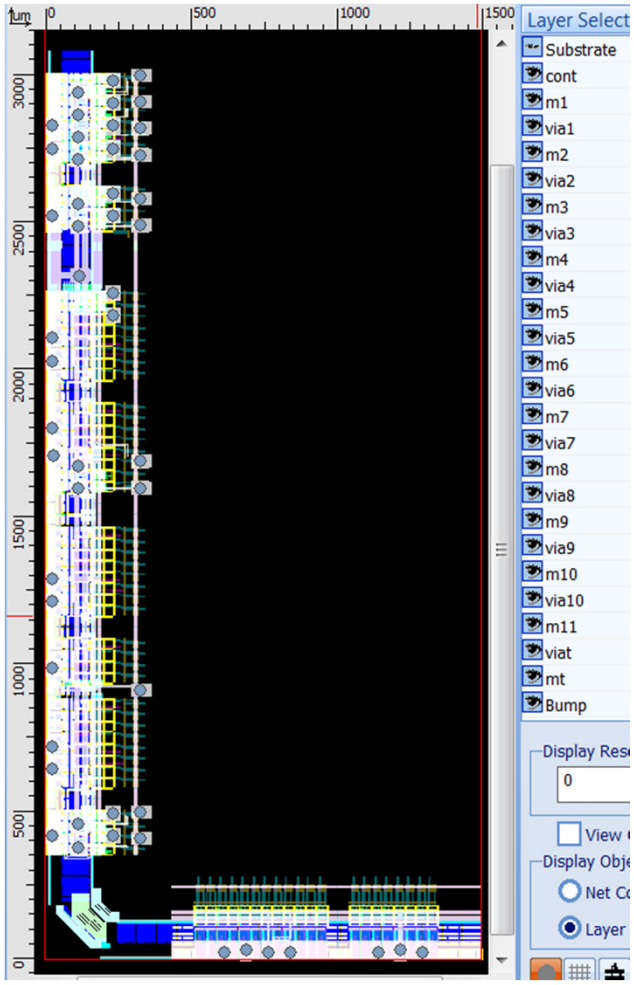
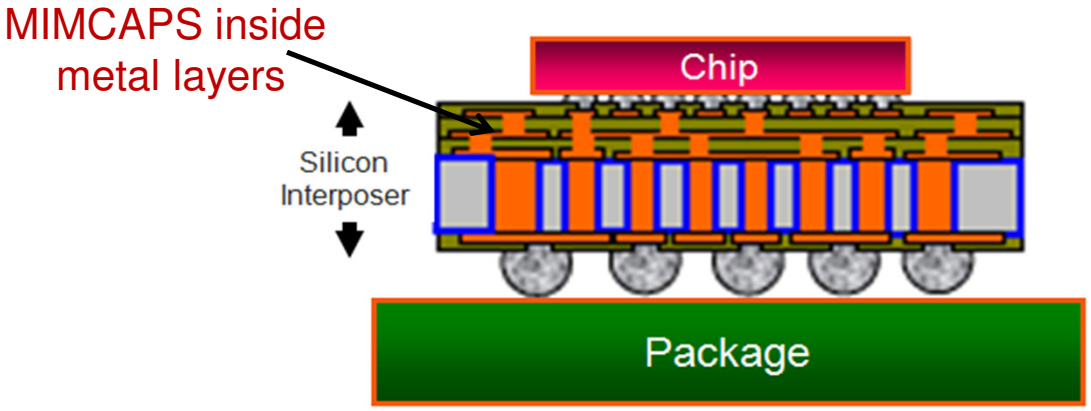
How to generate chip PDN model

- We need to categorize chip PDN model into 2 parts, one is transistor itself, the other is outside the transistor
- IBIS buffer model part only includes circuits and intrinsic parasitic.
- Chip PDN includes GDS layout and MOS capacitors of I/O region.
- Silicon interposer chip design becomes popular and MIMCAPs on interposer contribute sizable capacitance which need to be consider in chip PDN extraction





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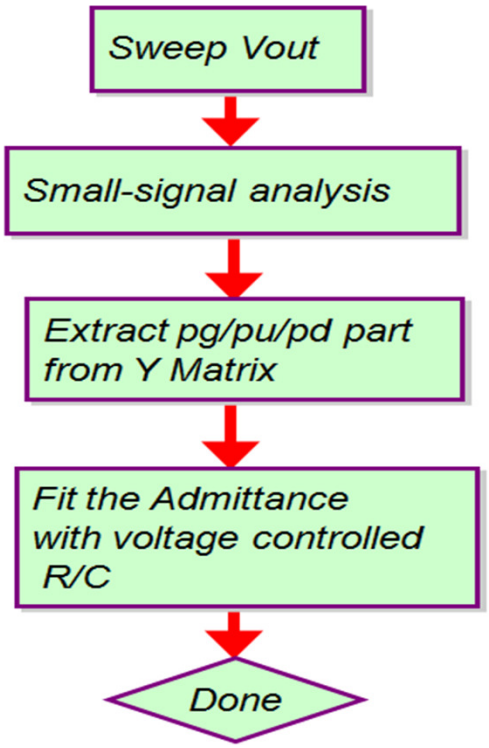
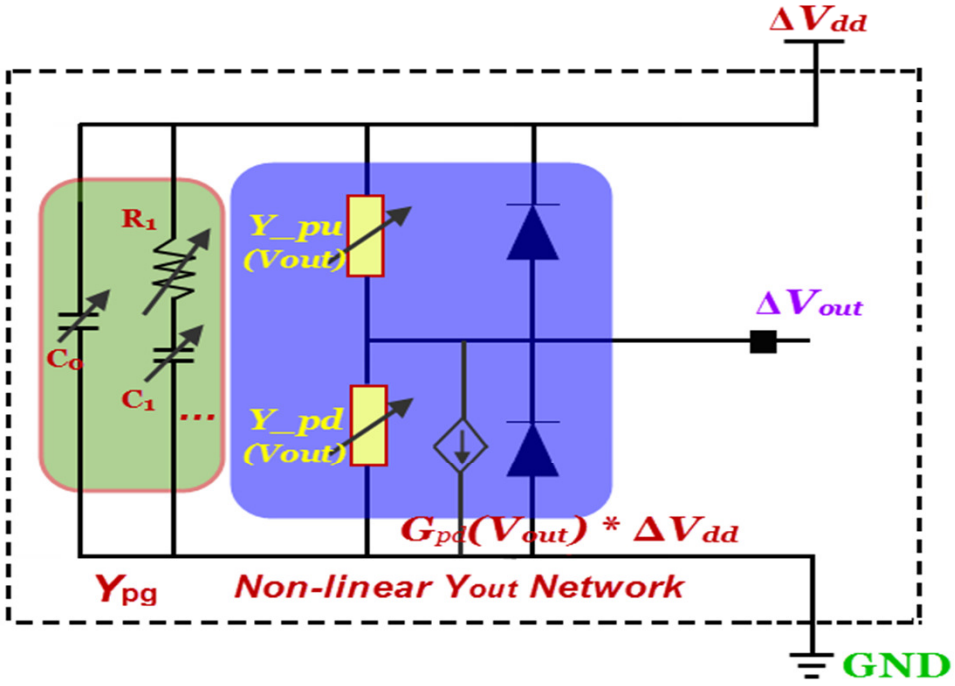
How to generate chip PDN model—transistor

- The IBIS Plus model proposed by Sigrity that dynamic capacitance is included while performing Y admittance extraction between power and ground.
- The equivalent circuit is extracted and added to power/ground pins through [External Model] circuit call in IBIS.





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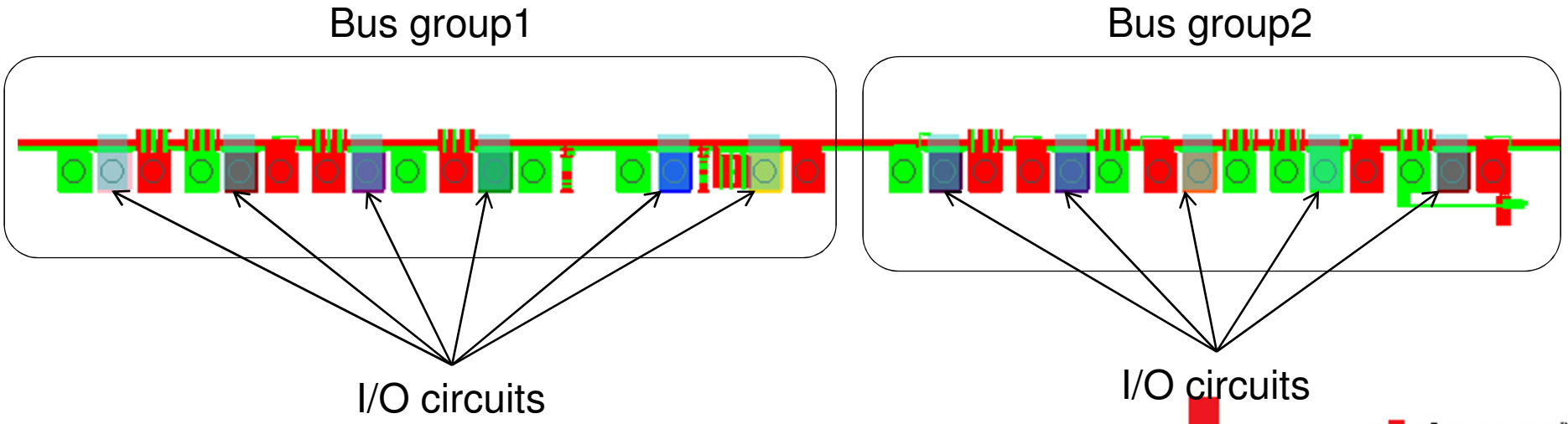
How to generate chip PDN model—outside transistor

- To extract chip PDN by I/O bus group. Same bus group share the same PDN model.
- To set power to ground ports on bumps by different bus group for model extraction
- Capacitance outside the transistor with MOS capacitors can be extracted through chip level extractor.
- The model can be lumped as simple RC value or distributed as SPICE circuit by the concern of frequency bandwidth.



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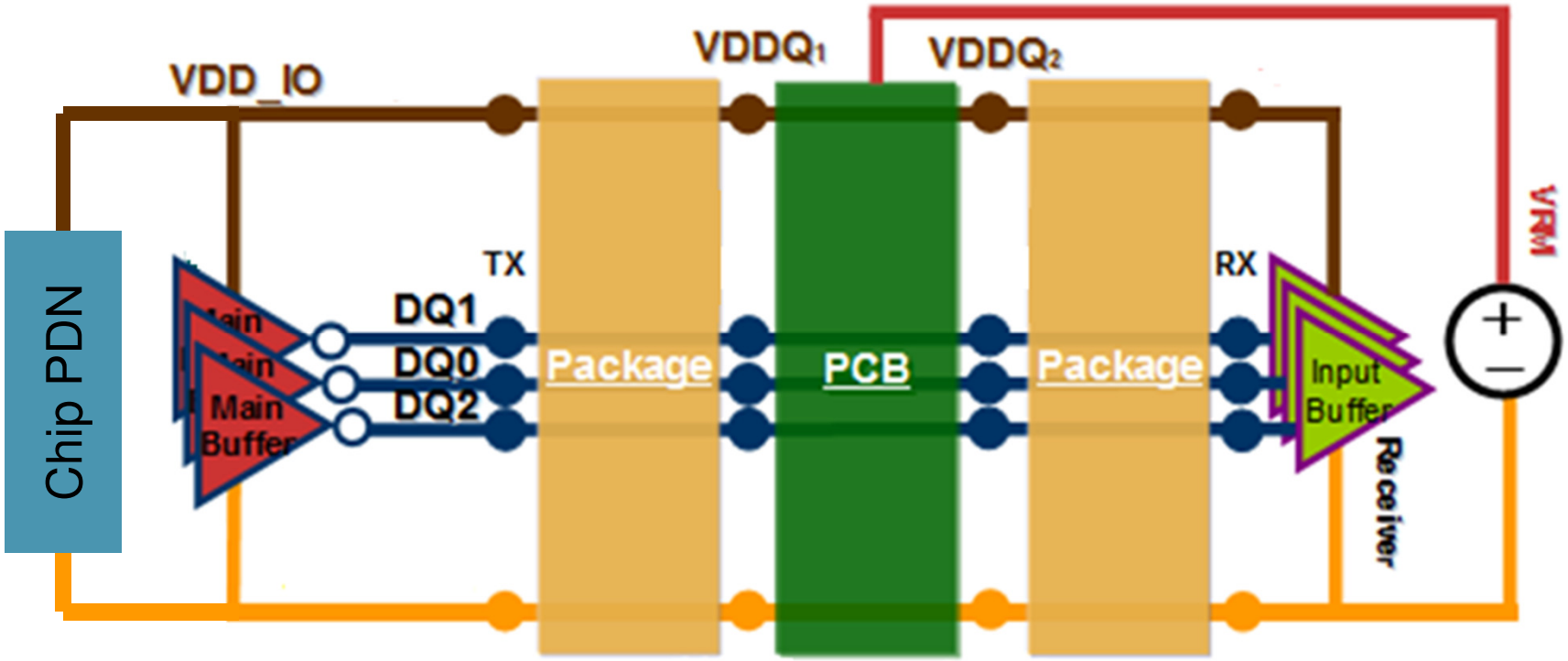
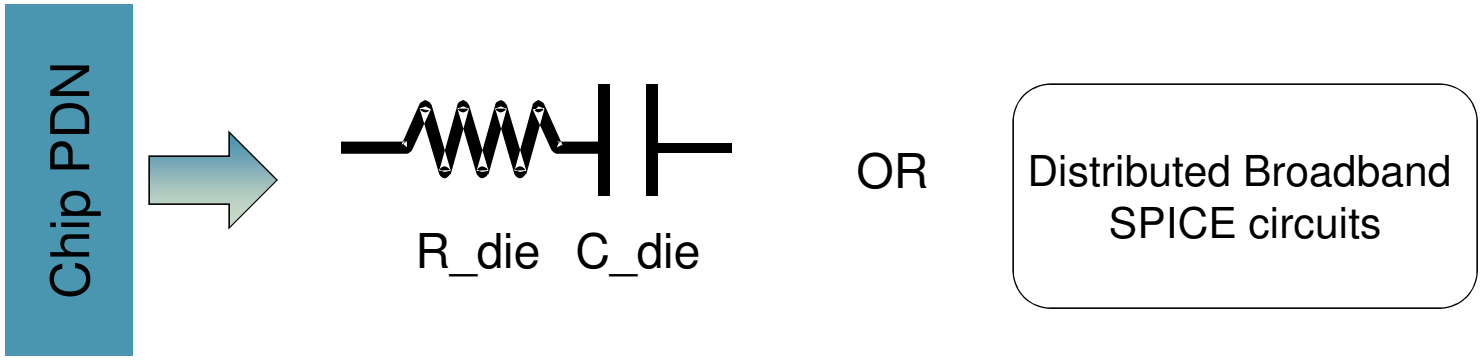
Case study—Using chip PDN in SSO analysis





- Lump RC and distributed broadband model will be applied for SSO analysis with PRBS patterns

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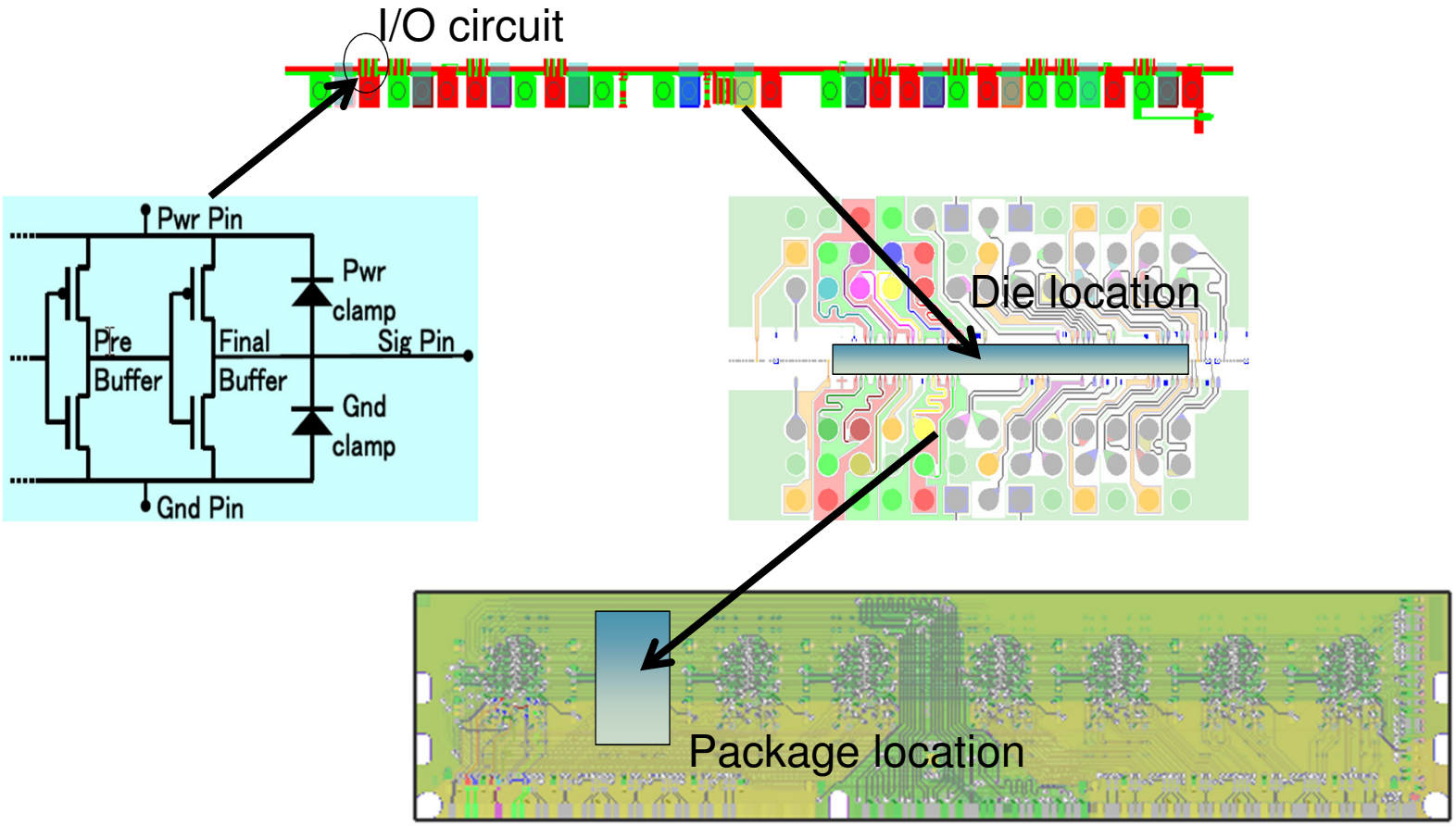
Case study—Using chip PDN in SSO analysis



- I/O circuit is converted into IBIS/IBIS plus model
- Chip is extracted by chip level extractor which include RLCK elements.
- PCB and package are extracted by EM solver and converted into broadband SPICE.
- Only 1 group DDR data is considered for this test

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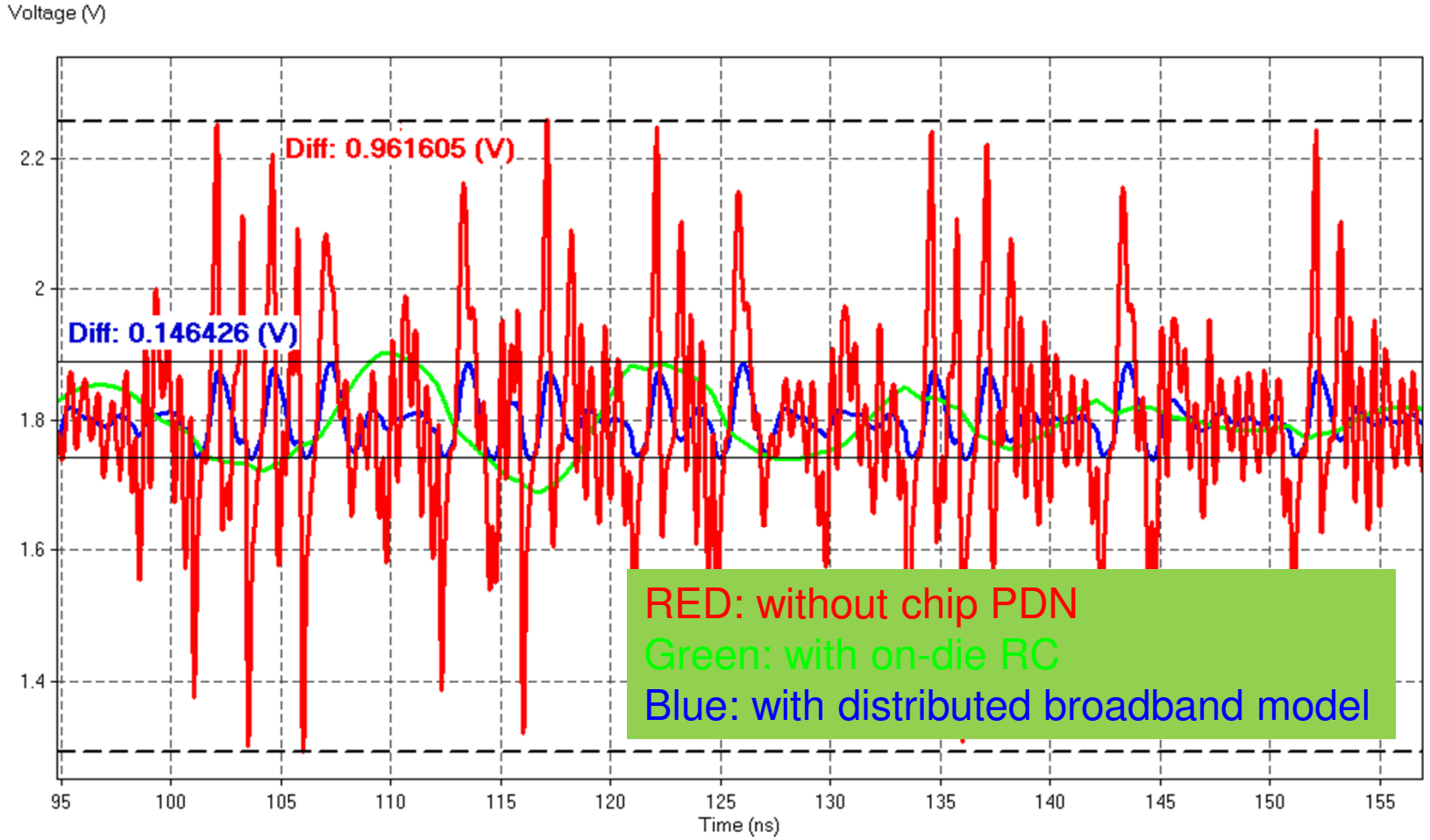
Case study—Using chip PDN in SSO analysis



- On-die RC or better distributed chip PDN model can yield realistic power/ground noise analysis.
- Chip PDN is responsible to filter high frequency noise

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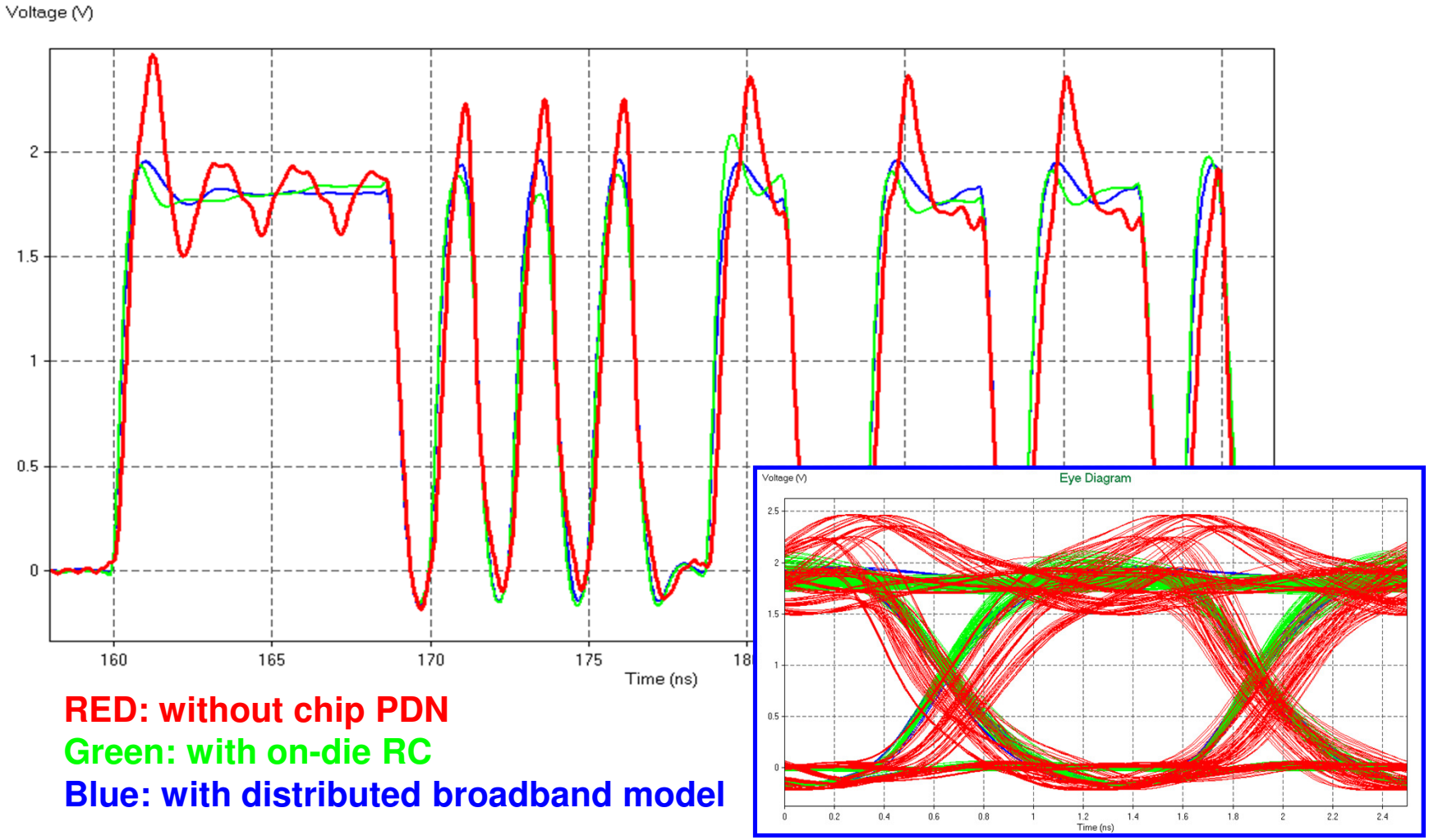
Case study—Using chip PDN in SSO analysis



RED: without chip PDN
Green: with on-die RC
Blue: with distributed broadband model

- Without Chip PDN model, artificially large power/ground noise impact the signal waveform significantly

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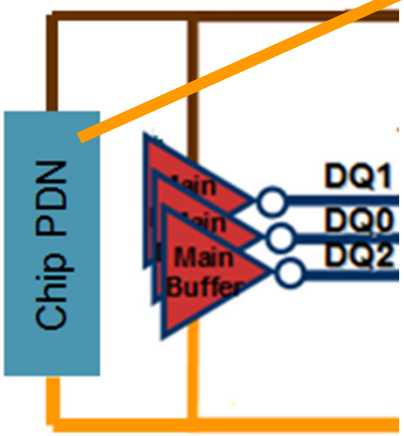
BIRD proposal to add chip PDN in IBIS

- Chip PDN model can be lump RC or SPICE distributed model.
- The chip distributed model is generated by different bus group.
- The bus group is mapping to the bus group in [Pin Mapping] section.
- [Chip PDN Model] can be included in IBIS by [External Model] call



Controller | **OnDie Parasitics** | Package Parasitics

None OnDie RC

File: Controller_pmemio_tsmc.sp ... Sub-circuit: Controller_TSMC_PMEMIO

Parameters

Short Resistor: 0.00 Ohm PDS 0.3 Ohm PDS Capacitor: 0.5n F Edit Default

```
.subckt Controller_TSMC_PMEMIO_Driver_OnDie_RC
+ in_1    in_2    in_3    in_4    in_5    in_6    in_7    in_8    in_9    in_10
+ in_11   in_12   in_14   in_16   in_18   in_20   in_23   in_25   in_27
+ in_29   in_31   in_33   in_13   in_15   in_17   in_19   in_21   in_24
+ in_26   in_28   in_30   in_32   in_34   out_1   out_2   out_3   out_4
+ out_5   out_6   out_7   out_8   out_9   out_10  out_11  out_12
+ out_14  out_16  out_18  out_20  out_23  out_25  out_27  out_29
+ out_31  out_33  out_13  out_15  out_17  out_19  out_21  out_24
+ out_26  out_28  out_30  out_32  out_34
* User-specified OnDie parasitics parameters
+ rshort = 0.001          $ Short Resistor
+ rpds = 0.3              $ PDS Resistor
```

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BIRD proposal to add chip PDN in IBIS

```
[Package Model] DDR3_WBGA_PKG
[Chip PDN Model] DDR_Chip
[Manufacturer]  Cadence
[Package]
.........
[Pin]
.........
[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
B2        GNDBUS2    NC
B3        GNDBUS2    PWRBUS2    GNDBUS2    PWRBUS2
B7        GNDBUS2    PWRBUS2    GNDBUS2    PWRBUS2
B8        GNDBUS2    NC
B9        NC         PWRBUS2
C2        GNDBUS2    PWRBUS2    GNDBUS2    PWRBUS2 |GNDBUS2 is VSSQ
C3        GNDBUS2    PWRBUS2    GNDBUS2    PWRBUS2 |PWRBUS2 is VDDQ
[Define Chip PDN Model]
[Manufacturer] Cadence
[Description]   3mmx3mm Flip-Chip
[External Model]
Language SPICE
|
| Corner  corner_name  file_name  circuit_name
Corner    Typ          chip_PDN.ckt   vddq_pdn
|
| Ports List of port names (in same order as in SPICE)
Ports A_puref A_pdref
```

bus name is mapping to sub-circuit nodes

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