WELCOME FROM MICHAEL MIRMAK, INTEL CORPORATION

On behalf of the I/O Buffer Information Specification (IBIS) Open Forum, I would like to welcome our presenters and guests to the Asian IBIS Summit in Shanghai.

Eight is truly a lucky number, as this year's event is the eighth annual IBIS Summit to be held in the People's Republic. We in the IBIS Open Forum consider ourselves very fortunate to be able to contribute to developing a stronger simulation community across the globe. We are also thankful for the opportunity to see our friends and colleagues in the People's Republic again, and for the detailed and thought-provoking technical program.

We are especially grateful to our sponsors Huawei Technologies, Agilent Technologies, ANSYS, Cadence Design Systems, Intel Corporation, IO Methodology Inc., Synopsys, Teledyne LeCroy and ZTE Corporation, for making this Summit possible.

Our thanks to you for participating and best wishes for a successful summit!

Sincerely,

马梦宽
Michael Mirmak
Chair, IBIS Open Forum

我仅代表 I / O 缓冲信息规范（IBIS）开放论坛，欢迎我们的嘉宾来参加在上海举行的亚洲 IBIS 峰会。

八是一个很幸运数字，今年是在中华人民共和国举行的第八次年度的 IBIS 峰会。IBIS 开放论坛能够为在全球范围内发展一个更强大的仿真社区作出贡献，我们认为自己是非常幸运的。我们也感谢有机会在中华人民共和国再次看到我们的朋友和同仁以及他们深入的技术方案和演讲。

我们要特别感谢我们的赞助商华为技术有限公司，安捷伦科技公司，ANSYS，Cadence Design Systems，IO Methodology，英特尔公司，Synopsys 公司, Teledyne LeCroy 公司和中兴通讯股份有限公司，他们使本次峰会成为可能。

感谢您的参与并预祝会议圆满成功！

马梦宽
主席，IBIS 开放论坛

WELCOME FROM LI JINJUN, HUAWEI TECHNOLOGIES

Ladies and Gentleman,

On behalf of Huawei Technologies, welcome to the eighth annual Asian IBIS Summit (China). I would like to express my appreciation to IBIS Open Forum and all the sponsors for co-organizing this event.

Since 2005, IBIS Asian Summit in China has been the top-level international conference in high speed digital design society in China. I am looking forward to work with IBIS members in China, and to expand our participations in the region.

Huawei has actively involved in all IBIS society's events. We hope to resolve high speed link issues with IBIS Open Forum, EDA vendors and IC vendors. Your comments and suggestions will be deeply appreciated!

Welcome all of you to Shanghai! Hope you will enjoy all the technical discussions and sharing throughout the meeting, and have a nice journey!

Thank you!
Li Jinjun
Huawei Technologies

各位专家，各位来宾：

我代表华为公司，欢迎大家来参加第 8 届亚洲 IBIS 技术研讨会，衷心地感谢 IBIS 协会组织本次会议。

自从 2005 年以来，IBIS 技术研讨会已经成为了中国高速设计领域的一次盛会。我很高兴有机会与 IBIS 协会一起促进和扩大在该领域的分享。

华为积极参与各项 IBIS 活动，希望与 IBIS 协会、EDA 软件、芯片公司一道来共同解决许多高速链路设计上的挑战，欢迎大家会上讨论和建议。

欢迎 IBIS 专家来到上海，希望你们能够喜欢所有的技术讨论和会议分享，度过美好一天。

谢谢大家
华为公司 厉进军

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

8:15 SIGN IN
- Vendor Tables Open at 8:30

8:45 **Welcome**
- Li, JinJun
  (Huawei Technologies, China)
- Wang, Lance
  (Vice-Chair, IBIS Open Forum, IO Methodology, USA)

9:00 **IBIS 5.1: An Overview 5**
Mirmak, Michael (Intel Corporation, USA)

9:25 **Using Latency Insertion Method to Handle IBIS Models 12**
Liu, Ping*#; Tan, Jilin*##; and Schutt-Aine, Jose**
(*Cadence Design Systems, #China, ##USA; and
**University of Illinois, USA)

10:00 BREAK (Refreshments and Vendor Tables)

10:25 **Channel Simulation Platform Creation in Matlab and IBIS-AMI 22**
Simulation Verification
Liu, Jason*; Xue, Harrison*; and Yan, Benny**
(*Celestica and **Cadence Design Systems, China)

10:50 **Effect Analysis of IL Resonance between 0.5~1 Normalized 30**
Frequency Bandwidth
Huang, ChunXiang; Dong, XianQing; and Yu, Lan
(Huawei Technologies, China)

11:20 **Efficient End-to-end Simulations of 25G Optical Links 38**
Liu, Jing-Tao*#; Rao, Fangyi*##; Gupta, Sanjeev**; and
Badesha, Amolak**
(*Agilent Technologies, #China, ##USA; and
**Avago Technologies, USA)

12:00 FREE BUFFET LUNCH (Hosted by Sponsors)
- Vendor Tables

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

IBIS 5.1: An Overview

Michael Mirmak (Intel Corporation)
Presented by
Lance Wang (IO Methodology)

Asian IBIS Summit
Shanghai, P.R. China
November 9, 2012

Expanded from original presented
June 5, 2012

http://www.eda.org/ibis/

Agenda

- Why is IBIS 5.1 different?
- Major Changes
- BIRDs in IBIS 5.1
- Technical Changes
- Before and After
- Next Steps for IBIS
- Your Role: Review and Use!

IBIS 5.1 – A Reformatted Document

- IBIS 5.1 was approved Aug. 24, 2012
- IBIS 5.1 doesn't just add new features and clarifications
  - It's entirely different in appearance and format
- Rationale
  - Ease of change submissions (BIRDs)
  - Ease of editing
  - Improved readability
  - Improved usability, with cross-references & hyperlinks

Major Changes

- Clarifications for AMI and new non-AMI features
  - http://www.eda.org/ibis/birds/
- Appearance based on Microsoft Word*
  - ASCII is no longer used for figures and tables
  - Standards document style has been enforced for headers and body text
- Organization has been unified and improved
  - Terminology has been made more consistent
  - AMI flow, AMI Executable files and AMI Parameters are now more clearly explained, in separate sections (6C, 10 and 10A)

BIRDs in IBIS 5.1

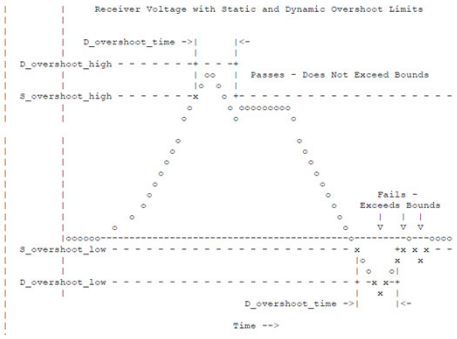
151	IBIS-AMI Modified Reserved Parameters for Jitter/Noise	9-Mar-12
149.1	Usage Out Syntax Correction	17-Feb-12
148	Allowable Model_types with IBIS-AMI	6-Jan-12
146	Clarify sample_interval for IBIS-AMI	9-Dec-11
143.1	Correcting the rules for AMI_Close	7-Oct-11
142	Clarification of [Test Data] and [Test Load] scoping	16-Sep-11
141	[Composite Current] Clarifications	16-Sep-11
140.2	Format Corner and Range Clarification for IBIS-AMI	6-Jan-12
139.2	Reserved_Parameters Order	16-Sep-11
138	IBIS-AMI Section 6c Tables Update	16-Sep-11
137.2	AMI_parameters_in, AMI_parameters_out, msg Clarifications	16-Sep-11
136	Defining Relationships between Type and Format	16-Sep-11
135.1	Add Boolean to BNF for IBIS-AMI	16-Sep-11
134	AMI Function Return Value Clarification	24-Jun-11
133.1	Model Corner C_comp	6-Jan-12
132	Clarification of the Table Format for IBIS_AMI	5-Aug-11
130	Crosstalk Clarification With Respect to AMI	24-Jun-11
127.4	IBIS-AMI Typographical Corrections	9-Dec-11
126	IBIS-AMI New Reserved Parameter AMI_Version	18-Feb-11
120.1	IBIS-AMI Flow Correction	22-Apr-11
115	Clarifying Min/Typ/Max in IBIS-AMI	22-Oct-10
114.3	IBIS-AMI Definition Clarifications	10-Dec-10
113.3	Weak tie-up or tie-down resistance and voltage	19-Nov-10
112	IBIS-AMI clock_times Clarification	11-Jun-10
111.3	Extended Usage of External Series Components in EBDs	24-Apr-09

AMI Technical Changes

- Old AMI files generally still work in IBIS 5.1
- Subtle AMI flow changes
  - Previous flow did not support non-LTI models in TX AMI_GetWave
    - For LTI models, the results should not change
  - AMI_Version identifies .ami files as specifically supporting 5.1 rather than 5.0
  - UseInitOutput has been deprecated
    - Avoids "double-counting" equalization in TX models

Before and After

- Figures and tables have been transformed



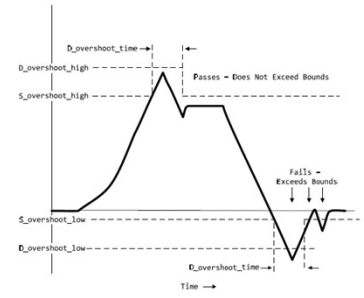


Figure 4 - Receiver Voltage with Static and Dynamic Overshoot Limits

Before...

- The presentation of AMI Parameters…

```
Tx_DCD:

Tx_DCD (Transmit Duty Cycle Distortion) can be of Usage Info
and Out.  It can be of Type Float and UI and can have Data
Format of Value, Range and Corner.  It tells the EDA platform
the maximum percentage deviation of the duration of a
transmitted pulse from the nominal pulse width.  Example of
TX_DCD declaration is:

(Tx_DCD (Usage Info)(Type Float)
        (Format Range <typ> <min> <max>))

Rx-only reserved parameters:

Rx_Clock_PDF and Rx_Receiver_Sensitivity

These reserved parameters only apply to Rx models.  These
parameters are optional; if the parameters are not specified,
the values default to "0".  If specified, they must be in the
following format:

(<parameter_name> (Usage <usage>)(Type <data_type>)
                  (Format <data format>) (Default <values>)
                  (Description <string>))
```

… and After

- The presentation of AMI Parameters…

Parameter: **Tx_DCD**
Required: No
Descriptors:
Usage: Info, Out
Type: Float, UI
Format: Value, Range, Corner, List, Increment, Steps
Default: <numeric_literal>
Description: <string_literal>
Definition: Tx_DCD (Transmit Duty Cycle Distortion) tells the EDA tool the maximum deviation of the duration of a transmitted pulse as a fraction of the nominal pulse width. Entries are assumed to be in units of seconds when declared as Type Float.
Usage Rules:
Other Notes:
Examples:

```
(Tx_DCD (Usage Info)(Type Float)
      (Range 2e-12 1e-12 3e-12))
```


5.1 Parser Now Available!

- A 5.1-compatible Golden Parser has been completed!
  - IBISCHK5, Version 5.1.2, released Oct. 6, 2012
- Free executables available
  - http://www.eda.org/ibis/ibischk5/
  - Source code available under license
- 5.1.2 checks many more .ami file features
- Numerous BUG reports addressed:
  - http://www.eda.org/ibis/bugs/ibischk/

Next Steps

- Future versions will renumber the sections to avoid names such as 10A, 6B, etc.
- Current BIRDs are being rewritten according to the new format
  - 16 BIRDs proposed for *the next IBIS version*
  - Package model improvements, repeaters and backchannel adaptive equalization are addressed
- The next major version: IBIS 6.0
  - Any IBIS 5.2 would be for standardization only

Your Role: Study and Use!

- Please create and test 5.1 models using the new specification and parser!
- Suggestions for the parser, including BUG reports, are welcome
- Review the latest BIRDs proposed for the next IBIS version
  - The schedule for IBIS specification development is accelerating

Thank you for your support of IBIS!

Q/A

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INVENTIVE

Using Latency Insertion Method to Handle IBIS models

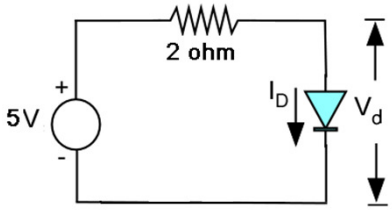
Ping Liu, Jilin Tan
Cadence Design Systems

Presented by: Ping Liu

José E. Schutt-Ainé
University of Illinois at Urbana-Champaign

Asian IBIS Summit
Shanghai, China
November 9, 2012

A simple non-linear Circuit



How to solve I_D and V_d?

Solve transcendental equations

$$I_d = 1pA \cdot \left[\exp\left(40 \cdot V_d\right) - 1 \right]$$

$$5 = V_d + 2 \cdot I_d$$

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Using Newton-Raphson Method

$$X_{n+1} = X_n - \frac{f(X_n)}{f'(X_n)}$$

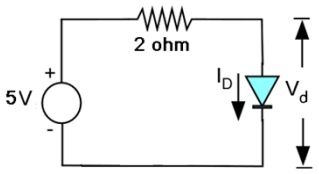
Newton-Raphson iterative process begins with an initial guess and terminates when the difference between successive guesses falls to zero.

$$I_d = 1pA \cdot \left[\exp(40 \cdot V_d) - 1\right]$$

$$5 = V_d + 2 \cdot I_d$$

$$f(V_d) = -5 + V_d + 2pA \cdot \left[\exp(40 \cdot V_d) - 1\right]$$

$$f'(V_d) = 0 + 1 + 80pA \cdot \exp(40 \cdot V_d)$$



$$V_d^{(n+1)} = V_d^{(n)} - \frac{-5 + V_d^{(n)} + 2pA \cdot \left[\exp(40 \cdot V_d^{(n)}) - 1\right]}{1 + 80pA \cdot \exp(40 \cdot V_d^{(n)})}$$

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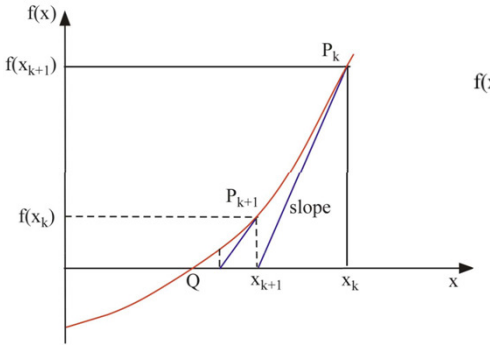
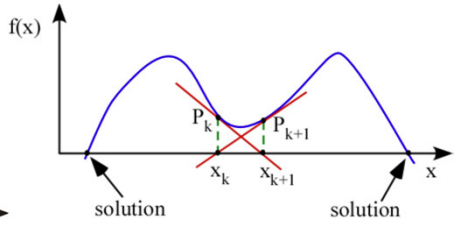
Newton-Raphson Method- Graphical Interpretation





Convergent **Divergent**

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Limitations*

- IBIS data can be unpredictable
- Transient response requires solution of nonlinear system
- Most simulators use Newton-Raphson (NR) technique combined with modified nodal analysis(MNA)
- NR may not converge
- NR may slow down simulation

* J. E. Schutt-Ainé, “IBIS modeling using Latency Insertion Method," European IBIS summit, Italy, May16, 2012.

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Why LIM? *

- LIM does not iterate on nonlinear problems
- There is no convergence issue
- MNA has super-linear numerical complexity
- LIM has linear numerical complexity
- LIM uses no matrix formulation
- LIM has no matrix ill-conditioning problems
- LIM is much faster than MNA for large circuits

* J. E. Schutt-Ainé, “IBIS modeling using Latency Insertion Method," European IBIS summit, Italy, may16, 2012.

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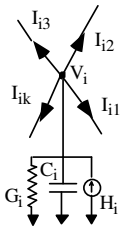
Latency Insertion Method**

- LIM is an efficient time-domain simulator for a large-scaled network
- Uses "leapfrog" scheme to solve node voltages and branch currents

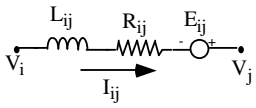
Nodes must have a shunt capacitor

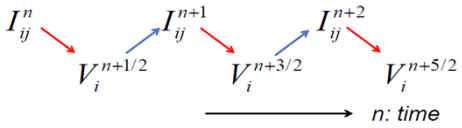
$$V_i^{n+1/2} = \frac{\frac{C_i V_i^{n-1/2}}{\Delta t} + H_i^n - \sum_{k=1}^{M_i} I_{ik}^n}{\frac{C_i}{\Delta t} + G_i}$$



Branches must have an inductor

$$I_{ij}^{n+1} = I_{ij}^n + \frac{\Delta t}{L_{ij}}\left(V_i^{n+1/2} - V_j^{n+1/2} - R_{ij} I_{ij}^n + E_{ij}^{n+1/2}\right)$$





** J. E. Schutt-Ainé, "Latency Insertion Method for the Fast Transient Simulation of Large Networks," IEEE Trans. Circuit Syst., vol. 48, pp. 81-89, January 2001.

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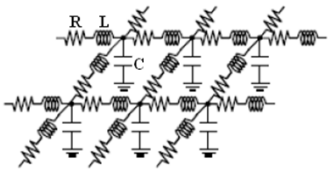
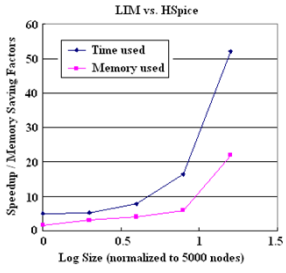
LIM is fast and get faster as circuit size increases





Number of Cells	HSPICE		LIM	
	Memory	Time	Memory	Time
200×200 cells	Memory overflow	abort	102M	1156 s
100×200 cells	320M	9361s	54M	573 s
100×100 cells	108M	2176s	28M	281 s
50×100 cells	53.3M	675s	16M	132 s
50×50 cells	12.4M	244s	9M	47 s

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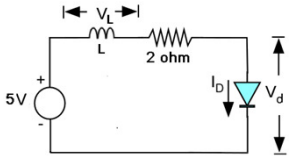
LIM has NO Convergence Issues



Introduce latency in diode circuit through a small L

$$V_L^{n+\frac{1}{2}} = L \cdot \frac{I_d^{n+1} - I_d^n}{\Delta t}$$

Use **Leapfrog:**

$$\left.\begin{aligned} V_L^{n+\frac{1}{2}} &= L \cdot \frac{I_d^{n+1} - I_d^n}{\Delta t} \\ V_L^{n+\frac{1}{2}} &+ 2 \cdot I_d^n + V_d^{n+\frac{1}{2}} = 5 \end{aligned}\right\} \Rightarrow I_d^{n+1} = \frac{\Delta t}{L}\left(5 - 2 \cdot I_d^n - V_d^{n+\frac{1}{2}}\right) + I_d^n$$

$$I_d^{n+1} = 1pA \cdot \left[\exp\left(40 \cdot V_d^{n+\frac{1}{2}}\right) - 1\right] \Rightarrow V_d^{n+\frac{1}{2}} = \frac{1}{40} \cdot \ln\left(\frac{I_d^n}{1pA} + 1\right)$$

Explicit!

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Application LIM to IBIS

- Ku/Kd extraction
- LIM-IBIS formulation
- LIM-IBIS simulation results
- Extension to Bird98
- Extension to Bird95
- Conclusion

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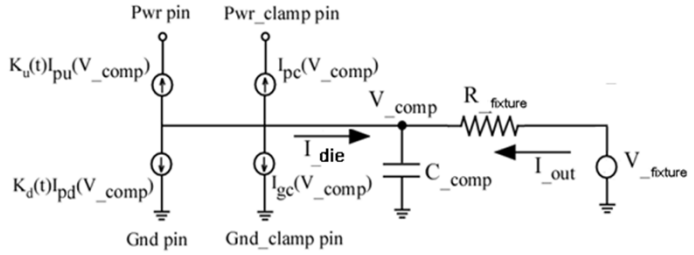
IBIS Ku/Kd Extraction



$$I_{out}^{n} = \left(V_{\_fixture} - \frac{V_{\_comp}^{n+\frac{1}{2}} + V_{\_comp}^{n-\frac{1}{2}}}{2} \right) / R_{\_fixture}$$

$$I_{\_comp}^{n} = C_{\_comp} \frac{V_{\_comp}^{n+\frac{1}{2}} - V_{\_comp}^{n-\frac{1}{2}}}{\Delta t}$$

$$I_{die}^{n} = I_{\_comp}^{n} - I_{out}^{n}$$

Find closest corresponding currents in static IV data
$V_{\_comp1}$ -> I_{pd1}, I_{pu1}, I_{gc1} and I_{pc1}
$V_{\_comp2}$ -> I_{pd2}, I_{pu2}, I_{gc2} and I_{pc2}

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IBIS Ku/Kd Extraction***

Two Equations Two Unknowns

$$-I_{die1}^{n} = K_{ur}^{n} I_{pu1}^{n} + K_{dr}^{n} I_{pd1}^{n} + I_{pc1}^{n} + I_{gc1}^{n}$$
$$-I_{die2}^{n} = K_{ur}^{n} I_{pu2}^{n} + K_{dr}^{n} I_{pd2}^{n} + I_{pc2}^{n} + I_{gc2}^{n}$$

The solution is

$$\begin{pmatrix} K_{ur}^{n} \\ K_{dr}^{n} \end{pmatrix} = \begin{pmatrix} I_{pu1}^{n} & I_{pd1}^{n} \\ I_{pu2}^{n} & I_{pd2}^{n} \end{pmatrix}^{-1} \begin{pmatrix} -I_{die1}^{n} - I_{pc1}^{n} - I_{gc1}^{n} \\ -I_{die2}^{n} - I_{pc2}^{n} - I_{gc2}^{n} \end{pmatrix}$$

The extraction of K_{uf} and K_{df} is similar.

*** Ying Wang, Han Ngee Tan "The Development of Analog SPICE Behavioral Model Based on IBIS Model", Proceedings of the Ninth Great Lakes Symposium on VLSI, GLS '99.

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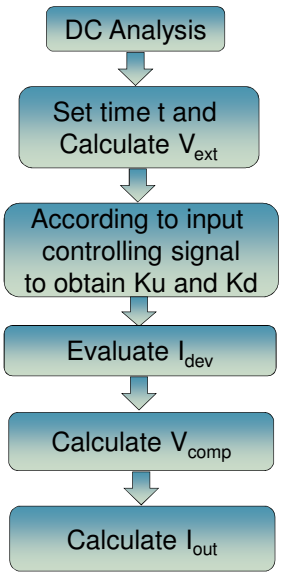
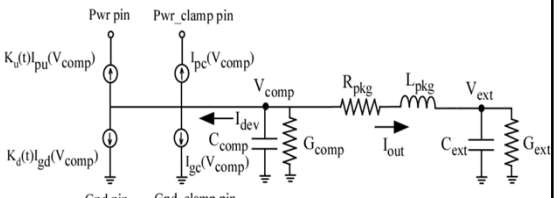
LIM-IBIS Simulation





$$V_{ext}^{n+\frac{1}{2}} = \frac{I_{out}^{n} + \left(\frac{C_{ext}}{\Delta t} - \frac{G_{ext}}{2}\right) V_{ext}^{n-\frac{1}{2}}}{\frac{C_{ext}}{\Delta t} + \frac{G_{ext}}{2}}$$

$$I_{dev}^{n} = K_u^{n} I_{pu}^{n}\left(V_{comp}\right) + K_d^{n} I_{pd}^{n}\left(V_{comp}\right) + I_{pc}^{n}\left(V_{comp}\right) + I_{gc}^{n}\left(V_{comp}\right)$$

Explicit equations

$$V_{comp}^{n+\frac{1}{2}} = \frac{-I_{out}^{n} - I_{dev}^{n} + \left(\frac{C_{comp}}{\Delta t} - \frac{G_{comp}}{2}\right) V_{comp}^{n-\frac{1}{2}}}{\left(\frac{C_{comp}}{\Delta t} + \frac{G_{comp}}{2}\right)}$$

$$I_{out}^{n+1} = \frac{\left(V_{comp}^{n+\frac{1}{2}} - V_{ext}^{n+\frac{1}{2}}\right) + I_{out}^{n}\left(\frac{L_{pkg}}{\Delta t} - \frac{R_{pkg}}{2}\right)}{\left(\frac{L_{pkg}}{\Delta t} + \frac{R_{pkg}}{2}\right)}$$

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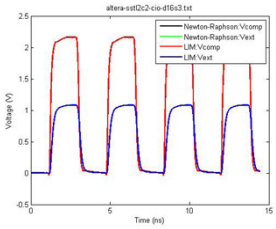
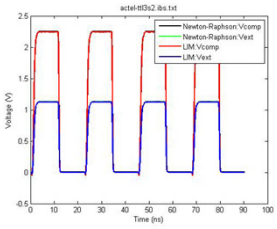
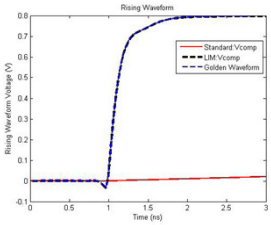
Transient Simulation Results*

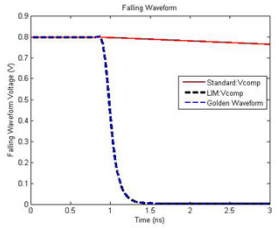
NR and LIM give the same results





In some cases NR fails to converge





* J. E. Schutt-Ainé, "IBIS modeling using Latency Insertion Method," European IBIS summit, Italy, may16, 2012.

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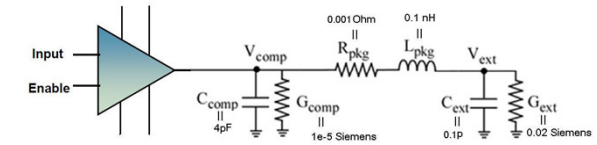
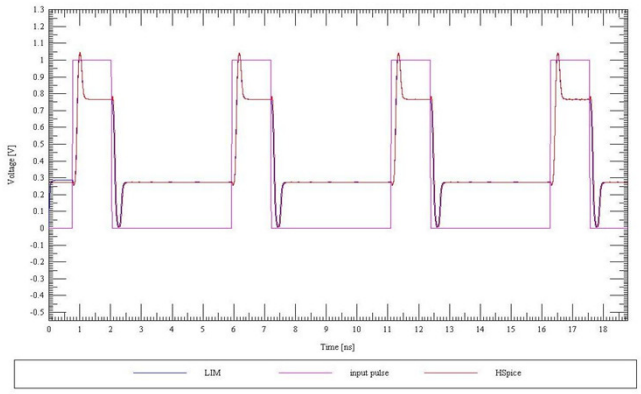
Comparison between LIM and HSPICE





AMI_TX model in ibisamiv2nodiff.ibs file

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Extension to Bird98

LIM-IBIS formulation can **easily be modified** to handle SSN problems

Procedures:

1. **use [ISSO PU] and [ISSO PD] tables (IV table) to generate Ksso_pd and Ksso_pu vectors** as follows:

   Ksso_pd(Vtable_pd) = Isso_pd(Vtable_pd)/Isso_pd(0)

   Ksso_pu(Vtable_pu) = Isso_pu(Vtable_pu)/Isso_pu(0)

2. **Add Ksso_pd and Ksso_pu coefficients to the equations**:

   *Ku(t)Ipu → Ksso_pu(Vtable_pu) *Ku(t)Ipu*

   *Kd(t)Ipd → Ksso_pd(Vtable_pd) *Ku(t)Ipd*

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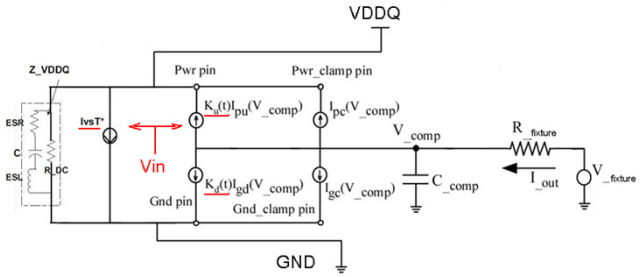
Extension to Bird95

Procedures:

1. Obtain composite currents **I_composite** from IBIS 5.0 file;
2. Obtain **I_B** from regular IBIS simulation during pre-simulation;
3. Obtain the pre-driver current **IvsT***, using

$$IvsT^*(t) = I\_composite(t) - I\_B(t)$$

4. Add **IvsT*(t)** as a voltage controlled current source (**VCCS**) in parallel with IBIS B element model.



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Conclusions

- LIM can be used to simulate **IBIS based circuits** accurately;
- LIM does not suffer from **convergence** problems in handling nonlinear circuits;
- LIM can be extended to handle **IBIS 5.0** models;
- LIM is expected to be several orders of magnitude **faster** for large circuits containing a multitude of IBIS models.

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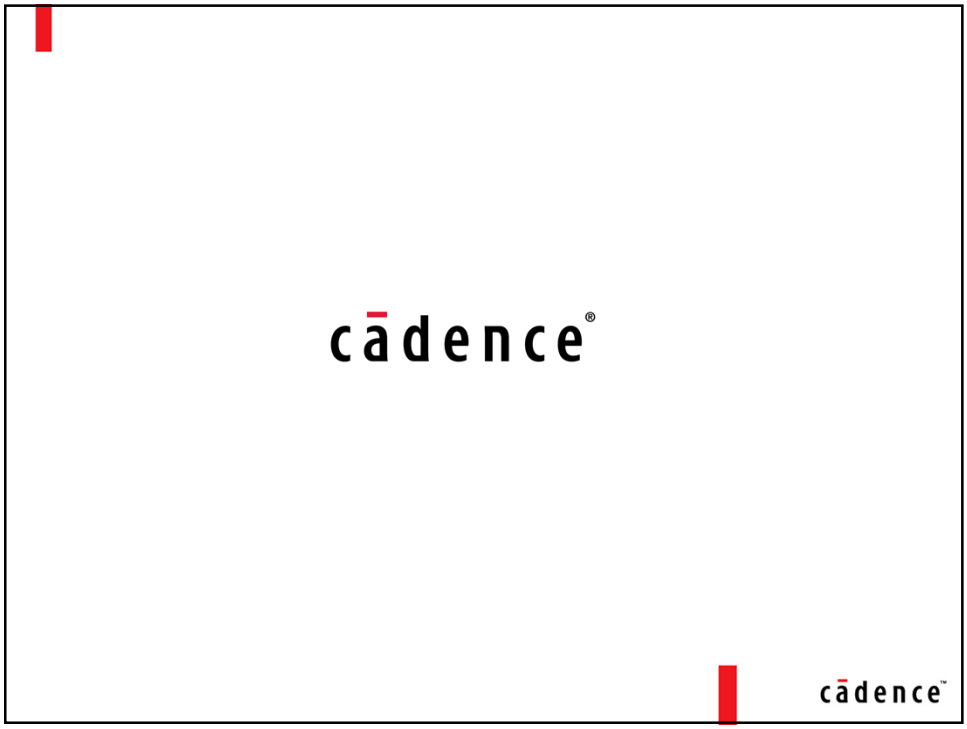
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Channel Simulation Platform Creation in Matlab and IBIS-AMI Simulation Verification

Jason Liu (柳雷), Celestica Shanghai R&D Center
Harrison Xue (薛飞), Celestica Shanghai R&D Center
Benny Yan (宴志), Cadence Design Systems, Inc.

Outline

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- As serial signal rates are rising to the 10+ Gbps, the eye is closed without equalization. Equalization (FFE, CTLE and DFE) can improve the quality of eye at receiver side.
- For a system-level high speed designer, the key to choosing an equalizer is not just to evaluate the characteristic of a lossy channel, but also to determine capability of the equalizers.
- A platform in Matlab is set up and introduced to perform channel simulation with FFE, CTLE and DFE equalization.
- The verification is done based on IBIS-AMI simulation in EDA tool, both results from EDA Tool and from the channel simulation platform are compared.

Channel Simulation Platform Flow

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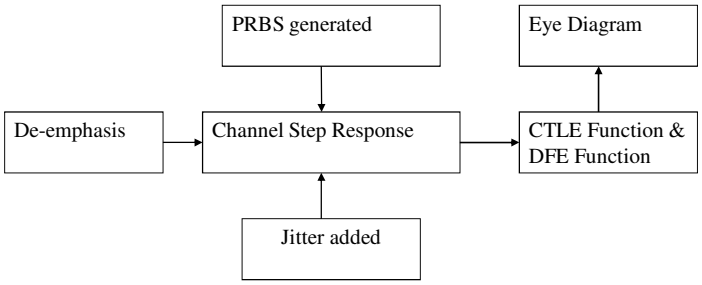

FFE Modeling

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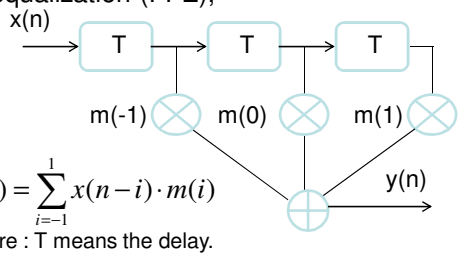
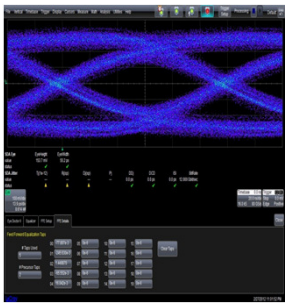
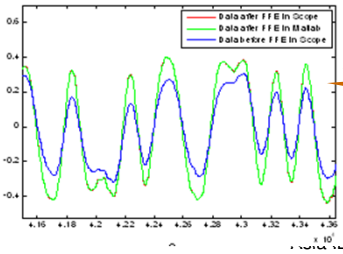
- 3 taps emphasis is modeled as feed-forward equalization (FFE),



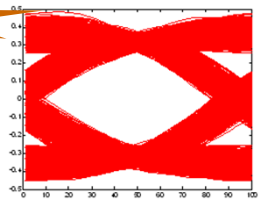
$$y(n) = \sum_{i=-1}^{1} x(n-i) \cdot m(i)$$

Where : T means the delay.





Matched!



Decision Feedback Equalization (DFE) Modeling

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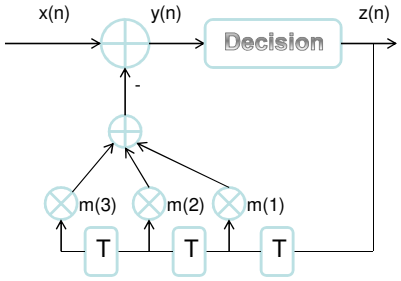
- 3 taps DFE modeling is shown below,



$$y(n) = x(n) - \sum_{i=1}^{3} z(n-i) \cdot m(i)$$

Where : T means the delay.

$$z(n) = \begin{cases} 1 & if\ y(n) >= threshold \\ -1 & if\ y(n) < threshold \end{cases}$$

- DFE tap parameters can be optimized by the equalization algorithm;

Continuous Time Linear Equalization (CTLE) modeling

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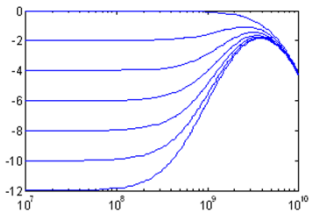
- CTLE is defined in high speed interface specifications to improve the quality of eye before DFE or at Rx side.
- It can be transformed to time domain for convolution.

$$H(s) = 2 \cdot pi \cdot 8e9 \cdot \frac{s + 2 \cdot pi \cdot 2e9 \cdot Adc}{(s + 2 \cdot pi \cdot 2e9) \cdot (s + 2 \cdot pi \cdot 8e9)}$$ where : Adc is DC Gain



Channel Pulse Response (CPR)

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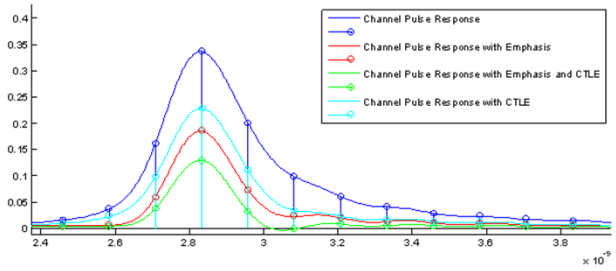
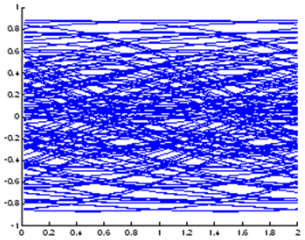


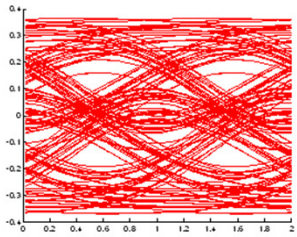
- Channel Pulse Response can not only be used to evaluate channel performance , but also to determine which equalization should be used in the channel.
- An equation is created to evaluate the performance of CPR:

$$M = \frac{P_{main} - \sum_{i \neq main} abs(P_i)}{\sum_{i} abs(P_i)}$$

where: P_{main} is the value of main cursor,
$\sum_{i \neq main} abs(P_i)$ is the sum of rest cursors.



(a) Eye without equalization



(b) Eye with Emphasis

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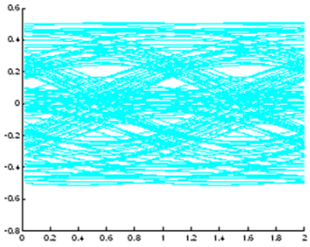
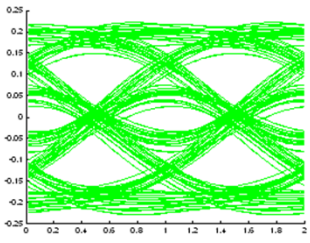


(c) Eye with CTLE



(d) Eye with Emphasis and CTLE

Jitter modeling

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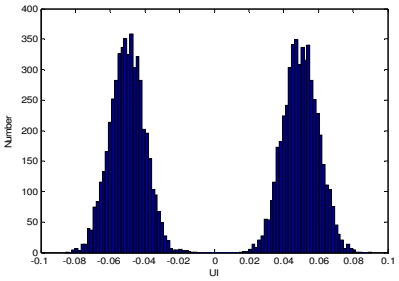
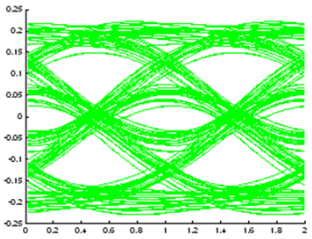
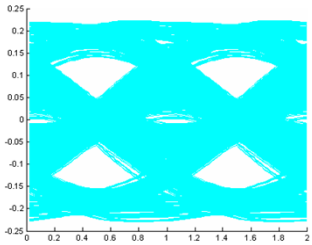
- Total Jitter (TJ) can be modeled as the random jitter (RJ) convolved with deterministic jitter (DJ).
- DJ can be modeled as Dual-Dirac model.





(d) Eye without TX Jitter

(e) Eye with TX jitter



IBIS-AMI Correlation between Matlab and EDA Tool

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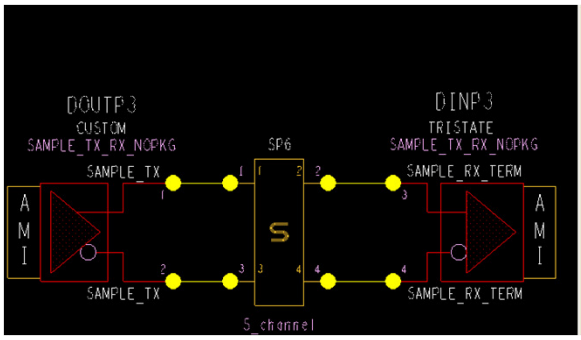
Table 1: EDA tool simulation condition

Pattern	Bits	Signal Rate	Ignore bits	Jitter
PRBS31	2000	5Gbps	250	0



CIRCUIT	
autoSolve	On
tlineDelayMode	length
userRevision	1.0
DESIGN	
DINP3	
bufferModelInverting	SAMPLE_RX_TERM
bufferModelNonInverti	SAMPLE_RX_TERM
sample_rx	AmiModel
tap4	-0.008
tap3	-.04
tap2	-.04
tap1	-.14
filter_on	False
DOUTP3	
bufferModelInverting	SAMPLE_TX
bufferModelNonInverti	SAMPLE_TX
sample_tx	AmiModel
filter_on	False
deemphasis	-3
SP6	

Channel Characteristic and Simulation Settings

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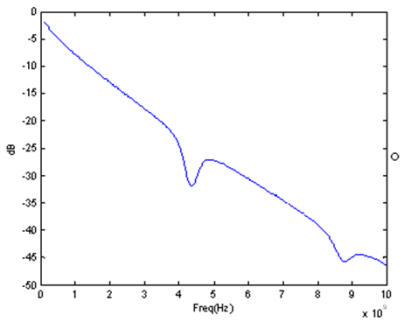

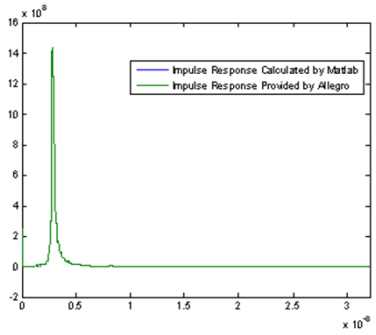

- The figure above is the magnitude of sdd21.
- The figure at above right is the impulse correlation between EDA tool and Matlab calculated from the step response which is obtained from EDA tool.
- Table at below right is the simulation settings.

Case	TX De-emphasis setting:	RX DFE setting:
Case 1	0dB (2 taps)	Off
Case 2	0dB (2 taps)	[0.2 0.05 -0.02 0.01]
Case 3	-3.5dB (2 taps)	Off
Case 4	-3.5dB (2 taps)	[0.1 -0.04 0.01 0.002]
Case 5	-6dB (2 taps)	Off
Case 6	-6dB (2 taps)	[0.05 -0.01 0.003 0.001]

Asia IBIS Summit, Shanghai
China, November 9, 2012

Simulation Correlation Results

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Case No.		#1	#2	#3	#4	#5	#6
EDA tool	Vertical Eye:(mV)	0	181.8	128.3	249.9	275.1	295.5
	Horizontal Eye:(UI)	0	0.451	0.395	0.581	0.688	0.729
Matlab	Vertical Eye:(mV)	0	188	114	267	262	280
	Horizontal Eye:(UI)	0	0.478	0.393	0.556	0.707	0.721
Difference Ratio	Vertical Eye:(%)	0	3.41	12.54	6.40	5.00	5.54
	Horizontal Eye:(%)	0	5.99	0.51	1.07	2.76	1.11

EDA Tool Simulation results

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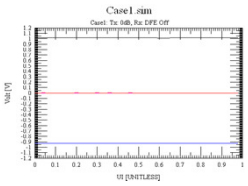
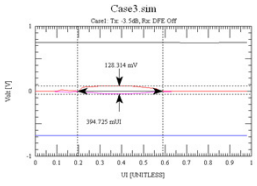
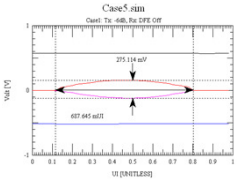


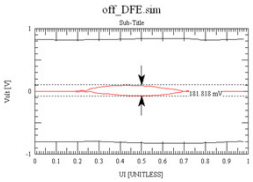
case1



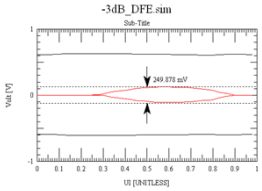
case3



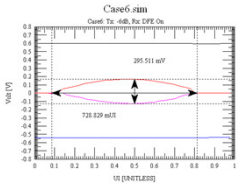
case5



case2



case4



case6

- The eye is closed when both de-emphasis and DFE are off, and the eye is much larger when the two equalization methods are applied.

Matlab Simulation results

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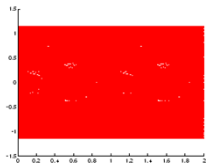
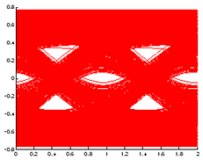
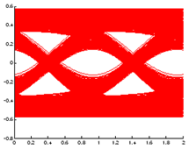


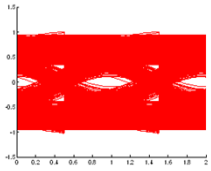
case1



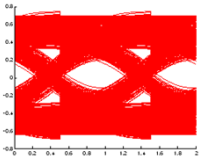
case3



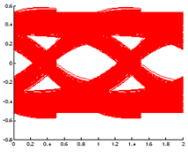
case5



case2



case4



case6

- The eye is closed when both de-emphasis and DFE are off, and the eye is much larger when the two equalization methods are applied. They are identical with the EDA tool simulation results.

Conclusion

- This channel simulation platform based on Matlab is created, which can do system level high speed simulation with FFE, CTLE, DFE and jitter analysis.
- The simulation results show that channel simulation platform based on Matlab is aligned well with EDA tool, the difference is caused by the different seeds of PRBS and different rise/fall time definitions.
- The platform can not only be used to evaluate the performance of a Channel, but also to determine the capability of an equalizer when choosing the equalizer in system-level high speed design.

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Thanks!

Asian IBIS Summit
Shanghai, P.R. China
November 9, 2012

Effect Analysis of IL Resonance between 0.5~1 Normalized Frequency Bandwidth

Huang Chunxing, Dong Xiaoqing , Yu Lan

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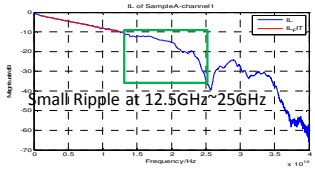
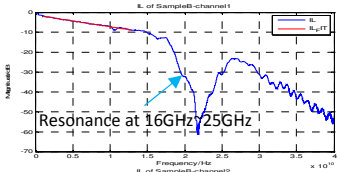
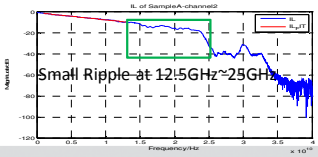
Table of Contents

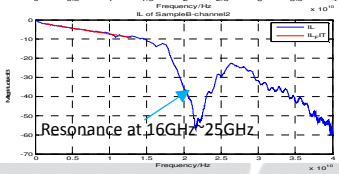
Backgrounds

- When data rate moves to 25Gbps, it is difficult to control stub length within an acceptable range. Resonance is likely to appear in insertion loss(IL) between half Baud-rate and Baud-rate frequencies;
- Two types of IL curves are shown in following four figures. Channel1 and channel2 of sample A have small IL ripples at 12.5GHz~25GHz frequencies, and other two channels of Sample B have big resonance at 16GHz.



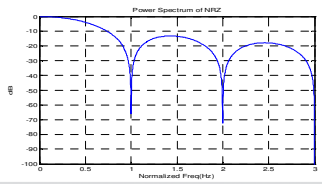


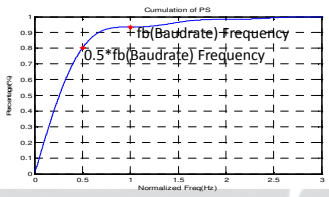




Backgrounds-"Rule of Thumb"

- Four channels of sample A and Sample B shows similar fitted IL performance at 1GHz~12.5GHz frequencies. The question is, will these four channels behave similarly when running 25Gbps data?
- Traditionally, it is a "rule of thumb" that the IL characters at frequencies higher than half baud-rate do have little effects on system performance:
  - Only 13% power are distributed at 0.5~1 baud-rate frequencies and nearly 80% percent power are distributed at 0~0.5 baud-rate frequencies.
- It seems like that IL resonance at 0.5~1 normalized frequencies has little or minor effects on system performance and the system performance of four channels should be very close to each other.





Backgrounds-Resonance effects

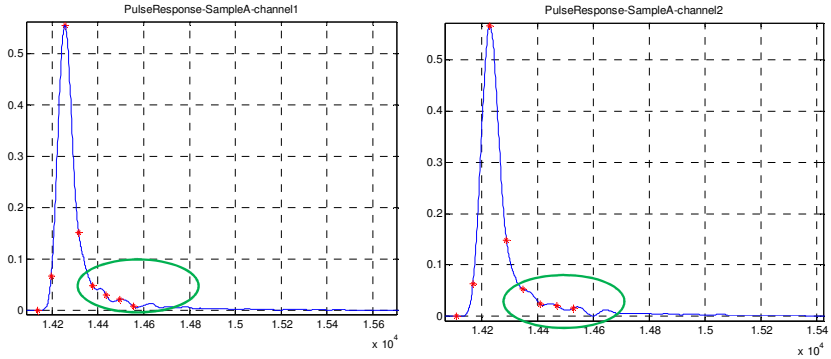
- Is the viewpoint true that IL resonance at 0.5~1 normalized frequencies has small effects on system performance?
  - The energy percentage can not fully represent time domain channel transfer function;
  - IL characteristics at 0.5~1 normalized frequencies also contribute to the output signal quality.
  - DFE and CDR may work differently under different distorted input signal.
- Further analysis should be done by checking performance of these two types of four channel from pulse response and full channel simulation.

Channel Pulse Response Analysis

- Channel pulse response represents transfer characteristics stimulated by a pulse.
- Pulse response of the passive channel could be used to identify time-domain performance impacted by passive channel only.
- Pulse response is a very useful way to quantify channel transfer function from time-domain, including the detailed information of main cursor, post-cursors and pre-cursors.

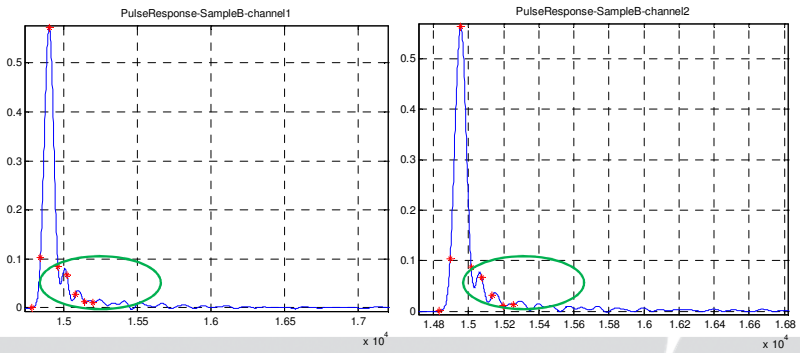
Pulse Response Analysis-Sample A

- Pulse Responses of the two channels from sample A roll down very smoothly and only some small ripples occur at post-cursors.
- It indicates that channel ISI is easy to be compensated by equalization. SerDes RX could see a clean eye.



Pulse Response Analysis-Sample B

- Pulse Responses of two channels from sample B are much different from that of sample A, and big resonances occur at post-cursors(2,3,4,5).
- It indicates that channel ISI is hard to be compensated by equalization. SerDes RX could see a relatively blurred eye and CDR will be more sensitive to this kind of signal due to increased jitter.



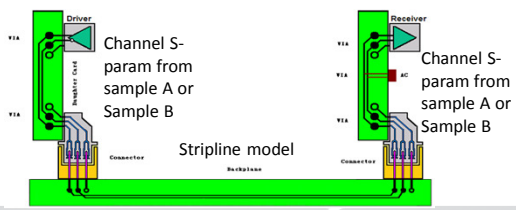
Full Channel Simulation Validation

- Channel pulse response analysis proves that transfer characteristics of sample A and sample B is indeed different.
  - Pulse responses of sample A roll down very smoothly and the resultant ISI is easy to be compensated;
  - Due to big resonances at pulse response post-cursors of sample B, channel ISI is hard to be compensated and CDR performance degrades a lot.
- Based on pulse response analysis result, sample B channels may degrade system BER performance more than sample A channels do. It is required to get SerDes maximum driving capability by performing full channel simulation.

Simulation condition

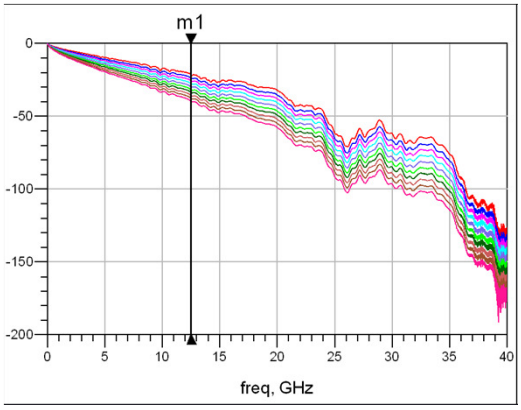
IBM HSS Link Simulator 2.4.5					
Transmitter		Channel	IL:	18~40dB@12.5GHz	Receiver
Core:	HSS28		XTL:	/	Core:	HSS28
Options:	NA	Data Pattern:		PRBS31	Options:	NA
Technology:	cu032	Frequency Offset:		0ppm	Technology:	cu032
Corner:	nominal	Data Rate:		25Gb/s	Corner:	nominal
Package:	fcpbga_21mm_100ohm	Number of Bits:		2Mbits	Package:	fcpbga_21mm_100ohm

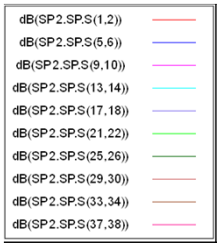
Channel S-parameter are constructed based on channels from sample A or sample B.



Sample A Channels

- Channel S-parameters of IL from 22dB to 40dB are constructed with 2dB increment, and these channels are used to do full channel simulation.

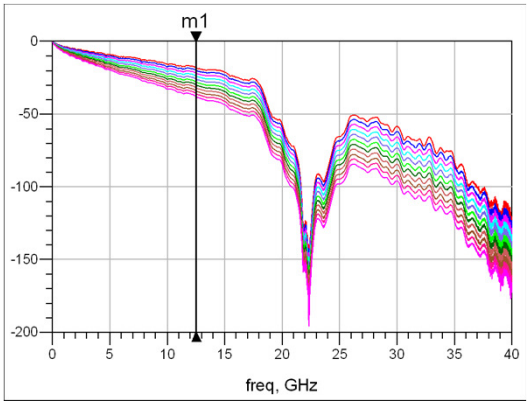




m1
freq=12.50GHz
dB(SP2.SP.S(1,2))=-21.965
dB(SP2.SP.S(5,6))=-24.096
dB(SP2.SP.S(9,10))=-26.003
dB(SP2.SP.S(13,14))=-27.942
dB(SP2.SP.S(17,18))=-29.989
dB(SP2.SP.S(21,22))=-32.021
dB(SP2.SP.S(25,26))=-33.897
dB(SP2.SP.S(29,30))=-35.950
dB(SP2.SP.S(33,34))=-37.966
dB(SP2.SP.S(37,38))=-39.976

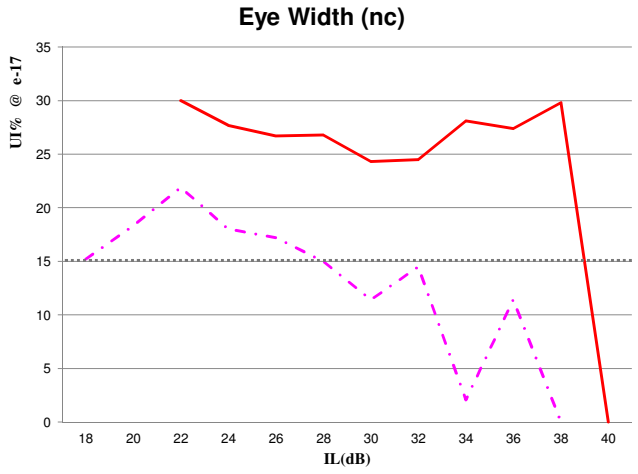
Sample B Channels

- Channel S-parameters of IL from 18dB to 38dB are constructed with 2dB increment, and these channels is used to do full channel simulation.



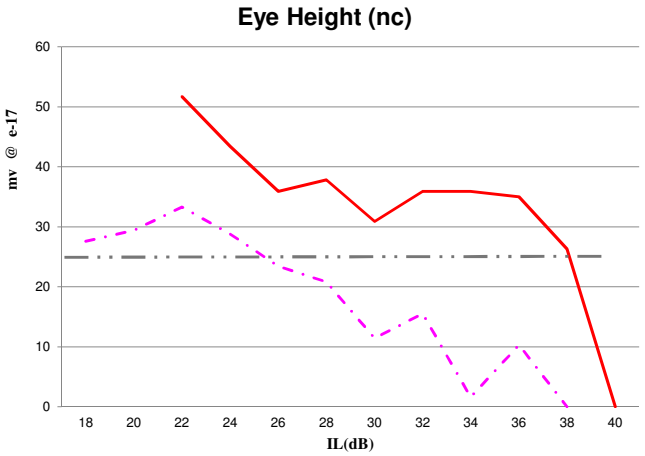
m1
freq=12.50GHz
dB(SP2.SP.S(1,2))=-18.061
dB(SP2.SP.S(5,6))=-20.069
dB(SP2.SP.S(9,10))=-22.066
dB(SP2.SP.S(13,14))=-24.042
dB(SP2.SP.S(17,18))=-26.016
dB(SP2.SP.S(21,22))=-28.010
dB(SP2.SP.S(25,26))=-30.000
dB(SP2.SP.S(29,30))=-31.964
dB(SP2.SP.S(33,34))=-34.090
dB(SP2.SP.S(37,38))=-35.970
dB(SP2.SP.S(61,62))=-38.007

Simulation result : Eye Width (nominal case)



Link	Eye width
Sample A	38dB
Sample B	28dB

Simulation result : Eye Height (nominal case)



Link	Eye height
SampleA	38dB
SampleB	25dB

Conclusions

- The SerDes's maximum driving capability under sample A and sample B channels shows very different results. When running at channels of Sample A, SerDes driving capability reaches 38dB but degrades to 25dB when running at Sample B channels.

SerDes core Driving capability--25Gbps, Nominal case, NO XTK			
Link	Bandwidth(GHz)	Driving Ability(dB)	Eye Mask:
Sample A	40(Measurement)	~38	EyeH: 25mv EyeV: 0.15UI
Sample B	40(Measurement)	~25	

Conclusions:

- The viewpoint that IL resonance at 0.5~1 normalized frequencies has small effects on system performance is not true.
- Take care to remove IL resonance between 0.5~1 normalized frequencies when designing 25Gbps system passive link. It helps SerDes reach its maximum link driving capability from the perspective of passive link optimization.

Thank you

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Efficient End-to-end Simulations of 25G Optical Links

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Shanghai, China

November 9, 2012

Outline

- Challenges in end-to-end optical link simulation
- AMI Modeling and Simulation Approach for Optical Channel
- Optical Models
- Simulation Results and Discussion
- Summary

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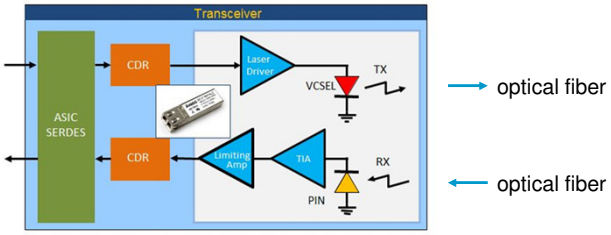
Bandwidth of traditional electrical link is increasingly limited by channel loss above 25G.

Advantages of optical channels:

- Much smaller loss and superior bandwidth
- Flawless connectivity between digital boards and backplanes
- Small footprint
- Reduced EMI
- Promising candidate to replace electrical links

Optical Link System



Inside SerDes Tx & Rx

- Equalization (FFE, CTLE & DFE)
- Clock-data recovery (CDR)

Inside optical module

- Input voltage signal drives VCSEL to emit photons
- Photons propagate along optical fiber
- Photons are converted into photocurrent in PIN
- TIA converts current into output voltage

Challenges in Full Channel Simulation

- Need to model both electrical and optical portions of the link
- Take into account SERDES equalizers and CDR
- Capture behaviors of optoelectronic devices
  - Thermal effects
  - Nonlinearity
  - Optical dispersion and loss
  - Device bandwidth
  - Laser and electrical noise
- Implementation details are proprietary for SERDES and optical Vendors
- Information typically not accessible to external simulator

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Algorithmic Modeling Interface (AMI) Overview

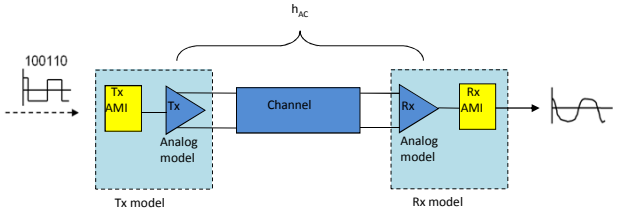
- AMI is introduced in IBIS 5.0
- Defines SERDES behavioral modeling interface
- An AMI model consists of analog model and algorithmic (AMI) block
- Analog model: regular IBIS model, represents rise/fall edge and impedance/load.
- AMI bock: SW executable, models Tx/Rx logics including gain control, equalizers and CDR
- AMI block implements three standard functions

  AMI_Init: performs model initialization and initial EQ optimization

  AMI_GetWave: takes a waveform as input, and returns a modified waveform

  AMI_Close: release model

AMI Simulation Methodology



- Assume Tx analog model, channel and Rx analog model are linear and can be represented by a combined impulse response, h_{AC}.
- Assume high impedance interface between analog model and AMI block so they are electrically decoupled.
- Simulation steps:
  1. Square wave representing bit sequence is sent into Tx AMI
  2. Tx output is convolved with h_{AC}
  3. Resulting waveform is sent into Rx AMI
  4. Rx output is used to calculate eye diagram and BER

Advantages and Limitation of AMI

Advantages of AMI

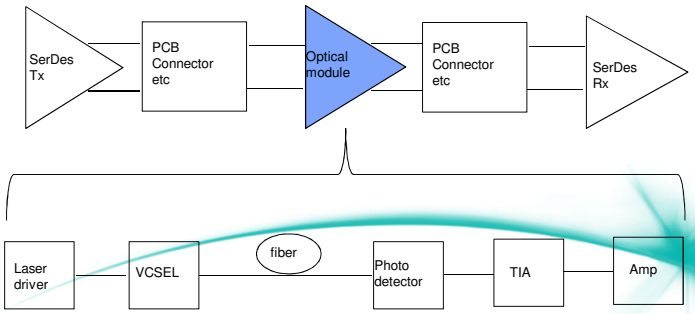
- Models capture SERDES internal functionalities
- IP protection: models are delivered as DLL or/and shared object, concealing implementation details.
- Interoperability between models from different vendors
- Highly efficient link simulation, capable to process millions of bits in minutes

Limitation

- Assumes linear channel
- Optical channel is known to be strongly nonlinear and noisy

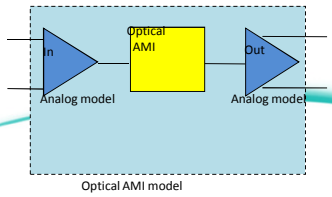
Extending AMI to Optical Channel

- Treat the entire optical module as a mid-channel repeater
- Encapsulate all optical behaviors inside the optical model
- Extend AMI simulation to include repeater



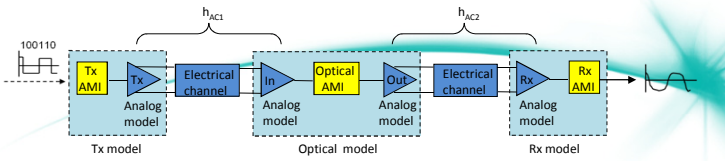
AMI Modeling for Optical Channel

- Model comprises input analog model, optical AMI block and output analog model
- Analog models represent load at input end and impedance at output end
- Optical AMI block encapsulates electrical-optical conversion and photon propagation inside the fiber.
- Optical model is defined in electrical domain. AMI_GetWave takes input voltage waveform, and returns output voltage waveform (same as regular AMI models).
- Interoperable with regular SERDES AMI models.
- Protects optical IP



Full Channel Optical Link Simulation Flow

- The link includes SERDES Tx and Rx AMI models and optical AMI model.
- SERDES and optical models are connected by two electrical channels (package, PCB, connector, …)
- Tx analog model, 1st electrical channel and optical input analog model are represented by h_{AC1}
- optical input analog model, 2nd electrical channel and Rx analog model are represented by h_{AC2}
- Simulation steps:
  1. Square wave representing bit sequence is sent into Tx AMI
  2. Tx output is convolved with h_{AC1}
  3. Resulting waveform is sent into optical AMI
  4. Optical output is convolved with h_{AC2}
  5. Resulting waveform is sent into Rx AMI
  6. Rx output is used to calculate eye diagram an BER
- Both SERDES and optics are taken into account w/o exposing SERDES or optical implementation details



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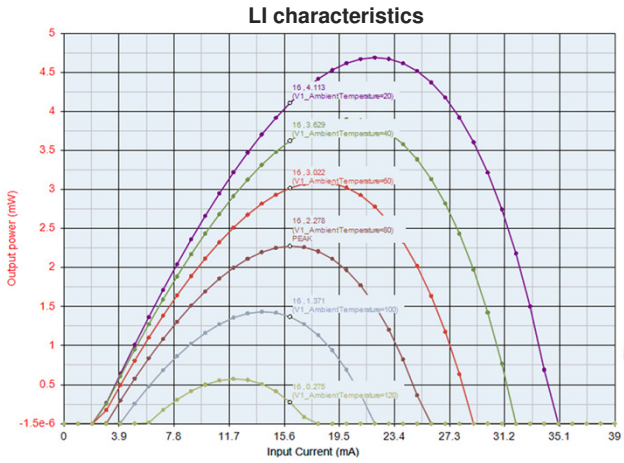
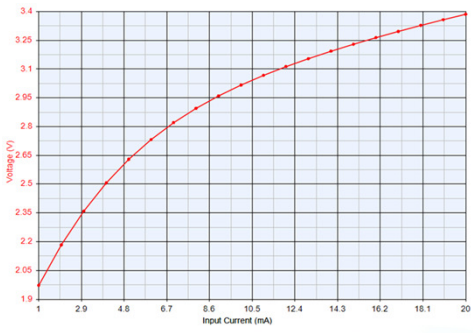
VCSEL Model



- Strong thermal dependency
- Temperature dependent I_{off}
- Output power rollover

VCSEL IV Characteristics



- IV curve is temperature dependent

Laser Rate Equations

$$\frac{dN}{dt} = \frac{\eta(I - I_{off}(T))}{q} - \frac{N}{\tau_n} - \frac{G_0(N - N_0)S}{1 + \varepsilon S}$$

$$\frac{dS}{dt} = -\frac{S}{\tau_p} + \frac{\beta N}{\tau_n} + \frac{G_0(N - N_0)S}{1 + \varepsilon S}$$

Thermal Rate Equation

$$T = T_0 + (IV - P_0)R_{th} - \tau_{th}\frac{dT}{dt}$$

$$P_0 = kS$$

IV Characteristics

$$V = f(I,T)$$

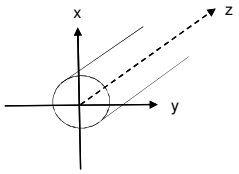
N: carrier number
S: photon number
I: injection current
I_{off}: threshold current
T: temperature
T_0: ambient temperature
P_0: optical power

- $I_{off}(T)$ and f(I,T) functions can be fitted from measured LI and IV curves
- Equations are simplified to improve simulation throughput while maintaining LI and IV characteristics.
- Spontaneous emission noise, gain compression and laser driver bandwidth are also included in the VCSEL model.

Fiber Model

Master Equation

$$\left(\nabla_\perp \frac{1}{\varepsilon(x,y)}\right) \times \left[(\nabla_\perp + ik_z\hat{z}) \times \vec{H}(x,y)\right] - \frac{1}{\varepsilon(x,y)}\nabla_\perp^2 \vec{H}(x,y) + k_z^2 \vec{H}(x,y) = \left(\frac{\omega}{c}\right)^2 \vec{H}(x,y)$$



Dispersion

- Determined by eigenvalues of $\omega(k_z)$
- Waveguide dispersion: photon confinement in fiber
- Material dispersion: frequency dependency of $\varepsilon(\omega)$
- Small pulse spectral width expansion

$$k_z(\omega_0 + \delta\omega) \approx \beta_0 + i\alpha + \beta_1\delta\omega + \frac{1}{2}\beta_2\delta\omega^2 + \cdots$$

ω_0:center frequency of laser spectrum
$k_z(\omega_0) = \beta_0 + i\alpha$

Nonlinear Schrodinger Equation of SM fiber

$$\frac{\partial A}{\partial z} + \alpha A + \beta_1\frac{\partial A}{\partial t} + \frac{i}{2}\beta_2\frac{\partial^2 A}{\partial t^2} = i\gamma|A^2|A$$

PIN Diode and TIA Models

Photon absorption in PIN creates electron-hole pairs and photocurrent

$$I_{ph} = \frac{\eta q}{\hbar \omega} \Phi$$

η:quantum efficiency
Φ: laser power

Other factors considered in the models

- Optical and electrical bandwidth
- Nonlinear transimpedance
- Thermal noise and shot noise

Outline

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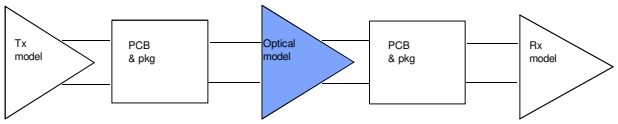
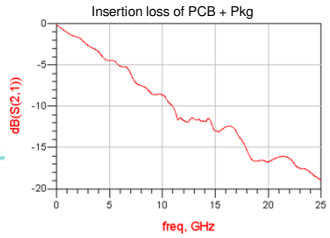
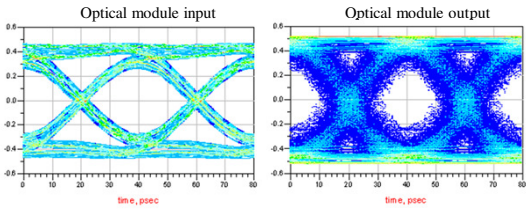
25G Optical Channel

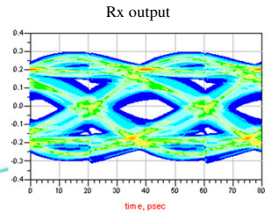


- Tx is a pass-through
- Rx implements voltage-gain control, CTLE, 5-tap DFE and CDR
- SERDES and optical module are connected by Tx/Rx package, PCB and optical package



Eye Diagrams at Room Temperature

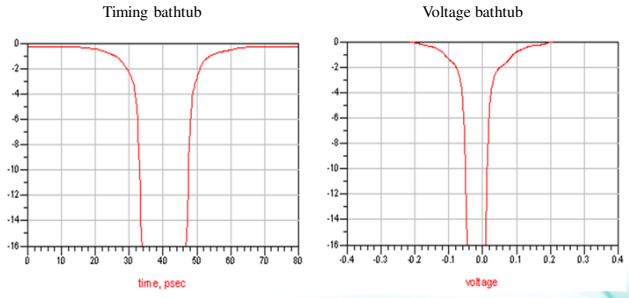




T = 27ºC
Fiber length = 50m

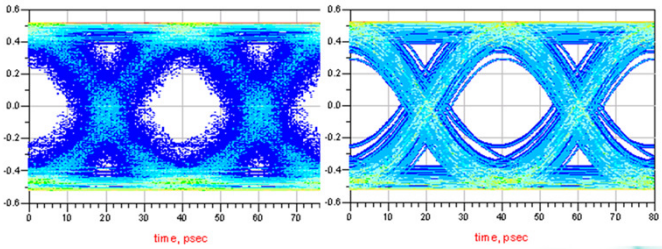
Bathtub Curves

Rx output



Optical Noise Effects

Eye at optical output

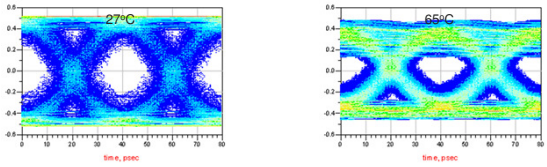


with optical noise

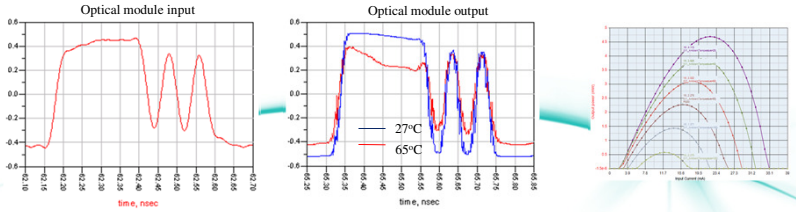
optical noise turned off

Temperature Effects

Eye at optical output

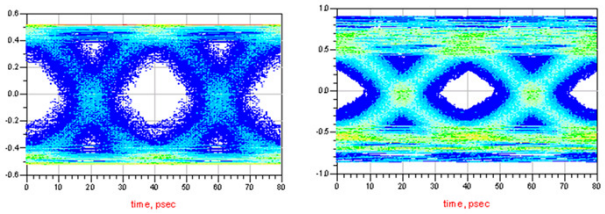


- Output level of long consecutive logic-1 sequence drops as temperature increases
- Caused by VCSEL output power rollover



Nonlinear Effects

Eye at optical output

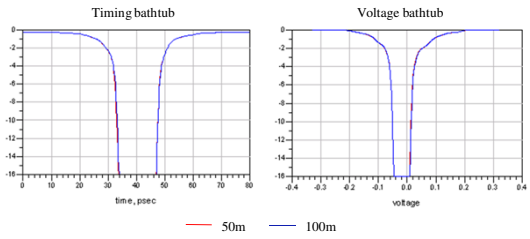


- TIA 1dB compression at 0.4V
- Output amplitude: 1V

- TIA 1dB compression at 2V
- Output amplitude: 1.8V

Fiber Length Effect

Bathtubs at Rx output



Due to low optical loss, length effect is unnoticeable.

Summary

- AMI methodology is applied to model and simulate optical channel
- IP protection to optical vendors
- Interoperable with SERDES models by supporting the same interface
- Enable co-simulation in electrical and optical domains to account for SERDES and optical effects
- Optical models are developed to describe behaviors of laser driver, VCSEL, fiber, PIN and TIA.
- Thermal effects, nonlinearity and optical noise are demonstrated in simulation results
- The approach provides a practical and efficient solution for end-to-end optical link analysis

Analysis of the Impact of Crosstalk in High-speed Serial Links

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Asian IBIS Summit
Shanghai, China
November 9, 2012

Agenda

- Introduction
- Crosstalk Contributors in High-Speed Serial Links
- Analysis of the Impact of Crosstalk in BGA area
- Summary

Why Crosstalk?

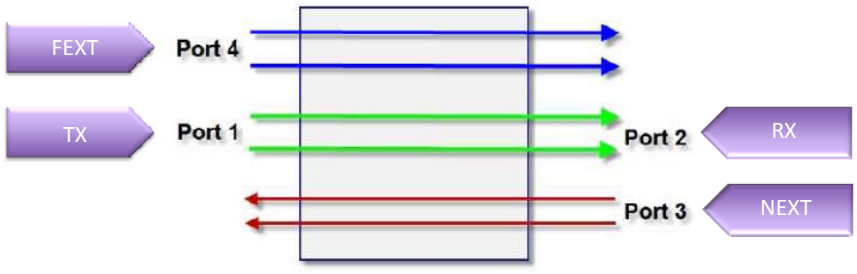
- 10Gbps and even more higher speed channels need to be designed. So, crosstalk is inevitable.
  - Signal rise time (Tr) in 10Gbps+ system is very small ,Which produces more high frequency components.
  - 10Gbps+ Interconnect System is very Sensitive with Impedance Mismatch , e.g., BGA fanout areas, Connectors, Pindrills and other Vias. Crosstalk from reflected aggressor signals and reflected crosstalk will further degrade the victim signal.
- The Crosstalk in High-speed Serial links must be carefully analyzed to meet the BER performance requirement.

ZTE中兴

Definition of Crosstalk in SerDes System

Crosstalk is usually subdivided to two parts. It is described in IEEE802.3ap as followed :

- Far-end crosstalk(FEXT) coming from data traveling in the same general direction as the channel of interest.
- Near-end crosstalk(NEXT) originating from a channel with a transmitter near the receiver of the channel of interest.



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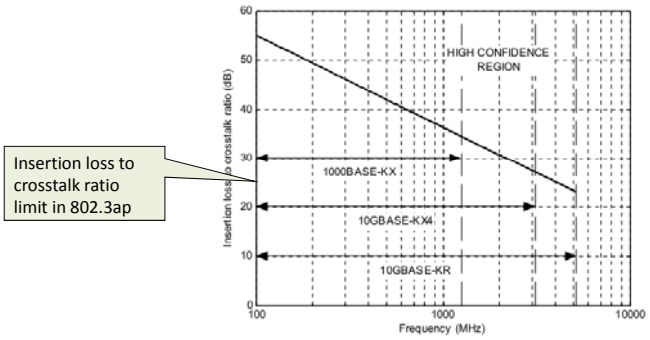
Crosstalk Requirement in IEEE 802.3ap

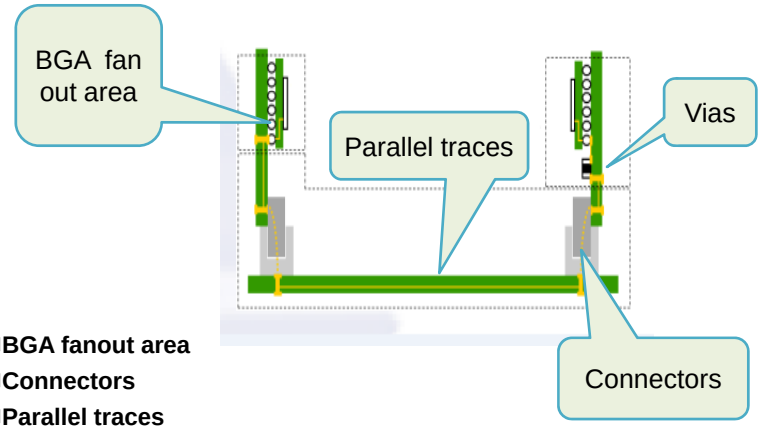
- Most of standards specify the requirement of crosstalk.
- In IEEE 802.3ap, it is specified as Insertion loss to crosstalk ratio（ICR）.



Agenda

- Introduction
- Crosstalk Contributors in High-Speed Serial Links
- Analysis of the Impact of Crosstalk in BGA area
- Summary

Crosstalk Contributors in High-Speed System



- **BGA fanout area**
- **Connectors**
- **Parallel traces**
- **Other Vias in channel**

Crosstalk Contributors in High-Speed System

- **BGA fanout area**

  Pay attention to BGA fanout area .The fanout patterns of differential pairs affect the crosstalk .

- **Connectors**

  Connectors are often the key contributor to crosstalk. Estimate TX/RX partition and pindrill to optimize the crosstalk performance.

- **Parallel traces**

  Find the longest parallel trace and carefully analyze the crosstalk to ensure the routing rules are suitable.

- **Other Vias in channel**

  The Vias for capacitors will cause crosstalk ,so keep appropriate distance between Vias of differential pairs.

Why do we focus on Crosstalk in BGA Area

- We often focus on the crosstalk caused by connectors, connectors' pindrills and parallel traces.
- We paid few attention to crosstalk in BGA area in the past.
- BGA area is also an important part needed to be carefully analyzed.
- In the rest of this paper, we will look into the impact of BGA area.

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Agenda

- Introduction
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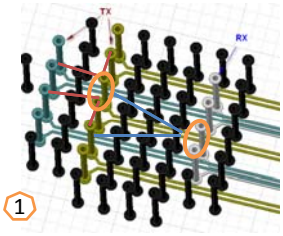
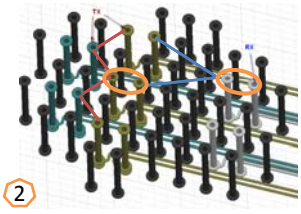
Modeling for Crosstalk Analysis

In BGA fanout area，There are Three samples and their primary differences:

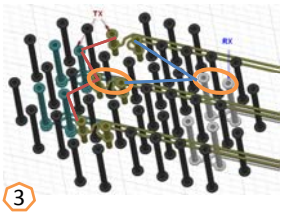
- Fanout pattern
- Distance between pairs
- Via length



Long Via, Fanout Pattern 1



Long Via, Fanout Pattern 2



Short Via, Fanout Pattern 3

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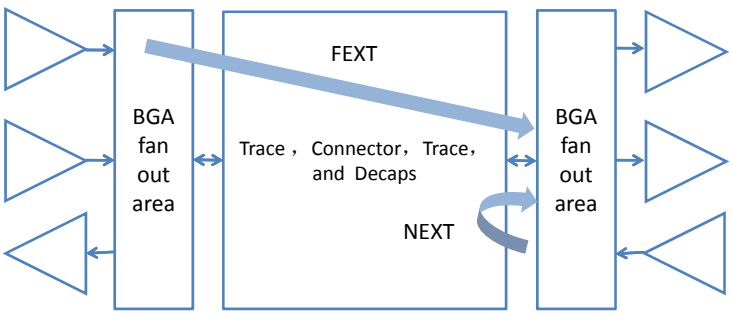
Modeling for Crosstalk Analysis

There are three serial links in model:

- Victim's channel ,aggressor channel for NEXT and aggressor channel for FEXT.
- S4p files for NEXT and FEXT.
- 40-inch length trace，3W space，a certain connector model.



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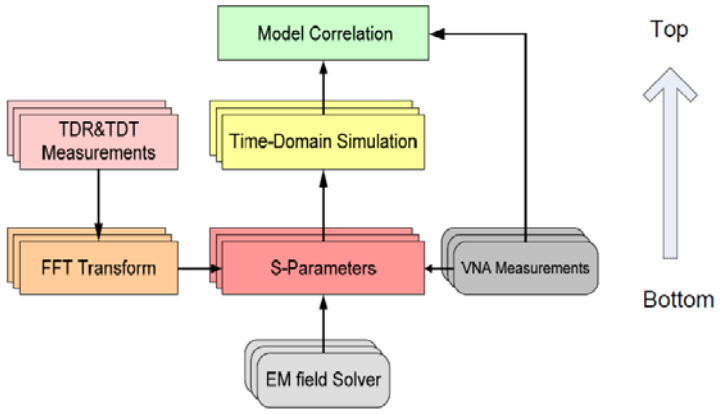
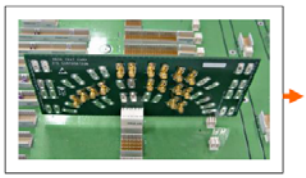
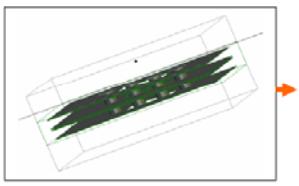
Using S-Parameters for Crosstalk Analysis



Using S-Parameters for Crosstalk Analysis



Measurement setup



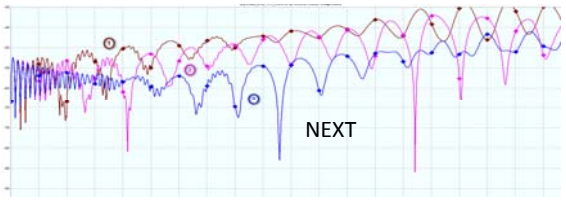
3D EM Solver Modeling

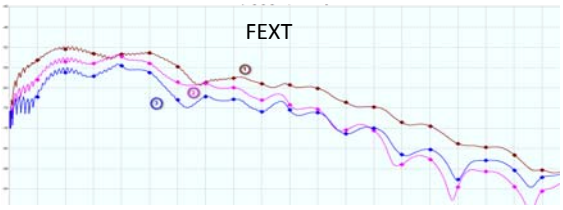
S-Parameter touchstone file

```
! FILE NAME
! DATE 10/20/05  22:27
! CORRECTED  DATA
# GHz  S    MA   R  50.00
0.010000000 3.217487E-02  25.539 1.433922E-02  73.163 7.022051E-04 -164.797 9.721752E-01 -14.501
            1.437112E-02  73.522 8.342298E-02  21.247 9.721735E-01 -14.643 1.031352E-03 152.923
            6.869677E-04 -166.566 9.750083E-01 -14.799 3.180707E-02  24.806 1.426077E-02  73.110
            9.757603E-01 -14.762 1.043164E-03 148.597 1.442420E-02  73.191 3.261170E-02  27.190
0.019987500 4.338055E-02  24.741 2.759167E-02  60.757 1.264493E-03 172.773 9.619784E-01 -28.320
            2.753260E-02  60.598 5.663544E-02  -7.471 9.629115E-01 -28.078 8.262120E-04 130.485
            1.252529E-03 171.672 9.652648E-01 -28.414 4.342042E-02  20.989 2.762920E-02  60.190
            9.660442E-01 -28.600 8.369133E-04 130.697 2.751868E-02  59.706 4.591656E-02  22.958
0.029975000 5.279364E-02  19.352 3.940318E-02  47.550 1.777378E-03 145.369 9.554404E-01 -42.013
            3.933148E-02  47.604 3.671105E-02  -9.347 9.577651E-01 -41.765 7.441007E-04 136.632
            1.751164E-03 143.245 9.584093E-01 -42.077 5.350023E-02  13.120 3.941780E-02  46.306
            9.575923E-01 -42.330 7.423362E-04 133.941 3.934892E-02  46.433 5.596628E-02  14.271
0.039962500 6.059968E-02  11.269 4.905304E-02  34.608 2.323297E-03 117.191 9.492754E-01 -55.661
            4.906615E-02  34.594 3.431321E-02  15.544 9.519293E-01 -55.371 1.174688E-03 136.972
            2.295646E-03 114.989 9.529339E-01 -55.758 6.189575E-02   3.980 4.901626E-02  33.024
            9.517830E-01 -55.968 1.161010E-03 136.920 4.896336E-02  33.055 6.299231E-02   3.407
0.049950000 6.662585E-02   1.555 5.628981E-02  21.659 2.841726E-03  90.468 9.434645E-01 -69.209
            5.633547E-02  21.883 5.111281E-02  22.288 9.453643E-01 -68.928 1.940923E-03 116.840
            2.788556E-03  88.049 9.454238E-01 -69.373 6.795117E-02  -5.423 5.627455E-02  19.599
            9.449649E-01 -69.579 1.899390E-03 117.875 5.611407E-02  19.671 6.618402E-02  -7.747
0.059937500 7.025610E-02  -9.871 6.094978E-02   8.924 3.319784E-03  63.903 9.380775E-01 -82.793
            6.093212E-02   6.964 6.999614E-02  11.224 9.395743E-01 -82.342 2.770354E-03  88.655
            3.227467E-03  61.858 9.384965E-01 -82.888 7.212381E-02 -15.124 6.077348E-02   6.385
            9.384112E-01 -83.188 2.774367E-03  89.391 6.085816E-02   6.319 6.634015E-02 -18.404
0.069925000 7.160252E-02 -22.097 6.273439E-02  -3.632 3.720456E-03  37.930 9.326985E-01 -96.370
            6.272058E-02  -3.522 8.357295E-02  -6.331 9.355087E-01 -95.783 3.570472E-03  57.951
            3.599259E-03  36.141 9.323274E-01 -96.278 7.376438E-02 -24.634 6.278425E-02  -6.705
            9.336231E-01 -96.646 3.602008E-03  58.589 6.281382E-02  -6.657 6.446640E-02 -26.081
0.079912500 7.081175E-02 -34.685 6.182219E-02 -16.100 4.040125E-03  12.437 9.270003E-01 -109.843
            6.179188E-02 -15.966 8.959131E-02 -26.534 9.309905E-01 -109.271 4.262746E-03  27.041
            3.903036E-03  11.300 9.269238E-01 -109.574 7.376363E-02 -34.289 6.182057E-02 -19.660
            9.282665E-01 -110.146 4.314952E-03  26.898 6.182886E-02 -19.667 6.259895E-02 -35.944
```

Modeling for Three Fanout Patterns

- Exchange the BGA fanout area model with former three samples, and we get three different results for system NEXT and FEXT.

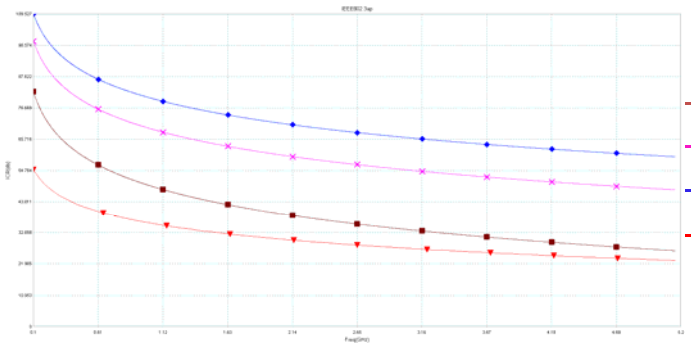




Fanout Pattern1
Fanout Pattern2
Fanout Pattern3

ICR Simulation for Three Fanout Patterns

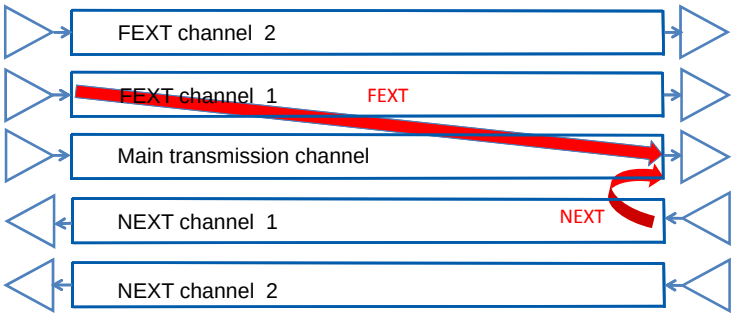
- Three ICR Simulation Results compare with ICR Requirement in IEEE 802.3ap.



Fanout Pattern1
Fanout Pattern2
Fanout Pattern3
10G-KR ICR

SNR & BER Simulation for Three Fanout Patterns

- Crosstalk Simulation Setup
  - Time domain simulation with SerDes buffer models.
  - 10.3125Gbps,64B66B.
  - Crosstalk phase assumed to be worst-case aligned signal.



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Comparisons of Simulation Results

Sample Channel	Eye Height	Eye Width	SNR	BER
Fanout Pattern1 without crosstalk	16.37%	0.35UI	21.9	7.2E-36
Fanout Pattern2 without crosstalk	16.35%	0.35UI	21.9	5.4E-36
Fanout Pattern3 without crosstalk	16.42%	0.35UI	21.9	6.3E-36
Fanout Pattern1 with 1 time crosstalk	15.65%	0.35UI	21.6	1.2E-33
Fanout Pattern2 with 1 time crosstalk	15.95%	0.35UI	21.8	9.8E-35
Fanout Pattern3 with 1 time crosstalk	16.22%	0.35UI	21.8	3.0E-35
Fanout Pattern1 with 2 times crosstalk	14.92%	0.35UI	21.3	2.0E-31
Fanout Pattern2 with 2 times crosstalk	15.64%	0.35UI	21.6	1.8E-33
Fanout Pattern3 with 2 times crosstalk	16.05%	0.35UI	21.8	1.0E-34

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Agenda

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Summary

- The crosstalk in BGA fanout area is not negligible but very important in 10Gbps+ SerDes links ,we need to select an optimized pattern for BGA fanout to improve the system performance.
- Connectors & pindrills, parallel traces and Vias are also very important parts to be analyzed.
- With carefully look into these crosstalk, we will do better work in serial links design.

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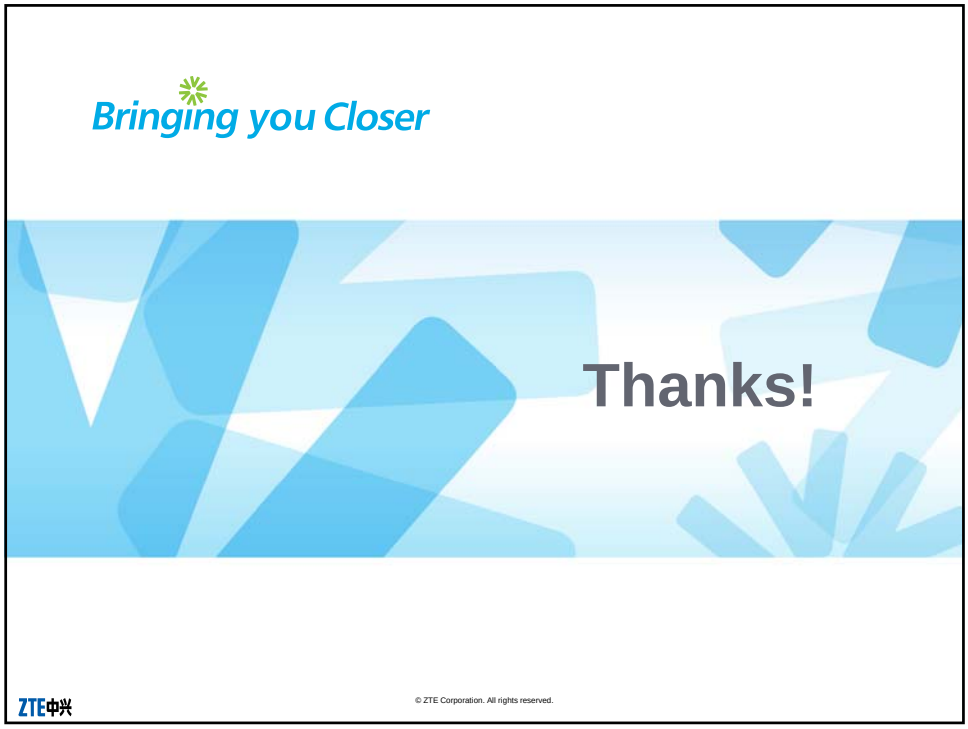
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Asian IBIS Summit
Shanghai, P.R. China
November 9, 2012

Verification of ICN Usability in Characterizing System Crosstalk

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ICN Definition

- ICN (Integrated Crosstalk Noise) early defined in the 10GBase-CR4/10 cable standards is used in CEI-25G standard and nowadays discussed in 802.3bj standards.
- It is rarely seen the correlation document in reliability and usability of ICN in the industry, so verifying the usability of ICN in characterizing link crosstalk noise through test comparison is important for 25G system applications.

$$MDNEXT_{loss}(f) = -10 \times \log_{10}\left(\sum_{i=0}^{(all\ NEXTs)} 10^{-(NLi(f))/10}\right)(dB)$$

$$W_{nt}(f) = (A_{nt}^2/4f_b)\,\mathrm{sinc}^2(f/f_b)\left[\frac{1}{1+(f/f_{nt})^4}\right]\left[\frac{1}{1+(f/f_r)^8}\right]$$

$$\sigma_{nt} = \left(2\Delta f \sum_n W_{nt}(f_n)10^{-MDNEXT_{loss}(f_n)/10}\right)^{1/2}$$

Where,
NLi(f) **represents the individual crosstalk frequency responses. And MDNEXT represents the power-sum near end crosstalks.**
W(f) **gives the weight at each frequency f_n. It serves as a low-pass filter.**
A_{nt} **represents the peak-to-peak amplitude of aggressors in mV.**

⟹ **ICN-next calculation procedure.(Here takes near-end crosstalk ICN calculation for example.) Far-end crosstalk ICN is defined the same way.**

$$\sigma_x = \sqrt{\sigma_{nt}^2 + \sigma_{ft}^2}$$

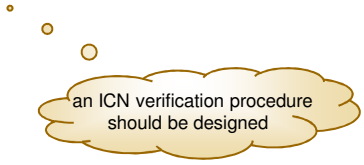
⟹ **Total ICN of both near-end and far-end crosstalks, it is defined as the RMS sum of ICN-next and ICN-fext.**

for 50 MHz ≤ f ≤ f_b **(Integration range)**

ICN Usability Questions

To learn whether ICN is usable in a PCB system or not, several questions should be answered:

1. Is ICN equivalent to time domain crosstalk noise?
2. Does the assumption of ICN -- RMS sum of single crosstalk noise results in a total crosstalk noise -- stand?
3. Does the total crosstalk noise from multiple aggressors equals to the RMS sum of each single aggressor crosstalk ICN? Which means that does the crosstalk power sum algorithm stand in the multi-crosstalk scenarios?



ICN Verification Method

The ICN verification procedure is quite straightforward and depends on the correlation with test.

1. ICN verification of Single crosstalk noise;
   1）Test the single-aggressor crosstalk noise RMS value n_i ;
   2）Test the amplitude and edge value of the single aggressor, calculate the single aggressor crosstalk ICN σ_i ;
   3）$\sigma_i \overset{?}{=} n_i$
2. Multi-Crosstalk noise RMS sum verification;
   1）Test the single-aggressor crosstalk noise RMS value n_i ;
   2）Test the multi-aggressor crosstalk total RMS noise N ;
   3）$N \overset{?}{=} \sum_{i} {}_{RMS\_sum} n_i$
3. RMS sum verification of single crosstalk ICN (i.e. crosstalk power sum verification of single crosstalk S- parameter) in calculating multi-aggressor total crosstalk noise.
   1）Calculate each single aggressor crosstalk ICN value σ_i according to each aggressor's amplitude and edge, then calculate the multi-aggressor crosstalk total noise ICN through RMS sum, $\sigma = \sum_{i} {}_{RMS\_sum} \sigma_i$;
   2）Test the multi-aggressor crosstalk total noise RMS value N ;
   3）$\sigma \overset{?}{=} N$

Verification Setup

Test environment (Instruments and boards):

	Tektronix Bertscope (working range:16~28G)
Test instruments	Agilent DCA-X 86100D + 86117A (equivalent sampling scope, bandwidth: 32/50GHz)
	Agilent DSA-X-93204A (real time sampling scope with 80G sample rate and 32GHz bandwidth)
SerDes	IBM 25G SerDes DEMO board
Passive link	WHISPER360 orthogonal connector test board
	XCEDEORTHOG 270oC 85ohm orthogonal connector test board

>> For crosstalk noise test:

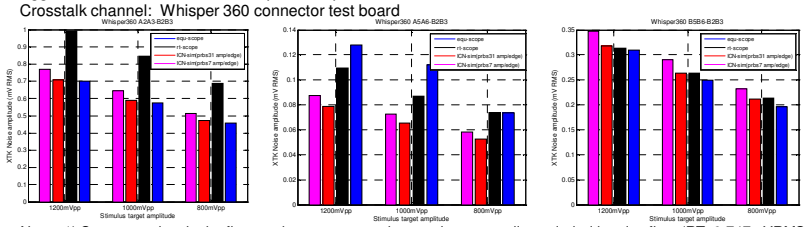
1) Equivalent sampling scope:
   - trigger in free run mode
   - noise RMS value is acquired through histogram measurement
2) Real time sampling scope (RT scope):
   - at least 50000UI time span's sample should be acquired
   - noise RMS value is acquired through histogram measurement

>> For stimulus amplitude / edge test:

PRBS31 is used to emulate real traffic data. Amplitude / edge is acquired from multiple measurements for each case.

Single Crosstalk ICN Usability Test __Experiment1

Aggressor characteristics: Bertscope, 25Gbps, RBS31, PRBS7
Crosstalk channel: Whisper 360 connector test board



Note: 1) Scope test data in the figures above represent the test data manually peeled with noise floor (RT: 0.747mVRMS, Equi: 0.9mVRMS
2) All the noise data in this experiment is close to or below the scope noise floor, it will be a main test error source.

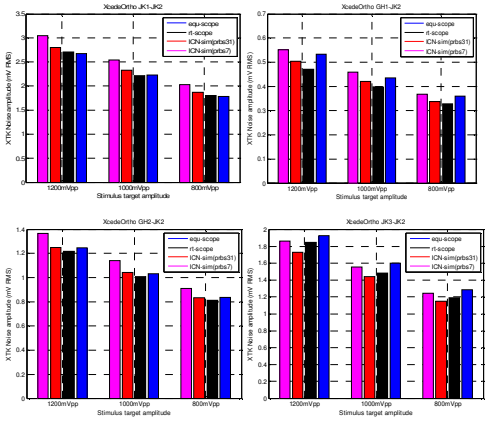
Difference(delta) between the crosstalk test data and calculated ICN value:

Aggressor		PRBS7 amp/edge		PRBS31 amp/edge	
aggressor	Amplitude	Equ_Scope	RT_Scope	Equ_Scope	RT_Scope
Whisper A2A3	1200	0.0711	0.2219	0.0088	0.2084
	1000	0.0686	0.2024	0.0145	0.2565
	800	0.0565	0.1745	0.0143	0.2167
Whisper A5A6	1200	0.0407	0.0223	0.0494	0.031
	1000	0.0392	0.0142	0.0468	0.0218
	800	0.0153	0.0158	0.0211	0.0216
Whisper B5B6	1200	0.0371	0.0339	0.0076	0.0044
	1000	0.04	0.0265	0.0143	0.0008
	800	0.03605	0.0178	0.0161	0.0022
Max Delta		**0.0711**	**0.2219**	**0.0494**	**0.2565**

1. Data in the green region of the table represents the difference (delta) between measured crosstalk noise data and calculated ICN data;
2. ICN calculation only uses aggressor amplitude, edge and crosstalk coupling S-parameter as inputs;
3. Data pattern(PRBS7 & PRBS31) only impacts aggressor amplitude and edge in terms of ICN calculation;
4. From the results, ICN and measured crosstalk noise data correlate in trends.

Single Crosstalk ICN Usability Test __Experiment2

Aggressor characteristics: Bertscope, 25Gbps, RBS31, PRBS7
Crosstalk channel: Xcede Orthogonal connector test board



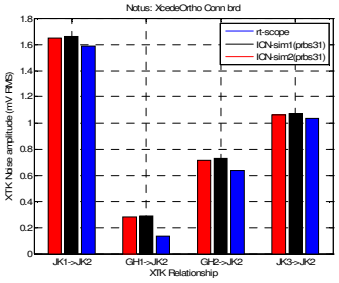
Difference(delta) between the crosstalk test data and calculated ICN value:

Aggressor		PRBS7 amp/edge		PRBS31 amp/edge	
Aggressor	Amplitude	Equ_Scope	RT_Scope	Equ_Scope	RT_Scope
XCEDE JK1	1200	0.3641	0.3342	0.1229	0.093009
	1000	0.3161	0.3225	0.1066	0.113036
	800	0.2434	0.225906	0.0799	0.062406
XCEDE GH1	1200	0.0187	0.078998	0.0276	0.032698
	1000	0.0246	0.063377	0.0157	0.023077
	800	0.009	0.039699	0.0223	0.008399
XCEDE GH2	1200	0.1183	0.147091	0.0038	0.032591
	1000	0.1041	0.129984	0.0043	0.030184
	800	0.074	0.096742	0.0035	0.019242
XCEDE JK3	1200	0.0633	0.013988	0.1965	0.119212
	1000	0.045	0.072692	0.16	0.042308
	800	0.0418	0.054597	0.1327	0.036303
Max Delta		**0.3641**	**0.3342**	**0.1965**	**0.11921**

1. In this experiment, crosstalk noise is mostly bigger than the scope noise floor, so the test results are much more stable;
2. From the results, ICN data matches pretty well with measured crosstalk noise data under single aggressor case;
3. In these experiments, it is recognized that the specific RT scope is working more stable and will be used for the following tests.

Single Crosstalk ICN Usability Test __Experiment3

Aggressor characteristics: IBM NotusV1, 25Gbps, PRBS31
Crosstalk channel: Xcede Orthogonal connector test board



	RT Scope Test Data		Calculated ICN		Delta	
Aggressor	Raw Data Test	Noise floor peeled	Sim1: Calculated ICN under amp/edge 1	Sim2: Calculated ICN under amp/edge 2	Delta Between Sim1 and Test Data	Delta Between Sim2 and Test Data
JK1->JK2	1.7664	1.5871	1.6591	1.65	0.072	0.0629
GH1->JK2	0.797	0.135	0.2883	0.2813	0.1533	0.1463
GH2->JK2	1.00266	0.6355	0.7298	0.715	0.0943	0.0795
JK3->JK2	1.2905	1.0316	1.071	1.0579	0.0394	0.0263
				Max delta	**0.1533**	**0.1463**

Note:
1. Data in the green region of the table represents the difference (delta) between measured crosstalk noise data and calculated ICN data;
2. In this experiment, ICN data matches pretty well with measured crosstalk noise data under single aggressor case.

Summary of Single crosstalk ICN usability verification:
1. From the 3 experiments, ICN data can correlate pretty well with measured crosstalk noise data under single aggressor cases when crosstalk noise is not covered by scope noise floor;
2. For the cases when crosstalk noise is close to or covered by the scope noise floor, test accuracy is degraded. Still, it can be concluded that ICN calculation is still valid under single aggressor cases.

Multi-Crosstalk RMS Sum Verification

Multi-crosstalk RMS sum formula:

$$N = \sqrt{n_1^2 + n_2^2 + ..n_i^2}$$

Step1. Test the RMS value of each single crosstalk:

Aggressor Label	Test XTK Noise Data (Noise floor peeled)
A-> V	1.5871
B-> V	0.135
C-> V	0.6355
D-> V	1.0316

'Calculated Data' is acquired from the RMS sum of the single crosstalk RMS values.

Step2. Test the total noise RMS value of multiple crosstalks , then comparing to the RMS sum of each single crosstalk's RMS value:

	RT Scope Test Data		Calculated Data		Delta	
Aggressor Label	Original test Data	Noise Floor Peeled	Calculated XTK with Noise Floor Reserved	Calculated XTK with Noise Floor Peeled	Delta between the purple columns (abs)	Delta between the blue columns (abs)
A+B-> V	1.784	1.617	1.781	1.6139	0.003	0.0031
B+C-> V	1.0345	0.7091	1.0283	0.7	0.0062	0.0091
A+C-> V	1.9154	1.761	1.885	1.728	0.0304	0.033
C+D-> V	1.45447	1.24419	1.45	1.239	0.00447	0.00519
A+D-> V	2.04936	1.90588	2.0538	1.911	0.00444	0.00512
A+B+C-> V	1.91285	1.75827	1.89967	1.744	0.01318	0.01427
A+B+D-> V	2.08737	1.9467	2.066	1.924	0.02137	0.0227
B+C+D-> V	1.482205	1.2765	1.4679	1.26	0.014305	0.0165
A+C+D-> V	2.176625	2.042	2.15769	2.022	0.018935	0.02
A+B+C+D-> V	2.19125	2.0577	2.169683	2.0347	0.021567	0.023
				Max Delta	0.0304	0.033

>>Summary:

1. The delta error introduced by the crosstalk power sum algorithm is less than 1%.
2. Multi-crosstalk RMS sum algorithm is valid.

Multi-Crosstalk ICN RMS Sum Verification

RMS sum formula of multi-crosstalk ICN: $\sigma_x = \sqrt{\sigma_m^2 + \sigma_{fi}^2}$

(The underlying meaning is that the power sum algorithm in the frequency domain stand.)

For the verification method, please refer to P3. In the table below:

1. Data in the 'RT Scope Test' column represents the multi-crosstalk noise measured results (scope noise floor is peeled);
2. Data in the 'Calculated ICN' column represents the calculated ICN data of multi-crosstalk noise through RMS sum of each crosstalk's ICN value.

	RT Scope Test	Calculated ICN		Delta	
Aggressor Label	Test Noise Data with Noise Floor Peeled	Sim1: Calculated ICN under amp/edge 1	Sim2: Calculated ICN under amp/edge 2	Delta Between Sim1 and Test Data	Delta Between Sim2 and Test Data
A+B-> V	1.617	1.68396	1.6738	0.06696	0.0568
B+C-> V	0.7091	0.78468	0.7683	0.07558	0.0592
A+C-> V	1.761	1.8125	1.7983	0.0515	0.0373
C+D-> V	1.24419	1.296	1.27686	0.05181	0.03267
A+D-> V	1.90588	1.97475	1.96	0.06887	0.05412
A+B+C-> V	1.75827	1.8353	1.82	0.07703	0.06173
A+B+D-> V	1.9467	1.995688	1.98	0.048988	0.0333
B+C+D-> V	1.2765	1.32769	1.30748	0.05119	0.03098
A+C+D-> V	2.042	2.10529	2.086355	0.06329	0.044355
A+B+C+D-> V	2.0577	2.12494	2.1052	0.06724	0.0475
			Max delta	0.07703	0.06173

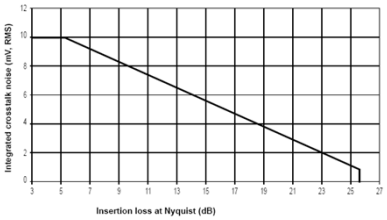
From this experiment, the 'RT Scope Test' data and the 'Calculated ICN' data matches pretty well, the delta error between the two is less than 1%. It can be concluded that multi-crosstalk ICN RMS sum algorithm is valid.

Summary

- ICN metric in quantifying link crosstalk is valid, under the condition that aggressor data pattern is PRBS31 alike (for example 64B/66B coding).
- It is recommended to measure the RMS value of crosstalk noise instead of the peak-to-peak amplitude. (The latter depends a lot on test time)
- In the cases that scope noise floor is bigger than or close to the target crosstalk noise under test, it is reliable to get the crosstalk noise data from ICN calculation.

ICN mask defined in current or upcoming 25G standards gives the relationship between the SerDes driving capability (described by through link insertion loss) and link crosstalk amount (ICN), it solves the partial ICR mask violation problem in certain extent.

ICN mask defined in CEI-25G-LR:



- It is recommended to use ICN as an input parameter for stress channel simulation in high speed links, to help the users generate ICN masks of their links using different SerDes models. ICN noise can be represented by a Gaussian white noise.

Thank you

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Chip PDN Model for Power Aware Signal Integrity Analysis

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Raymond Y. Chen
Presented by: Haisan Wang

Asian IBIS Summit
Shanghai, China
November 9, 2012

Outlines

- Traditional SSO analysis
- Chip PDN impact
- Limitation in current IBIS SSO simulation
- Chip PDN contribution to capacitance
- How to generate chip PDN model
- Case study—Using chip PDN in SSO analysis
- BIRD proposal to add chip PDN in IBIS

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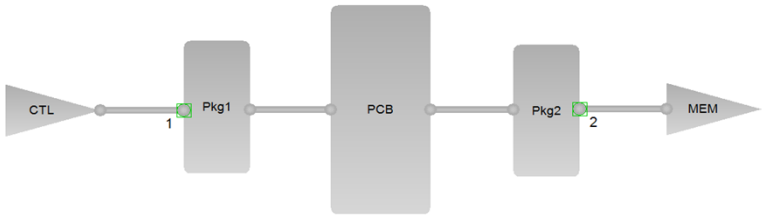
Traditional SSO analysis



- PCB/Package model is extracted by EM solver with signal and power/ground information.
- IBIS without power/ground current and package [Pin]/[Package Model] model are used.
- "Artificially large" power ground fluctuations is observed in SSO analysis due to the lack of PDN model.
- “What if “ RC on die model to mitigate power/ground noise till reasonable level.

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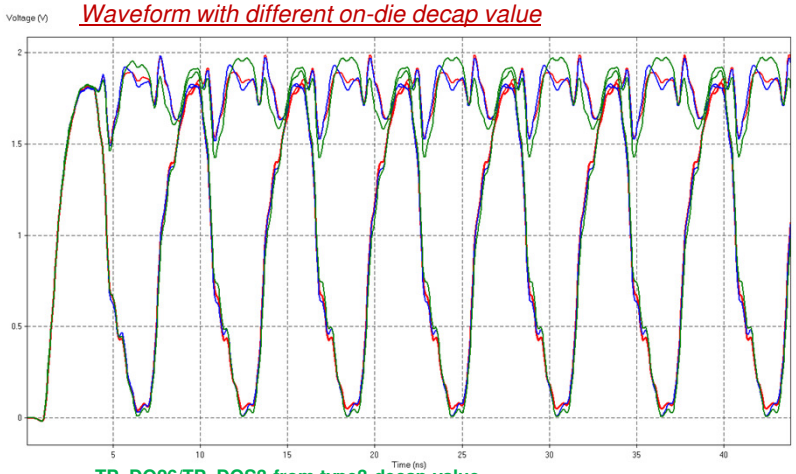
Traditional SSO analysis

1. Driver:1.3nF/0.3 ohms ; Receiver: 1.0nF/0.3 ohms
2. Driver:2nF/0.3 ohms ; Receiver: None
3. Driver:0.5nF/0.3 ohms ; Receiver: 0.5nF/0.3 ohms

Waveform with different on-die decap value



– TP_DQ26/TP_DQS3 from type3 decap value
– TP_DQ26/TP_DQS3 from type2 decap value
– TP_DQ26/TP_DQS3 from type1 decap value

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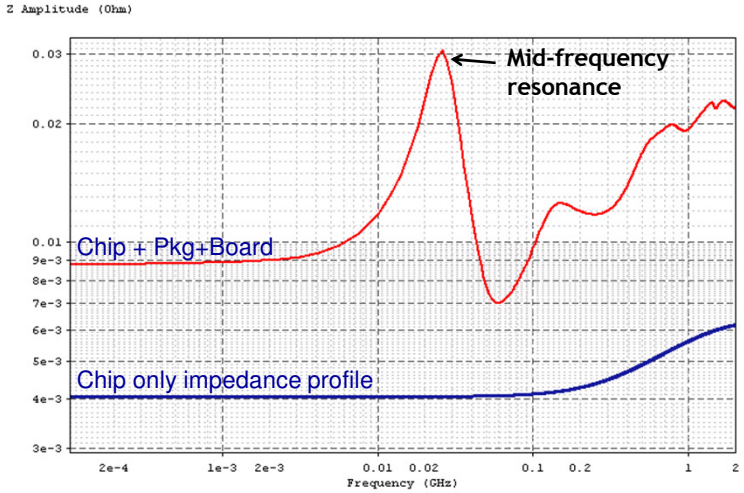
Chip PDN impact



- Chip PDN will help to identify the mid-frequency resonance of the whole system
- This will enhance the power/ground noise if working frequency meet the resonance

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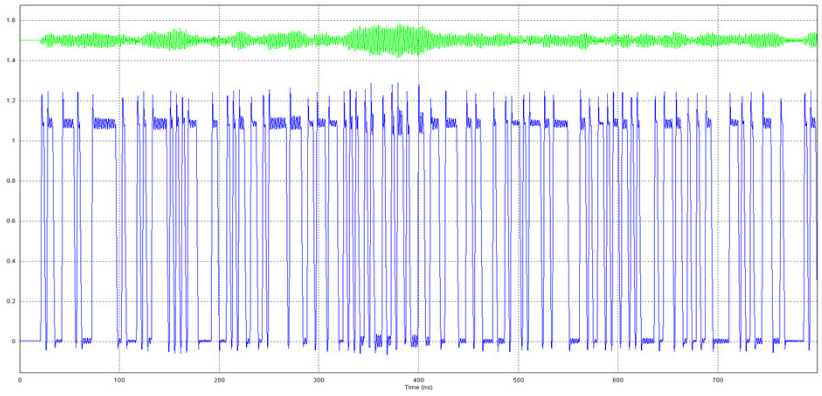
Chip PDN impact



- While performing SSO analysis with random bits pattern, lower frequency transition bits may meet the middle-frequency resonance and lead to larger power/ground noise and worse signal quality.

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Limitation in current IBIS SSO simulation

- IBIS v5.0 is more accurate to simulate the power/ground current with pre-driver/crowbar current and I-V adjusted with Vgs. But IBIS v5.0 only can't still get reasonable power/ground noise.
- Feasible on-die RC model still play a dominant role that impacts the accuracy of the SSO analysis
- On-die RC model is not available from IBIS file.
- On-die capacitance is just estimated from IC designer by how much of MOS caps they placed around I/O cells or estimated by average power dissipation (eq.1)?
- From chip point of view, what are the factors that contribute total on-die capacitance?

C: capacitance of core
P: average power dissipation
f : clock frequency
V: power supply voltage

$$C \sim \frac{P}{V^2 f} \quad \text{Eq.1}$$

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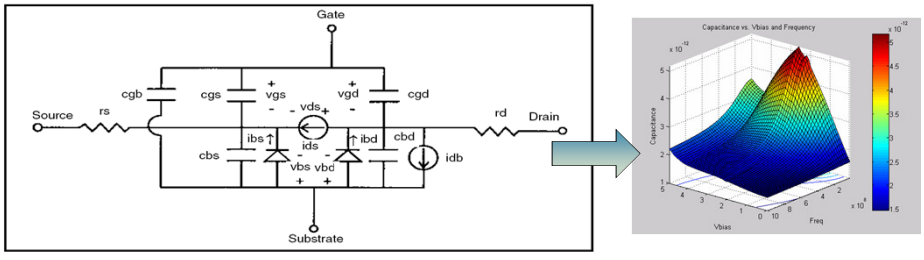
Chip PDN contribution to capacitance

- Parasitics from transistor
  - Parasitic capacitance exists between all MOSFET terminals
  - For the I/O pin, this is modeled in IBIS by C_comp
  - A new compensation capacitor is needed for the power and ground parasitics which is frequency and voltage dependency (first propose by Sigrity in DesignCon 2005)



- MOS Capacitors
  - Like n-MOS capacitors that distributed around I/O circuits

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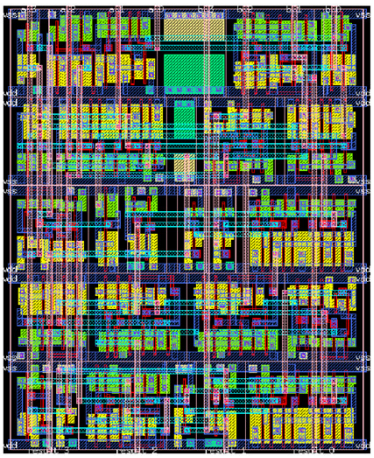
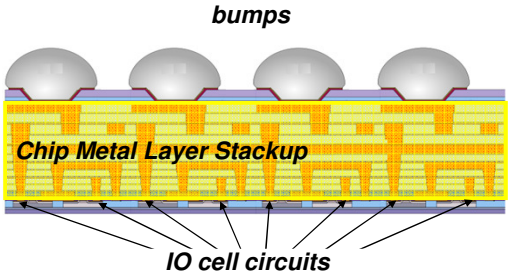
Chip PDN contribution to capacitance

- Outside of the transistors





—Power/ground metal grids outside transistors that contribute capacitance.
—Except MOS caps around I/O cell, MIM caps are distributed on interposer that contributes larger capacitance in current 2.5D IC design

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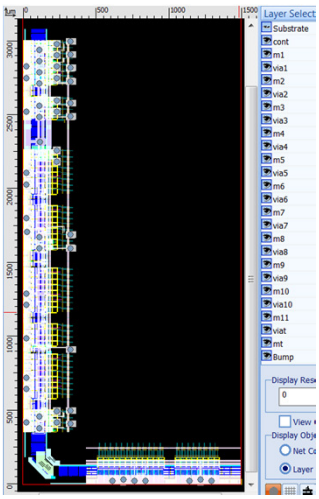
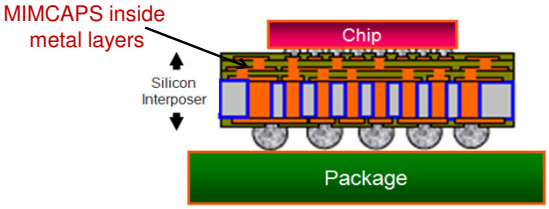
How to generate chip PDN model

- We need to categorize chip PDN model into 2 parts, one is transistor itself, the other is outside the transistor
- IBIS buffer model part only includes circuits and intrinsic parasitic.
- Chip PDN includes GDS layout and MOS capacitors of I/O region.
- Silicon interposer chip design becomes popular and MIMCAPs on interposer contribute sizable capacitance which need to be consider in chip PDN extraction





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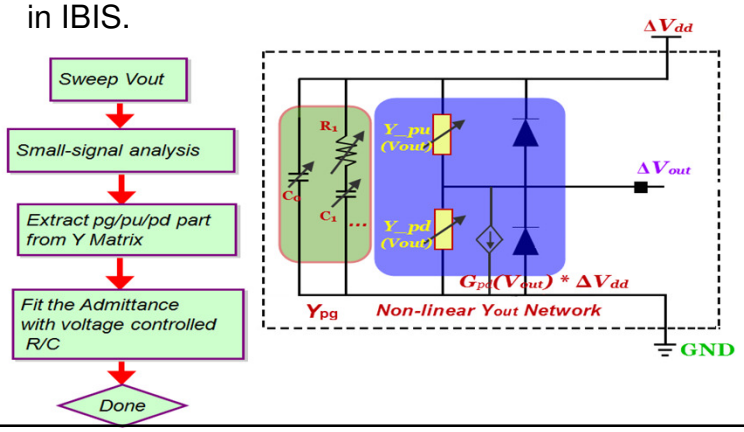
How to generate chip PDN model—transistor

- The IBIS Plus model proposed by Sigrity that dynamic capacitance is included while performing Y admittance extraction between power and ground.
- The equivalent circuit is extracted and added to power/ground pins through [External Model] circuit call in IBIS.



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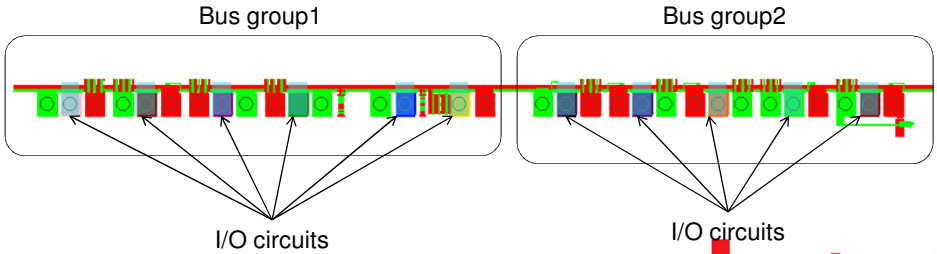
How to generate chip PDN model—outside transistor

- To extract chip PDN by I/O bus group. Same bus group share the same PDN model.
- To set power to ground ports on bumps by different bus group for model extraction
- Capacitance outside the transistor with MOS capacitors can be extracted through chip level extractor.
- The model can be lumped as simple RC value or distributed as SPICE circuit by the concern of frequency bandwidth.



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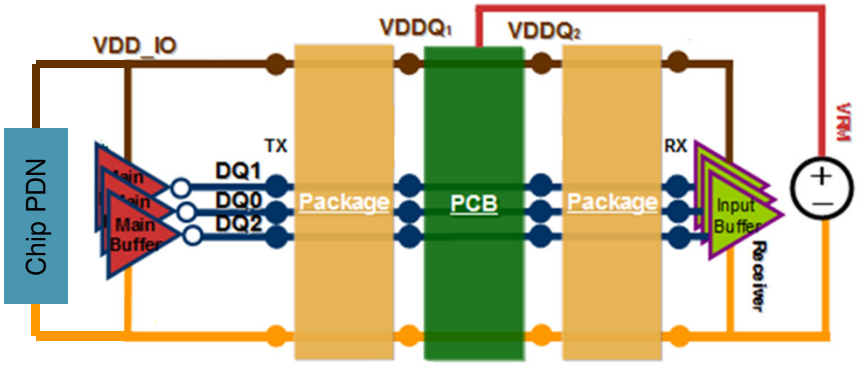
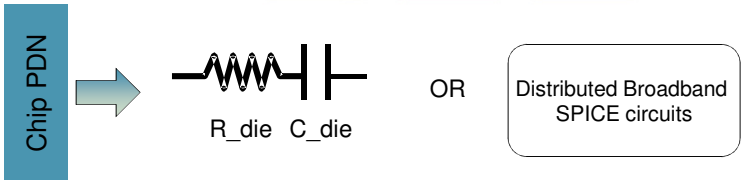
Case study—Using chip PDN in SSO analysis





- Lump RC and distributed broadband model will be applied for SSO analysis with PRBS patterns

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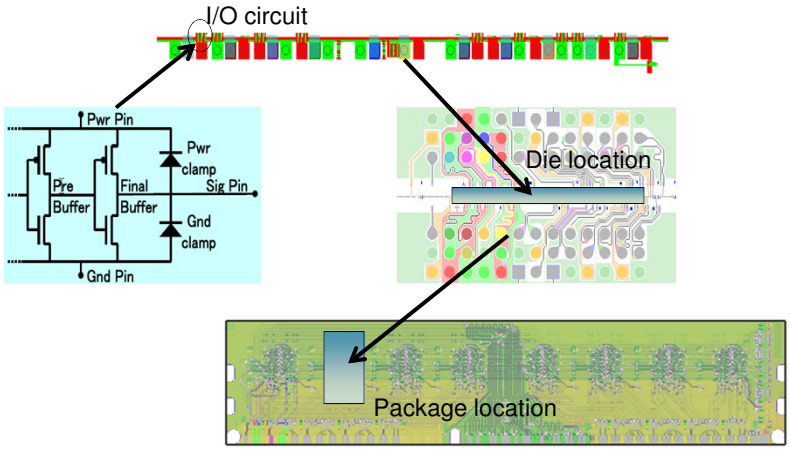
Case study—Using chip PDN in SSO analysis



- I/O circuit is converted into IBIS/IBIS plus model
- Chip is extracted by chip level extractor which include RLCK elements.
- PCB and package are extracted by EM solver and converted into broadband SPICE.
- Only 1 group DDR data is considered for this test

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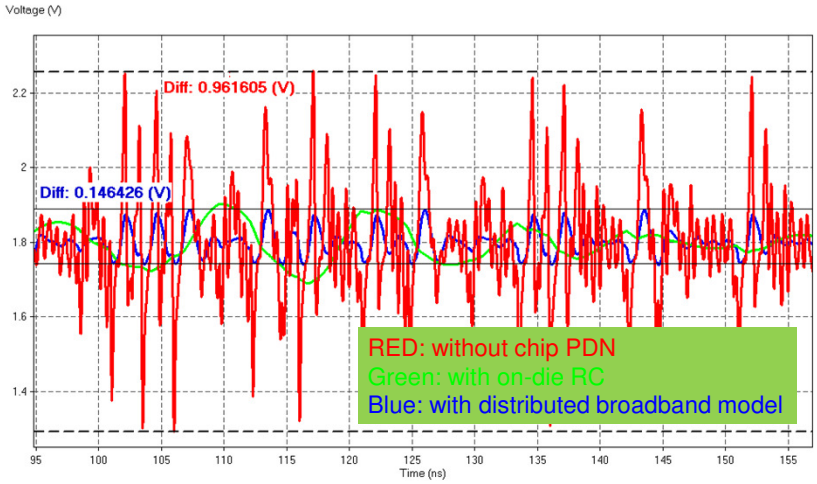
Case study—Using chip PDN in SSO analysis



- On-die RC or better distributed chip PDN model can yield realistic power/ground noise analysis.
- Chip PDN is responsible to filter high frequency noise

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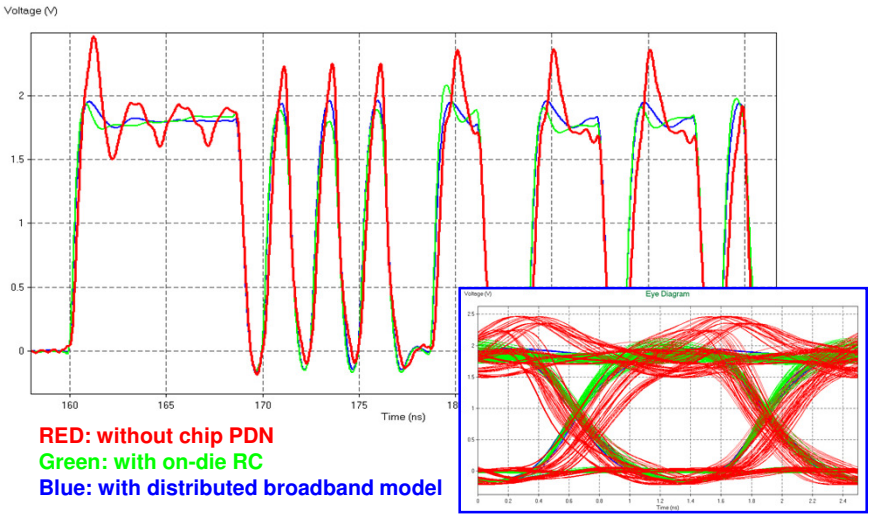
Case study—Using chip PDN in SSO analysis



- Without Chip PDN model, artificially large power/ground noise impact the signal waveform significantly

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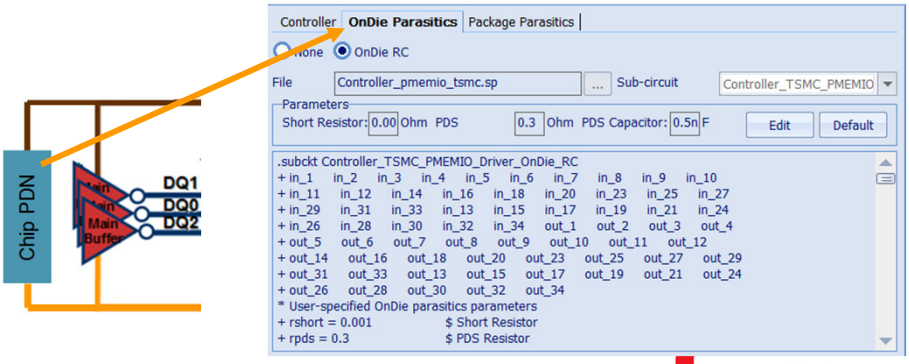
BIRD proposal to add chip PDN in IBIS

- Chip PDN model can be lump RC or SPICE distributed model.
- The chip distributed model is generated by different bus group.
- The bus group is mapping to the bus group in [Pin Mapping] section.
- [Chip PDN Model] can be included in IBIS by [External Model] call



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BIRD proposal to add chip PDN in IBIS

```
[Package Model] DDR3_WBGA_PKG
[Chip PDN Model] DDR_Chip
[Manufacturer]  Cadence
[Package]
.........
[Pin]
.........
[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
B2      GNDBUS2   NC
B3      GNDBUS2   PWRBUS2   GNDBUS2   PWRBUS2
B7      GNDBUS2   PWRBUS2   GNDBUS2   PWRBUS2
B8      GNDBUS2   NC
B9      NC        PWRBUS2
C2      GNDBUS2   PWRBUS2   GNDBUS2   PWRBUS2 |GNDBUS2 is VSSQ
C3      GNDBUS2   PWRBUS2   GNDBUS2   PWRBUS2 |PWRBUS2 is VDDQ
[Define Chip PDN Model]
[Manufacturer] Cadence
[Description]   3mmx3mm Flip-Chip
[External Model]
Language SPICE
|
| Corner  corner_name  file_name  circuit_name
Corner   Typ        chip_PDN.ckt   vddq_pdn
|
| Ports List of port names (in same order as in SPICE)
Ports A_puref A_pdref
```

bus name is mapping to sub-circuit nodes

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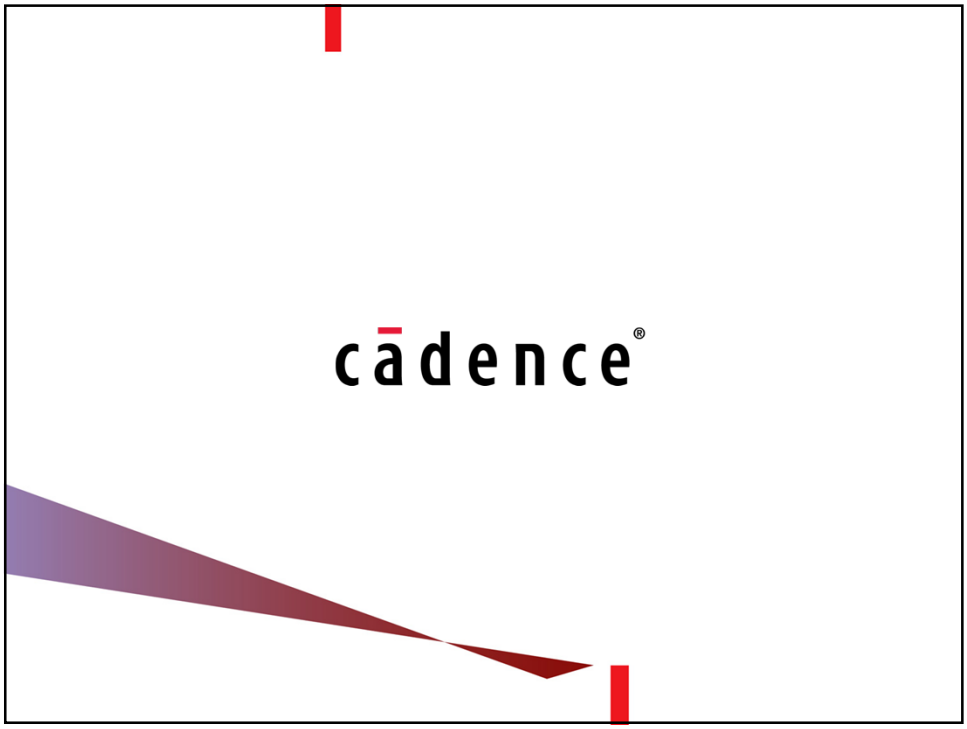
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IBIS Parser Update

Bob Ross
Asian IBIS Summit
Shanghai, China
November 9, 2012
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(presented by Anders Ekholm, Ericsson)

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Outline, Specifications and Parsers

- IBIS through Version 5.1
  - ibischk5
- Touchstone Version 2.0
  - tschk2
- Conclusions

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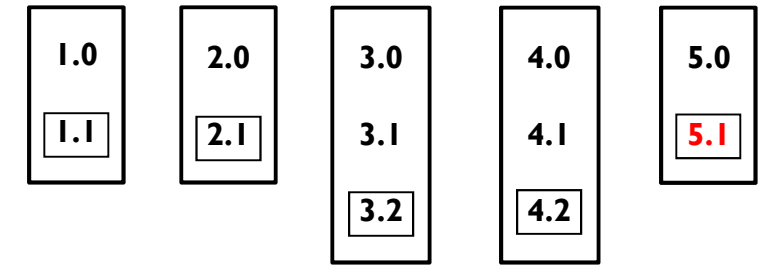
Valid IBIS Versions and Latest ibischk Versions



ibis_chk	ibischk2	ibischk3	ibischk4	ibischk5
V1.1a	V2.1.17	V3.2.9	V4.2.2	**V5.1.2**

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IBIS Parser Major Version Logic

- Subversions upgraded to **last** major version
  - **V5.1** upgrades V5.0
  - **V4.2** upgraded V4.0 and V4.1
  - **V3.2** upgraded V3.0 and V3.1
  - **V2.1** upgraded V2.0
  - **V1.1** upgraded V1.0
- **V5.1** checks **V1.1**, **V2.1**, **V3.2**, **V4.2**, and **V5.1** levels for features and corrections

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Downward Compatibility

- Current IBIS **downward compatible** with all earlier features and syntax
  - Prior EDA implementations supported
  - Existing models remain valid
  - Specification includes all features
  - Earlier specification mistakes corrected
- Specification well tested and corrected

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IBIS-AMI Version Exception

- IBIS-AMI subversions supported by the **.ami** format
- **AMI_Version** required for "**5.1**" files and **later**
  - First Reserved Parameter
  - Use_Init_Output **not legal**
- **Omission** of **AMI_Version implies** "5.0" level
  - Use_Init_Output **legal**
  - **All other AMI_Version "5.1" rules apply**
- Later AMI_Version levels will have more features and possible deprecation at the subversion level
- Later Specification will track all subversion changes

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"ibischk5" Parser

- Ibischk5, Version 5.1.2
  - Free executables: http://www.eda.org/ibis/ibischk5/
  - Bug reports: http://www.eda.org/ibis/bugs/ibischk/
- Checks all [IBIS Ver]s of IBIS files
- Over $117,000 of contracted work since 1993
- Supports .ibs, .pkg, .ebd, and .ami formats
  - directly or through higher level linkages

Flags in ibischk5

```
Usage: ibischk5       <IBS filename>
     : ibischk5  -ebd <EBD filename>
     : ibischk5  -pkg <PKG filename>
     : ibischk5  -ami <AMI filename>
Usage: ibischk5  -caution -numbered       <IBS filename>
     : ibischk5  -caution -numbered -ebd <EBD filename>
     : ibischk5  -caution -numbered -pkg <PKG filename>
     : ibischk5  -caution -numbered -ami <AMI filename>
The flags prior to the file name can be in any order,
and the -caution and/or -numbered flags are optional.
```

- **–ami** for <file_name>.ami (algorithmic model interface control file)
- **–numbered** for numbered **E**rror, **W**arning, **N**otes and **C**aution messages

ibischk5 {–numbered} –ami file4.ami

```
Checking file4.ami for IBIS 5.0 Compatibility...

ERROR - Illegal Usage value A specified for Param1
ERROR - Illegal Type value B specified for Param1
ERROR - Illegal Format value C specified for Param1
ERROR - No Reserved_Parameters found

Errors  : 4

File Failed
```

```
Checking file4.ami for IBIS 5.0 Compatibility...

E4627 - Illegal Usage value A specified for Param1
E4627 - Illegal Type value B specified for Param1
E4627 - Illegal Format value C specified for Param1
E4622 - No Reserved_Parameters found

Errors  : 4

File Failed
```


Message Number File Being Updated (Over 1150 unique message strings)

Number	Symbol in Code	Message string	Parameters	Comment	Category	Clasification
100	MDL_ERR_0	Unable to Allocate Memory: %s %d	filename, line number	The code failed to allocate memory in <filename> at <linenumber>	Internal Error	E
101	MDL_ERR_1	Unable to get IBIS structure		Program data structures are corrupt	Internal Error	E
102	MDL_ERR_2	Orphan Model keyword.		Model keyword found but not within a Model declaration	Error with IBIS file Line number	E
103	MDL_ERR_3	Illegal Digital Port <%s> (not allowed in SPICE Ports section)	portname	Improper use of Digital port <portname>	Error with IBIS file Line number	E
104	MDL_ERR_4	D_switch not allowed with (D_drive,D_receive,or D_enable) in		Improper use of D_switch	Error with IBIS file Line number	E
105	MDL_ERR_5	%s not allowed with D_switch in Ports/A2D/D2A Section			Error with IBIS file Line number	E
106	MDL_ERR_6	Reserved Digital Port <%s> used as	portname	Improper use of Reserved Digital port <portname>	Error with IBIS file Line number	E
107	MDL_ERR_7	Orphan data line keyword.		A Model related data line was found where none was expected	Error with IBIS file Line number	E
108	MDL_ERR_8	TTgnd Typical value should be > 0		Improper TTgnd typical value	Error with IBIS file Line number	E
109	MDL_ERR_9	TTgnd Min value should be > 0		Improper TTgnd minimum value	Error with IBIS file Line number	E
110	MDL_ERR_10	TTgnd Max value should be > 0		Improper TTgnd maximum value	Error with IBIS file Line number	E
111	MDL_ERR_11	TTgnd typ value is not in between		Improper range for TTgnd	Warning	W
112	MDL_ERR_12	TTpower Typical value should be > 0		Improper TTpower typical value	Error with IBIS file Line number	E
113	MDL_ERR_13	TTpower Min value should be > 0		Improper TTpower minimum value	Error with IBIS file Line number	E
114	MDL_ERR_14	TTpower Max value should be > 0		Improper TTPower maximum value	Error with IBIS file Line number	E
115	MDL_ERR_15	TTpower typ value is not in between		Improper range for TTPower	Warning	W
116	MDL_ERR_16	[Model Spec] should be specified immediately after all the subparameters of a model and		Improper positioning of [Model Spec]	Error with IBIS file Line number	
117	MDL_ERR_17	[Receiver Thresholds] should not be specified for model type %s	modeltype	Receiver thresholds are not allowed for a <modeltype> which is not an Input or I/O model type	Warning with IBIS file Line number	W
118	MDL_ERR_18	[Add Submodel] should be specified before other keywords for a model		Improper positioning of [Ad Submodel]	Error with IBIS file Line number	E
119	MDL_ERR_19	%s Already Defined For Model '%s'	sub parameter/keyword, modelname	A model <sub-parameter or keyword> was already defined for <modelname>	Error with IBIS file Line number	E
120	MDL_ERR_20	[Receiver Thresholds] should be specified immediately after all the subparameters of a model and before the other keywords of a		Improper positioning of [Receiver Thresholds] keyword	Error with IBIS file Line number	E
121	MDL_ERR_21	Expecting Keyword. Invalid Line		An invalid line was found where a keyword was expected	Error with IBIS file Line number	E

Recent ibischk5 Version 5.1.2

- Major IBIS-AMI syntax implementation
  - IBIS Version 5.1 – rules clarified and CHECKED
  - Table-syntax defined and now parsed
  - **Major Errors now detected** (versus not being checked in the older Version 5.0.7)
- 23 BIRDs on IBIS and IBIS-AMI syntax
- 13 BUG reports on file testing for specification compliance closed through BUG138
- Source code checked with 44 new test files since V5.0.7
- Unfortunately, some new BUGs may be discovered with more usage

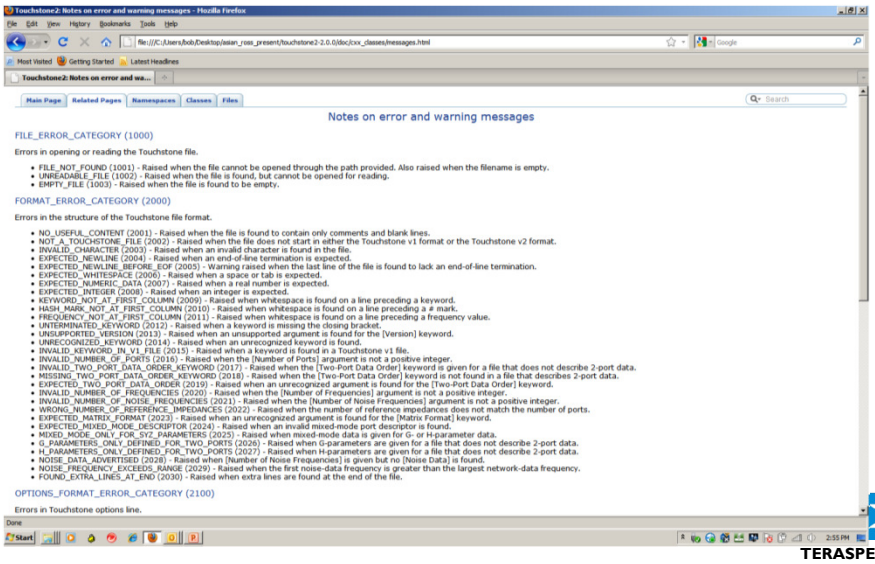
"tschk2" Parser

- Checks Touchstone Version 1.0 (TS1) and Version 2.0 (TS2)
  - Error and Warning numbers
  - Free executables: http://www.eda.org/ibis/tschk2/
- Converts TS1 to TS2, TS2 to TS1 where practical with **-canonical*** flags
- Provides comment headers and real, imaginary format (RI) with **-describe** flag
- Source code package includes 440+ test cases
- C++, well documented
- Only one mixed mode BUG found so far

tschk2 {-canonical*} FILE

- **{-canonical | -canonical-v2}**
  - **TS1, TS2 → TS2**
  - Provides number of ports, frequencies and other information
  - Un-normalizes TS1 Y-, Z-, G- and H-parameters and effective noise resistance
- **{-canonical-v1}**
  - **TS1, TS2 → TS1** where practical
  - Applies column formatting rules and 2-port 21_12 ordering
  - Normalizes TS2 Y-, Z-, G- and H-parameters and effective noise resistance
  - No mixed mode or selectable reference resistance processing

71 tschk2 Messages



Conclusions

- ibischk5 and tschk2 parsers - **officially** check files for specification compliance
- Parsers helps test specification rules for clarity and accuracy
- BUG process continues to improve the parsers and eliminate mistakes

- **Parsers are critical to IBIS success**

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Useful Links Under IBIS Home Page: www.eda.org/ibis/

ver5.1/	**IBIS Version 5.1** (August 24, 2012)
ibischk5/	**ibischk5 Version 5.1.2** (October 2012)
touchstone_ver2.0/	**Touchstone Version 2.0** (April 24. 2009)
tschk2/	**tschk2 Version 2.0.0** (December 2009)
quality_ver2.0/	**IBIS Quality Specification** (Oct. 30, 2009)
ibis-iss_ver1.0/	**Interconnect SPICE Subcircuit Specification Version 1.0** (October 7, 2011)
editorial_wip/	**Editorial Task Group** (wip)
interconnect_wip/	**Interconnect Task Group** (wip)
macromodel_wip/	**Advanced Technology Task Group** (wip)
quality_wip/	**Quality Task Group** (wip)

(wip: work in progress)

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IBIS Model Validation Review

Lance Wang
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IBIS Asian Summit 2012
Nov. 9, 2012
Shanghai, PR China

Outlines

- Motivation
- History
- Method Review
- Common Mistakes
- Conclusion

Motivation

- Why model validation is the MUST?
  - Models are artificial representations of the real devices. This applies to all the models including our SI simulation models
  - System design engineers need the validated models to analyze their High-Speed system designs through simulations
  - "Garbage in, Garbage out" is true for all the simulations
- Proper IBIS model validation method is required
  - IBIS is the behavioral model which is no way to verify internal structures or monitor internal signals
- Common mistakes for IBIS validation and correction methods

Note: this presentation is focusing on "traditional" IBIS buffer model validation methods only.

History

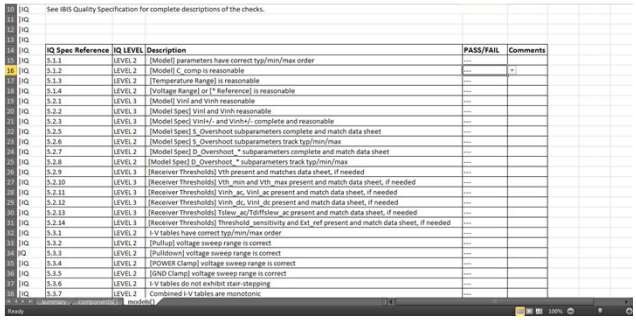
- 1997 – the IBIS Accuracy Subcommittee (IAS) was established
  - 1998 - IAS release their initial version of the IBIS Accuracy Specification, which later becomes the I/O Buffer Accuracy Handbook.
- 2007 - the IBIS Quality Task Group (IQTG) was formed
  - It is still ON in the regular teleconference basis
  - Several IBIS Quality Specifications have been released as the IBIS Standard Specification documents
  - A Quality Checklist also has been release from IQTG
- In the past few years, many system companies start to ask their device vendors to have their specific IBIS model quality control documents to be filled before the devices used in their high-speed designs

Method Review

- IBIS Validation Goal
  - Correlate IBIS model simulation results with the desired Golden sources (measurements and simulations) for specific test loads
- Common Used Correlation/Comparison Methods
  - From IQTG
    - Quality Checklist
  - From the Accuracy Handbook
    - Curve Overlay Metric
    - Curve Envelop Metric
  - From Xilinx and Huawei
    - Threshold based Metric
  - From IO Methodology
    - Differential Index based Metric

Quality Checklist from IQTG

- Great start! A lot of good suggestions
- Simply follow the list for the check items
- Too many items asking for “reasonable” and “visual” checking
- Not easy to implement by using a computer program
- Incomplete especially for correlations



See IBIS Quality Specification for complete descriptions of the checks.

IQ Spec Reference	IQ LEVEL	Description	PASS/FAIL	Comments
5.1.1	LEVEL 2	[Model] parameters have correct typ/min/max order	---	
5.1.2	LEVEL 2	[Model] C_comp is reasonable	---	
5.1.3	LEVEL 2	[Temperature Range] is reasonable	---	
5.1.4	LEVEL 2	[Voltage Range] or [* Reference] is reasonable	---	
5.2.1	LEVEL 3	[Model] Vinl and Vinh reasonable	---	
5.2.2	LEVEL 3	[Model Spec] Vinl and Vinh reasonable	---	
5.2.3	LEVEL 3	[Model Spec] Vinl+/- and Vinh+/- complete and reasonable	---	
5.2.5	LEVEL 2	[Model Spec] S_Overshoot subparameters complete and match data sheet	---	
5.2.6	LEVEL 2	[Model Spec] S_Overshoot subparameters track typ/min/max	---	
5.2.7	LEVEL 2	[Model Spec] D_Overshoot_* subparameters complete and match data sheet	---	
5.2.8	LEVEL 2	[Model Spec] D_Overshoot_* subparameters track typ/min/max	---	
5.2.9	LEVEL 3	[Receiver Thresholds] Vth present and matches data sheet, if needed	---	
5.2.10	LEVEL 3	[Receiver Thresholds] Vth_min and Vth_max present and match data sheet, if needed	---	
5.2.11	LEVEL 3	[Receiver Thresholds] Vinh_ac, Vinl_ac present and match data sheet, if needed	---	
5.2.12	LEVEL 3	[Receiver Thresholds] Vinh_dc, Vinl_dc present and match data sheet, if needed	---	
5.2.13	LEVEL 3	[Receiver Thresholds] Tslew_ac/Tdiffslew_ac present and match data sheet, if needed	---	
5.2.14	LEVEL 3	[Receiver Thresholds] Threshold_sensitivity and Ext_ref present and match data sheet, if needed	---	
5.3.1	LEVEL 2	I-V tables have correct typ/min/max order	---	
5.3.2	LEVEL 2	[Pullup] voltage sweep range is correct	---	
5.3.3	LEVEL 2	[Pulldown] voltage sweep range is correct	---	
5.3.4	LEVEL 2	[POWER Clamp] voltage sweep range is correct	---	
5.3.5	LEVEL 2	[GND Clamp] voltage sweep range is correct	---	
5.3.6	LEVEL 2	I-V tables do not exhibit stair-stepping	---	
5.3.7	LEVEL 2	Combined I-V tables are monotonic	---	

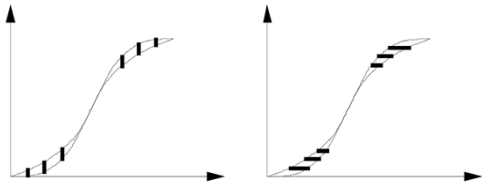
Curve Overlay Metric

- Relatively simply method
- Easy to implement by using a computer program
- Large error occurs when the most points are not perfectly aligned up even visual check seems to be good
- Do not count the error due to waveform shifting
- Not a great reference for automation purposes

4.3 Curve Overlay Metric

The Curve Overlay Metric applies to cases in which the measured and simulated data should theoretically lie directly on top of each other. For example, a structural simulation of a 50 Ω load and a behavioral simulation of the same load should theoretically yield identical results. Another example is the measurement of a known-typical sample component and a structural simulation of the same network under identical process-voltage-temperature conditions. The Curve Overlay Metric measures how well the two curves or waveforms match each other by summing the absolute value of the x-axis (or y-axis) differences between the two data points, weighing the sum against the range of data points along that axis, and dividing by the number of data points.

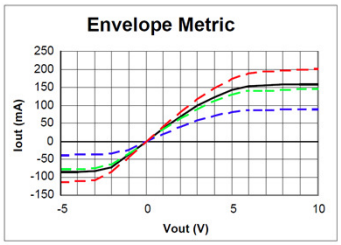
$$FOM = 100 \cdot \left[1 - \frac{\sum_{i=1}^{N} |X_i(golden) - X_i(DUT)|}{\Delta X \cdot N} \right]$$



Curve Envelop Metric

4.4 Curve Envelope Metric

The Curve Overlay Metric applies to cases in which the measured data are, in theory, bounded by two curves (or waveforms) that represent process-voltage-temperature extremes. In general, this metric is useful when the processing conditions of the sample component are unknown. The Curve Overlay Metric returns a yes/no value depending on whether or not every one of the data points falls within the envelope boundaries defined by the min and max curves. The plot below demonstrates a lab pull-down curve (solid line) that is slightly stronger than the typical curve (middle dashed line) and lies well within the (outer dashed lines).



The Curve Envelope Metric presents a difficulty in the case of unterminated transmission line loads. Because these waveforms overshoot normal logic levels and ring back, the min and max waveforms intersect each other and do not define an envelope. Therefore, the Curve Envelope Metric may not be applied to the Open Transmission Line load or the Transmission Line and Receiver load.

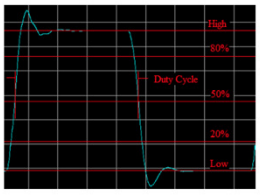
- Good to be used for measurement correlation cases
- Applies a good estimate for unknown/hard_to_ control operation conditions
- No result that indicates how accurate the model is

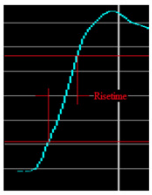
Threshold based Metric from Xilinx

- Uses 5 the most important thresholds to measure the correlation result
- Simple and easy to use a computer program for the results
- Ignores some transition effects
- Difficulty to be used for some abnormal waveform correlations

5 Metrics Defined

- We propose the following 5 metrics/features for waveform comparison:
  - high level, low level, rise time, fall time, and duty cycle

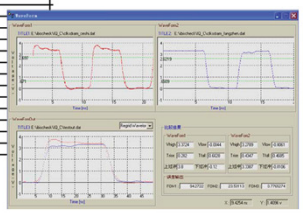




IBIS-to-Spice Correlation 10 Xilinx XILINX

Threshold based Metric from Huawei

验证项	检查要素
统计量化验证	1.1 FOM1
	1.2 FOM2
电气指标验证	2.1 高电平稳定电压（V）
	2.2 低电平稳定电压（V）
	2.3 高电平过冲(V)
	2.4 低电平过冲(V)
	2.5 高电平有效位宽(ns)
	2.6 低电平有效位宽(ns)
	2.7 上升时间(ns)
	2.8 下降时间(ns)
	2.9 边沿是否单调
辅助验证项	3.1 高电平回冲
	3.2 低电平回冲
	3.3 眼宽
	3.4 眼高



FOM:

$$FOM1 = 100 \cdot \left[1 - \frac{\sum_{i=1}^{N} |Y1_i - Y2_i|}{YW \cdot N}\right]$$

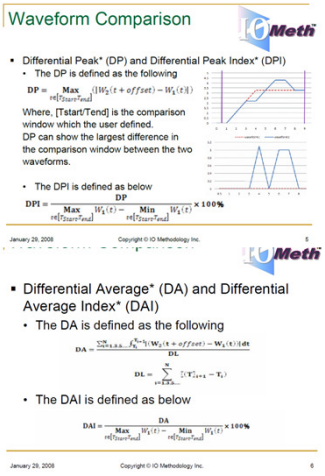
$$FOM2 = 100 \cdot \left[\frac{\max|Y1_i - Y2_i|}{YW}\right]$$

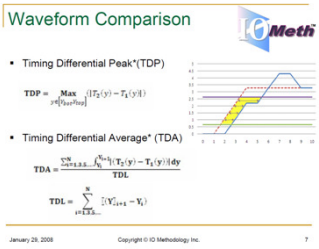
$$FOM3 = \max|Y1_i - Y2_i|$$

HUAWEI TECHNOLOGIES CO., LTD. Page 7 HUAWEI

- Uses more thresholds to measure the correlation result including overshoots, monotonicity and eye measurements, etc. Plus FOM and customized FOMs
- Getting more difficult to use a computer program for the results but kind of manageable
- Still difficulty to be used for some abnormal waveform correlations

Differential Index based Metric from IO Methodology





- Brings 3 differential indexes (peek, average and timing) measuring together for the result (generic waveform comparison approach)
- Close to human visual predictions
- No dependency for threshold settings
- Works find even for abnormal waveforms
- Must use a computer program to calculate

Common Mistakes

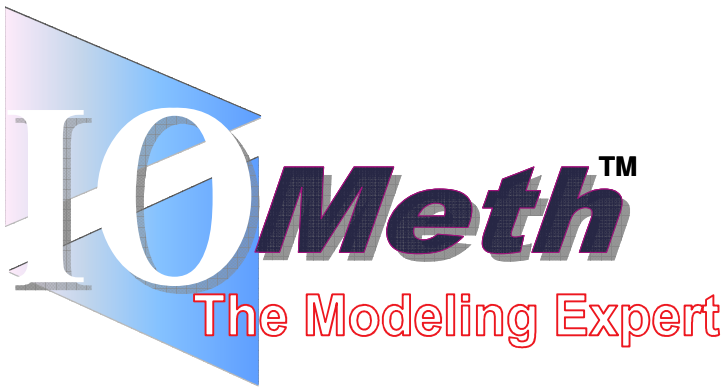
- Syntax Check
  - IBIS Golden Parser is a good first-pass tool for legal IBIS syntax check
  - The most of simulators will stop if your IBIS file contains syntax errors
  - No error and warning doesn't mean it is a good IBIS model for simulations
  - With warning messages, the IBIS model might still produce the accurate results against golden sources
- Test Circuit
  - Proper test circuit is important to get meaningful validation results
    - Your IBIS model might not be operable for certain conditions. It might heavily depend on your extraction conditions
  - Use application level test circuit for your correlations

Common Mistakes (continue)

- I-V / V-T Curves
  - Individual I-V might not within your expectations. Need to check the combined curves instead
  - IBIS Spec only accepts 100 data points for I-V curves
    - A number of system vendors asked for 1000 I-V points
  - Do not always use/ask 2 sets of V-T curves with 50 ohm + V_fixture=VCC/GND
    - Some buffers are only working properly for high-impedance load
    - Some buffers will produce a straight line for V_fixture=VCC or GND. e.g. OPEN type buffers
    - For some differential buffers, you might have to set V_fixture=Common_mode_voltage
  - Be careful about I-V / V-T mismatch error/warning
    - The most of times, this mismatch indicates your IBIS extraction settings are improper or inconsistent
    - Be aware of fixing
      - Don't fix it if it is not just a numerical error. It might have to be extracted again

Conclusion

- Validation is better to be done by IBIS model vendors
- Comparison methods are vary. Use them wisely to fit your buffer model needs
- IBIS user should ask for the vendor for reasonable validation report and/or test bench files
  - I/O buffers are vary. Be sure the contents you asked are reasonable
  - The different simulators could give out different IBIS simulation results



http://www.iometh.com

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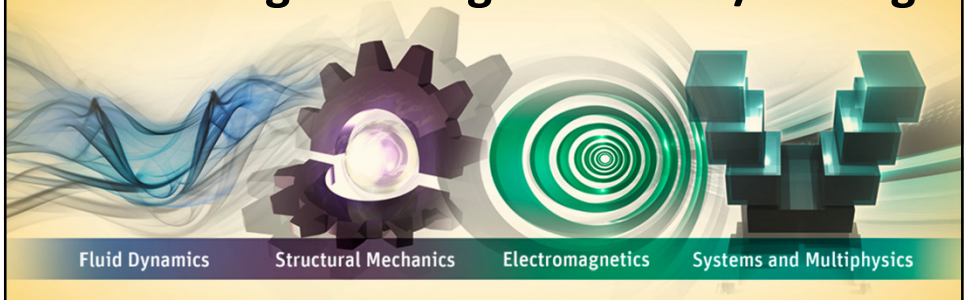
The Evolution of DDR Memory and Overcoming Challenges of DDR3/4 Design



Asian IBIS Summit
Shanghai, China
November 9, 2012

Steven G. Pytel, PhD.
SI Product Manager

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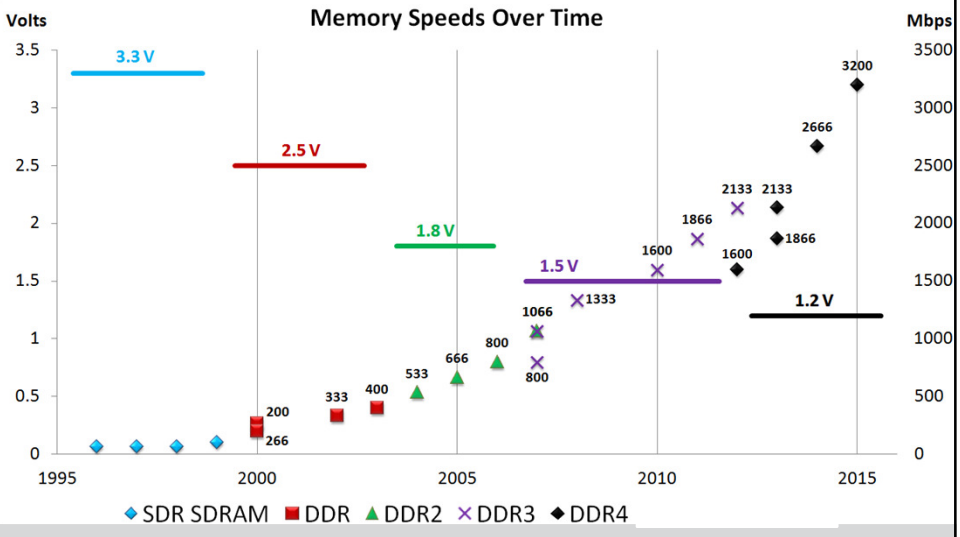
Memory Speeds Over Time



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DDR4

- JEDEC recently announced the DDR4 standard
  - September 25th, 2012
  - JESD79-4
- Major Implications:
  - Point to Point Architecture
  - x4, x8, and x16 supported
  - 2GB to 16 GB SDRAMs
  - 1.2 V system
    - Vrefdq – on die reference voltage for DDR4
    - Up to 40 % reduction in power
    - Pseudo Open Drain Silicon architecture vs. push/pull
      - Pulled to Vdd thereby only drive low to zero
  - Data bus inversion
    - Limits # of SSO at a single time to improve SI and reduce power
  - Write leveling for CMD/ADD, CNTL and CLKs to control skew due to Fly-by topology
  - Server design
    - Distributed buffers for each byte lane compared to single buffer for all 64 bits
    - Point to Point topology requiring a switch between DIMMs
  - Support for Chip Stacking
    - TSV Supported architectures for SDRAMs

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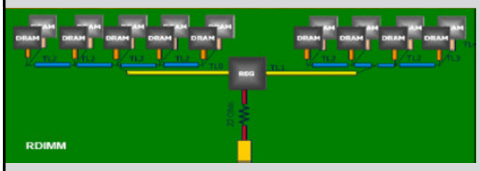
T-topology vs. Fly-by topology

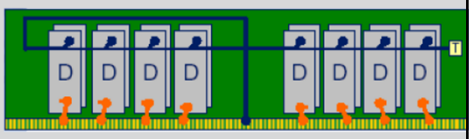
DDR2 T-topology



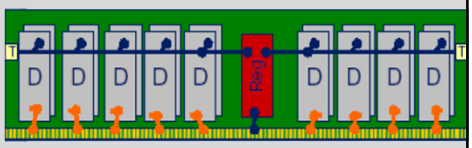
DDR2 RDIMM

Clock arriving time to all DRAMS
on a DIMM are expected to be the same

DDR3 Fly-by topology

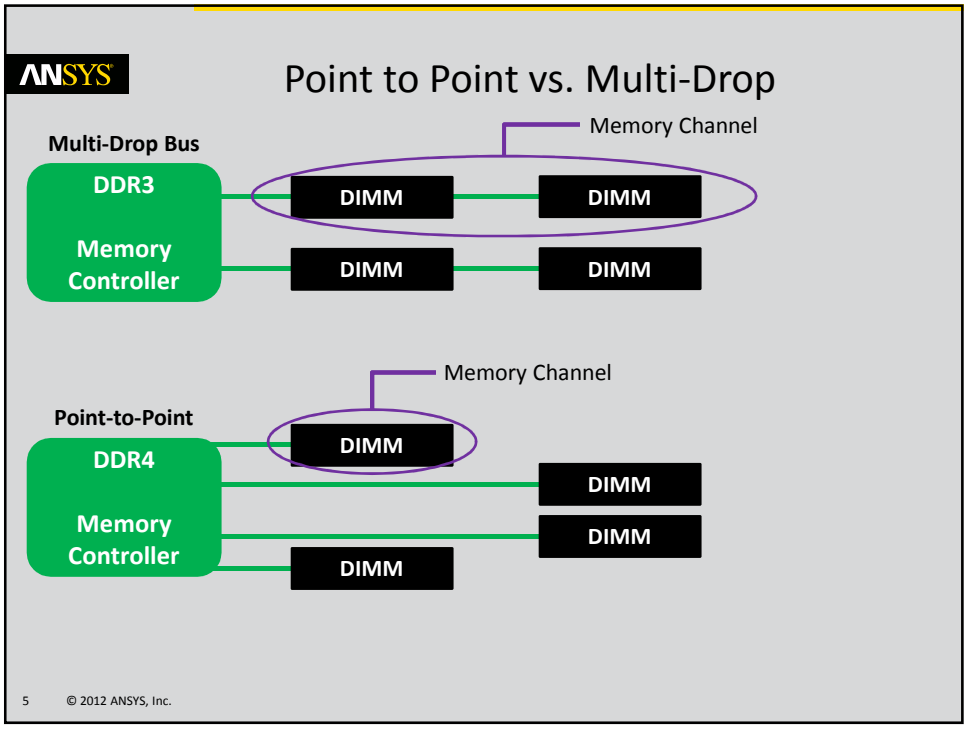


DDR3 UDIMM



DDR3 RDIMM

Clock arriving time to each DRAM
on a DIMM are different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Point to Point vs. Multi-Drop
Multi-Drop Bus
DDR3
Memory Controller
Memory Channel
DIMM
DIMM
DIMM
DIMM
Point-to-Point
DDR4
Memory Controller
Memory Channel
DIMM
DIMM
DIMM
DIMM
5
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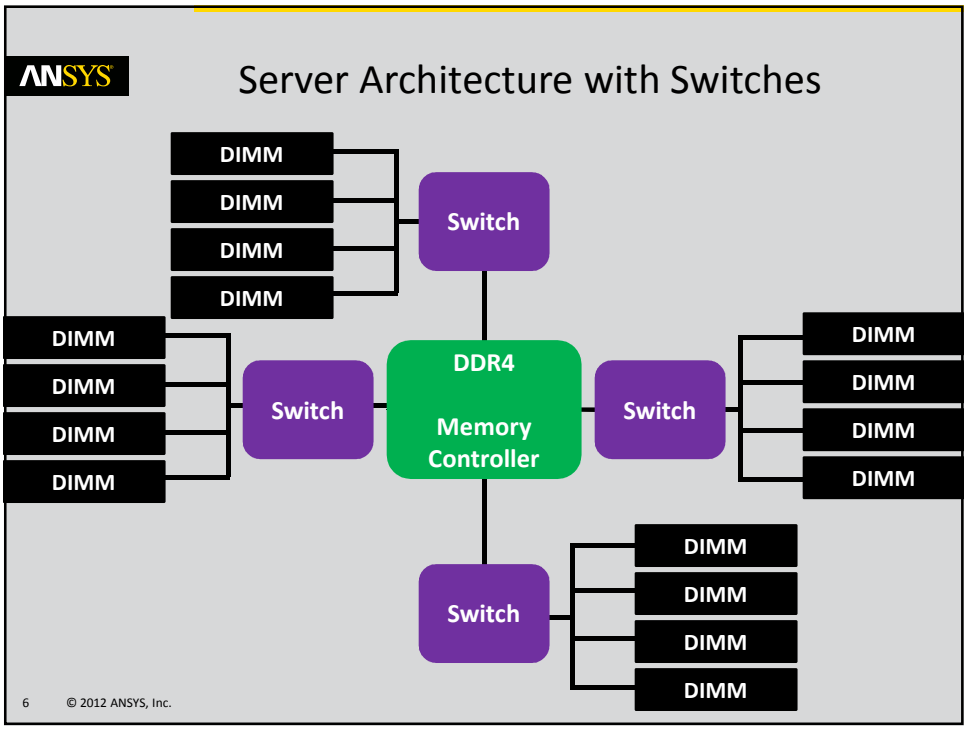
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Server Architecture with Switches
DIMM
DIMM
DIMM
DIMM
Switch
DIMM
DIMM
DIMM
DIMM
Switch
DDR4
Memory Controller
Switch
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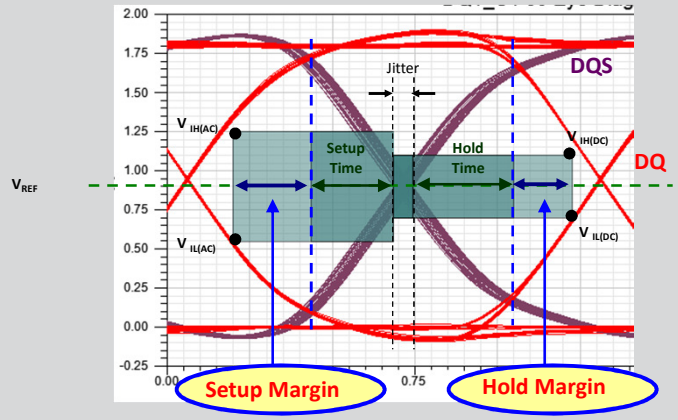
DDR 3 Key Spec

Setup Margin & Hold Margin



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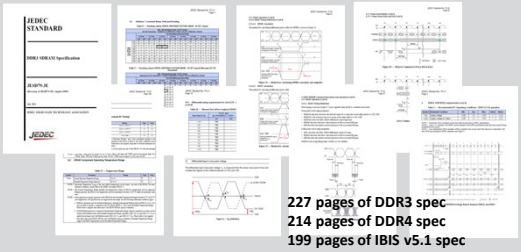
DDRX Technology & Challenges

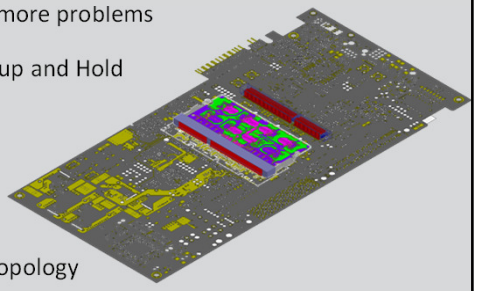
- Design challenges?
  - Validation
    - Prototype
    - Measurement
    - Interpret and implementation(calculation) of Design Spec such as DDR3/4, LPDDR2/3 and more…
    - Large amount output data report of results
  - Capacity or Complexity and Time
    - Chip to Chip or Chip to PKG
    - Chip + Package + PCB + Connector/Cable + PCB + Package + Chip
    - Full System



227 pages of DDR3 spec
214 pages of DDR4 spec
199 pages of IBIS v5.1 spec

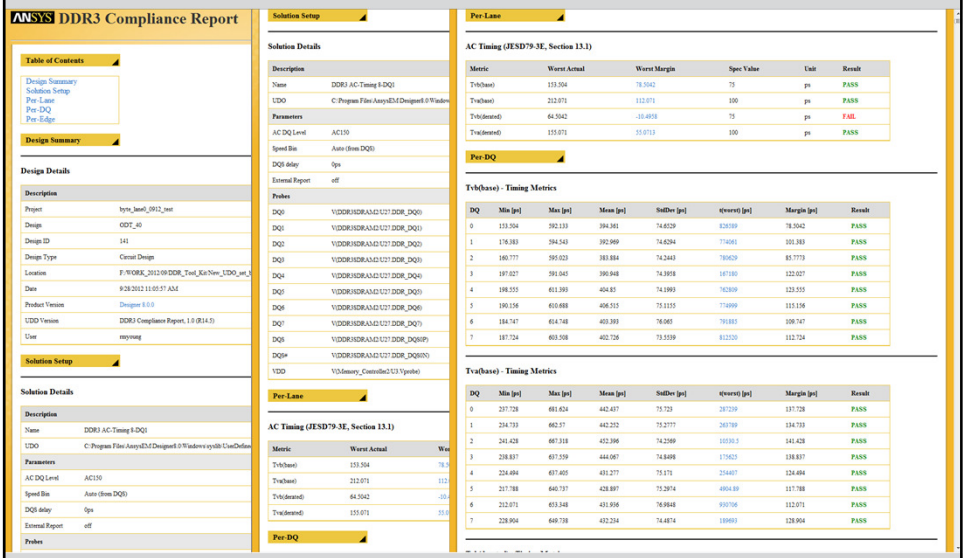
DDRX Technology & Challenges

1. Higher Speeds
   - 66 Mbps to 3200 Mbps and beyond
   - Higher speed and edge rates cause more problems with skew, coupling, radiation, etc…
   - Timing margins become tighter; Setup and Hold timings
     - DDR 400 has a window of 2.5 ps
     - DDR4 3200 has a window of 312.5 ps



2. Changes with design topology
   - DDR2 started ODT support
   - DDR3 started Fly by topology vs. T topology
   - DDR3 uses only differential strobes
   - DDR4 architecture is point to point
     - One controller to 1 DIMM
   - DDR4 is Psuedo Open Drain vs. Push/Pull

DDRX Technology Challenges



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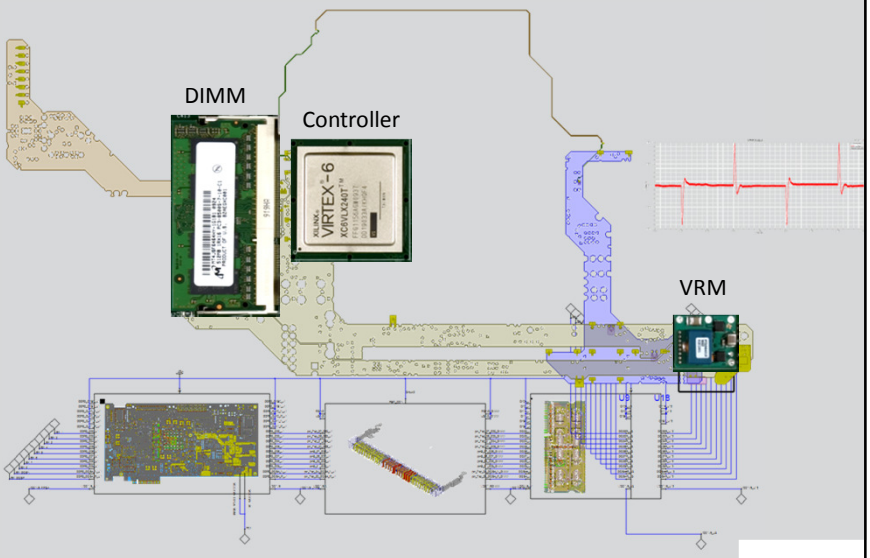
DDR3 1.5V PDN with VRM



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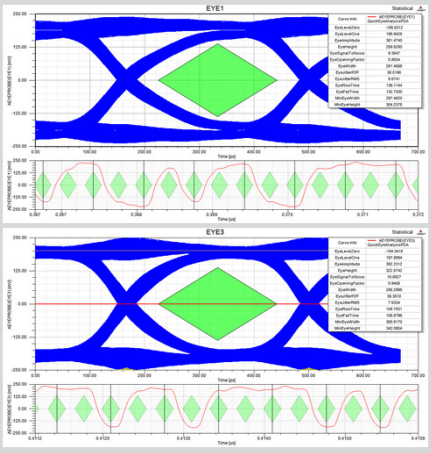
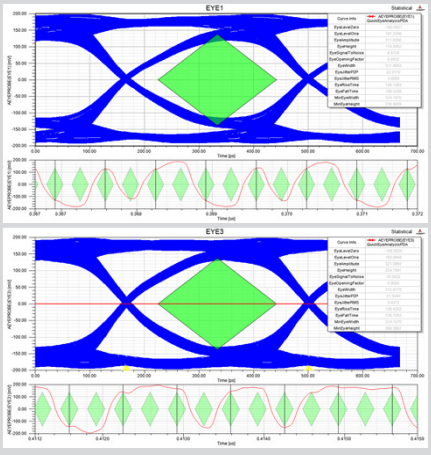
DDR3 Connector Impact (Reflections)

Without Connector



With Connector



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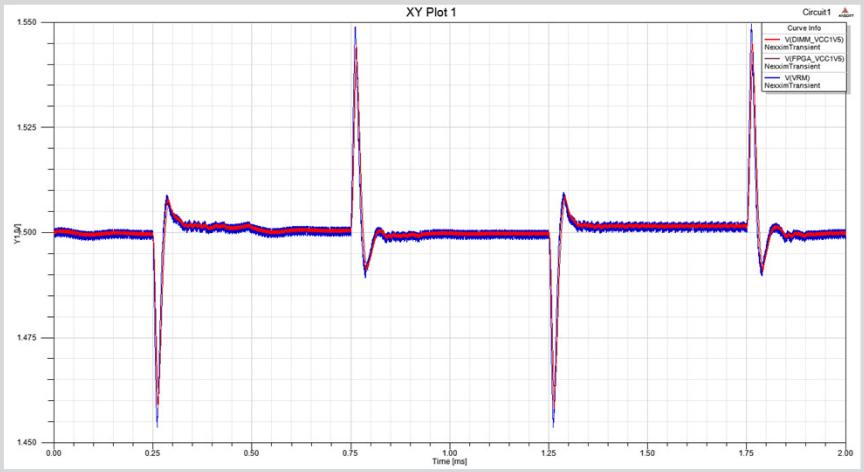
DDR3 1.5V PDN with VRM



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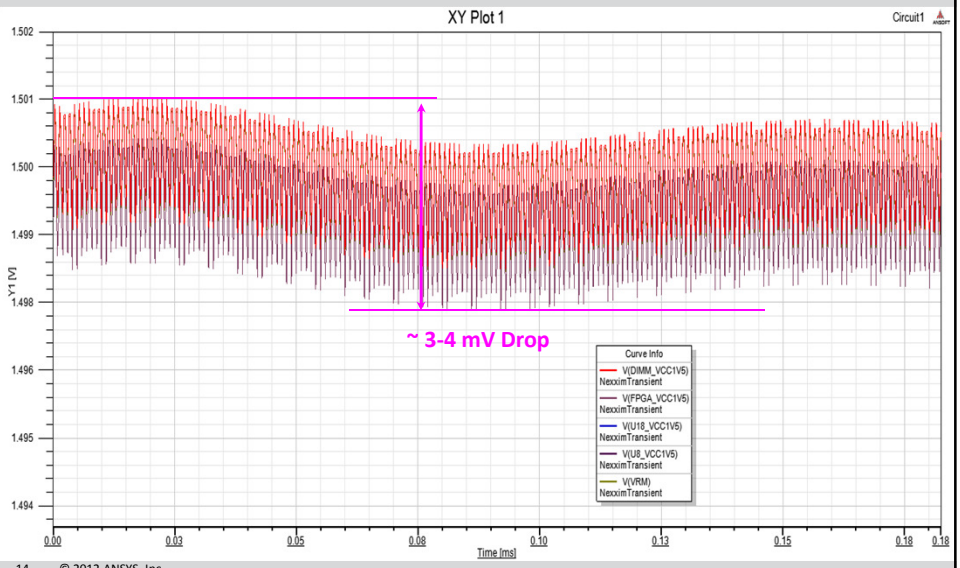
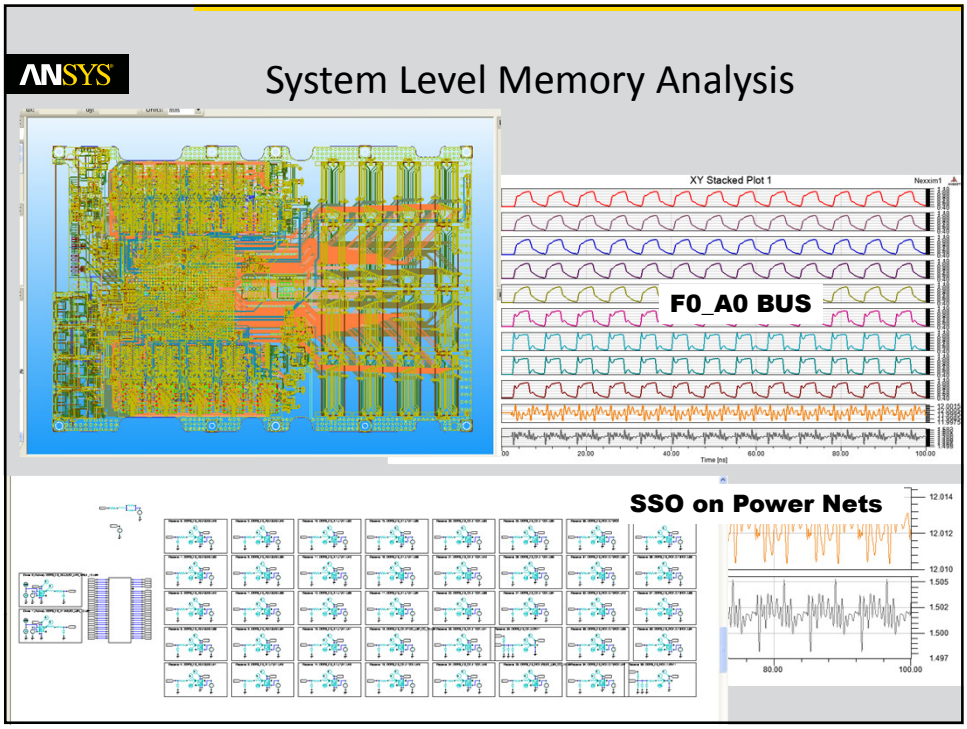
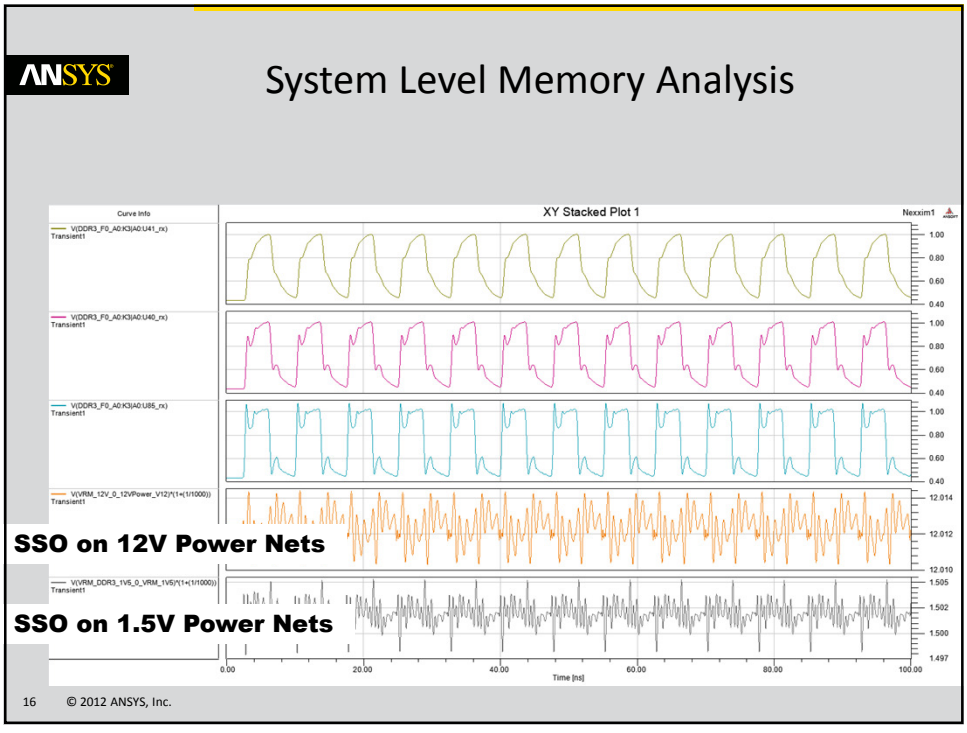
DDR3 1.5V PDN with VRM




ANSYS
System Level Memory Analysis
XY Stacked Plot 1
Nexxim1
F0_A0 BUS
SSO on Power Nets


ANSYS
System Level Memory Analysis
Curve Info
XY Stacked Plot 1
Nexxim1
SSO on 12V Power Nets
SSO on 1.5V Power Nets
Time [ns]
16
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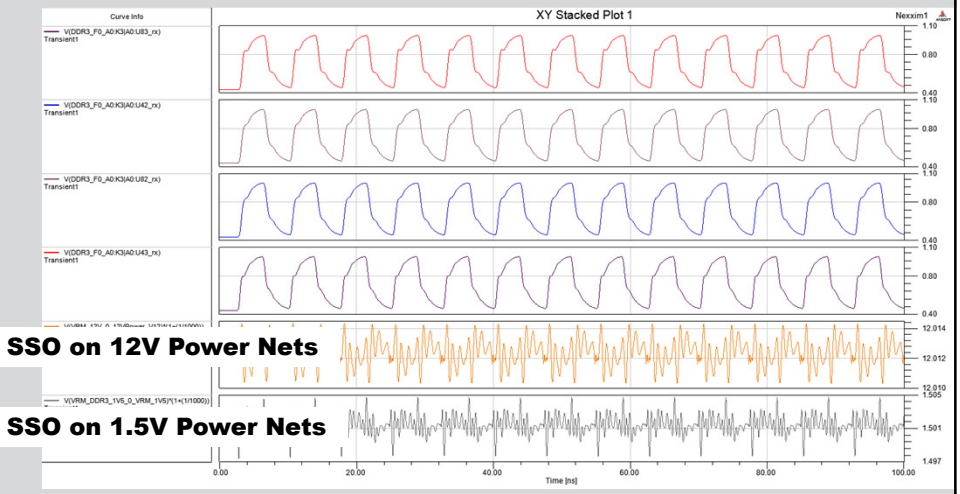
System Level Memory Analysis



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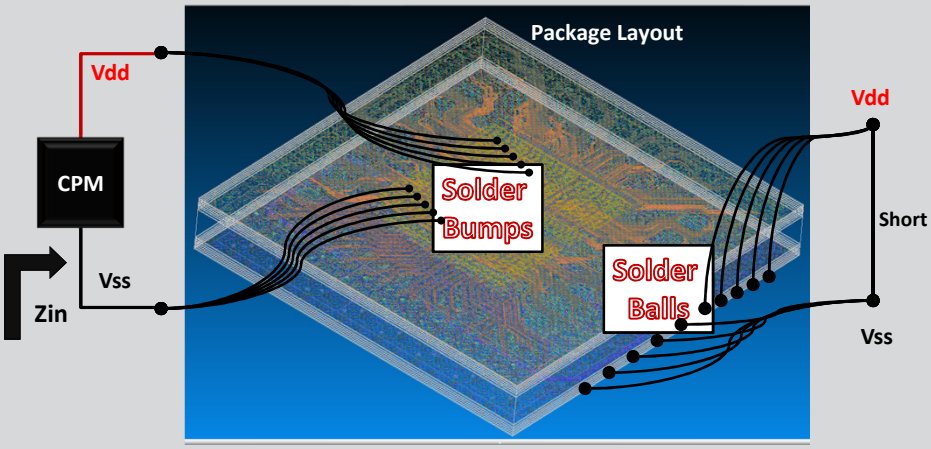
Recall Chip Impedance



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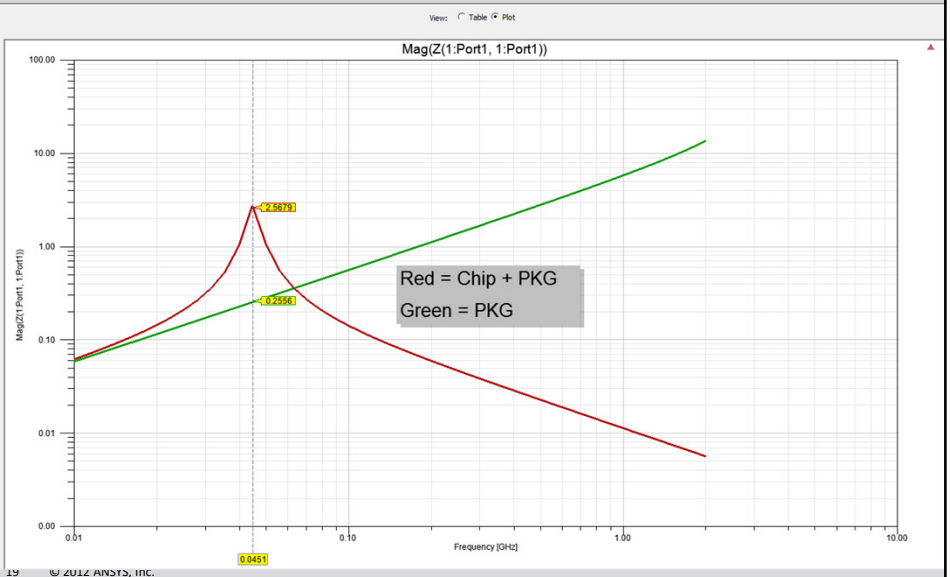
Impedance Results with & without Chip



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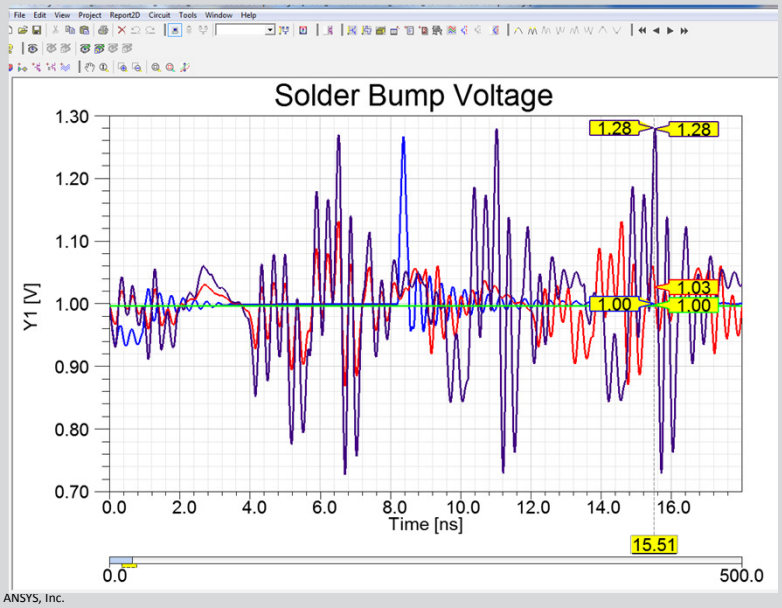
Die Solder Bump Voltage



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Conclusion

- DDR4 Standard was recently released
  - Interconnect challenges due to Chip, PKG, & PCB
    - Reduced Voltage (1.2V -> 1.05V expected)
    - Increased Data Rates (1600 Mbps -> 4266 Mbps expected)
    - Future stacking of SDRAMs expected with TSV technology
- System level performance must include:
  - Accurate PKG/PCB extractions including connectors
  - Accurate Die Models: IBIS + current?

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INVENTIVE

Designing DDR3 system using Static Timing Analysis in conjunction with IBIS simulations

Taranjit Kukal, Zhangmin Zhong, Heiko Dudek
Cadence Design Systems, Inc.
Presented by: Zhangmin Zhong

Asian IBIS Summit
Shanghai, China
November 9, 2012

Agenda

- Key Design Challenges
  - DDR3 Timing and SI specifications
- Problem Statement
  - Piecemeal simulations do not guarantee optimal design
- Solution
  - Static Timing Analysis in conjunction with IBIS simulations
- Use-cases
  - Step-by-step method to optimally use EDA flows
- Summary

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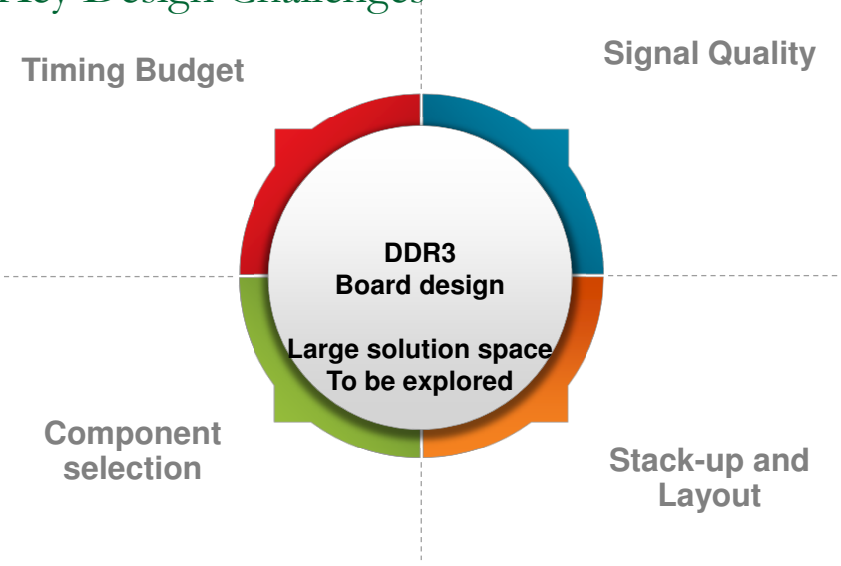
Key Design Challenges



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Key Design Challenges: Timing Budget

- Set-up / Hold Times
  - Data write w.r.t strobe
  - Data read w.r.t strobe
  - Addressing w.r.t clock
- Strobe w.r.t clock
  - Data w.r.t Address
- Account for
  - Clock/Strobe Jitters and Interconnect Jitters
  - Slew-rates and hence derating of setup/hold

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Key Design Challenges: Signal Quality

- Thresholds
  - DC and AC
  - Noise-Margins
- Overshoots/Undershoots
  - Magnitude
  - Area
- tVac
  - Minimum time for signal to stay above threshold
- Eye
  - Data-Valid Window after accounting Jitter
- Slews that in-turn affect timing
  - Rise/Fall times

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Key Design Challenges: Component Selection

- Memory-Buffers
  - Trade-off between read-write cycles
- Controller Driver strength
  - Trade-off between read-write cycles
- Connector
  - Insertion loss
- Strobe/Clock differential buffers
  - Should satisfy tDVac and overshoot/undershoot area requirements

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Key Design Challenges: Layout Constraints

- Trace-lengths
  - Relational Propagation-delays Data-Strobe for balanced setup/hold
  - Relational Propagation-delays Address-Clock for balance setup/hold
  - Relational Propagation-delays Strobe-Clock for successful write-leveling
- Topology schedules
  - Point to Point for Data
  - FlyBy for Address
- Trace Impedance
  - Example: Lead-in section (45 ohm) to Load-in section (60 ohm) through neck-down (~5 to 10 mm) for clock
  - Percentage variation that can be tolerated
- Differential matching (CLK, STROBE)
  - Maximum unparallel length

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Problem Statement: Multiple constraints across Timing / SI

- DDR3 has several SI and Timing constraints and getting all of them to meet is a big solution-space to explore.
- Designer tries to fix a few; and in the process puts other measurements-of -interest out of specifications.

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Problem Statement: Timing Closure across read/write/address

- Timing-Closure is time-consuming as there are too many constraints to be met
  - Etch delays needed for timing-closure during Read cycle may not work during Write cycle.
  - It is not enough to get just positive Setup/Hold margins; optimal design needs setup and hold margins that equally distributed.
- Requirement of relative delays between Data (Strobe) vs Address (Clock) brings additional challenge.
- It is also important to budget for signal and interconnect jitters on various signals.
  - What may look to be meeting the constraint is likely to fail due to jitter causing uncertainty in the signal.

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Problem Statement: SI affects timing

- Slew-rates affect Setup/Hold time-constraints.
  - SI simulations provide slew-rates of signals that in-turn need to be considered for timing constraints. For example, hold-time constraint could be 160pS for slew-rate of 1V/ns while it could be 200pS when the signal slew-rate is 2V/ns
- Eye-shape could indicate a need for different relative etch-lengths for equal setup/hold margins.
  - While Static Timing Calculations would provide one set of readings for etch-delays, the eye-shape (that could be narrow on one side) may force the designer to refine the relative delays for balanced setup/hold times.
- Stack-up variation and Cross-talk causes interconnect jitter that needs to be accounted for in the timing-checks.
  - It is important that such jitter is estimated through SI simulations and then annotated to the Timing-models for timing closure.

12

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Problem Statement (Current approach): Ad-hoc analysis and verification (Leading to Non-optimal design)

- Timing-checks are done using hand-calculations at times and then the focus is to do post-layout verification using SI simulations to ensure correctness.
- Limitations:
  - Goal is to just meet constraints as against optimal design with enough margins on all constraints.
  - Manual timing-budget calculations are time-consuming and inefficient
  - No way to include SI effects into timing-calculations

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Problem Statement (Current approach) : Ad-hoc analysis and verification (Leading to Non-optimal design)

- Designers use layout rules provided by device manufacturers
- Limitation:
  - Limits flexibility. PCB designers refrain from trying variations in terms of component selection from different vendors and in trying different board dimensions and circuit configurations.
  - Over-design at times as layout guidelines are usually on the stricter side to ensure working of system

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Problem Statement (Current approach) : Ad-hoc analysis and verification (Leading to Non-optimal design)

- SI simulations are usually done as audit at verification step following a piecemeal approach
- Limitations:
  - Use of real-time simulations to do exhaustive timing-verification is too time-consuming and difficult.
  - It is very difficult to manage optimal parameter selection across constraints spread across read/write and address cycles.

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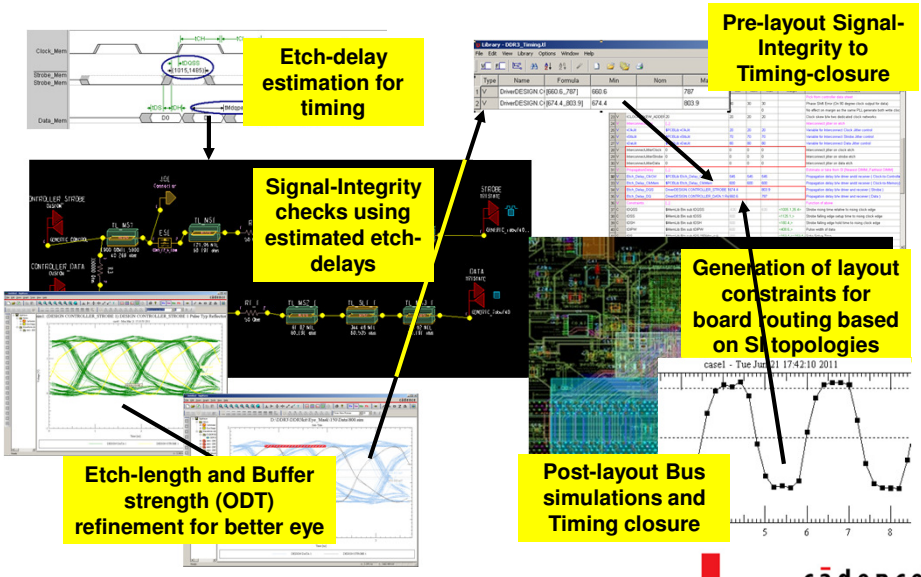
Unified SI/STA flow for DDR3



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Solution: Static Timing analysis

- Static Timing exploration independent of time-expensive SI simulations can provide seed for etch estimation.
- Automatic update of constraint limits based on data-rate, slew-rate of signals, threshold-values selected for design can make easy computation.
- Automatic calculation of relative etch-delays for balanced setup/hold times while accounting for uncertainty in signals due to jitter can save multiple iterations.

18

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Solution: Timing analysis feeds SI simulations

- Results of STA feed into SI simulations.
  - Estimated etch-delays (flight-time) of data, strobe, address, clock map to interconnect flight-times
  - Estimated jitter becomes constraint for cross-talk (interconnect and data-dependent)
- SI Simulations with IBIS buffers
  - Building on interconnect details (vias, trace-lengths, stack-up) keeping the flight-time constraint from STA
  - Improving on interconnect topologies to meet SI constraints and better centering of strobe w.r.t data

19

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Solution: SI simulations that feedback STA

- Feed-back updated flight-times (switch-delays), worst-jitter and slew-rates from real-time SI simulations to timing-models to close timing-constraints.
- Generation of layout constraints from interconnect topologies
  - Routing the board based on layout constraints
- Post-route SI simulations followed by timing-closure.

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Agenda

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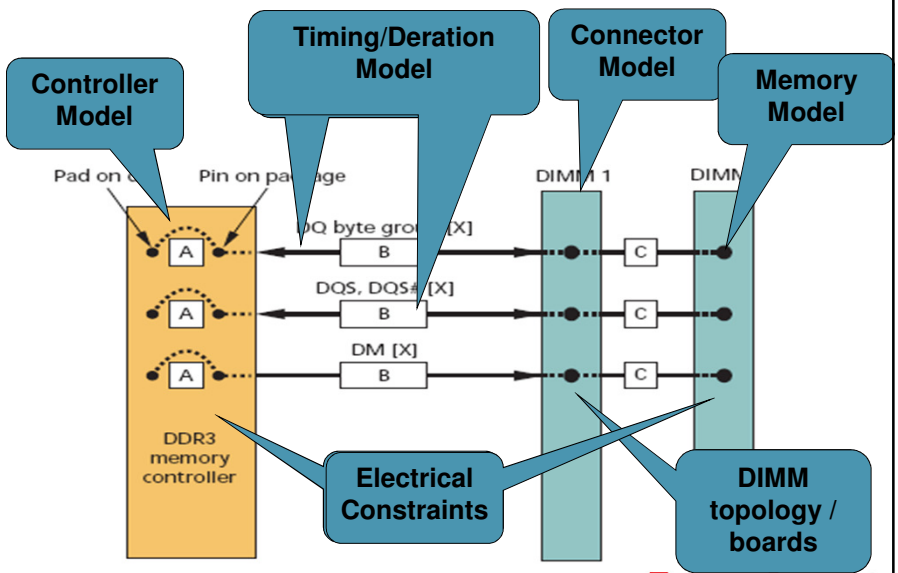
Use-case



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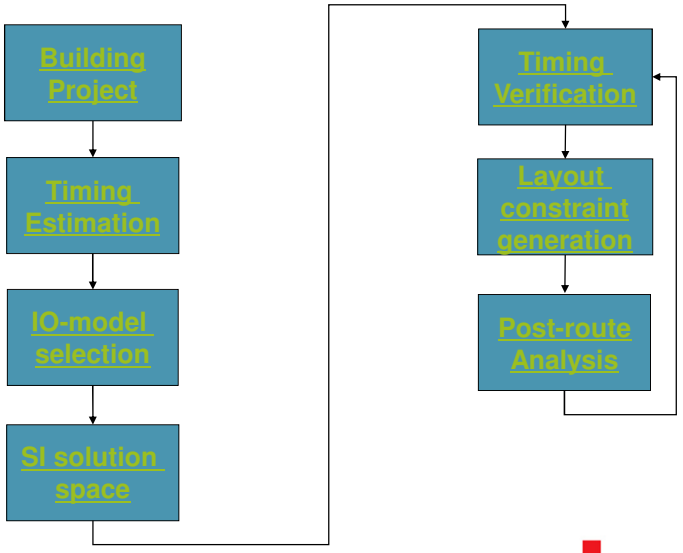
Use-case



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Building Project

- Frequency of operation and AC threshold levels
  - *Configures TD models*
  - *Configures custom measurements*
- Address (1T / 2T)
  - *Configures TD models*
- New DIMMs (Or On-board) vs Existing DIMMs
  - Pre-created Topologies vs Extracted DIMM topologies
- DIMM Card Type
  - *Configures topologies and ECSets*

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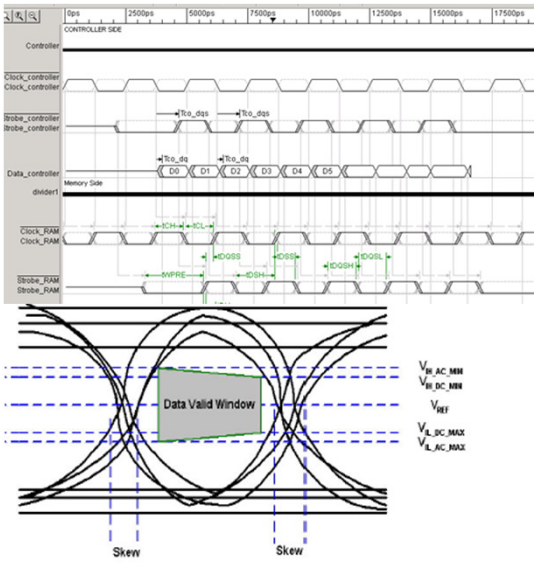
Timing estimation

- Data-Strobe
  - Write
  - Read
- Address-Clock (1T or 2T)
- Decide etch-delays that can meet timing specifications



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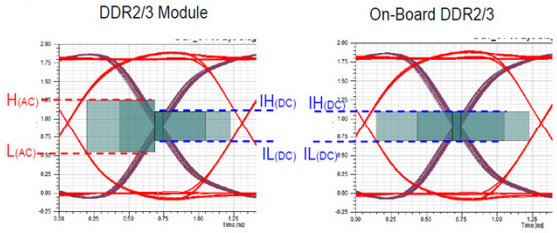
IO-model selection/Exploration

- For best noise-margins and Eye for read/write

- Controller Model
  - Impedance
- Memory Model
  - ODT
- Connector Model
- Strobe
  - tvac, shoot-area



Configuration		Write To	DRAM Controller	Slot 1		Slot 2	
Slot 1 (DIMM 1)	Slot 2 (DIMM 2)			Rank 1	Rank 2	Rank 1	Rank 2
Dual rank	Dual rank	Slot 1	ODT off	120Ω	ODT off	ODT off	30Ω
		Slot 2	ODT off	ODT off	30Ω	120Ω	ODT off
Dual rank	Single rank	Slot 1	ODT off	120Ω	ODT off	20Ω	n/a
		Slot 2	ODT off	ODT off	20Ω	120Ω[1]	n/a
Single rank	Dual rank	Slot 1	ODT off	120Ω[1]	n/a	ODT off	20Ω
		Slot 2	ODT off	20Ω	n/a	120Ω	ODT off
Single rank	Single rank	Slot 1	ODT off	120Ω[1]	n/a	30Ω	n/a
		Slot 2	ODT off	30Ω	n/a	120Ω[1]	n/a
Dual rank	Empty	Slot 1	ODT off	40Ω	ODT off	n/a	n/a
Empty	Dual rank	Slot 2	ODT off	n/a	n/a	40Ω	ODT off
Single rank	Empty	Slot 1	ODT off	40Ω	n/a	n/a	n/a
Empty	Single rank	Slot 2	ODT off	n/a	n/a	40Ω	n/a

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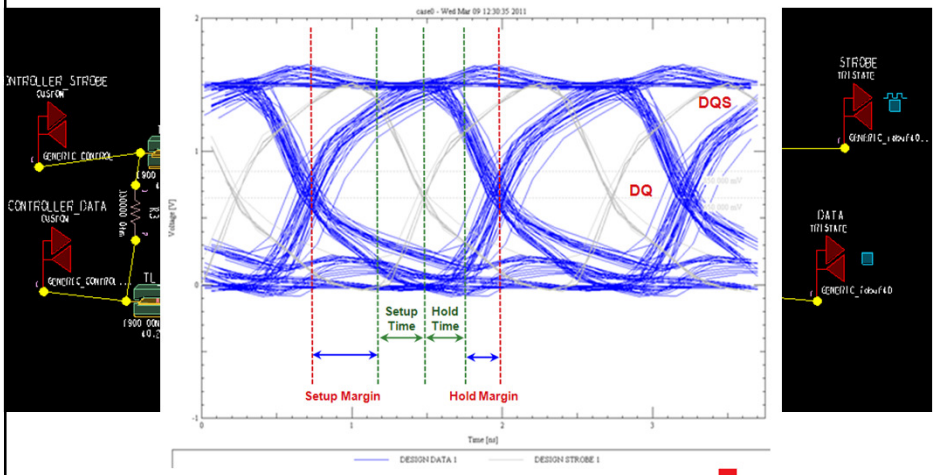
SI Solution Space for Relational Topologies - Explore data w.r.t strobe; address w.r.t clock



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Timing Verification after SI-annotation

- Re-verify timing after import of flight delays and jitter from SI simulations

Name	Formula	Min	Nom	Max	Margin	Comment
JitterSpecifications	[...]					Pick from controller data sheet
tPLL_PSERR	30	30	30	30		Phase Shift Error (On 90 degree clock output for data)
tPLL_Jitter	0	0		0		No effect on margin as the same PLL generate both write clo
tCLOCK_SKEW_ADDER	20	20	20	20		Clock skew b/w two dedicated clock networks
InterconnectJitter	[...]					Interconnect jitter on etch
vClkJit	$PCBLib:vClkJit	20	20	20		Variable for Interconnect Clock Jitter control
vStbJit	$PCBLib:vStbJit	70	70	70		Variable for Interconnect Strobe Jitter control
vDatJit	$PCBLib:vDatJit	80	80	80		Variable for Interconnect Data Jitter control
InterconnectJitterClock	0	0	0	0		Interconnect jitter on clock etch
InterconnectJitterStrobe	0	0	0	0		Interconnect jitter on strobe etch
InterconnectJitterData	0	0	0	0		Interconnect jitter on data etch
PropagationDelay	[...]					Estimate or take from SI [Nearest DIMM_Farthest DIMM]
Etch_Delay_ClkCtrl	$PCBLib:Etch_Delay_ClkCtrl	545	545	545		Propagation delay b/w driver andd receiver (Clock-to-Controll
Etch_Delay_ClkMem	$PCBLib:Etch_Delay_ClkMem	600	600	600		Propagation delay b/w driver andd receiver (Clock-to-Memory
Etch_Delay_DQS	DriverDESIGN.CONTROLLER_STROBE.1	674.4		803.9		Propagation delay b/w driver and receiver (Strobe)
Etch_Delay_DQ	DriverDESIGN.CONTROLLER_DATA.1:Re	660.6		787		Propagation delay b/w driver and receiver (Data)
Constraints	[...]					Function of above
tDQSS	$MemLib:Bin:sub:tDQSS	-630		630	<1005.1,35.4>	Strobe rising time relative to rising clock edge
tDSS	$MemLib:Bin:sub:tDSS	500			<1125.1,>	Strobe falling edge setup time to rising clock edge
tDSH	$MemLib:Bin:sub:tDSH	500			<180.4,>	Strobe falling edge hold time to rising clock edge
tDIPW	$MemLib:Bin:sub:tDIPW	600			<408.6,>	Pulse width of data
tDS	$MemLib:Bin:sub:tDS:150(der_su)	200			<163.4,><163.4,	Data Setup Time
tDH	$MemLib:Bin:sub:tDH(der_hl)	200			<275.7,><275.7,	Data Hold Time

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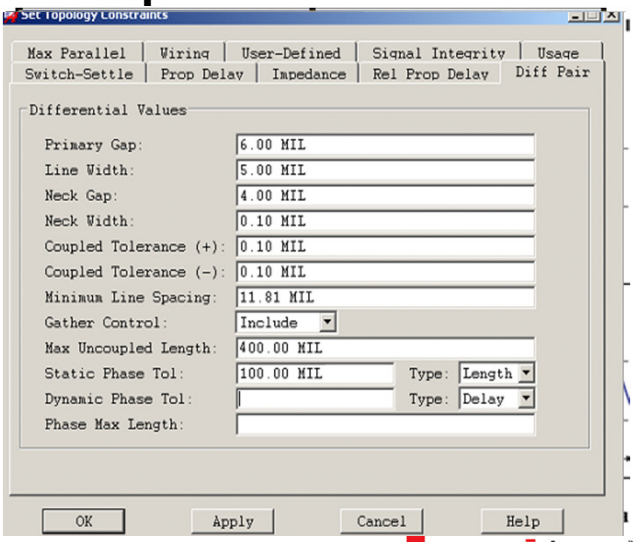
Setting up Layout constraints depending on SI exploration

- Propagation Delays
- Impedance
- Relative Propagation delays
- Max Parallel



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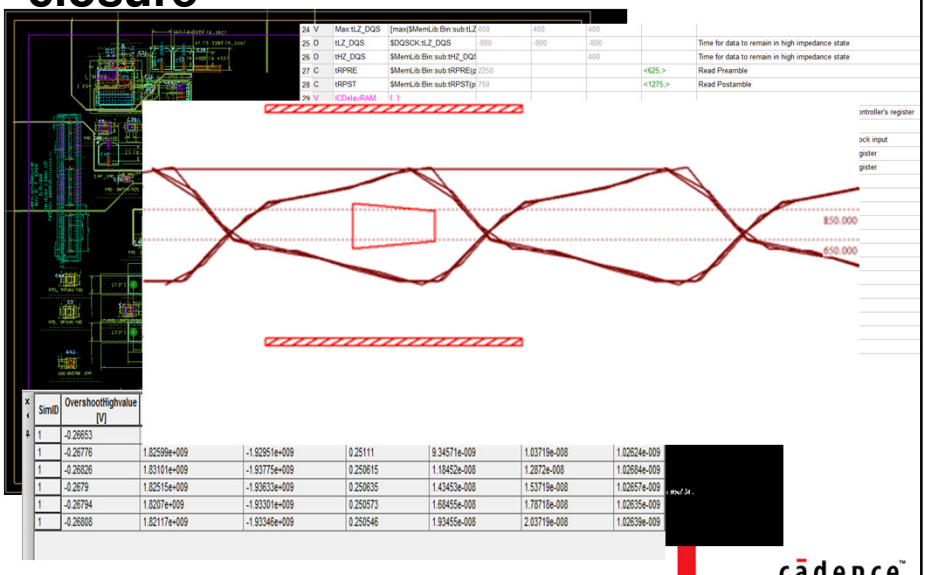
Post-layout verification and Timing closure



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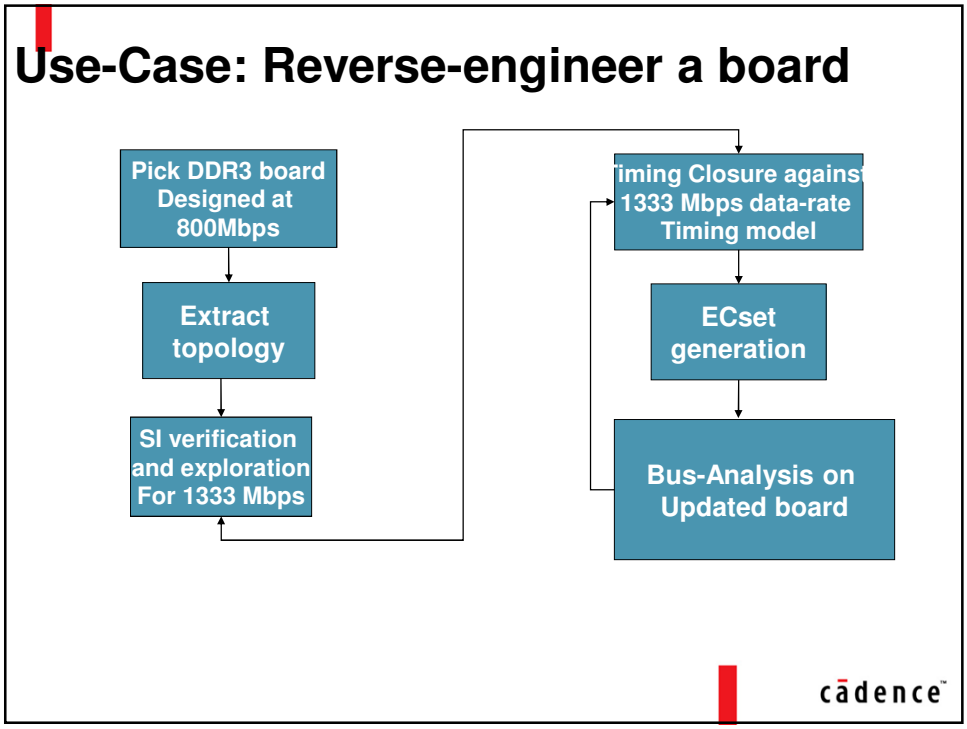
Use-Case: Reverse-engineer a board
Pick DDR3 board Designed at 800Mbps
Extract topology
SI verification and exploration For 1333 Mbps
Timing Closure against 1333 Mbps data-rate Timing model
ECset generation
Bus-Analysis on Updated board
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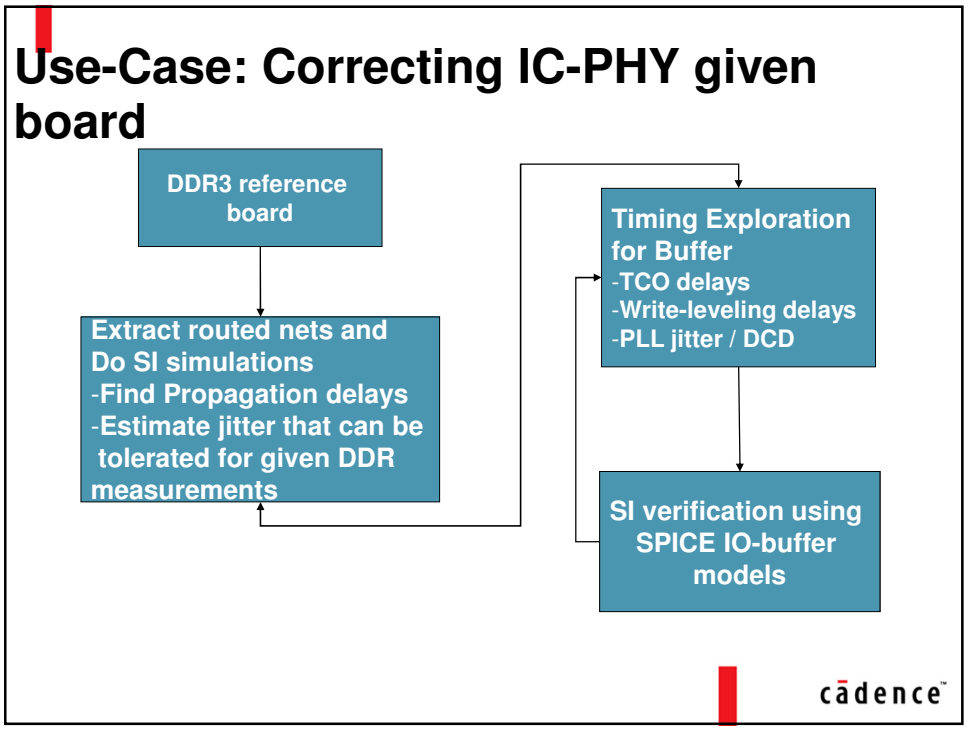
Use-Case: Correcting IC-PHY given board
DDR3 reference board
Extract routed nets and Do SI simulations
-Find Propagation delays
-Estimate jitter that can be tolerated for given DDR measurements
Timing Exploration for Buffer
-TCO delays
-Write-leveling delays
-PLL jitter / DCD
SI verification using SPICE IO-buffer models
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Summary

- DDR3 compliance requires multiple specifications to be met, covering timing and signal-integrity measurements.
- Just using SI simulations to meet all specifications and explore solution space is difficult.
- Use of tools in a piecemeal approach can validate specifications but may not result in the most optimal IC/package/board design

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Summary

- Use of STA in conjunction with SI simulations in a methodical manner is needed to achieve optimal design.
- Timing models should be able to handshake data with IBIS simulations at pre-route exploration and post-route verification stages to ensure that both SI and Timing constraints are met.

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