

IBIS Open Forum Minutes

Meeting Date: **November 21, 2011**

Meeting Location: **Taipei, Taiwan**

VOTING MEMBERS AND 2011 PARTICIPANTS

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Xpeedic Technology	Feng Ling, Wenliang Dai, Shisheng Wu
Yazaki	Kazuki Hattori
YDC	Yoshiaki Manabe
YDK	Yoshio Takemura
Independent	Yoichi Niioka, [Mike LaBonte], Mingwei Chen, Liping Wang

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
December 9, 2011	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

<https://ciscosales.webex.com/ciscosales/j.php?J=205475958>

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The IBIS Open Forum summit was held at the Sherwood Hotel in Taipei, Taiwan. About 131 people representing 51 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

<http://www.eda.org/pub/ibis/summits/nov11c/>

Michael Mirmak convened the meeting and introduced Scott C.S. Li of Foxconn for his comments. Scott welcomed the attendees and thanked the IBIS Open Forum for their ongoing support of the IBIS Summit series.

Michael continued the meeting by thanking the co-sponsors: Cadence Design Systems, Foxconn, Intel Corporation, IO Methodology, Sigrity and Synopsys.

IBIS STATUS AND FUTURE DIRECTION

Michael Mirmak (Intel Corporation, USA)

Michael Mirmak summarized the recent accomplishments of the IBIS Open Forum as an organization. He noted the recent approval of IBIS-ISS, a specification to describe SPICE interconnect subcircuits, and how it offers an opportunity to update support offered by EBD, PKG and ICM. Michael also presented plans for changes to the IBIS and Touchstone specifications, to take effect within the next few months.

IBIS PARSERS

Bob Ross (Teraspeed Consulting Group, USA)

Bob Ross described the basic coverage and features of the IBISCHK IBIS parser and the TSCHK2 Touchstone 2.0 parser. He also described the specific messages provided plus the bug reporting system for both.

POWER AWARE FEATURES OF IBISV5.0 – ACCURACY AND CHALLENGES

Vipul Pursottam Patel, Prabhat Ranjan, and Richa Ahuja (STMicroelectronics, India)

Prabhat Ranjan summarized power delivery support in IBIS 5.0, including the [ISSO_PU]/[ISSO_PD] and [Composite Current] keywords, plus related parser support. He noted that [Composite Current] requires identical time points for I-t and V-T tables, but that any point-reduction used to provide the "best" points for a V-T table may not be the "best" for an I-t table. Related to this, adjustment of table data to accommodate overclocking, including shortening of quiet time in V-T tables, may result in eliminating critical I-t table information. Finally, Prabhat noted that Pulldown reference terminal currents may be important to note independent of other currents, but are assumed to be equal to the sum of Pullup and I/O currents.

Prabhat concluded by presenting correlation results between simulations featuring IBIS 5.0 power delivery enabled models and SPICE models at 50 MHz. IBIS 5.0 performance was good, but can be improved more by inclusion of per-buffer decoupling capacitance for power and ground supplies. Prabhat suggested that this be added to IBIS in a future release.

MODELING THE ON-DIE DE-CAP OF IBIS 5.0 PDN-AWARE BUFFERS

Lance Wang*, Randy Wolff** (*IO Methodology and **Micron Technology, USA)

Lance Wang, with reference to Prabhat Ranjan's presentation, reviewed the two recent improvements in IBIS 5.0 for modeling power delivery behaviors. Incorporating these into buffer models can result in very good matching to SPICE simulations. However, some current and voltage behaviors for non-ideal supplies may not be captured correctly without adding on-die package resistance and on-die decoupling circuits. Lance noted that some current IBIS keywords can help address these issues in limited cases, but that support for on-die power delivery features, including possibly those in BIRD145, should be added to ensure best accuracy.

POWER-AWARE I/O MODELING FOR HIGH-SPEED PARALLEL BUS SIMULATION

Jack W.C. Lin#, Zuli Qin##, Haisan Wang##, and Raymond Y. Chen### (Sigrity, #ROC, ##PRC and ###USA)

Jack W.C. Lin presented a summary of issues and solutions related to high-speed simulation and power delivery for parallel busses. Current memory interface speeds are increasingly limited by power delivery effects, which should be modeled in IBIS due to its speed and IP protection advantages. Jack noted that IBIS 5.0 includes useful power delivery features, but still omits on-die power delivery network impedances and represents buffer capacitance too simply. Adding Zpd, Zpu and Zpg (power-ground impedance) elements through multi-lingual features can improve the accuracy of IBIS 5.0 while still preserving the IBIS speed advantage over SPICE. Jack concluded by showing a case study of DDR3 power delivery effects modeled using IBIS 5.0 and "IBIS Plus" (using the multi-lingual power delivery elements).

BOARD-ONLY POWER DELIVERY PREDICTION FOR VOLTAGE REGULATOR AND MOTHER BOARD DESIGNS

Jiangqi He# and Y.L. Li## (Intel Corporation, #USA, ##ROC)
[Presented by Jimmy Hsu (Intel Corporation, ROC)]

Jimmy Hsu presented a simplified approach for power delivery simulation using behavioral SPICE models. The method involves transient simulations based on resistor models of the PCB, R & L modeling of any sockets, voltage regulator models and current-versus-time data from suppliers. The simplified model's transient results characterize the whole system and would be compared against targets provided by IC vendors. Jimmy showed case studies where voltage regulator performance could be assessed and numbers of decoupling capacitors could be optimized.

SUPPORTING EXTERNAL CIRCUIT AS SPICE OR S-PARAMETERS IN CONJUNCTION WITH I-V/V-T TABLES

Kent Drumstad*#, Adge Hawes*##, Taranjit Kukal***#, Feras Al-Hawari**#, Ambrish Varma**#, and Terry Jernberg**# (*IBM, #USA, ##United Kingdom, **Cadence Design Systems, ###India, #USA)
[Presented by Charlie Shih (Cadence Design Systems, ROC)]

Charles Shih presented on a proposal to add new keywords and features to IBIS to support S-parameters and SPICE. For specific cases, such as on-die terminations or on-die networks that vary with frequency, both SPICE circuit models and S-parameters can be highly useful. A simple way to combine these with traditional table-based IBIS model data is needed. While Touchstone files may be wrapped within a supporting SPICE circuit, a proposal is presented that supports Touchstone S-parameter files in IBIS directly. Further, some high-speed buffer behaviors may be more conveniently modeled in SPICE, but must be used in combination with existing IBIS data. Charles concluded by showing an extended set of examples of syntax enabling IBIS buffer data to be combined with Touchstone or SPICE information, as proposed in BIRD144 and BIRD145.

Audience members asked questions about external circuit support with generic SPICE. Charles suggested they contact individual EDA vendors for specifics.

T-COILS AND BRIDGED-T NETWORKS

Bob Ross (Teraspeed Consulting Group, USA)

Bob Ross presented an overview of T-coil technology, its history and how it applies to signal integrity applications. T-coils can provide a constant ideal termination with increased bandwidth over other termination solutions, which has benefits for high-speed designs as compensation for ESD structures or high-bandwidth terminations. Bob showed how T-coils can clean the responses of terminated transmission lines, plus the closed-form equations that can be used to calculate T-coil component values using Wang algebra. Bob concluded by summarizing several historical applications and noting several areas of potential use for T-coils in IBIS.

PSEUDO TRANSIENT EYE ANALYSIS BY CONVOLUTION METHOD

Baolong Li (ANSYS, PRC)
[Presented by Daniel Chang (ANSYS, ROC)]

In an additional presentation, Daniel Chang summarized how convolution can be used for both linear and non-linear systems to construct eyes. He also noted how pseudo-transient eyes can closely match SPICE transient eyes using step responses from SPICE simulation, with large increases in efficiency.

Questions from the audience included inquiries about using step responses for PCBs and linear vs. non-linear systems, as a step response assumes balanced or equal rising and falling behaviors. Additionally, an audience member asked about power delivery support. Daniel answered that this method was intended primarily to capture channel ISI.

CONCLUDING ITEMS

Michael Mirmak thanked the co-sponsors, presenters and attendees for their participation and support, and reminded the attendees to register. The meeting adjourned shortly before 5 PM.

NEXT MEETING

The next IBIS Open Forum teleconference will be held December 9, 2011 from 8:00 to 10:00 AM US Pacific Time. Votes on BIRD127.4 and BIRD146 are scheduled.

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NOTES

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This meeting was conducted in accordance with the TechAmerica Legal Guides and TechAmerica Manual of Organization and Procedure.

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In the body, for the IBIS Open Forum Reflector:
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In the body, for the IBIS Users' Group Reflector:
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To join, change, or drop from either or both:
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IBIS Users' Group Reflector (ibis-users@eda.org)
State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the IBIS Open Forum as a full Member.

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To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

<http://www.eda.org/ibis/bugs/ibischk/>
<http://www.eda.org/ibis/bugs/ibischk/bugform.txt>

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

<http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt>
<http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt>
<http://www.eda.org/ibis/bugs/s2iplt/bugspl.txt>

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

<http://www.eda.org/ibis>

Check the IBIS file directory on eda.org for more information on previous discussions and results:

<http://www.eda.org/ibis/directory.html>

To create an account on the TechAmerica KAVI workspace, check out:

<http://workspace.techamerica.org/kwspub/join/>

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IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status				
			October 28, 2011	November 15, 2011	November 18, 2011	November 21, 2011
Advanced Micro Devices	Producer	Active	X	-	X	-
Agilent Technologies	User	Active	X	-	X	-
Altera	Producer	Inactive	-	-	-	-
ANSYS	User	Active	-	X	X	X
Apple Computer	User	Inactive	-	-	-	-
Applied Simulation Technology	User	Inactive	-	-	X	-
Cadence Design Systems	User	Active	X	X	X	X
Cisco Systems	User	Inactive	-	X	-	-
Ericsson	Producer	Active	X	X	X	X
Foxconn Technology Group	Producer	Inactive	-	-	-	X
Freescale	Producer	Inactive	-	-	X	-
Green Streak Programs	General Interest	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	X	-	-
IBM	Producer	Inactive	X	-	-	X
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	-	X	-	X
IO Methodology	User	Active	-	X	-	X
LSI	Producer	Inactive	X	-	-	-
Mentor Graphics	User	Active	X	-	X	-
Micron Technology	Producer	Inactive	X	-	-	-
Nokia Siemens Networks	Producer	Inactive	X	X	-	-
QLogic	Producer	Inactive	-	-	-	-
Signal Integrity Software	User	Inactive	X	-	-	-
Sigrity	User	Inactive	-	X	-	X
Synopsys	User	Inactive	-	X	-	-
Teraspeed Consulting	General Interest	Active	X	X	X	X
Texas Instruments	Producer	Inactive	-	-	-	-
Toshiba	Producer	Inactive	-	-	X	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	X	-	-
Zuken	User	Inactive	-	-	X	-

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH TECHAMERICA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.