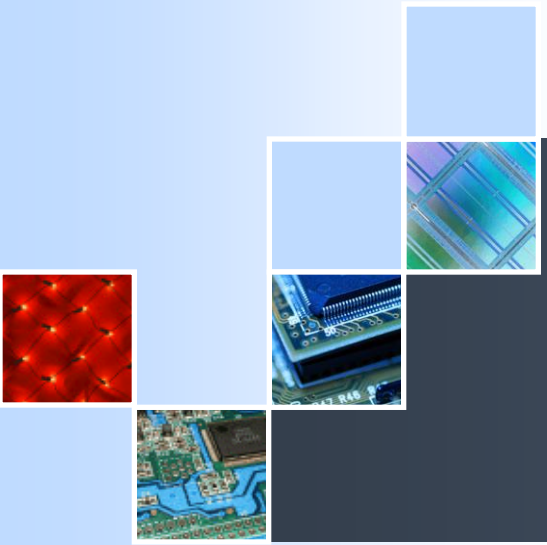

Power-aware I/O Modeling for High-Speed Parallel Bus Simulation

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Taipei Taiwan
November 21, 2011

(Portions previously given at Asian IBIS Summit on November 15, 2011)

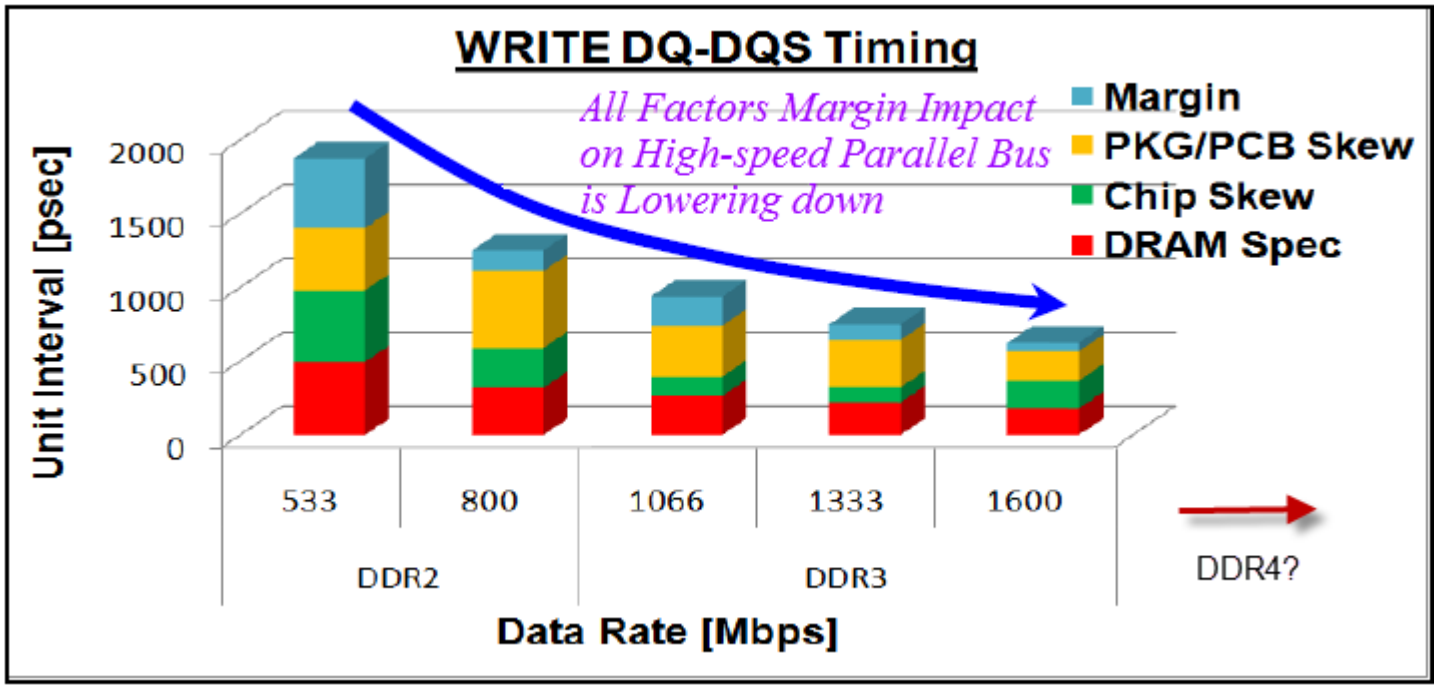
SIGRITY

Outline

- Challenge of High-speed Parallel Bus Simulation
- Necessity of Power-aware Signal Integrity Analysis
  - The Importance of Power-aware Analysis
  - IBIS5.0 Enhancement (BIRD95/BIRD98)
  - Go beyond with IBIS5.0 – IBIS Plus
- Apply Power-aware I/O Model in Parallel Bus SSO Simulation
  - DDR2 System-level SSO Simulation
- Summary

Challenge of High-speed Parallel Bus Simulation

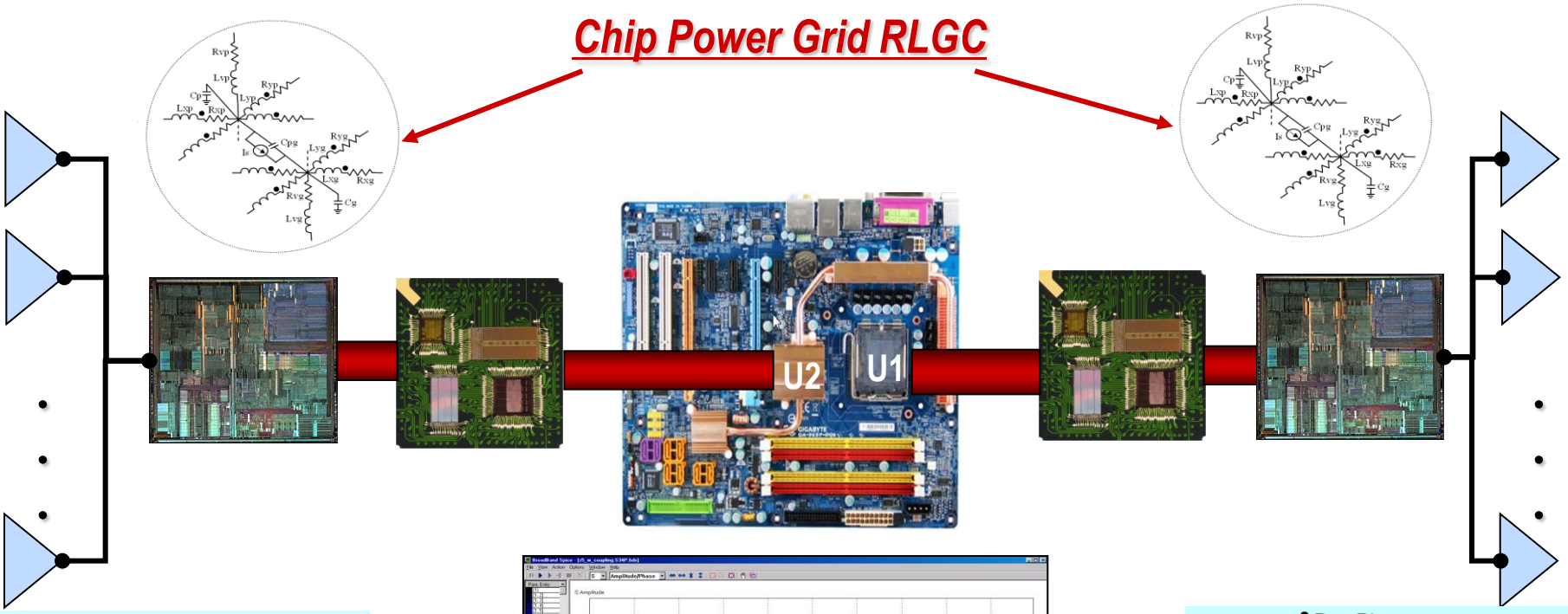
Challenge for High-speed Parallel Bus Design

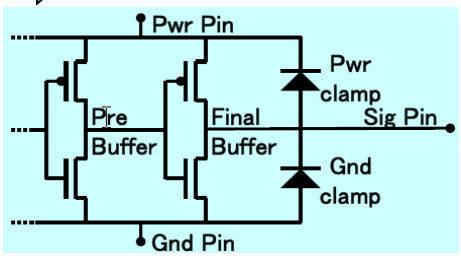


- The margin for jitter/skew is getting smaller in current high-speed parallel bus design
- The power/ground noise has became a dominant reason that causes parallel bus failure
- Power/ground to signal EM coupling should be considered in system level SSO analysis for current high-speed parallel bus timing sign-off

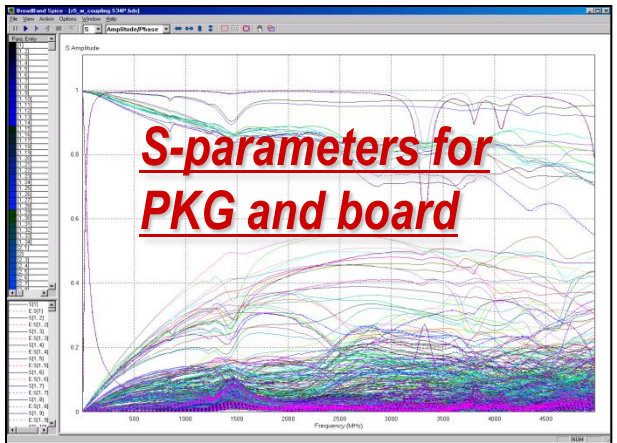
Challenge for High-speed Parallel Bus SSO Simulation

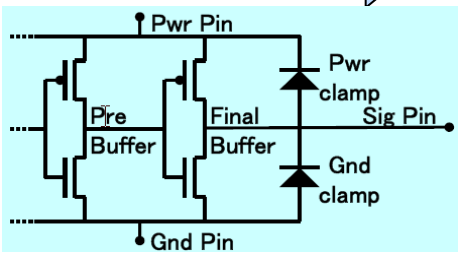
- If this is a 32-bit data SSO analysis, how long will this SPICE DECK run? will the waveform converge?





Transistor model

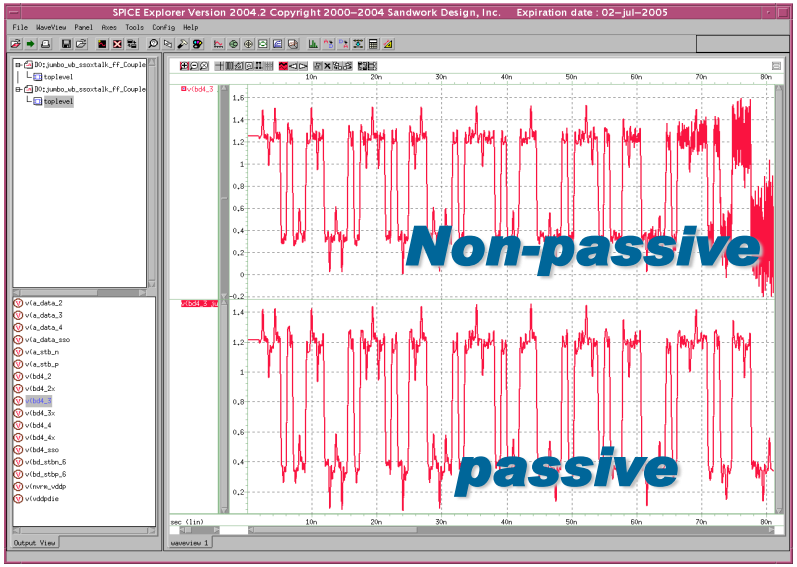




Transistor model

Problems in High-speed Parallel Bus SSO Simulation

- The complex manual task for the node linkages between circuits.
- No guaranteed for passivity and causality on each circuit block especially if model is from measurement
- Non-linearity of the whole system circuit network which includes transistor models of drivers and receivers
- Lost DC accuracy without low frequency data from EM solver, especially for SI analysis with power aware
- Long run time
- Waveforms are non-convergent
- …….

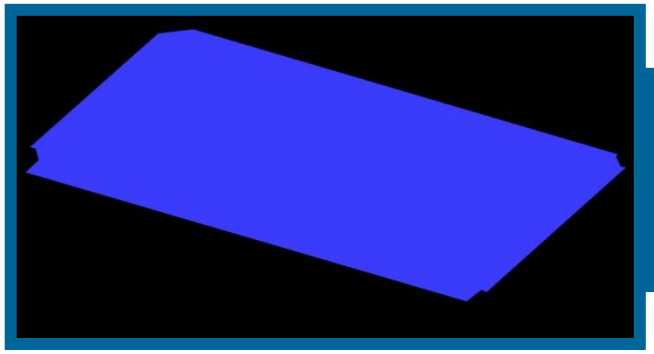


IBIS in SSO Simulation

- IBIS models have in the past addressed nonlinear voltage and current for signals, but not supported proper modeling of power/ground currents
- As frequency of circuit I/O getting higher, SSO simulation in the past with IBIS buffer model that have result be in-accurate and under-estimated
- Most of time, non-convergence issue in SSO simulation can be resolved by replacing buffer model from transistor to IBIS; but getting an accurate result still be a challenge.

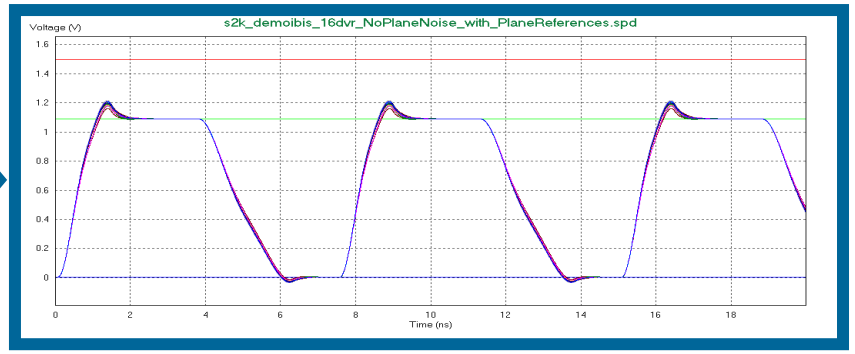
Power-aware I/O Modeling Progress

The Importance of Power-aware Analysis

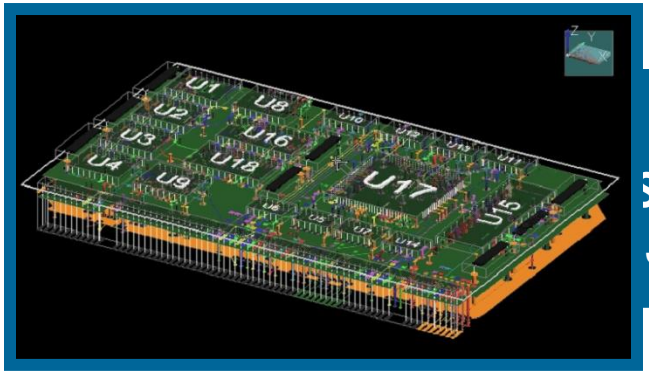


Signal data only

Predicts No SSN

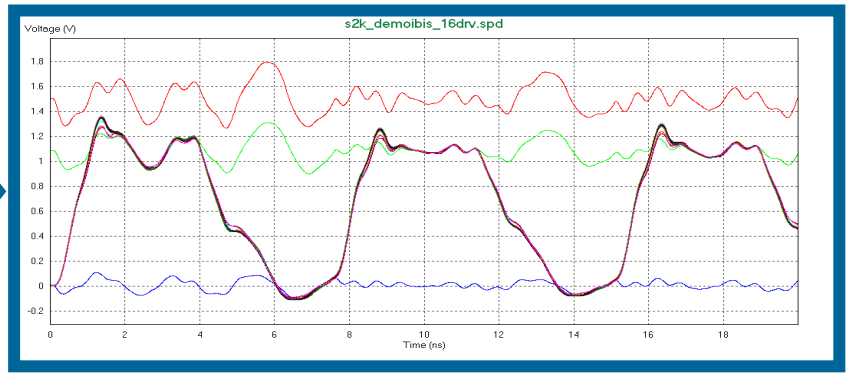


Simulation assuming ideal power delivery network



Signals, accurate planes, vias

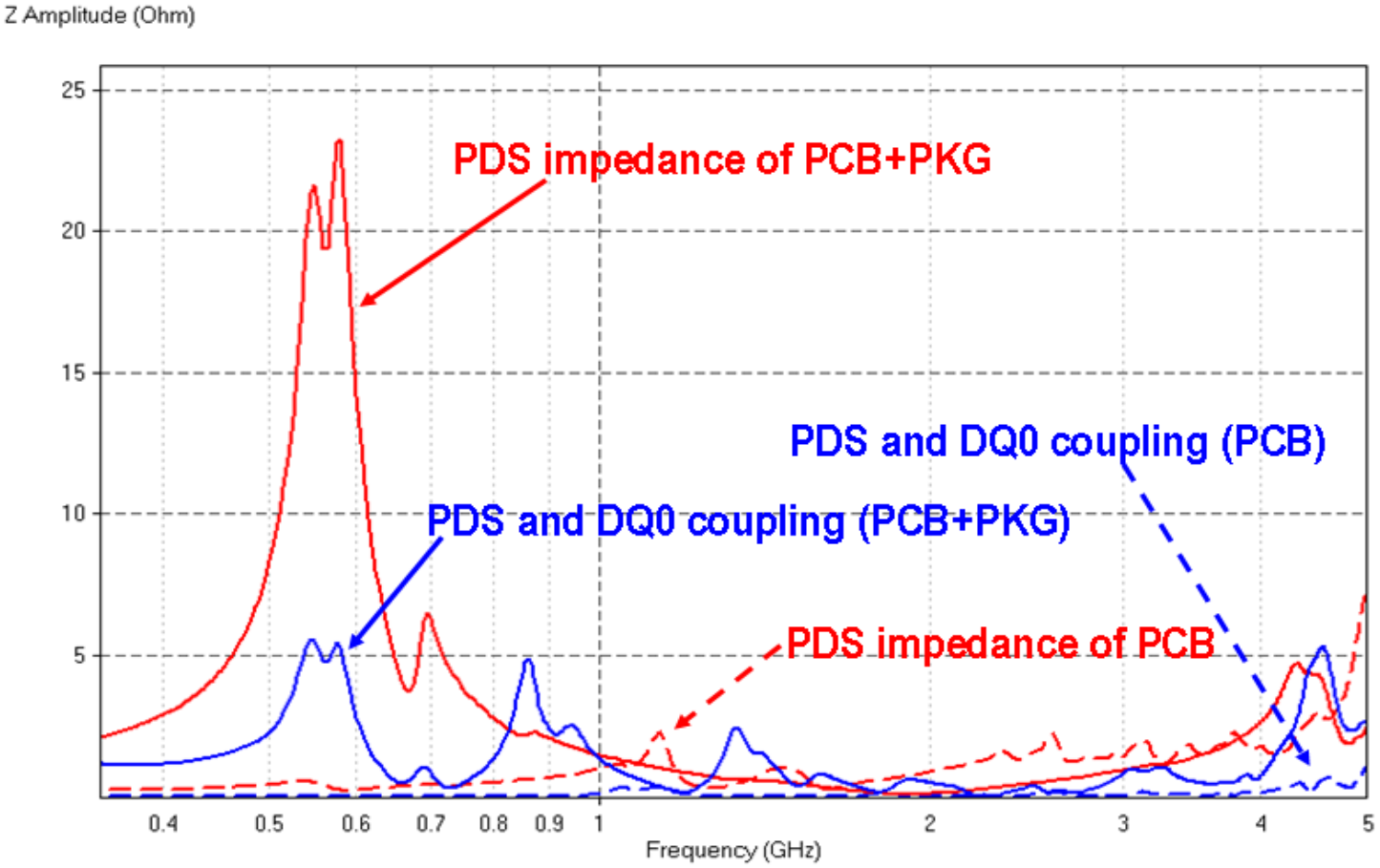
Predicts Significant SSN Risk



Simulation with all power delivery effects

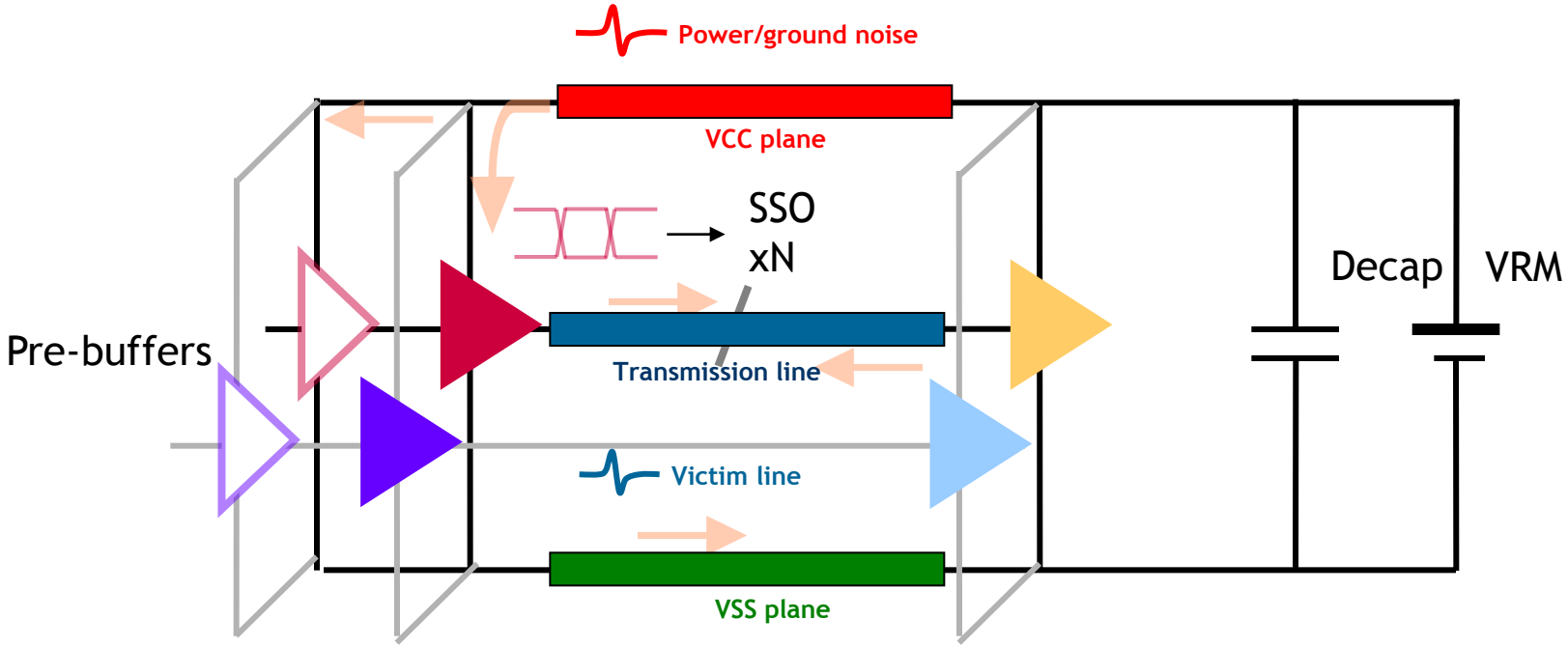
- Transmission line only analysis can't reveal the real signaling among ICs in current high speed parallel bus design.
- High-speed parallel bus with power-aware analysis can help to identify design defects and find out the root cause behind the problem.

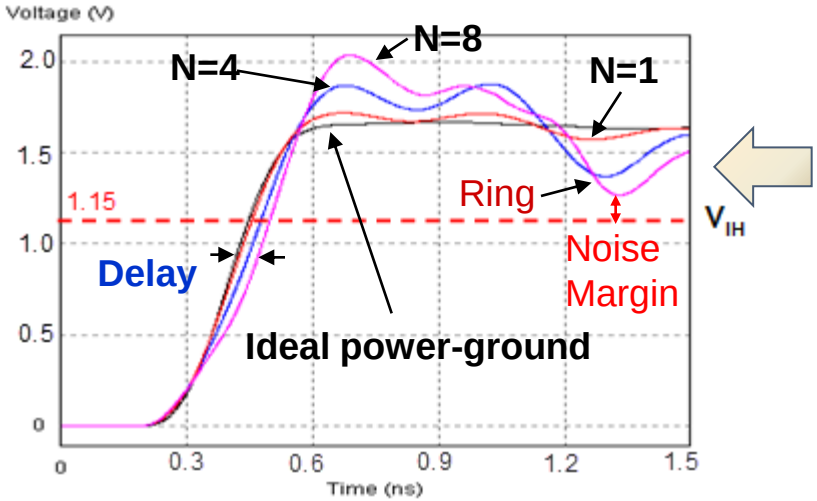
The Importance of Power-aware Analysis



- Signal quality can be significantly affected by PDS resonance in system level.
- Power/ground to signal coupling will be under-estimated with in-accurate IBIS buffer modeling.

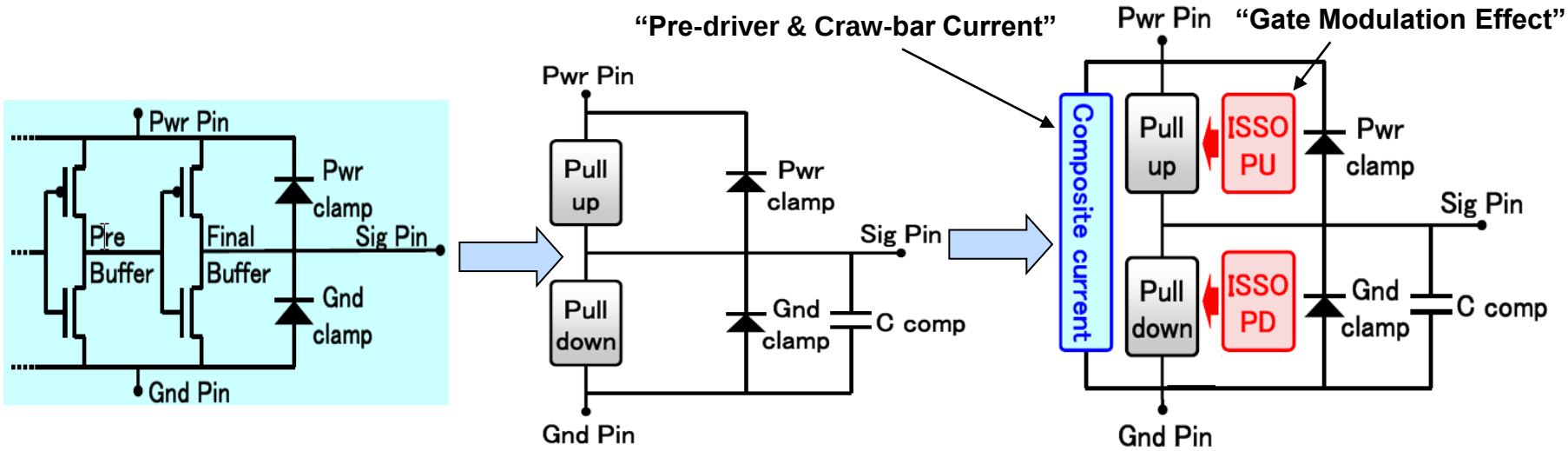
How SSN Noise Impacts Signal Quality



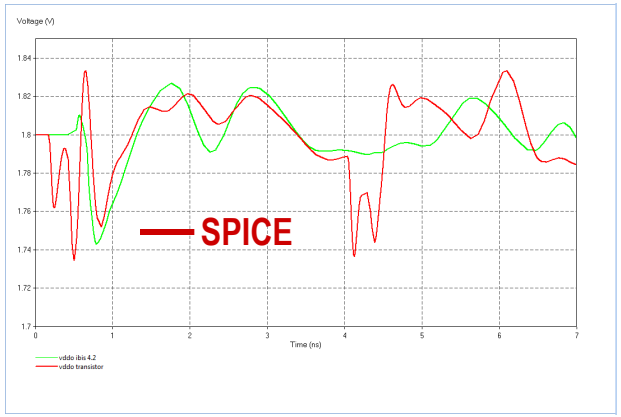


- **SSN noise greatly reduces the noise margin at receiver bump**
- ***SSN noise increases the buffer output delay and finally the jitter, which may cause error-sampling at receiver side***

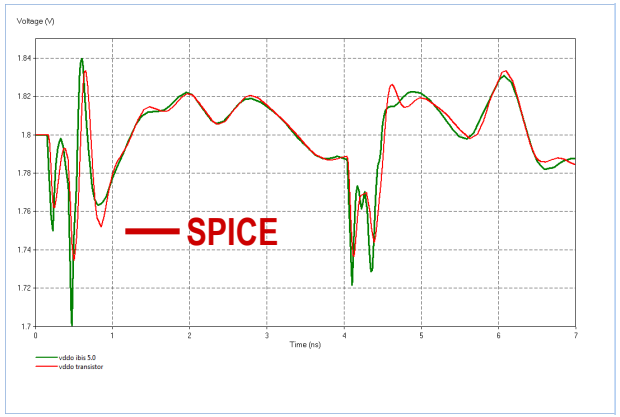
Power-aware Solution in IBIS5.0 (BIRD95/BIRD98)



Accuracy is always a concern when using behavior model. Is it good enough for IBIS5.0?



IBIS4.2 vs. Transistor



IBIS5.0 vs. Transistor

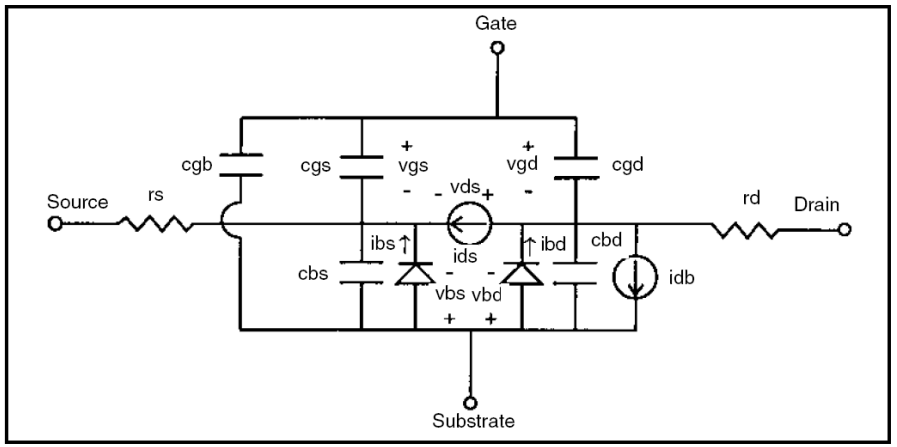
Go Beyond with IBIS5.0

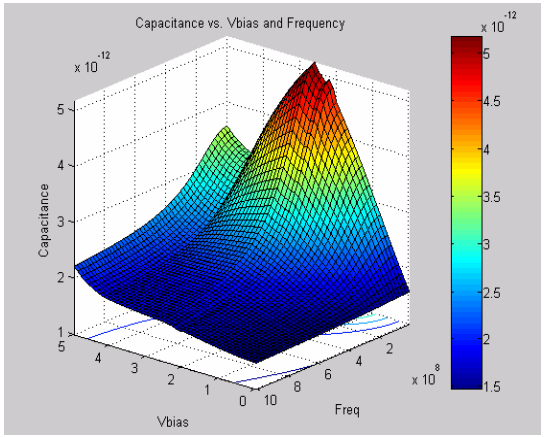
Advantage

- IBIS5.0 is designed for more accurate SI simulation with non-ideal power distribution system (PDS)
- IBIS5.0 greatly improve the correlation accuracy with transistor model with simple but effective methodology
  - By including composite current, more accurate power noise simulation can be performed to have better power/signal integrity evaluation
  - Dynamic power noise impact on signal output waveform is considered in IBIS5.0, which greatly improve the efficiency of using IBIS model in high-speed parallel bus timing sign-off

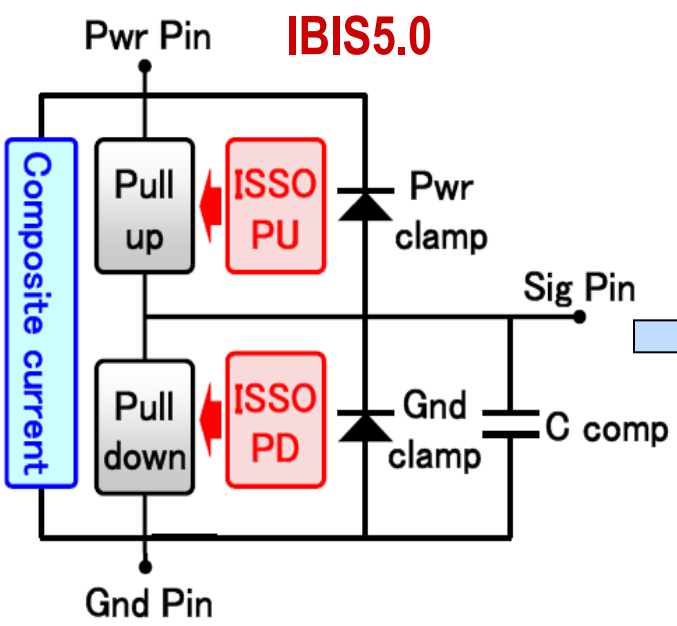
But it's good enough?

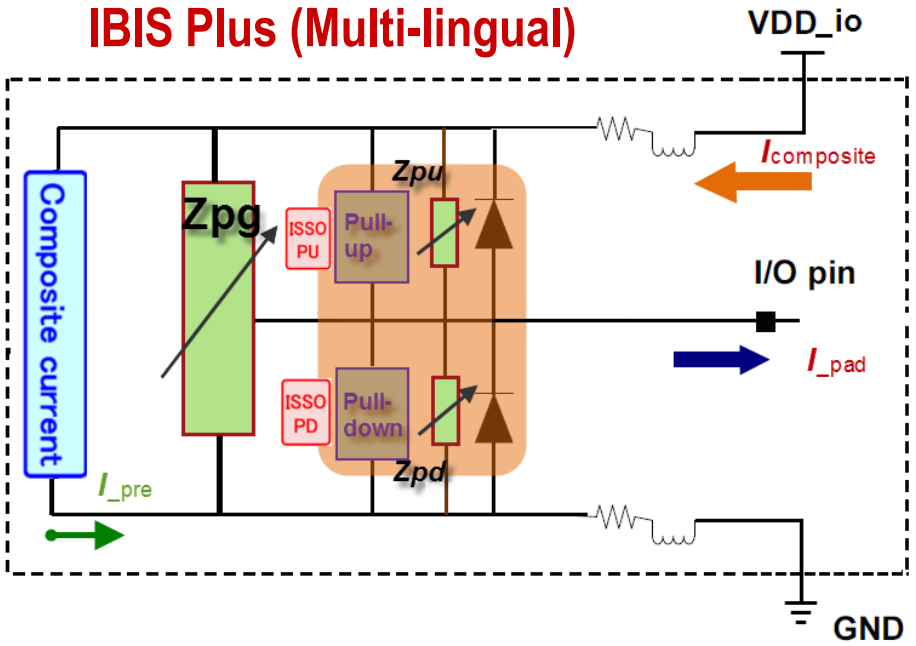
- On-die power/ground impedance is omitted
- The state-dependent non-linear output impedance is modeled with single or split die capacitance, which may over- or under-estimate the buffer AC effects

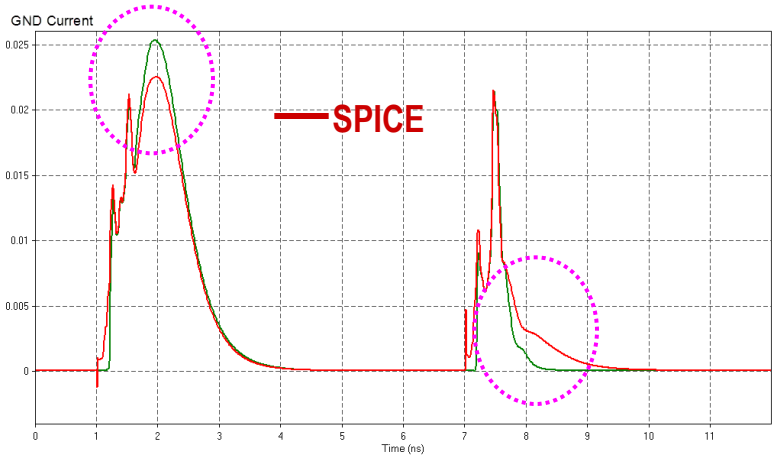




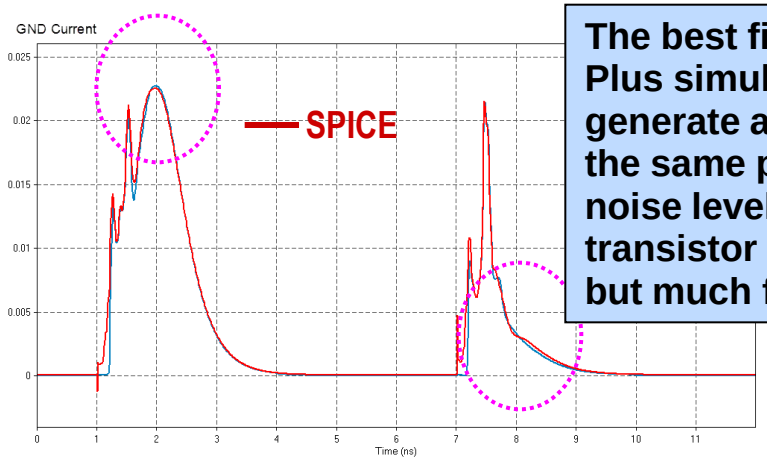
Go Beyond with IBIS5.0







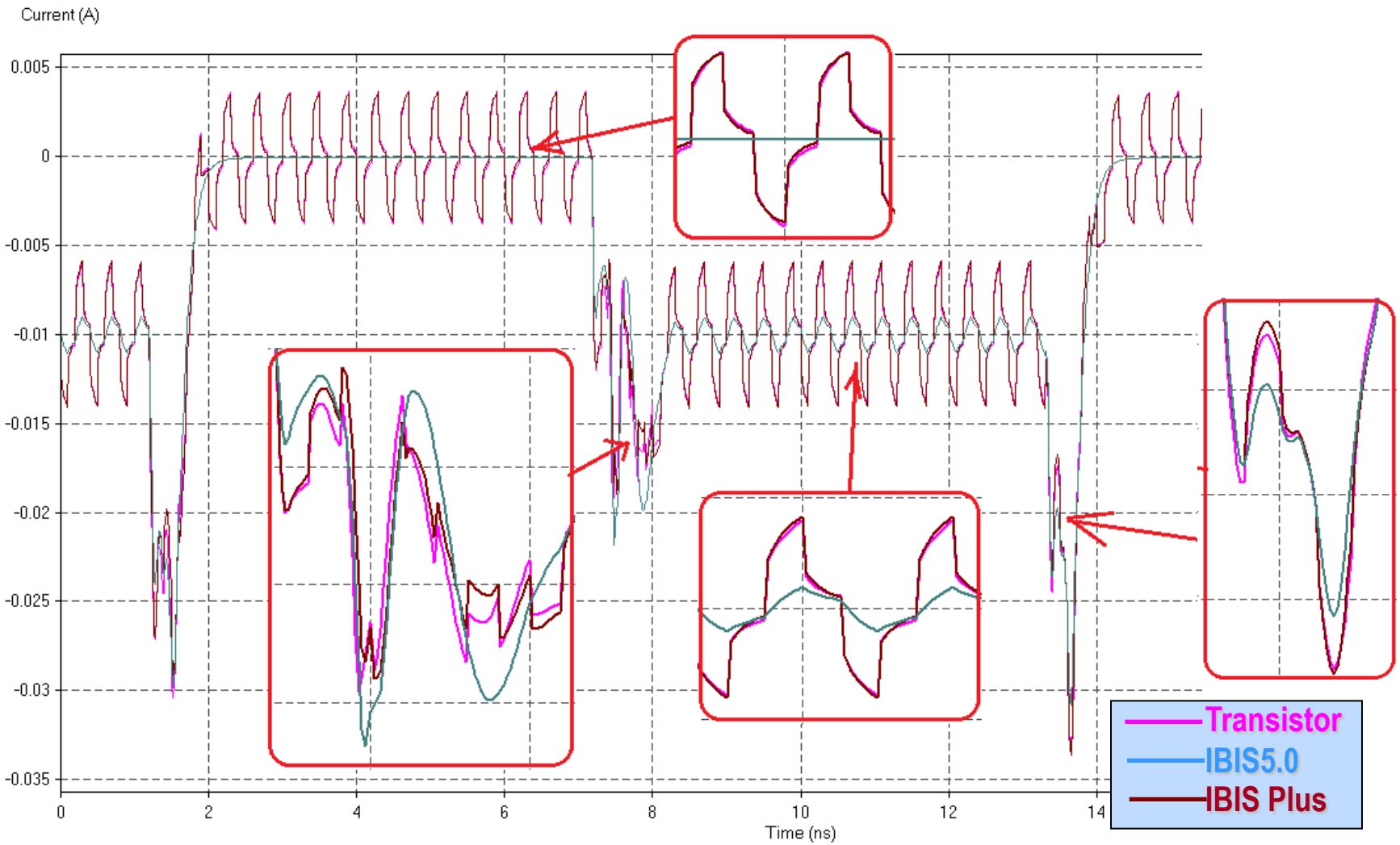
IBIS5.0 vs. Transistor



IBIS Plus vs. Transistor

The best fitted IBIS Plus simulation generate almost the same power noise level with transistor model but much faster

Go Beyond with IBIS5.0 (case study)

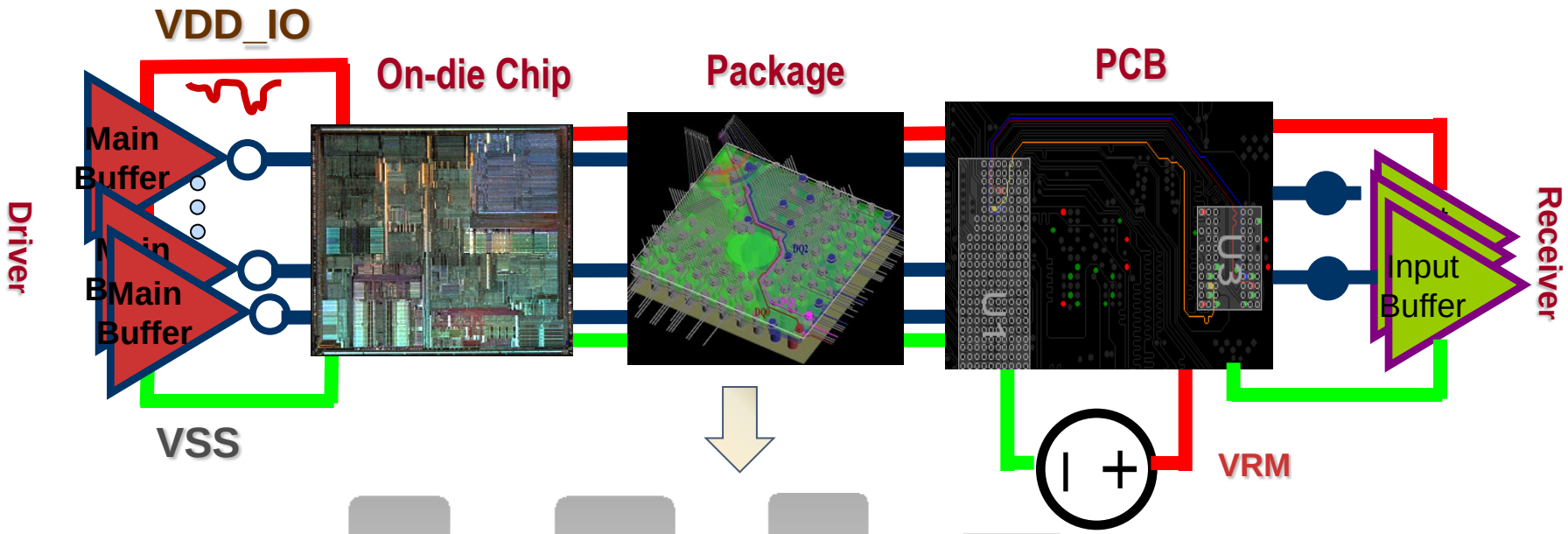


* *HSTL18 I/O, 150 Ohm termination in parallel with 1pF*

VCC=1.8V, 0.05V 2.5GHz AC noise

High-speed Parallel Bus SSO Simulation

DDR2 System-level SSO Simulation (case study)

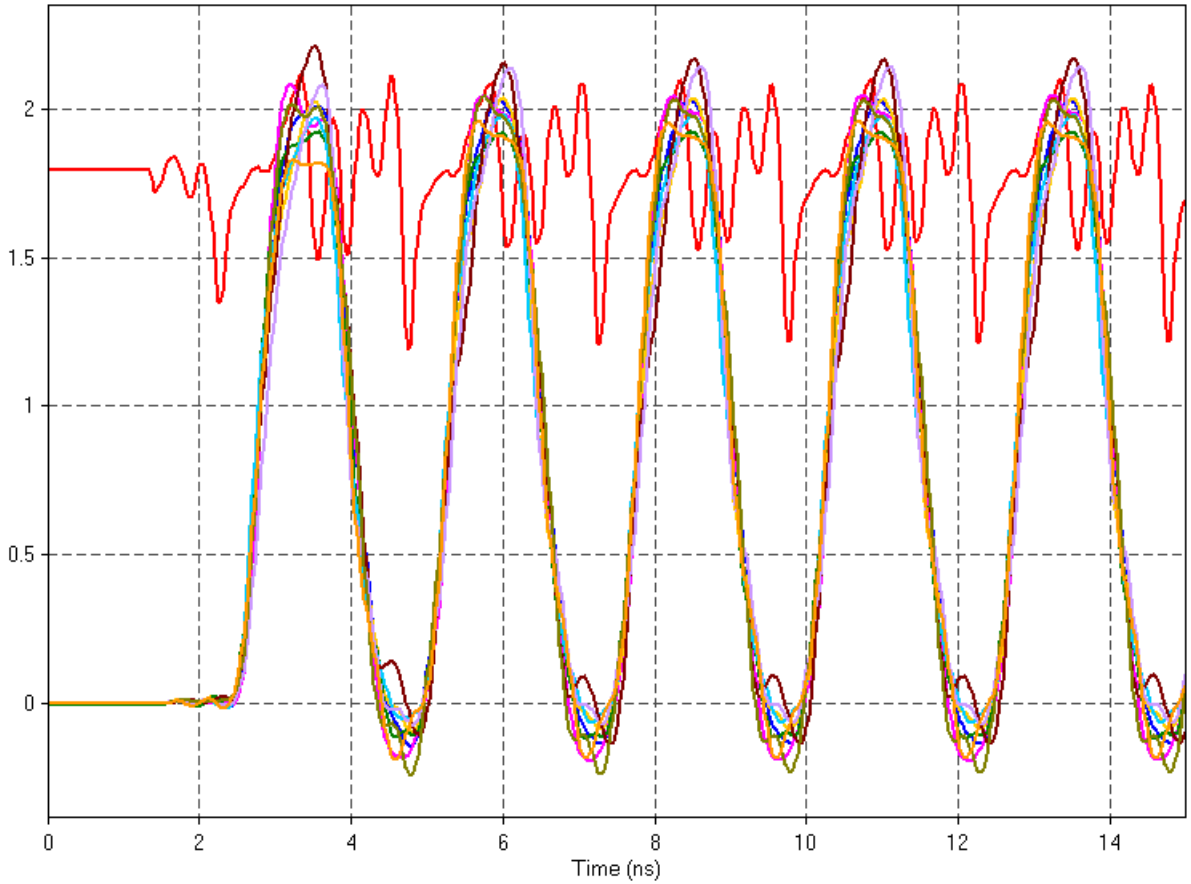


- Package, board and on-die power grid model are considered in system-level view
- On-die power grid chip model is extracted in distributed format with all MOS caps included

- Non-ideal power/ground noise is accurately predicted by use of IBIS 5.0 buffer model
- To improve the convergence for time domain analysis, broadband PKG/board S-parameter model are converted into broadband SPICE circuit

DDR2 System-level SSO Simulation (case study)

Noise Measured at CTL side



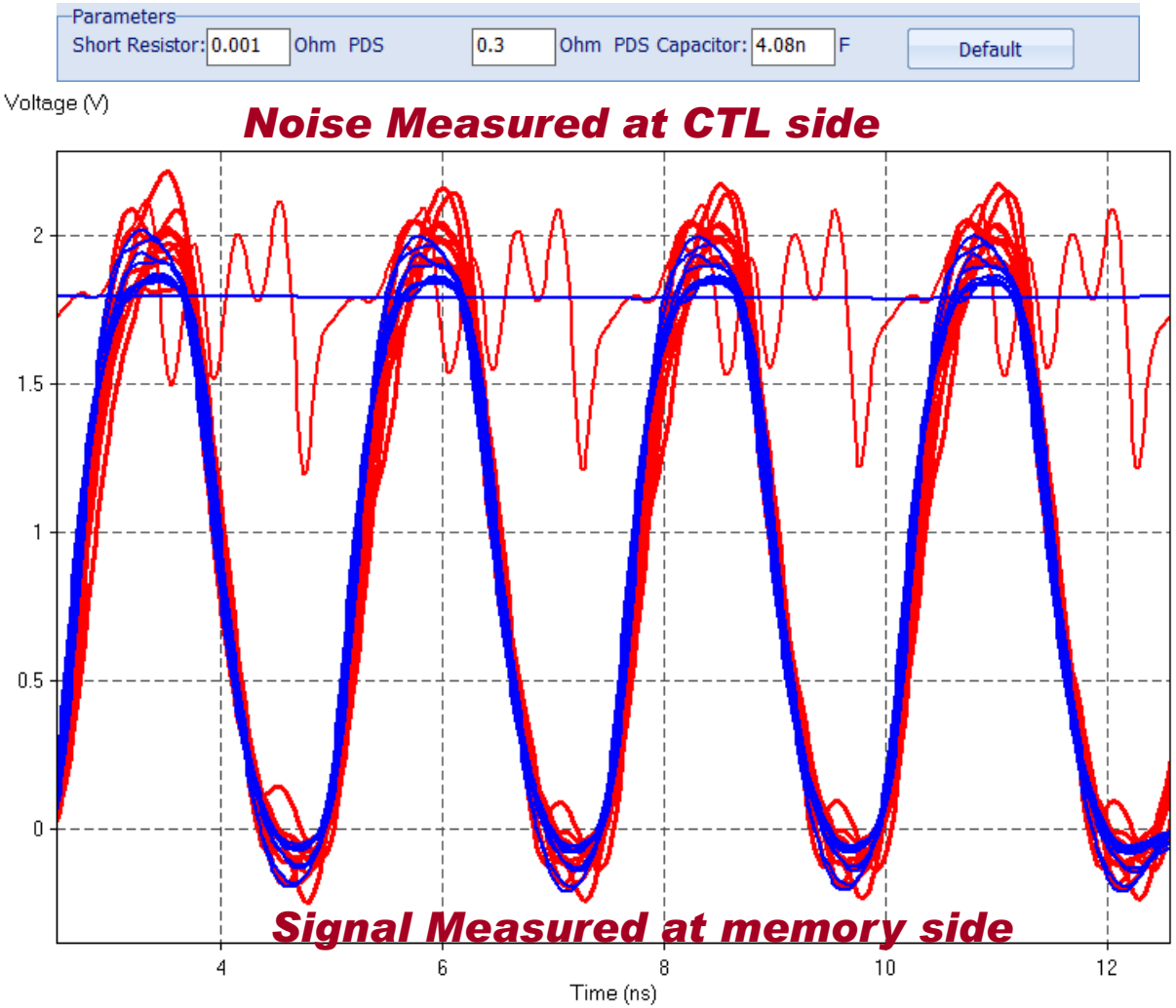
Signal Measured at memory side

① One memory byte SSO study with 800Mbps data rate

② Package and board are considered only

③ Without chip equivalent model and on-die decaps that leads to larger power /ground noise at CTL side

DDR2 System-level SSO Simulation (case study)



Red: without on-die lump model

Blue: with on-die lump model

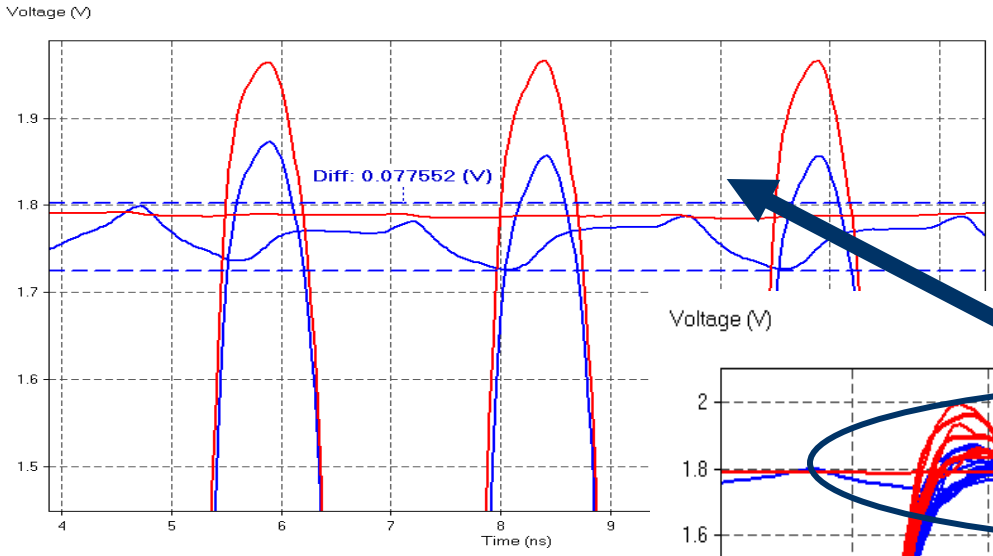
① Add on-die decaps from I/O circuit information

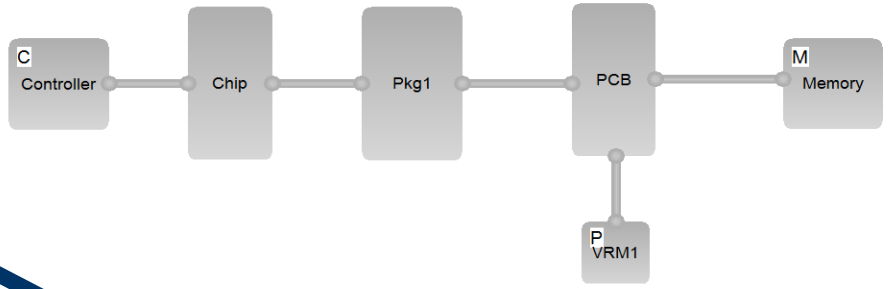
② On-die decap is lump on die-power and ground pins.

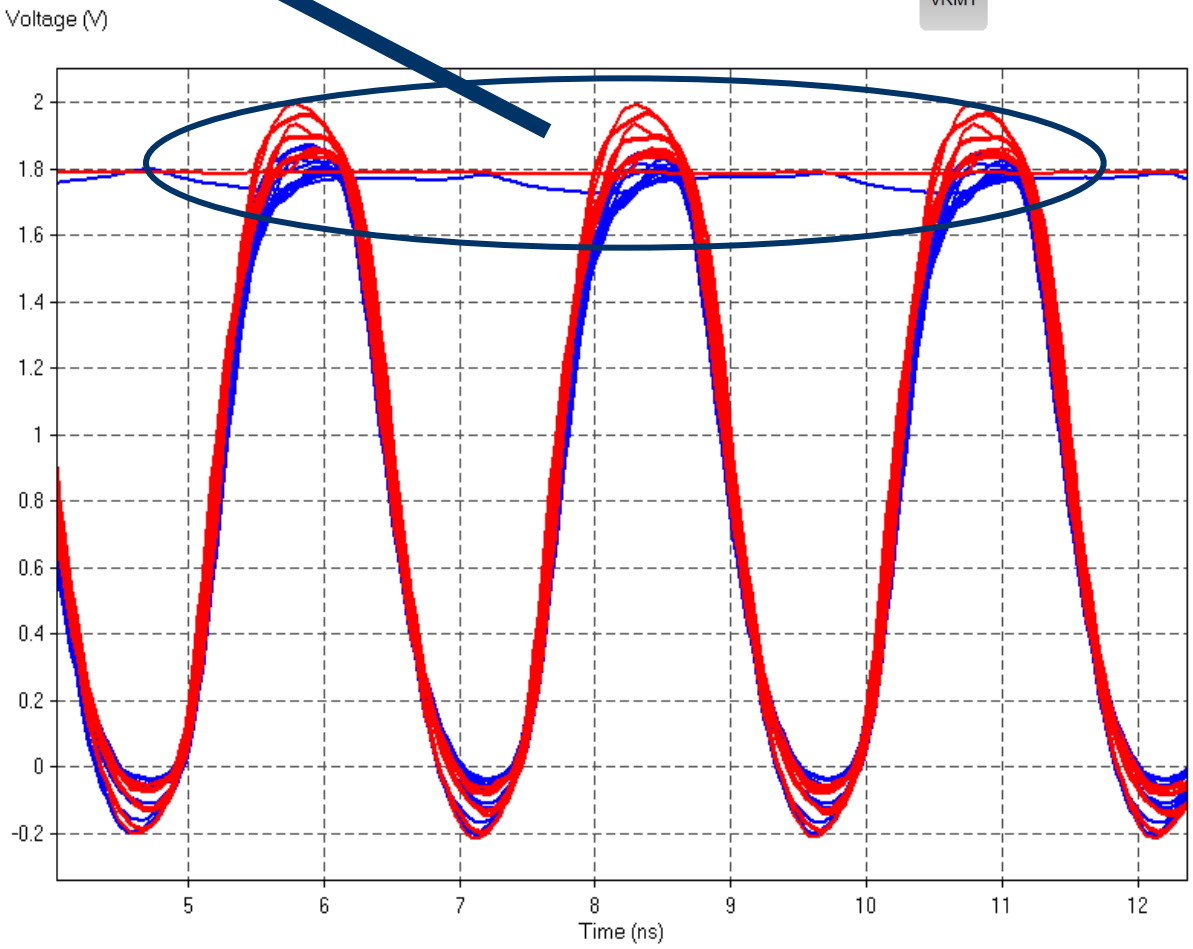
③ Lump on-die decap model can't reveal real chip PDS behavior and it acts like an AC short on chip PDS and make less P/G fluctuation

④ Incorrect on-die circuit will lead to over/under assessment on PDN noise

DDR2 System-level SSO Simulation (case study)



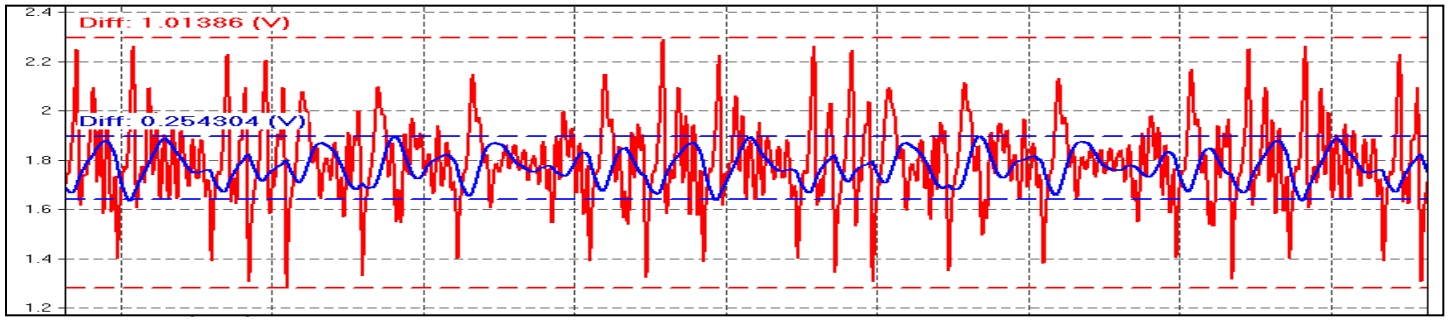


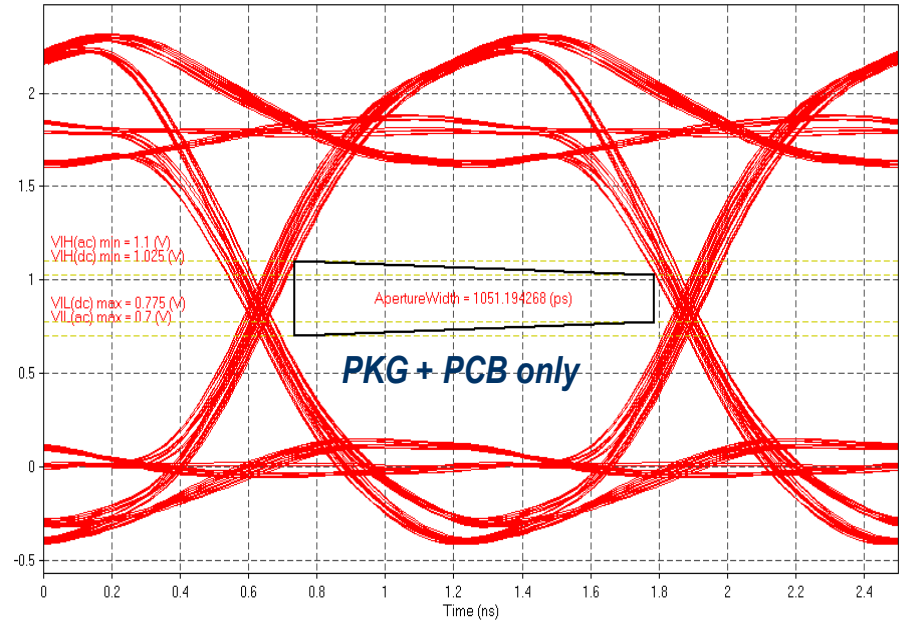


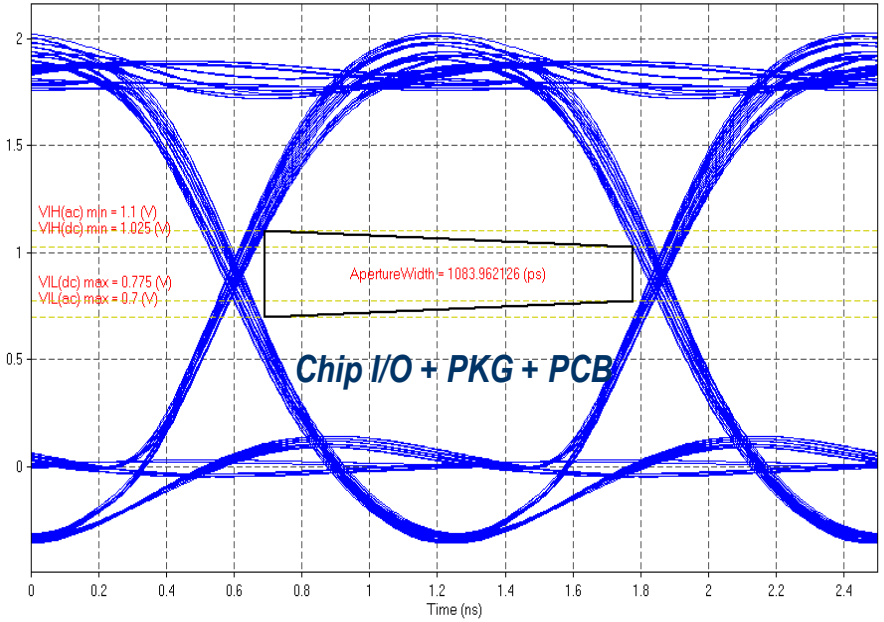
① Chip I/O P/G grids with on-die decaps are extracted from chip level extraction tool.

② MOS caps around the I/O are not common shared with all I/O circuits

DDR2 System-level SSO Simulation (case study)







- Power/ground noise has dramatically reduced in system level SSO simulation.
- Aperture width and jitter are improved

Summary

- Current high-speed parallel-bus and serial-link SI analysis require power-aware I/O model to run accurate SI analysis
- Latest IBIS5.0 improve on power-aware I/O buffer modeling can be an alternative for a complex system-level SSO simulation
- Demonstrate a new method to generate a more accurate behavioral circuit model (IBIS Plus) based on frequency-domain response fitting that can be delivered in an IBIS compatible multi-lingual external model
- Block-level system-level simulation automation tool eases the simulation platform setup
- Need to expand the buffer modeling technology to differential (true/half) I/O and more complex I/O designs

Thank You!