Supporting External circuit as Spice or S-parameters in conjunction with I-V/V-T tables

Kent Dramstad, Adge Hawes
IBM Microelectronics

Taranjit Kukal, Feras Al-Hawari, Ambrish Varma, Terry Jernberg
Cadence Design Systems, Inc.

Presented by: Charlie Shih, Cadence Design Systems, Inc.
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Agenda

- **Requirement**
- **Current Limitations of [External Circuit]**
- **Solution**
  - **Supporting S-parameters in [External Circuit] (BIRD144)**
  - **Simulating [External Circuit] in conjunction with I-V/V-T tables (BIRD145)**
- **Summary**

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Agenda

- **Requirement**
- Current Limitations of [External Circuit]
- Solution
  - Supporting S-parameters in [External Circuit]
  - Simulating [External Circuit] in conjunction with I-V/V-T tables
- Summary

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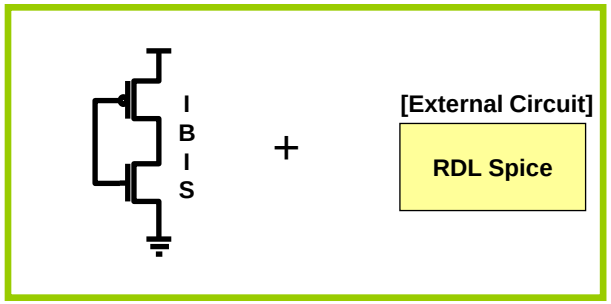
Requirement

- **At high frequencies, we need ways over and above I-V, V-T tables and AMI to model the buffer.**
  - On DIE Terminations (ODT) that vary with frequencies need to be expressed as S-parameters or RLGC Spice files
  - On DIE Re-distribution layer (RDL) parasitics become significant and vary with frequencies and hence have to be expressed as S-parameters
  - Analog portion of IO-buffer get expressed as Spice as against I-V/V-T curve; S-parameters get used to describe transfer characteristics of linear IO-buffer amplifiers.

Requirement

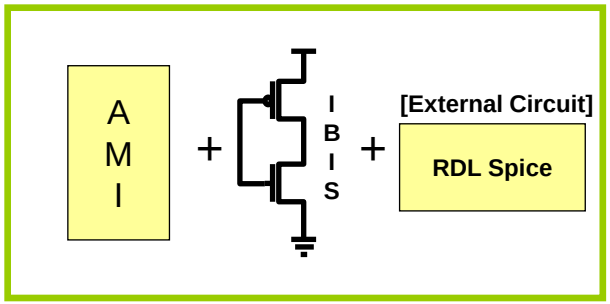
- **At high frequencies, we need ways over and above I-V, V-T tables and AMI to model the buffer.**
  - Some algorithmic portion of IO-buffer model could be expressed as behavioral Spice to augment AMI code
    - Example: ‘if-then-else kind of spice’ to pick right sub-circuit based on parameter values/processes
    - Example: Modeling continuous filters as behavioral spice to augment digital filters in AMI code

Requirement
- Various Cases that need to be covered



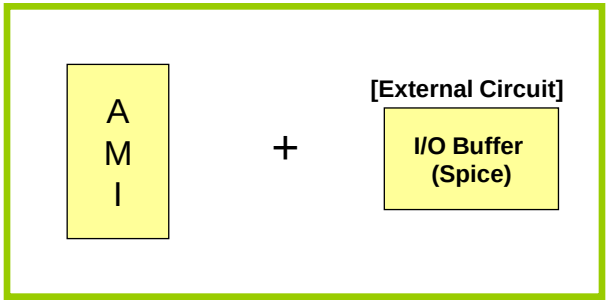
Simulating RDL parasitics in conjunction with I-V/V-T tables

Case 1



Simulating RDL parasitics in conjunction with I-V/V-T tables and AMI

Case 2



Simulating AMI with IO-buffer expressed as Spice

Case 3

Agenda

- Requirement
- **Current Limitations of [External Circuit]**
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  - Supporting S-parameters in [External Circuit]
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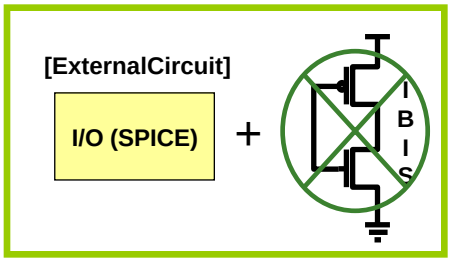
Current Limitations - [External Circuit]

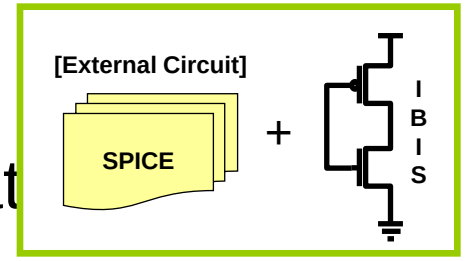
- Today, S-parameters have to be wrapped into Spice models (vendor specific) and then used under [External Model/Circuit] Keyword.
  - On similar lines, BIRDs 116-118 propose that Touchstone file name can be parameterized for the IBIS-ISS sub-circuit, which means that IBIS-ISS wrapper could be written for the S-parameter element.
- **NEED**: Extend support for direct usage of S-parameters

Current Limitations - [External Circuit]

- The current [External Circuit] and [Circuit Call] usage rules do not allow the direct interconnection and instantiation of existing IBIS I/O models with the rest of the [External Circuit] blocks. Traditionally, users either use Spice or I-V/V-T tables.



- **NEED**: Extend use of [External Circuit] keyword to point to Spice sub-circuits that augment I-V/V-T data for complete characterization of IO-buffer.



Current Limitations - [External Circuit]

- In order for a model developer to use an IBIS I/O model in an [External Circuit] the following steps need to be followed:
  - Develop SPICE like wrappers in which the corresponding typ, min, and max IBIS I/O sub-circuits are instantiated
  - Develop an [External Circuit] to point to the wrapper sub-circuits
  - Use the [Circuit Call] keyword to call the [External Circuit].
- These usage rules are cumbersome especially when the developer can just directly call the desired IBIS I/O model without the need to develop a SPICE like wrapper as well as an [External Circuit] section.

Agenda

- Requirement
- Current Limitations of [External Circuit]
- **Solution**
  - **Supporting S-parameters in [External Circuit] (BIRD144)**
  - Simulating [External Circuit] in conjunction with I-V/V-T tables
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Solution: Leveraging [External Model/Circuit] to Support Package S-parameters

- For support of package S-parameters:
  - IBIS model should have Keywords to support Touchstone S-parameters under Package section, with fields to
    - Point to Touchstone file from the Package section
    - Provide port-mapping of IO-buffer pins to S-parameter ports
    - R/L/C values should be ignored by SI tools if S-parameter file is used
- For support of S-parameters when representing elements beyond package parasitics: This can be achieved through use of [External Model] keyword that directly instantiates Touchstone file

Solution: Leveraging [External Model/Circuit] to Support S-parameters (beyond Package)

- Positioning S-parameters as a method to completely define IO-buffer model or portions of IO-buffer requires support for:
  - Direct support of S-parameters without the need for wrapping
  - Port mapping of S-parameters
  - Corners beyond typ/min/max to provide flexibility of choosing various S-parameter files under different conditions

Solution: Leveraging [External Model/Circuit] to Support S-parameters (beyond Package)

- Support for Language 'Touchstone' with port-map

```
|-----------------------------------------------------------------
| Example of True Differential [External Model] using TOUCHSTONE:
|-----------------------------------------------------------------
|
[Model] Ext_TOUCHSTONE,_Diff_Buff
Model_type I/O_diff
Rref_diff = 100
|
| Other model subparameters are optional
|
                    typ      min      max
[Voltage Range]     3.3      3.0      3.6
|
[Ramp]
dV/dt_r          1.57/0.36n    1.44/0.57n    1.73/0.28n
dV/dt_f          1.57/0.35n    1.46/0.44n    1.68/0.28n
|
[External Model]
Language TOUCHSTONE
|
| Corner corner_name file_name    circuit_name (.subckt name)
Corner     Typ          diffio.s8p   NA
Corner     Min          diffio.s8p   NA
Corner     Max          diffio.s8p   NA
|
| Ports List of port names (in same order as in TOUCHSTONE)
Ports A_signal_pos A_signal_neg my_receive my_drive my_enable
Ports A_puref A_pdref A_pcref A_gcref A_extref my_ref A_gnd
|
| D_to_A d_port    port1       port2     vlow vhigh trise tfall corner_name
D_to_A     D_drive   my_drive    my_ref     0.0   3.3    0.5n   0.3n   Typ
D_to_A     D_drive   my_drive    my_ref     0.0   3.0    0.6n   0.3n   Min
D_to_A     D_drive   my_drive    my_ref     0.0   3.6    0.4n   0.3n   Max
D_to_A     D_enable  my_enable   my_ref     0.0   3.3    0.5n   0.3n   Typ
D_to_A     D_enable  my_enable   my_ref     0.0   3.0    0.6n   0.3n   Min
D_to_A     D_enable  my_enable   my_ref     0.0   3.6    0.4n   0.3n   Max
|
| A_to_D d_port      port1          port2          vlow    vhigh corner_name
A_to_D     D_receive  A_signal_pos   A_signal_neg   -200m   200m   Typ
A_to_D     D_receive  A_signal_pos   A_signal_neg   -200m   200m   Min
A_to_D     D_receive  A_signal_pos   A_signal_neg   -200m   200m   Max
|
[End External Model]
```

Solution: Leveraging [External Model/Circuit] to Support S-parameters (beyond Package)

- Picking different S-parameter files for different corners

```
|-------------------------------------------------------------------
| Example of True Differential [External Model] using TOUCHSTONE:
|-------------------------------------------------------------------
|
[Model] Ext_TOUCHSTONE,_Diff_Buff
Model_type I/O_diff
Rref_diff = 100
|
| Other model subparameters are optional
|
                    typ      min      max
[Voltage Range]     3.3      3.0      3.6
|
[Ramp]
dV/dt_r          1.57/0.36n    1.44/0.57n    1.73/0.28n
dV/dt_f          1.57/0.35n    1.46/0.44n    1.68/0.28n
|
[External Model]
Language TOUCHSTONE
|
| Corner corner_name file_name    circuit_name (.subckt name)
Corner     Typ           diffio.s8p   NA
Corner     Min           diffio.s8p   NA
Corner     Max           diffio.s8p   NA
|
| Ports List of port names (in same order as in TOUCHSTONE)
Ports A_signal_pos A_signal_neg my_receive my_drive my_enable
Ports A_puref A_pdref A_pcref A_gcref A_extref my_ref A_gnd
|
| D_to_A d_port    port1       port2     vlow vhigh trise tfall corner_name
D_to_A     D_drive   my_drive    my_ref     0.0   3.3    0.5n   0.3n   Typ
D_to_A     D_drive   my_drive    my_ref     0.0   3.0    0.6n   0.3n   Min
D_to_A     D_drive   my_drive    my_ref     0.0   3.6    0.4n   0.3n   Max
D_to_A     D_enable  my_enable   my_ref     0.0   3.3    0.5n   0.3n   Typ
D_to_A     D_enable  my_enable   my_ref     0.0   3.0    0.6n   0.3n   Min
D_to_A     D_enable  my_enable   my_ref     0.0   3.6    0.4n   0.3n   Max
|
| A_to_D d_port      port1          port2          vlow    vhigh corner_name
A_to_D     D_receive  A_signal_pos   A_signal_neg   -200m   200m   Typ
A_to_D     D_receive  A_signal_pos   A_signal_neg   -200m   200m   Min
A_to_D     D_receive  A_signal_pos   A_signal_neg   -200m   200m   Max
|
[End External Model]
```

Solution: Leveraging [External Model/Circuit] to Support S-parameters (beyond Package)

- Supporting user-defined corners – each user-defined corner maps to typ/min/max IBIS corners

```
|-----------------------------------------------------------------
| Example [External Model] using TOUCHSTONE with 2 userdef corners:
|-----------------------------------------------------------------
|
[Model] ExLinearBufferTouchstoneWithTwoUserDefCorners
Model_type Output
|
| Other model subparameters are optional
|
|                  typ      min      max
[Voltage Range]    3.3      3.0      3.6
|
[Ramp]
dV/dt_r         1.57/0.36n   1.44/0.57n   1.73/0.28n
dV/dt_f         1.57/0.35n   1.46/0.44n   1.68/0.28n
|
[External Model]
Language TOUCHSTONE
|
| Corner corner_name file_name          circuit_name
Corner     Typ          buffer_typ.s2p    NA
Corner     Min          buffer_min.s2p    NA
Corner     Max          buffer_max.s2p    NA
|
| Parameters List of parameters
Parameters MinNumber MaxNumber
|
| User_defined_corner user_defined_corner_name parameter_name parameter_value file_name corner_name
User_defined_corner     Min1     MinNumber    1     buffer_min1.s2p  Min
User_defined_corner     Max1     MaxNumber    1     buffer_max1.s2p  Max
|
```

Solution: Leveraging [External Model/Circuit] to Support S-parameters (beyond Package)

- Use in [External Model] and [External Circuit]

```
|-----------------------------------------
| Example [External Model] using TOUCHSTONE:
|-----------------------------------------
|
[Model] ExBufferTOUCHSTONE
Model_type I/O
Vinh = 2.0
Vinl = 0.8
|
| Other model subparameters are optional
|
                  typ      min     max
[Voltage Range]   3.3      3.0     3.6
|
[Ramp]
dV/dt_r         1.57/0.36n   1.44/0.57n   1.73/0.28n
dV/dt_f         1.57/0.35n   1.46/0.44n   1.68/0.28n
|
[External Model]
Language TOUCHSTONE
|
| Corner corner_name file_name       circuit_name (.subckt
Corner    Typ          buffer_typ.s7p  NA
Corner    Min          buffer_min.s7p  NA
Corner    Max          buffer_max.s7p  NA
|
| Ports List of port names (in same order as in TOUCHSTONE)
Ports A_signal my_drive my_enable my_receive my_ref
Ports A_puref A_pdref A_pcref A_gcref A_extref
|
| D_to_A d_port   port1     port2    vlow vhigh trise tfall
D_to_A   D_drive  my_drive   my_ref   0.0  3.3   0.5n  0.3n
D_to_A   D_enable my_enable  A_gcref  0.0  3.3   0.5n  0.3n
|
| A_to_D d_port    port1       port2       vlow  vhigh  corner_name
A_to_D   D_receive  my_receive  my_ref  0.8   2.0    Typ
|
| Note: A_signal might also be used instead of a user-defined interface port
| for measurements taken at the die pads
|
[End External Model]|
|
```

```
|-----------------------------------------
| Example [External Circuit] using TOUCHSTONE:
|-----------------------------------------
|
[External Circuit] BUFF-TOUCHSTONE
Language TOUCHSTONE
|
| Corner corner_name file_name       circuit_name (.subckt name)
Corner    Typ          buffer_typ.s9p  NA
Corner    Min          buffer_min.s9p  NA
Corner    Max          buffer_max.s9p  NA
|
| Ports List of port names (in same order as in TOUCHSTONE)
Ports A_signal int_in int_en int_out A_control
Ports A_puref A_pdref A_pcref A_gcref
|
| D_to_A d_port   port1   port2    vlow vhigh trise tfall corner_name
D_to_A   D_drive  int_in  my_gcref 0.0  3.3   0.5n  0.3n  Typ
D_to_A   D_drive  int_in  my_gcref 0.0  3.0   0.6n  0.3n  Min
D_to_A   D_drive  int_in  my_gcref 0.0  3.6   0.4n  0.3n  Max
D_to_A   D_enable int_en  my_gnd   0.0  3.3   0.5n  0.3n  Typ
D_to_A   D_enable int_en  my_gnd   0.0  3.0   0.6n  0.3n  Min
D_to_A   D_enable int_en  my_gnd   0.0  3.6   0.4n  0.3n  Max
|
| A_to_D d_port     port1     port2     vlow vhigh corner_name
A_to_D   D_receive  int_out   my_gcref  0.8  2.0   Typ
A_to_D   D_receive  int_out   my_gcref  0.8  2.0   Min
A_to_D   D_receive  int_out   my_gcref  0.8  2.0   Max
|
[End External Circuit]
```

Agenda

- Requirement
- Current Limitations of [External Circuit]
- **Solution**
  - Supporting S-parameters in [External Circuit]
  - **Simulating [External Circuit] in conjunction with I-V/V-T tables(BIRD145)**
- Summary

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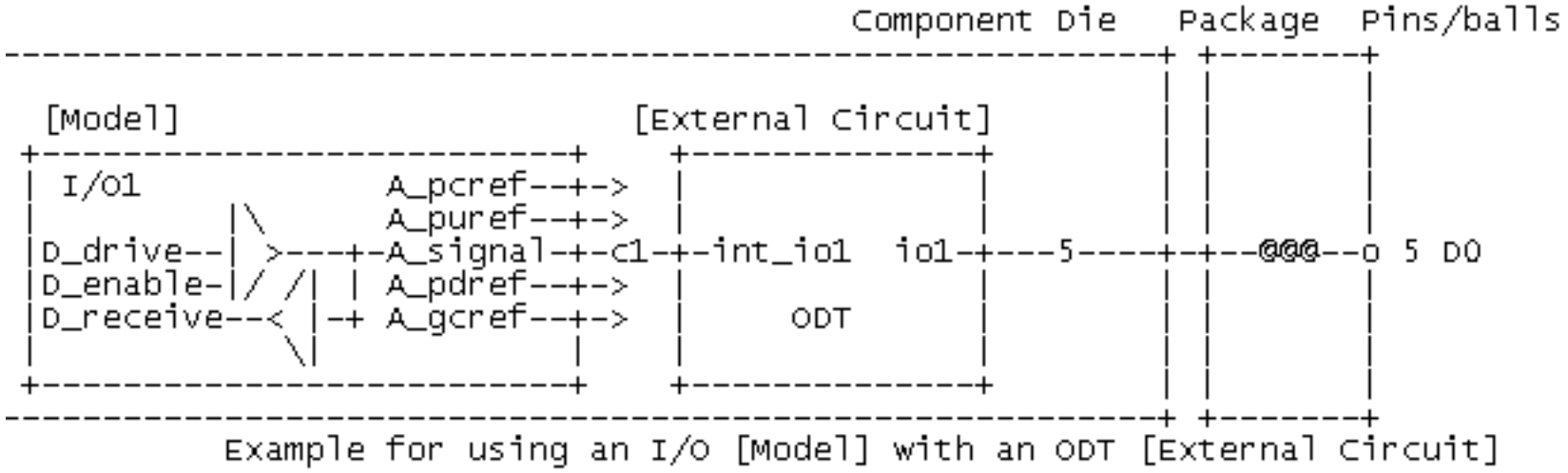
Solution: Include IBIS I/O table model in an [External Circuit] using the new [Model Call]

- Ability to connect External Circuit to IBIS I/O model. The External Circuit could represent RDL parasitics, portion of active I/O buffer, some algorithmic part of I/O buffer.



Example for using an I/O [Model] with an ODT [External Circuit]

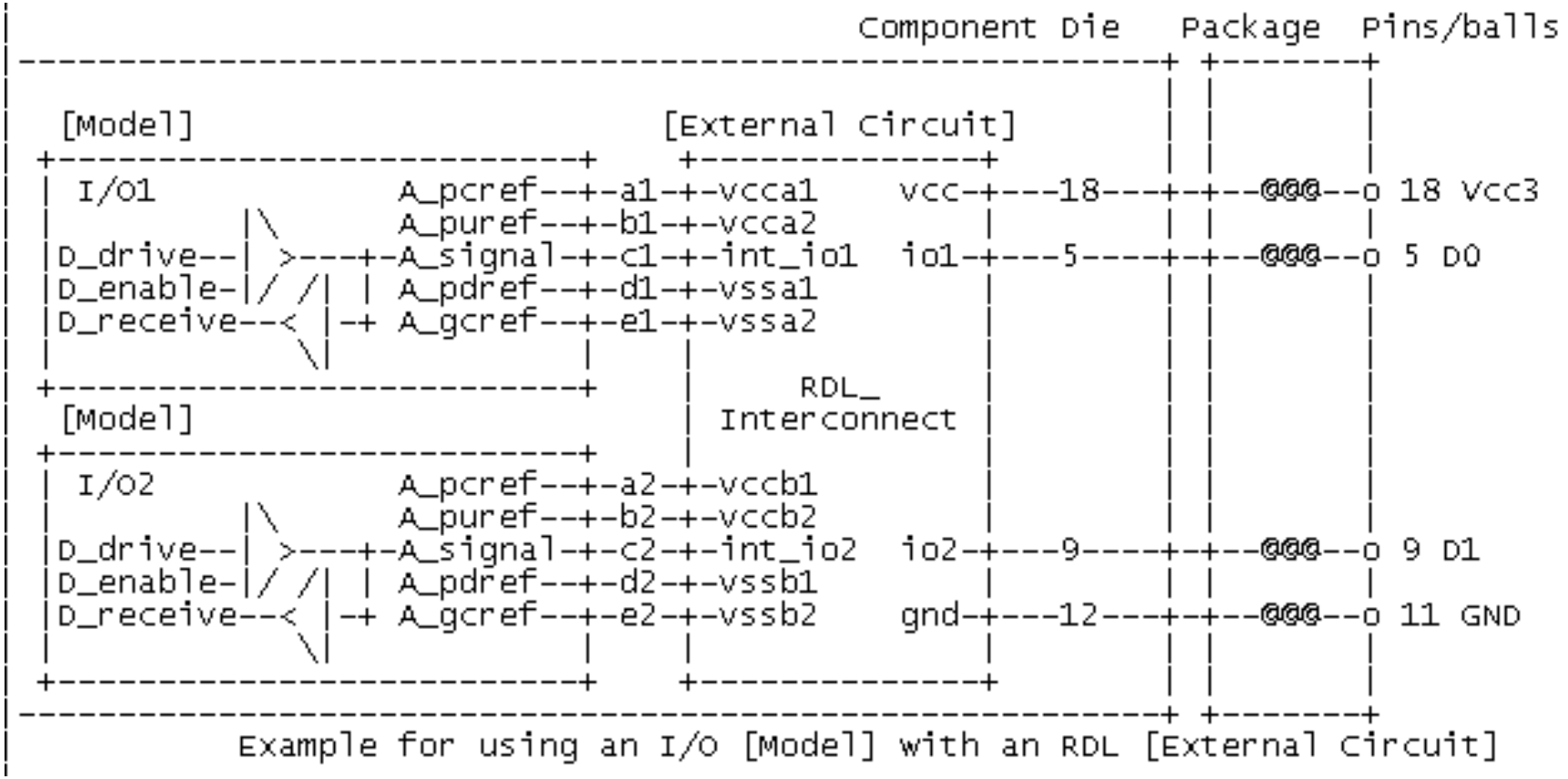
Solution: Include IBIS I/O table model in an [External Circuit] using the new [Model Call]

- [Pin] signal_name model_name R_pin L_pin C_pin
- 1 RAS0# Buffer1 200.0m 5.0nH 2.0pF
- 2 RAS1# Buffer2 209.0m NA 2.5pF
- 3 EN1# Input1 NA 6.3nH NA
- 4 A0 3-state
- **5 D0 I/O1**
- 6 RD# Input2 310.0m 3.0nH 2.0pF
- 7 WR# Input2
- 8 A1 I/O2
- **9 D1 I/O2**
- 10 GND GND 297.0m 6.7nH 3.4pF
- 11 RDY# Input2
- 12 GND GND 270.0m 5.3nH 4.0pF

HERE DO, D1 are to be modeled as I/O1, I/O2 buffers followed by RDL Spice and represent a differential buffer

Solution: Include IBIS I/O table model in an [External Circuit] using the new [Model Call]

- I/O1 and I/O2 are followed by RDL Spice model



Solution: Include IBIS I/O table model in an [External Circuit] using the new [Model Call]

- **[Node Declarations]** **| Must appear before any [Circuit Call] or [Model Call] keyword**
- |
- | Die nodes
- a1 b1 c1 d1 e1 | List of die nodes representing signals that connect models
- a2 b2 c2 d2 e2
- |
- **[End Node Declarations]**
- |
- | NOTE:
- | A [Model] named "I/O1" must be present in the IBIS file in order to enable
- | the tool to instantiate and connect the called model "as usual" based on
- | the I-V and T-V curves as well as the subparameters under the corresponding
- | [Model] section.
- |
- **[Model Call] I/O1** **| Instantiates [Model] named "I/O1"**
- |
- | mapping port pad/node
- |
- Port_map A_pcref a1 | Port to internal node connection
- Port_map A_puref b1 | Port to internal node connection
- Port_map A_signal c1 | Port to internal node connection
- Port_map A_pdref d1 | Port to internal node connection
- Port_map A_gcref e1 | Port to internal node connection
- |
- **[End Model Call]**
- |

Solution: Include IBIS I/O table model in an [External Circuit] using the new [Model Call]

- | NOTE:
- | A [Model] named "I/O2" must be present in the IBIS file in order to enable
- | the tool to instantiate and connect the called model "as usual" based on
- | the I-V and T-V curves as well as the subparameters under the corresponding
- | [Model] section.
- |

- **[Model Call] I/O2** **| Instantiates [Model] named "I/O2"**
- |
- | mapping port pad/node
- |
- Port_map A_pcref a2 | Port to internal node connection
- Port_map A_puref b2 | Port to internal node connection
- Port_map A_signal c2 | Port to internal node connection
- Port_map A_pdref d2 | Port to internal node connection
- Port_map A_gcref e2 | Port to internal node connection
- |
- **[End Model Call]**
- |

Solution: Include IBIS I/O table model in an [External Circuit] using the new [Model Call]

- **[Circuit Call] RDL_Interconnect** **| Instantiates [External Circuit] named "RDL_Interconnect"**
- |
- | mapping port pad/node
- |
- Port_map vcc 18 | Port to implicit pad connection
- Port_map gnd 12 | Port to implicit pad connection
- Port_map io1 5 | Port to implicit pad connection
- Port_map io2 9 | Port to implicit pad connection
- Port_map vcca1 a1 | Port to internal node connection
- Port_map vcca2 b1 | Port to internal node connection
- Port_map int_io1 c1 | Port to internal node connection
- Port_map vssa1 d1 | Port to internal node connection
- Port_map vssa2 e1 | Port to internal node connection
- Port_map vccb1 a2 | Port to internal node connection
- Port_map vccb2 b2 | Port to internal node connection
- Port_map int_io2 c2 | Port to internal node connection
- Port_map vssb1 d2 | Port to internal node connection
- Port_map vssb2 e2 | Port to internal node connection
- |
- **[End Circuit Call]**

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- **Summary**

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Summary

- With increase in frequencies, we need enhanced usage of External Model / Circuit
  - S-parameters are becoming common way to model portions of I/O buffers and package parasitics; Hence need to have direct support of S-parameter model under [External Model/Circuit]. *This has been proposed as BIRD144*
  - Significant portion of I/O buffer gets modeled as Spice/S-parameters to augment the main analog buffer to capture the high frequency behavior; Hence need to have easy way to connect External Circuit to I-V/V-T table-model. *This has been proposed as BIRD145*

Summary

- BIRD144 and BIRD145 can be accessed at

  http://www.eda.org/pub/ibis/birds/

  - The BIRDs would be considered and discussed by the IBIS open forum
  - Other BIRDs will also be considered that might be alternatives or add-on to this proposal


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