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DDR3 SI/PI Analysis using IBIS5.0

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November 18, 2011

Outline

- **Problems of DDR3 SI/PI Analysis**
- **DDR3 SI/PI Analysis using IBIS5.0**
- **Summary**
- **Expecting of IBIS**

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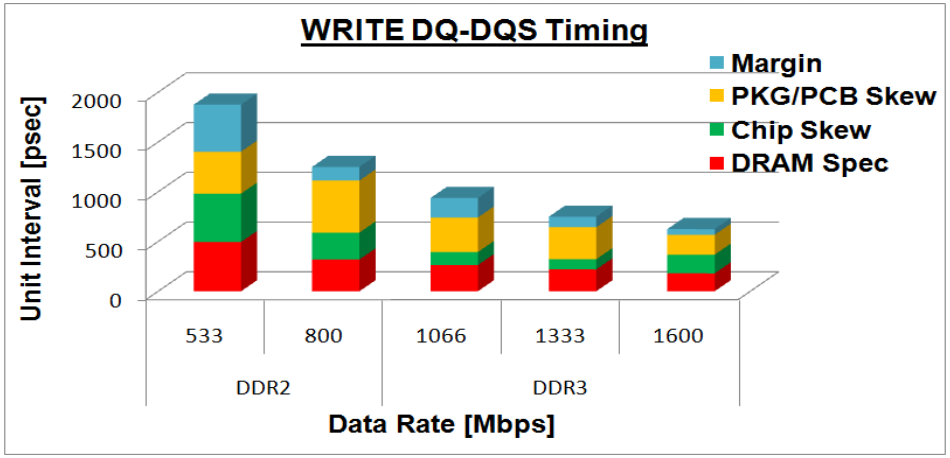
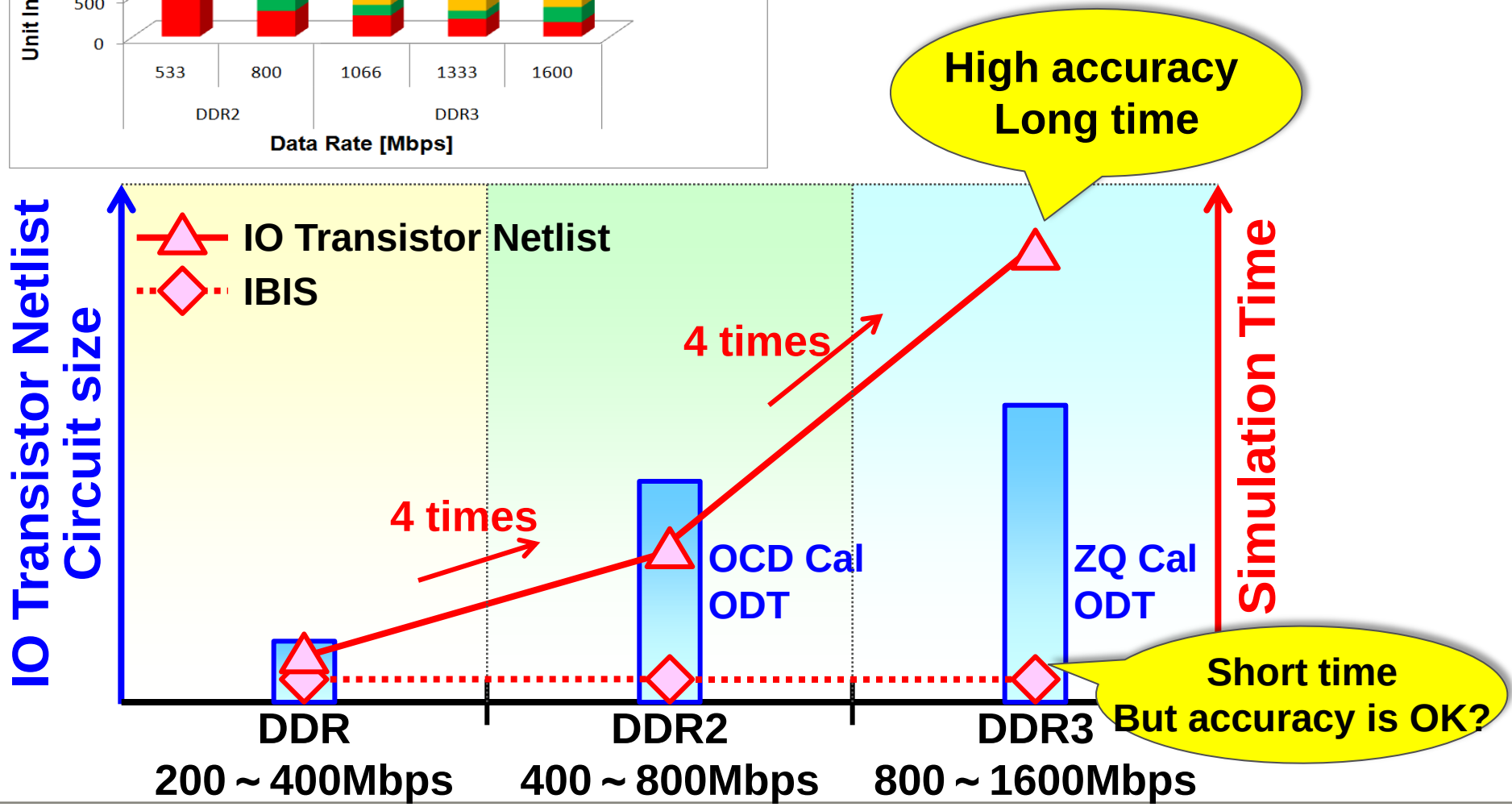
Problems of DDR3 SI/PI Analysis



- Decrease of margin
- It's necessary to execute SI/PI analysis of high accuracy



IO Transistor Netlist vs IBIS

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Contents

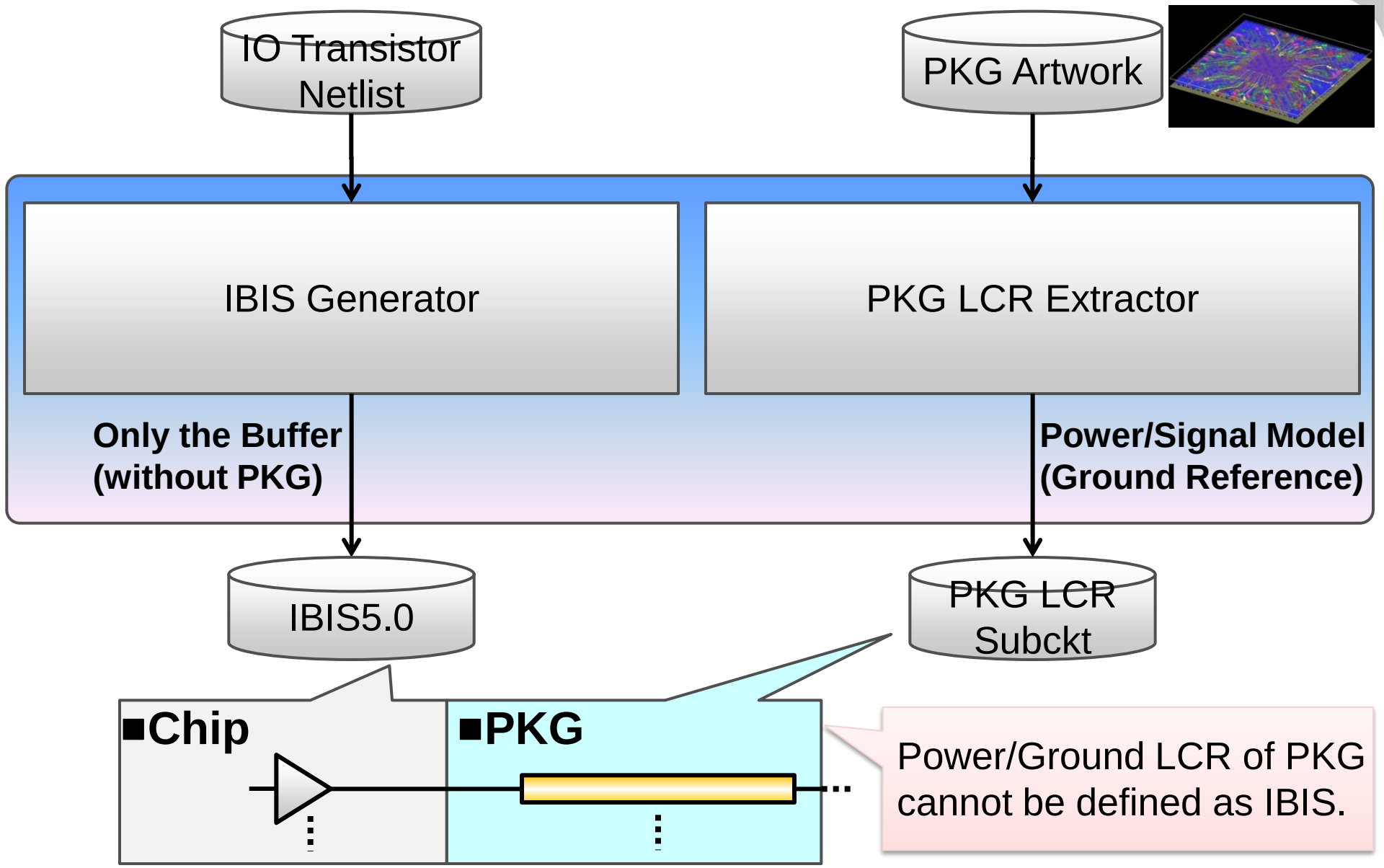
IO Transistor Netlist	IBIS
Detailed circuits and netlists (transistor level)	I-V/V-T tables for IO final buffer

Trade-off

	IO Transistor Netlist	IBIS
Simulation Time	Slow (Several to 10 times slower than IBIS)	Fast
Format	Bad (Encryption and NDA are necessary)	Good (Open format)
EDA Tools Utilization	Bad (Specific simulator is necessary for encrypted models)	Good (Many SI/PI tools support)
Accuracy (SI)	Good	Reasonably good
Accuracy (PI)	Good	? (Supported SSO from Ver.5.0)

We have evaluated an ability of IBIS5.0 in terms of SI/PI.

IBIS5.0 Generation



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- Summary
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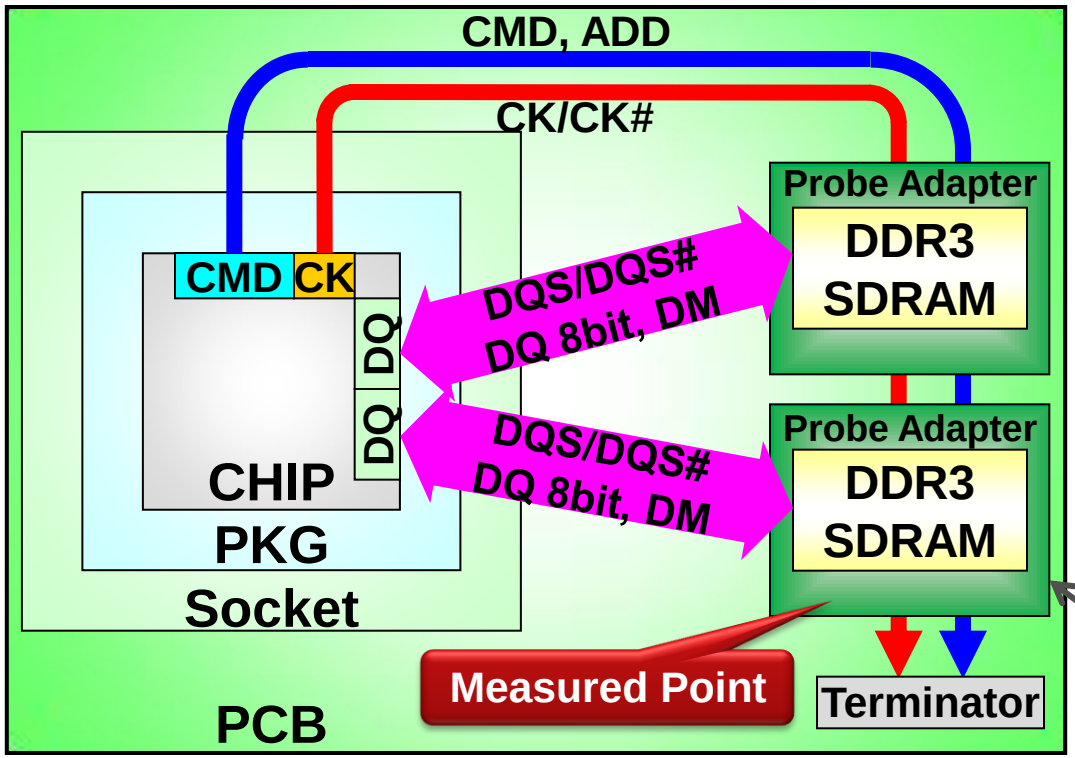
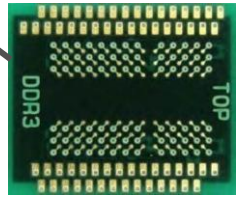
Evaluation Environment



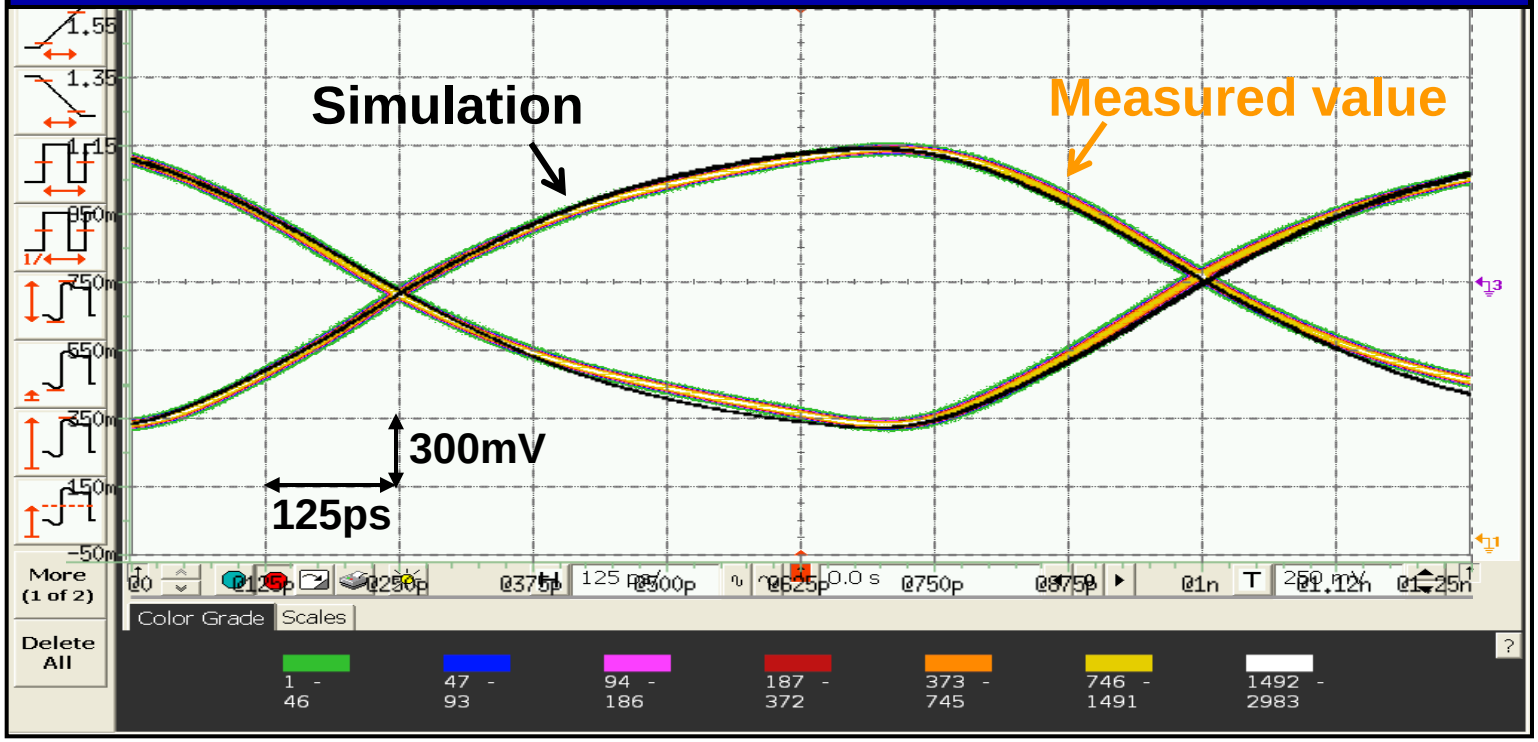


Probe Adapter

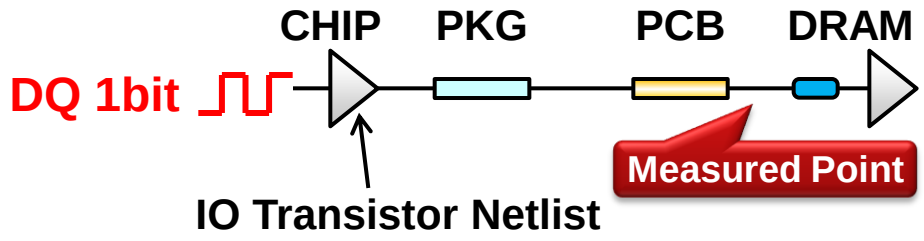
Item	Explanation
CHIP (mounted on Socket)	65nm DDR3 Interface Test Chip 16bit Data Rate : 1333Mbps
PKG	Wire Bond BGA 4Layer 900ball 31mmx31mm
PCB	6Layer
DRAM (mounted on Probe Adapter)	DDR3 SDRAM 8bitx2 on Board (Fly-by architecture)

Validity of Simulation Model

Measurement vs Simulation (Eye)



DQ 1bit 1333Mbps



Simulation model is highly accurate.

IBIS4.2 vs IBIS5.0

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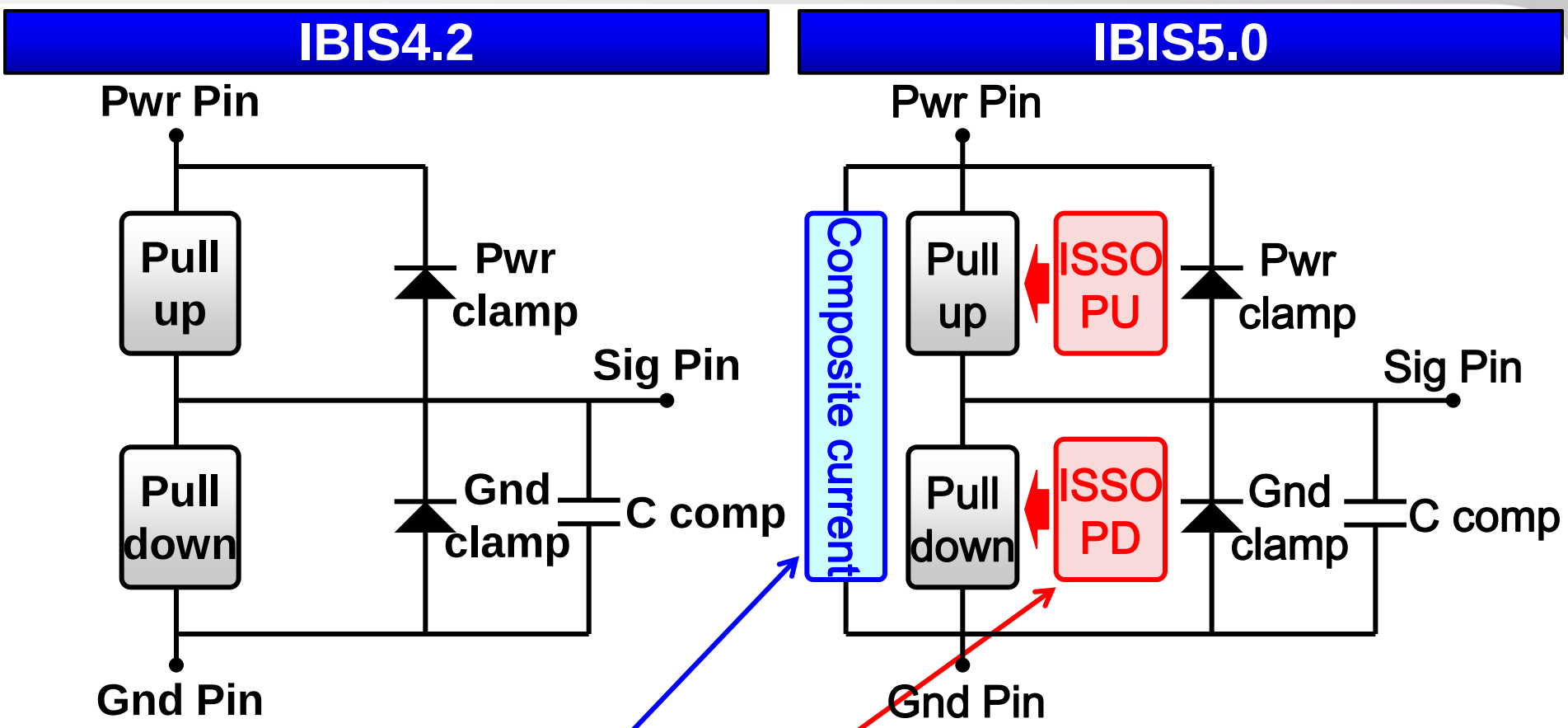
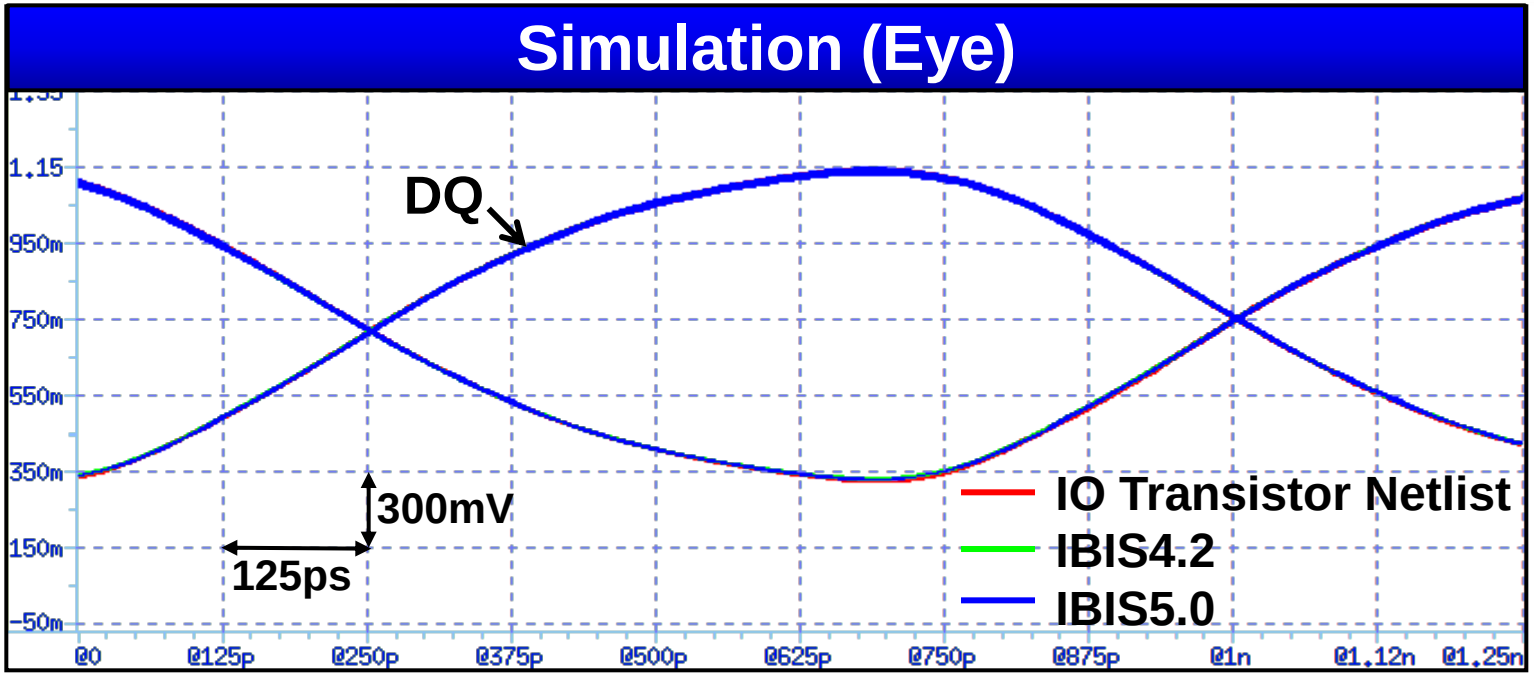
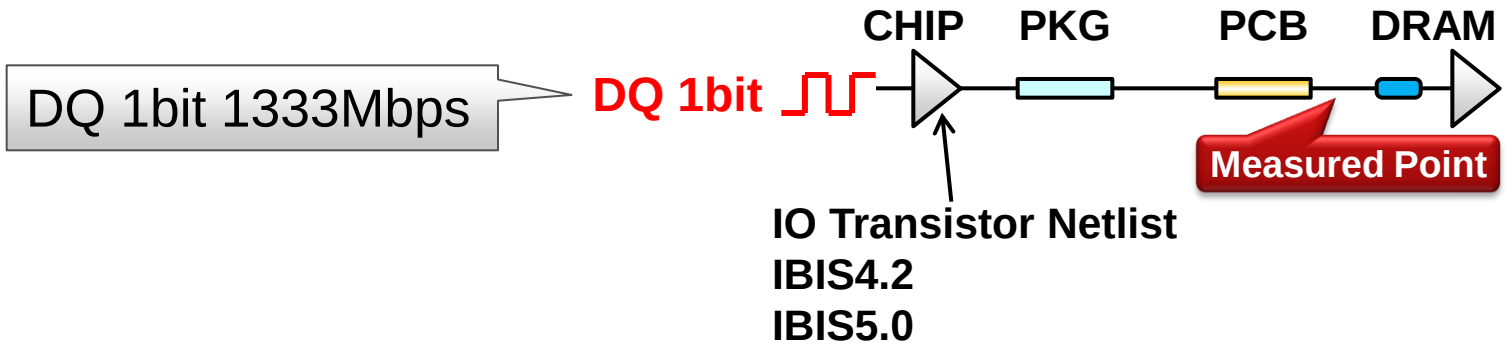


- **Composite current (BIRD95)**
  - Characterizes currents from the supply rail through the buffer, as the buffer switches into a known load. It can show accurately driving current of IO.
- **ISSO PU / ISSO PD (BIRD98)**
  - Characterizes buffer current modulation due to supply variation. It can show a change of driving current by voltage fluctuation.

DDR3 SI Analysis using IBIS5.0





Both IBIS4.2 and IBIS5.0 are highly accurate.(in case SI analysis)

DDR3 PI Analysis using IBIS5.0 (SSO Noise)

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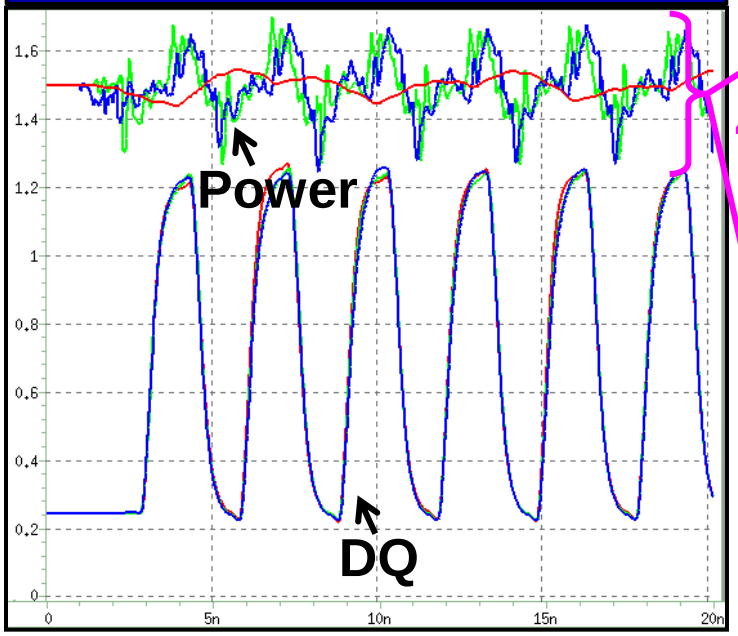
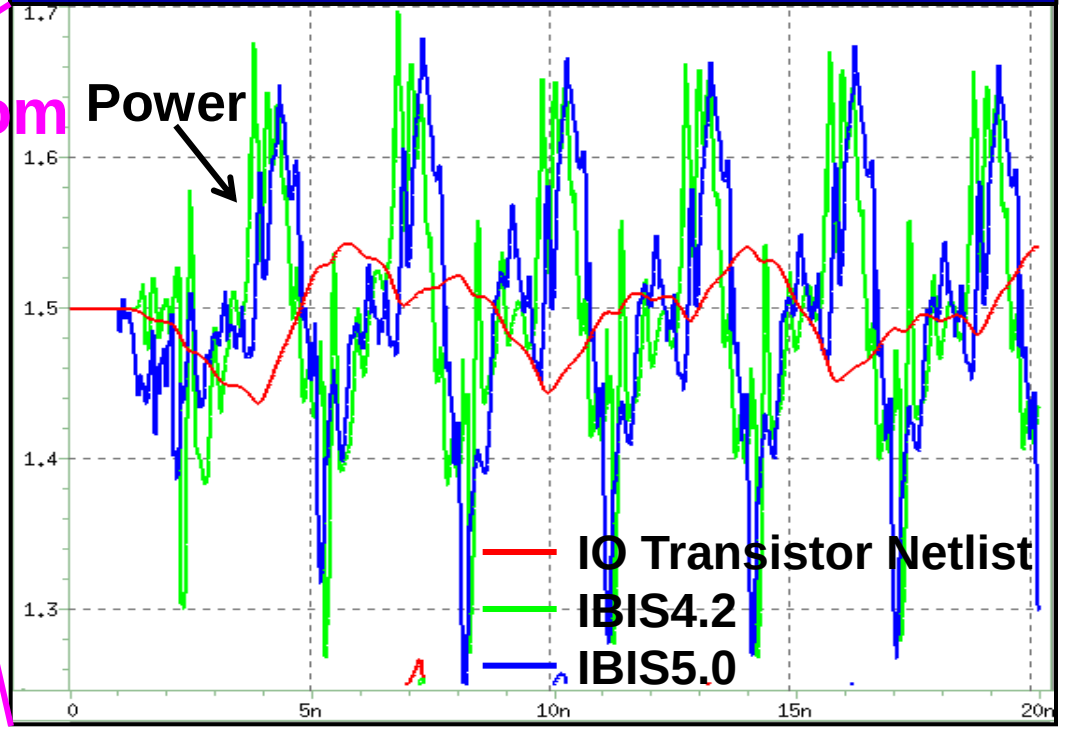
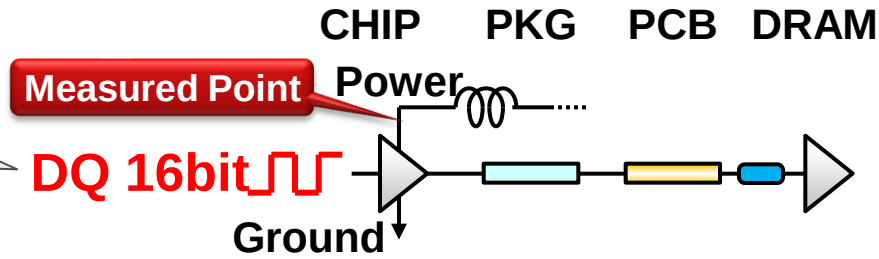
Simulation (Overall)



Zoom

Simulation (Closeup)

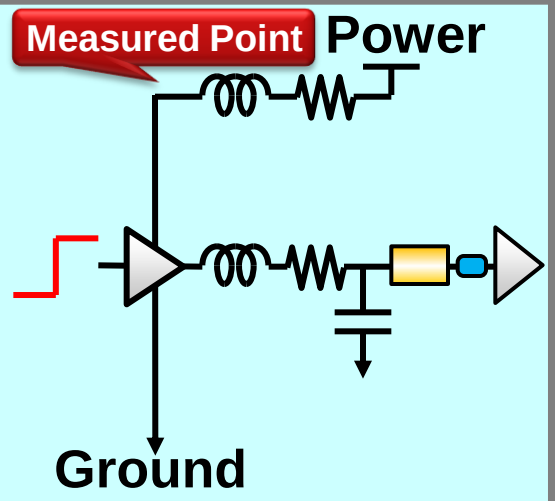
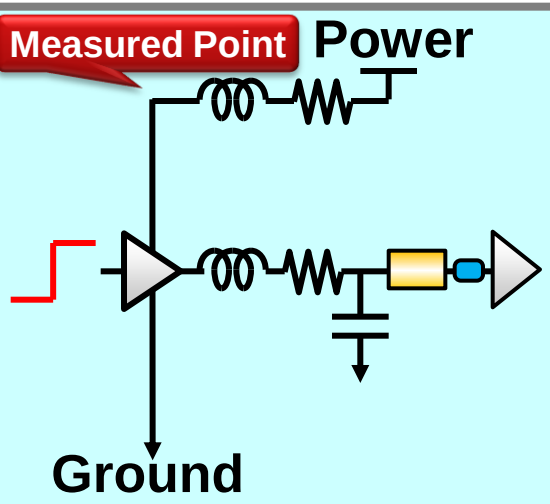
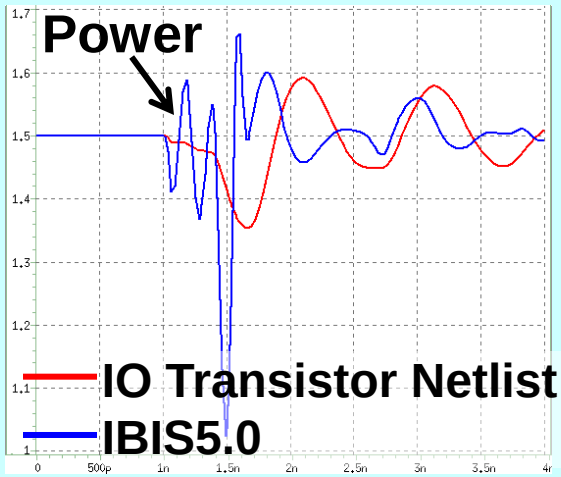
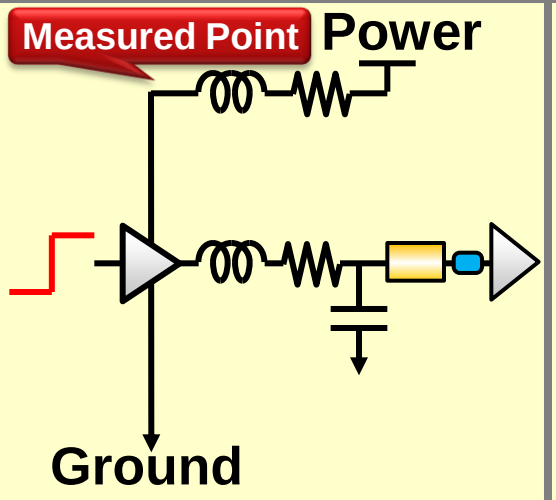
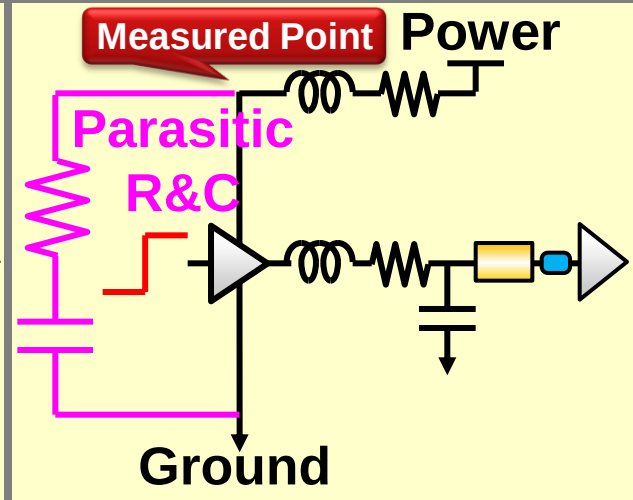
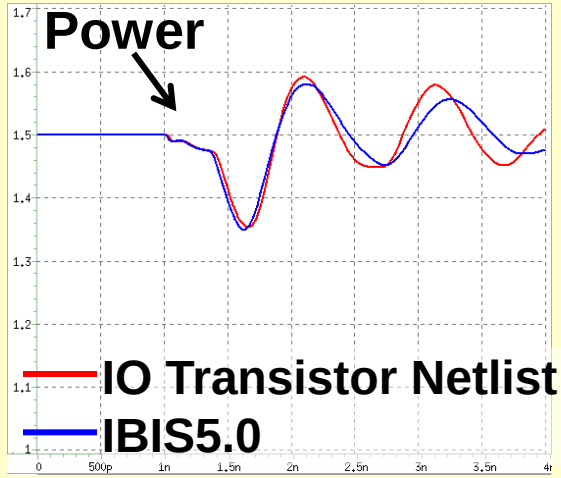




DQ 16bit 667Mbps Common Mode

SSO Noise using IBIS5.0 is different from that using Transistor Netlist.

Reason that SSO Noise is different

	IO Transistor Netlist	IBIS5.0	Simulation
Without Parasitic R&C			
With Parasitic R&C			

Parasitic RC circuit between Power and Ground was not modeled in the previous simulation.

DDR3 PI Analysis using IBIS5.0 (Improved)

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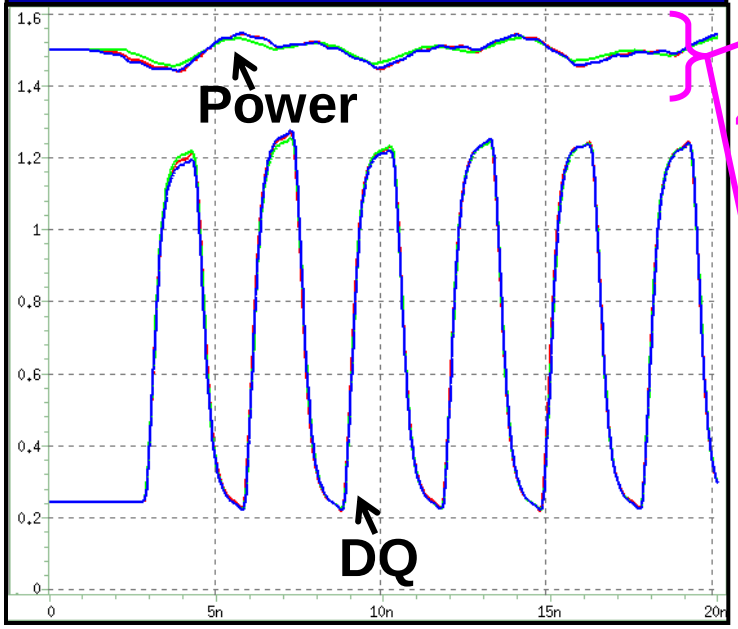
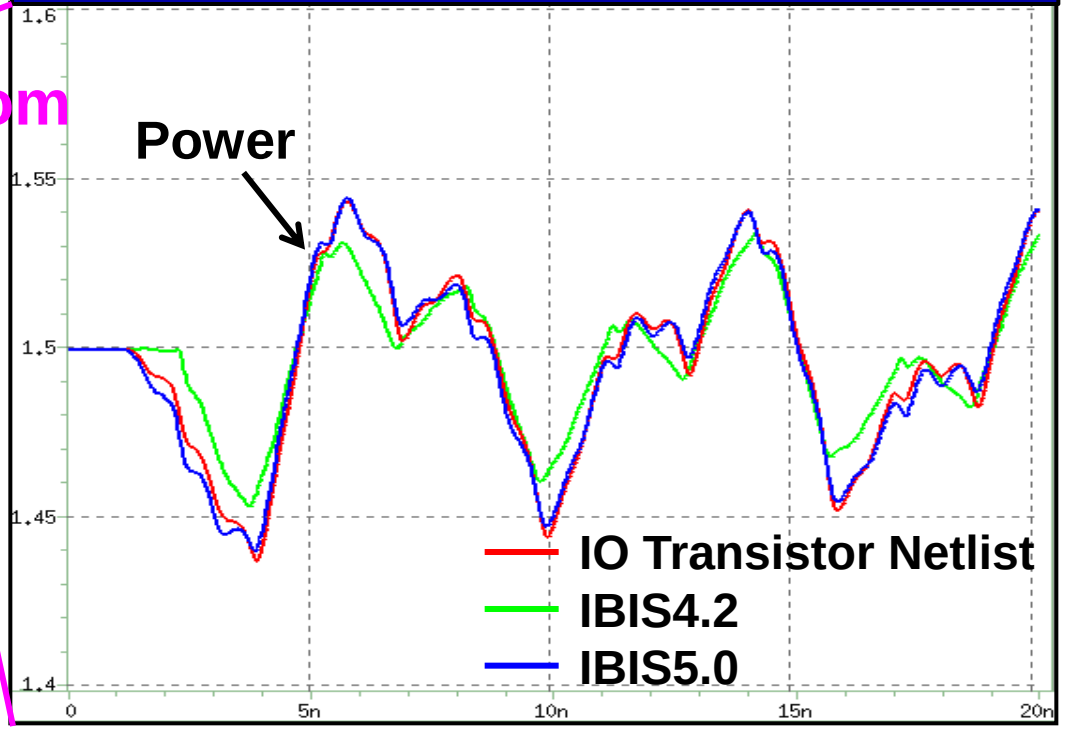
Simulation (Overall)

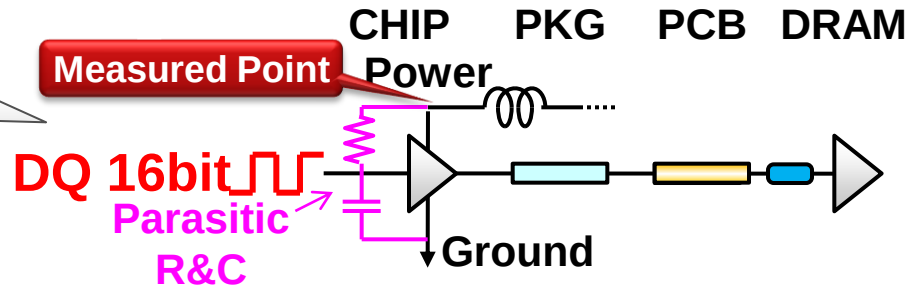


Zoom

Simulation (Closeup)



DQ 16bit 667Mbps Common Mode



IBIS5.0 is highly accurate about SSO Noise ! (IBIS4.2 is NG.)

DDR3 PI Analysis using IBIS5.0 (Signal)

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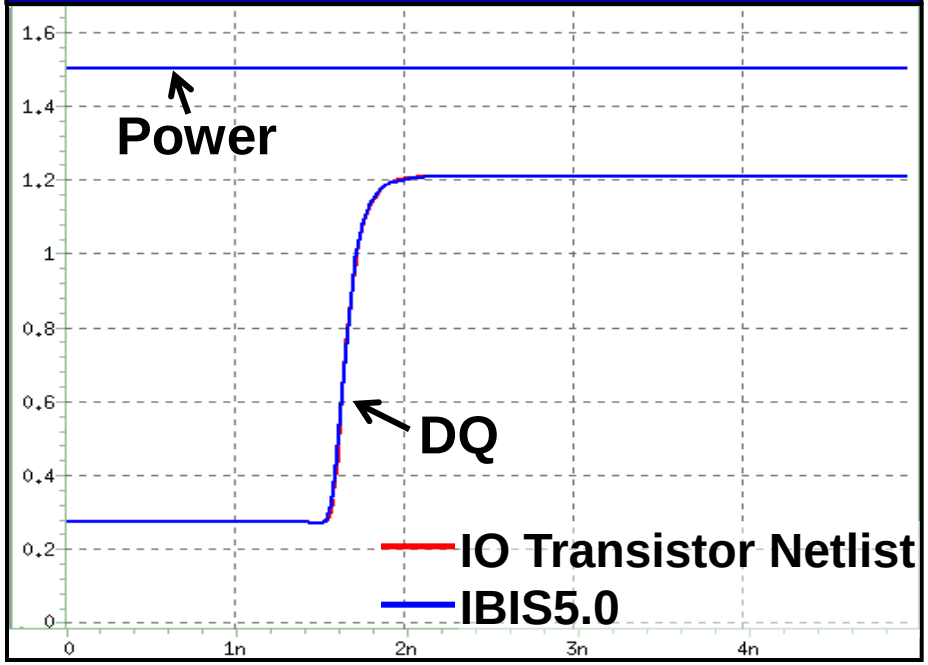
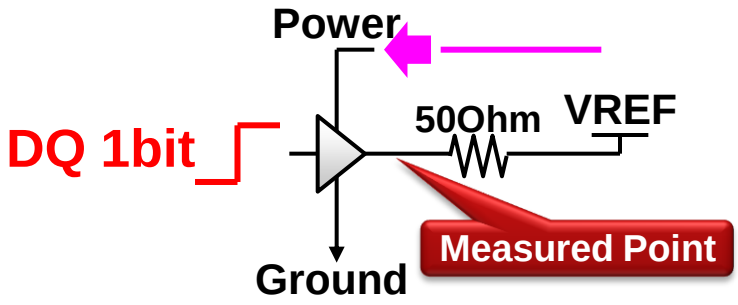
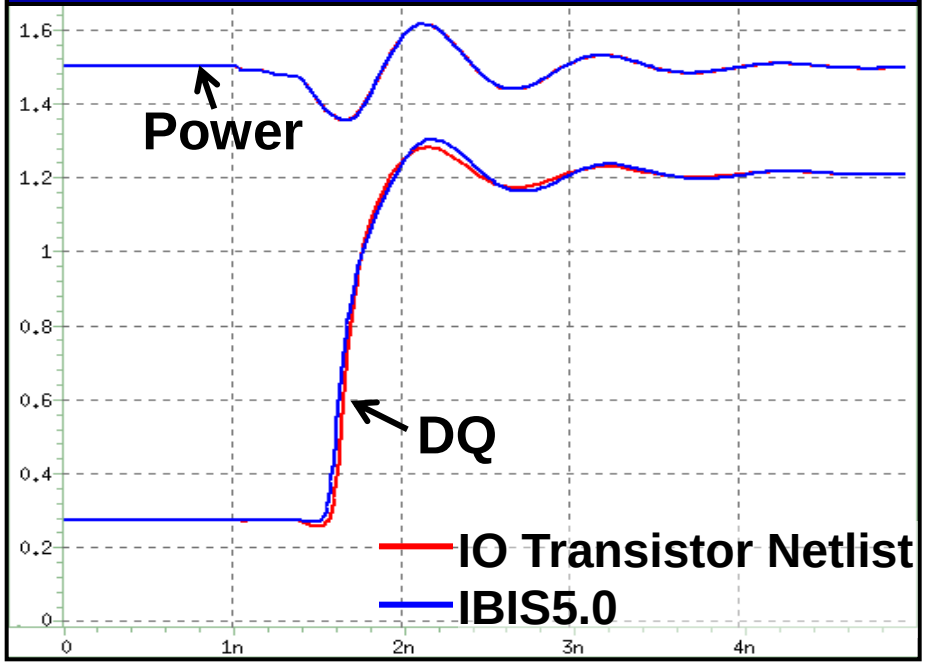
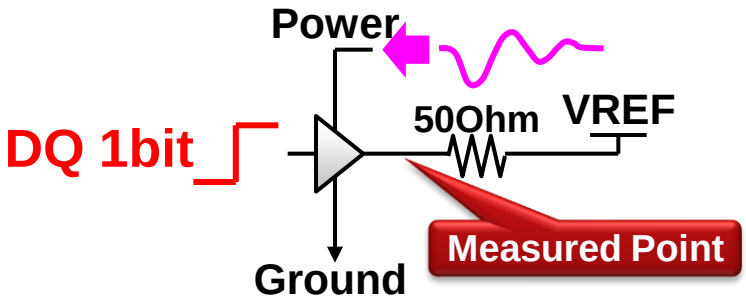
Without SSO Noise





With SSO Noise





IBIS5.0 can show signal distortion related to SSO Noise.

DDR3 PI Analysis using IBIS5.0 (Delay Penalty)

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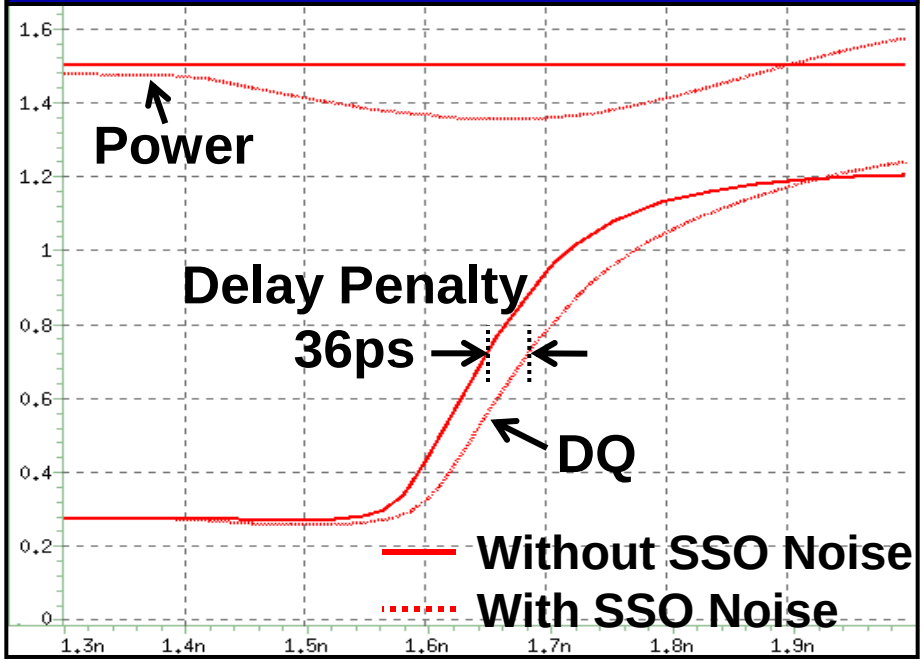
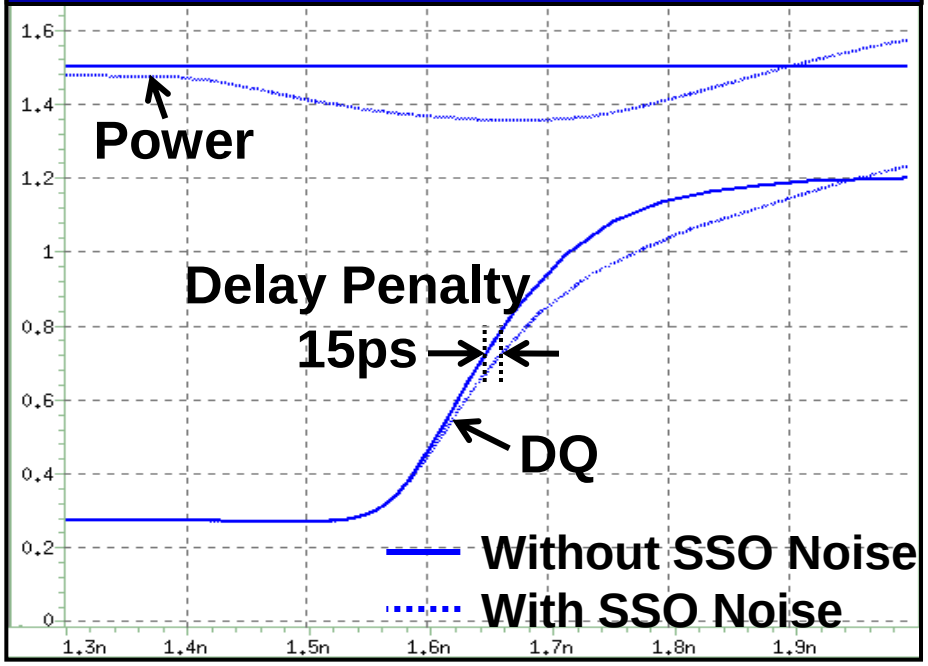
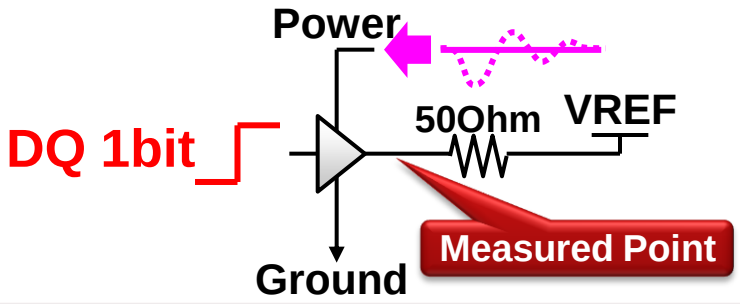
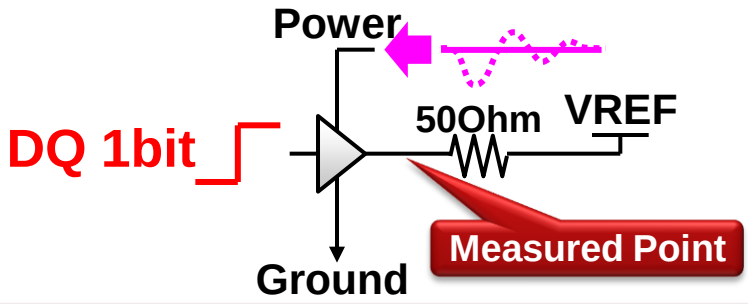
IO Transistor Netlist



IBIS5.0







IBIS5.0 can not show Delay Penalty accurately.
(IBIS5.0 can show only Delay Penalty of IO final buffer.)

Outline

- Problems of DDR3 SI/PI Analysis
- DDR3 SI/PI Analysis using IBIS5.0
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- Expecting of IBIS

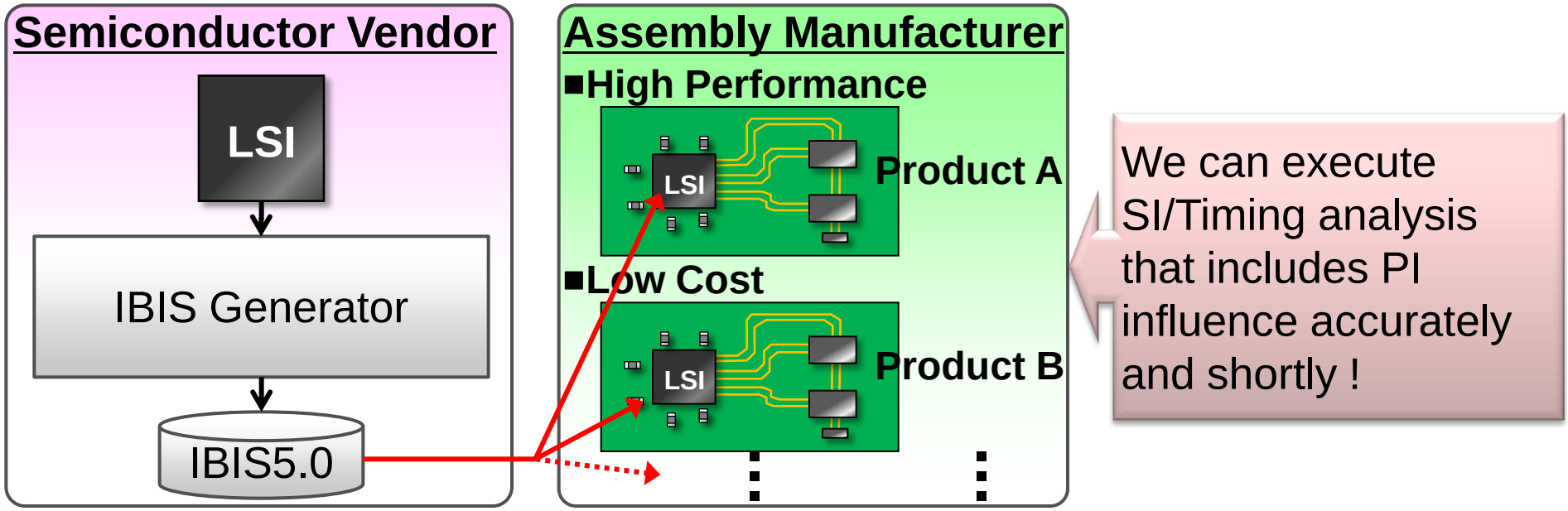
Summary

Item	IO Transistor Netlist	IBIS5.0	IBIS4.2
SI (Ideal Power)	○	○	○
PI (SSO Noise)	○	○	×
PI (Signal)	○	○	×
PI (Delay Penalty)	○	△	×
Sim. time ※1	1020 minutes	24 minutes	24 minutes

※1. 50ns Transient Analysis

97% Down

■If we can show Delay Penalty accurately in IBIS5.0 …



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Expecting of IBIS

- Problems in IBIS5.0
  - It's impossible to define Power/Ground LCR of PKG in IBIS5.0
  - Parasitic RC circuit doesn't exist in a circuit defined as IBIS5.0(Refer to Figure1)
  - IBIS5.0 can not show IO Delay Penalty accurately (Refer to Figure2)

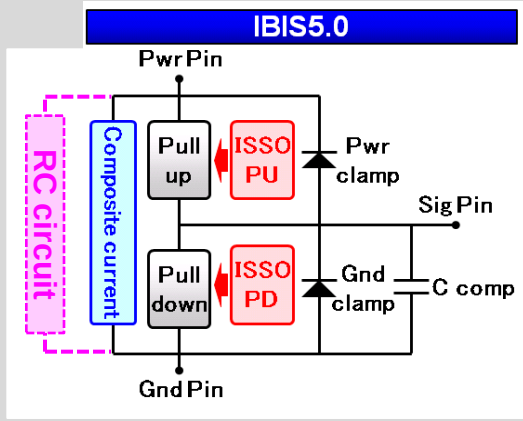


Figure1

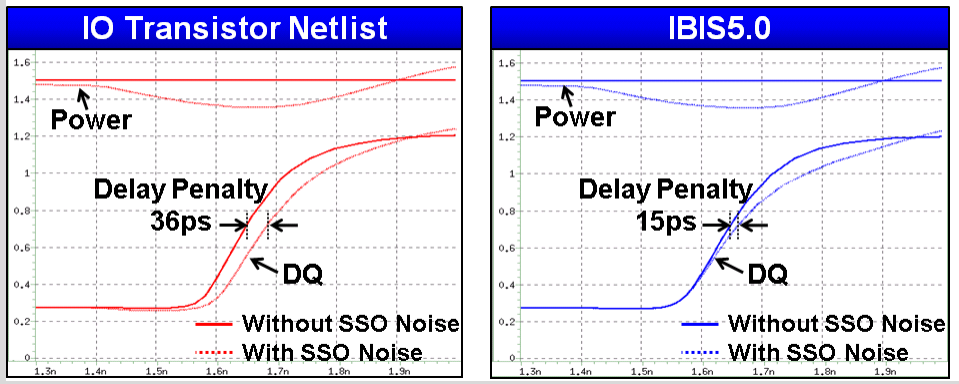
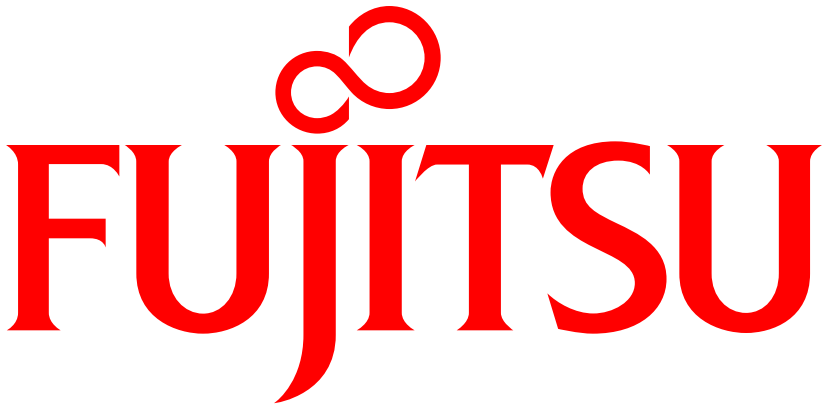


Figure2

Please improve above-mentioned problems in IBIS5.0.



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