IBIS Open Forum Minutes

Meeting Date: **November 18, 2011** Meeting Location: **Yokohama, Japan**

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Sigrity	Raymond Chen, Kumar Keshavan, Yingxin Sun Li Li, Kezhou Li, Jing Wang, Xingfeng Li, Haisan Wang, Zuli Qin, Lily Luo
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	Meihua Xu, Changgang Ying, Qiang Zhang, Wei Zhou, Zhi Zhou, Jiangrong Xiao, Xiaobing Zhang, Zhiwei Yang, Shenghu Wang, Dawei Sun, Cheng Li, Lu Li, Li Wang, Renjie Wang, Jie Yu, Shunlin Zhu
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AET	Mikio Kiyono, Chihiro Ueda*
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Apache Design Solutions	Shulong Wu
Apollo Giken	Mitsuo Kaetsu*, Naoya Iisaka*, Satoshi Endo*
Arrow Electronics	lan Dodd
ATE Service	Yutaka Honda*
Avant Technology	Enson Lee
Avago	Weiping He, Minh Quach, Sari Tocco

Axell Bayside Design Broadcom Canon

Canon Components Casio Computer Celestica

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Fujitsu VLSI

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Signal-Lab

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Atsuhito Noda* Sei Shida*

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Trident Microsystems	Andy (Zhiguang) Li
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WADOW	Kazuhiko Kusunoki*
Wens	Heien Hirokawa*
Xpeedic Technology	Feng Ling, Wenliang Dai, Shisheng Wu
Yazaki	Kazuki Hattori*
YDC	Yoshiaki Manabe*
YDK	Yoshio Takemura*
Independent	Yoichi Niioka, [Mike LaBonte], Mingwei Chen,
	Liping Wang

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 21, 2011	Asian IBIS Summit – Taipei -	 no teleconference
December 9, 2011	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed

within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The IBIS Open Forum summit was held in Yokohama, Japan, co-located with the Electronics Design Solutions Fair (EDS Fair) at the Pacifico Yokohama Conference Center. About 131 people representing 74 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/pub/ibis/summits/nov11b/

Bob Ross (on behalf of Michael Mirmak) opened the sixth Asian IBIS Summit in Japan at 1:30 PM.

Yasutaka Oodake (JEITA EC Working Group Chair and Toshiba Corporation) welcomed everyone and thanked the international attendees.

Bob Ross provided some brief remarks, thanked the co-sponsors ANSYS, ATE Service Corporation (Sigrity), Cadence Design Systems, Mentor Graphics Corporation and Zuken. Bob noted that this was the sixth meeting and that cooperation with JEITA had provided strong IBIS support. He cited the recent publication in Japanese of a signal integrity book with strong IBIS content. He thanked JEITA for arranging the meeting and providing excellent facilities.

IBIS UPDATE AND PARSERS

Bob Ross (Teraspeed Consulting Group, USA)

Bob Ross first gave a brief overview of the IBIS Open Forum and its recent activities. He showed the revised home page and then described its organization within TechAmerica and under the SSTC (Standards and Technology Council). IBIS-ISS (IBIS-Interconnect Spice Subcircuit) Specification, a subset of HSpice was recently introduced. Work is continuing on IBIS Version 5.1. Work on IBIS Version 5.2 (or 6.0), and Touchstone Version 2.1 is continuing. Also, ibischk5 and touchstone2 parsers are being maintained.

Bob summarized the latest parser release, ibischk5, Version 5.0.7. The IBIS committee has spent over \$114,000 since the beginning in 1993. Bob illustrated some of the recent flags and functionality and showed how 1155 unique Error, Warning, Notes, and Caution message strings are documented in a spreadsheet format. This allows sorting of messages in several ways such as by severity or by source code modules. Messages for specific areas (such as for the IBIS-AMI .ami syntax) can be grouped. This will be released in the future, but at this time only

about 350 of the 1,155 messages have descriptions filled in. The recent parser fixed problems with the dV check, the [Model Spec timing test load entry processing and demoted the Error check for [ISSO PU] and [ISSO PD] time alignment to a Caution message (in anticipation for the removal of the requirement in IBIS Version 5.1).

The tschk2 parser was also summarized. It allows both checking of Touchstone Version 2.0 and Touchstone Version 1.0 and conversion between the two formats. The parser source code package already contains the documentation of 71 Error and Warning messages in an html format. Bob illustrated how these messages are grouped.

Both of these parsers serve to check the specification and also check actual files for specification and value compliance. As a result, the parsers are critical to IBIS success.

QUALITY OF S-PARAMETER MODELS

Yuriy Shlepnev (Simberian, USA)

Yuriy Shlepnev indicated that S-parameter models including Touchstone files have these quality issues: reciprocity failure, passivity and causality violations, and common sense violations. These issues can cause different tools to produce different time-domain and frequency-domain responses. Discrete models are approximated by the discrete Fourier transform and by rational functions. Some common problems in models include bandwidth deficiency (DC and high frequency), discreteness (interpolation required), and distortions (measurement artifacts, passivity violations, and causality violations).

Yuriy showed the derivations and provided estimation methods for quantifying these defects. He suggested metrics, normalized to a 0 to 100% range: Passivity Quality Measure (PQM), Reciprocity Quality Measure (RQM), and Causality Quality Measure (CQM). He also suggested ranges for which models are good, acceptable, inconclusive and bad. The acceptable level is PQM > 99%, RQM > 99% and CQM > 80%. Yuriy also suggested using rational or broad band models for more consistent time and frequency domain analysis.

IBIS MODEL AS DE-FACTO STANDARD

Kazuhiko Kusunoki* and Wenliang Dai** (*WADOW, Japan and **Xpeedic Technology, China)

Kazuhiko Kusunoki questioned whether the same IBIS model produced the same results in different simulators. He presented the results of differential buffer IBIS model test cases analyzed on six different simulators. No two results were identical, and the differential buffer output crossing points ranged from 600 mV to 764 mV.

The IBIS Quality Framework within JEITA is attempting to address this issue. It sets a framework where IBIS models can be checked and where simulators can be validated against reference IBIS models with known simulation results. Kazuhiko also noted that operator experience is a factor. In one experiment, different operators produced different results for the same simulator. What the industry needs is good IBIS models, good tools, good engineers and good support.

Yuriy Shlepnev suggested that the Touchstone models also be checked in a similar manner against different simulators, and Kazuhiko stated that he would consider doing this.

DDR3 SI/PI ANALYSIS USING IBIS5.0

Shintaro Ohtani (Fujitsu Semiconductor, Japan)

Shintaro Ohtani stated that SI/PI (signal integrity, power integrity) analysis is becoming necessary for higher speed DDR3 design. Traditional netlist analysis is too slow and may require encrypted models available only through NDA and for specific tools. He showed that IBIS simulation is very accurate for SI analysis when he compared by an eye diagram simulation with measured results.

Shintaro illustrated the composite current (BIRD95) and ISSO_PU/ISSO_PD advances (BIRD98) in IBIS Version 5.0 to support SSO analysis. He also noted that the parasitic RC between power and ground was needed to make the results nearly identical for SSO noise and signal distortion with reference to transistor level simulations. However, he showed delay penalty differences for the DQ signal between the transistor level results and the IBIS simulation results (36 ps versus 15 ps). This prompted several questions and discussion. Shintaro concluded that the delay penalty difference is a limitation in IBIS 5.0 and is a future challenge that needs to be addressed.

IBIS AMI SEEN FROM USER'S VIEWPOINT

Shinichi Maeda (KEI Systems, Japan)

Shinichi Maeda compared IBIS and Spice. Good support exists for standard IBIS. IBIS-AMI gives new life to IBIS for SerDes analysis. Shinichi then gave a brief overview of the [Begin Algorithmic Model] calling sequence and the parameter file (.ami file content).

From a user's perspective, Shinichi stated that verification is needed to trust IBIS-AMI model accuracy. More support is needed (cookbook, golden parser, tools, curve viewer, tune-up guidance, supporting tools). He stated that some tools work better than others. Also needed are verification tools, more documentation that includes a simulation result example and trouble-shooting guidance and a model quality document. With more IBIS-AMI infrastructure, both legacy IBIS and IBIS-AMI models can be released.

ANALYZING CROSSTALK'S IMPACT ON BER PERFORMANCE: METHODS AND SOLUTIONS

Minoru Ishikawa (Mentor Graphics Corporation, Japan)

Minoru Ishikawa presented some historical background since 2006. He provided an overview for IBIS-AMI to dynamically link compiled algorithmic models with IBIS buffer models for channel interconnects in SerDes designs. In addition to the standard IBIS flow, IBIS-AMI includes TX equalization, RX equalization, and clock data recovery.

Minoru presented multi-channel analysis with some examples showing how the victim is

impacted by near end (NEXT) and far end (FEXT) aggressors. Two time-domain approaches for crosstalk are used. For linear channels, the frequency response can be converted by IFFT, and for non-linear channels actual time-domain simulation is performed.

In addition, four combinations exist: synchronous or asynchronous time-domain crosstalk, and synchronous or asynchronous statistical time-domain crosstalk. Synchronous analysis assumes that there are constant phase of transitions, and asynchronous analysis assumes that the phases in different channels are statistically independent. Minoru listed the features and advantages of these approaches and compared some eye diagrams for each. He stated that it is important to understand the advantages and limitations of 4-port S-parameter models, neither synchronous nor asynchronous methods are perfect, but information from either method can be useful.

SUPPORTING EXTERNAL CIRCUIT AS SPICE OR S-PARAMETERS IN CONJUNCTION WITH I-V/V-T TABLES

Kent Dramstad# and Adge Hawes## (IBM, #USA, ##United Kingdom); Taranjit Kukal###, Feras AI-Hawari#, Ambrish Varma#, and Terry Jernberg# (Cadence Design Systems, ###India, #USA)

Yukio Masuko (Cadence Design Systems, Japan) introduced two sets of requirements that are related to proposed BIRDs: BIRD144 - to connect IBIS with S-parameters directly, and BIRD145 - to connect IBIS buffers with on-die terminations (ODT) or with re-distribution layer (RDL) parasitics. The current proposals have S-parameter models wrapped within Spice models (IBIS-ISS). IBIS models need to be connected directly to [External Circuit]s.

BIRD144 proposes a new language "Touchstone" to connect S-parameter models for [External Circuit] and [External Model] support without involving Spice wrappers. Standard Typ/Min/Max corners can be supported, and Yukio showed how this can be extended to new user-defined corners with some sample listings.

BIRD145 proposes a new keyword, [Model Call], to connect IBIS models and on-die [External Circuit]s for ODT and RDL connections. Yukio showed several examples to illustrate these connections.

Yukio concluded that both BIRD144 and 145 are needed enhancements for higher frequency analysis.

MODEL CONNECTIVITY IN PDN ANALYSIS FOR 3D-SIP

Brad Brim# and Yutaka Honda## (Sigrity, #USA, ##Japan)

Yutaka Honda showed 3D-SiP power distribution networks (PDN) for distributed dies (e.g., power/ground mesh on silicon imposer), stacked dies (e.g., vertical paths with through silicon vias), and wirebond connections from a package. Decoupling capacitors shape the SSO frequency and time domain noise characteristics. SSO analysis is influenced by including adjacent circuits, by actual physical die location, and by coupling through packages.

To handle all of these effects in a unified flow, a model connection protocol (MCP) is needed. Yutaka illustrated a protocol that contains IBIS-like keywords and describes pin_name, node_name, net, and coordinate. Such a protocol had been presented at earlier IBIS Summits to interface chip, package, and board models. (The proposal was also considered by the IBIS committee, but is now being considered by the Silicon Integration Initiative (Si2) organization, which focuses more on chip modeling.) One MCP feature is its density control to map the pin resolution to the same level as the destination circuit (by grouping a node per power domain). Yutaka showed some examples of applying the MCP for what-if analysis.

CONCLUDING ITEMS

Bob Ross thanked Atsushi Ishikawa and Yasutaka Oodake of JEITA for arranging the meeting. Bob also thanked the sponsors and the presenters. He thanked Yukio Masuko (Cadence Design Systems) and Shinichi Maeda (KEI Systems) for assisting in English-to-Japanese translation. He also thanked the attendees for providing strong support, and he looked forward to another Summit in 2012. The meeting adjourned at approximately 5:45 PM.

NEXT MEETING

The Asian IBIS Summit – Taipei will be held November 21, 2011. The next IBIS Open Forum teleconference will be held December 9, 2011 from 8:00 to 10:00 AM US Pacific Time. Votes on BIRD127.4 and BIRD146 are scheduled.

NOTES

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This meeting was conducted in accordance with the TechAmerica Legal Guides and TechAmerica Manual of Organization and Procedure.

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To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting

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ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/ http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/ http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/ http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

To create an account on the TechAmerica KAVI workspace, check out:

http://workspace.techamerica.org/kwspub/join/

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IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

		Standards				
		Ballot				
	Interest	Voting	October 7,	October	November	November
Organization	Category	Status	2011	28, 2011	15, 2011	18, 2011
Advanced Micro Devices	Producer	Active	Х	Х	-	Х
Agilent Technologies	User	Active	-	Х	-	Х
Altera	Producer	Inactive	Х	-	-	-
ANSYS	User	Active	-	-	Х	Х
Apple Computer	User	Inactive	-	-	-	-
Applied Simulation	User	Inactive	-	-	-	Х
Technology						
Cadence Design Systems	User	Active	-	Х	Х	Х
Cisco Systems	User	Inactive	-	-	Х	-
Ericsson	Producer	Active	-	Х	Х	Х
Foxconn Technology Group	Producer	Inactive	-	-	-	-
Freescale	Producer	Inactive	-	-	-	Х
Green Streak Programs	General Interest	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	-	Х	-
IBM	Producer	Inactive	Х	Х	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	Х	-	Х	-
IO Methodology	User	Active	Х	-	Х	-
LSI	Producer	Inactive	Х	Х	-	-
Mentor Graphics	User	Active	Х	Х	-	Х
Micron Technology	Producer	Inactive	Х	Х	-	-
Nokia Siemens Networks	Producer	Active	Х	Х	Х	-
QLogic	Producer	Inactive	-	-	-	-
Signal Integrity Software	User	Inactive	Х	Х	-	-
Sigrity	User	Inactive	-	-	Х	-
Synopsys	User	Inactive	-	-	Х	-
Teraspeed Consulting	General Interest	Active	Х	Х	Х	Х
Texas Instruments	Producer	Inactive	-	-	-	-
Toshiba	Producer	Inactive	-	-	-	Х
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	Х	-
Zuken	User	Inactive	-	-	-	Х

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS
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