DDR3 System Timing Budget Analysis by SI&PI Co-Simulation

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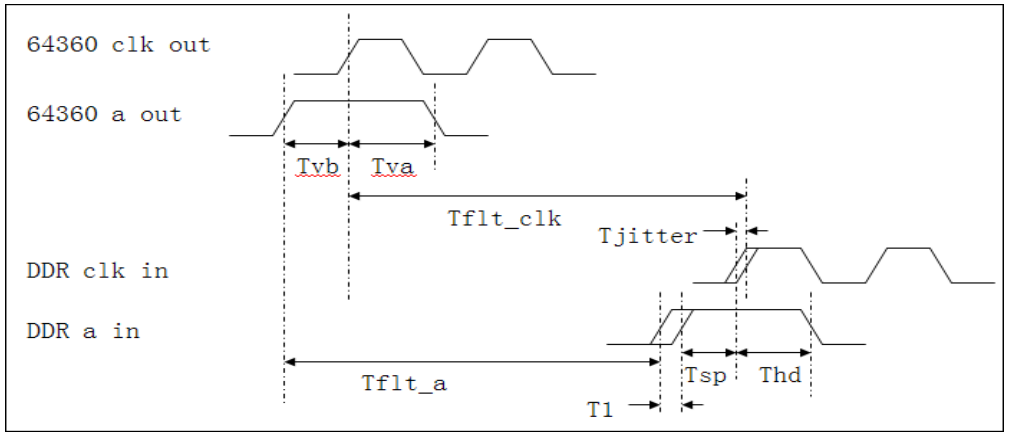
Agenda

- Traditional Timing Design for DDRx System
- Methods for DDR3 System Timing Budget Analysis
- Comparison of Two Simulation Results
- Summary

Traditional Timing Design for DDRx System

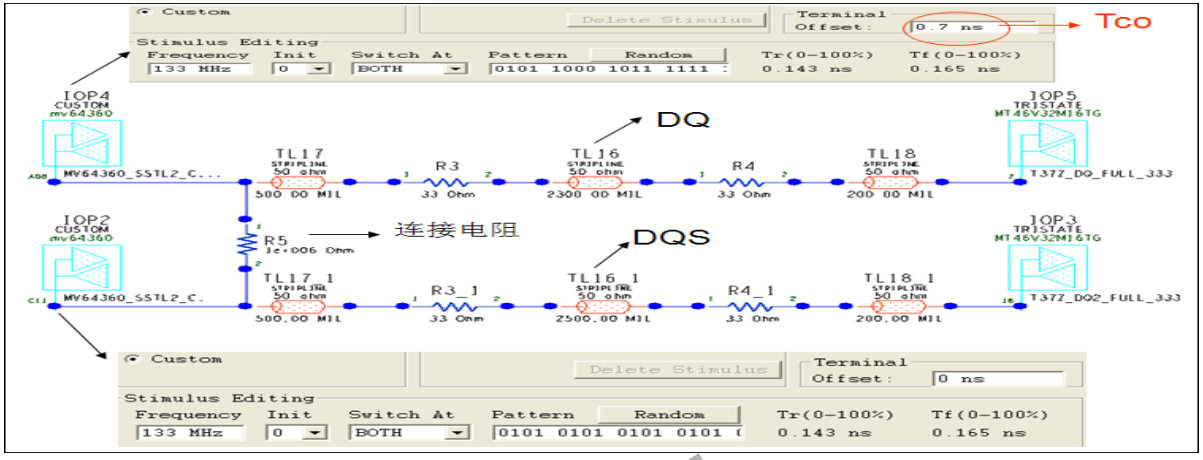
- Using Tables

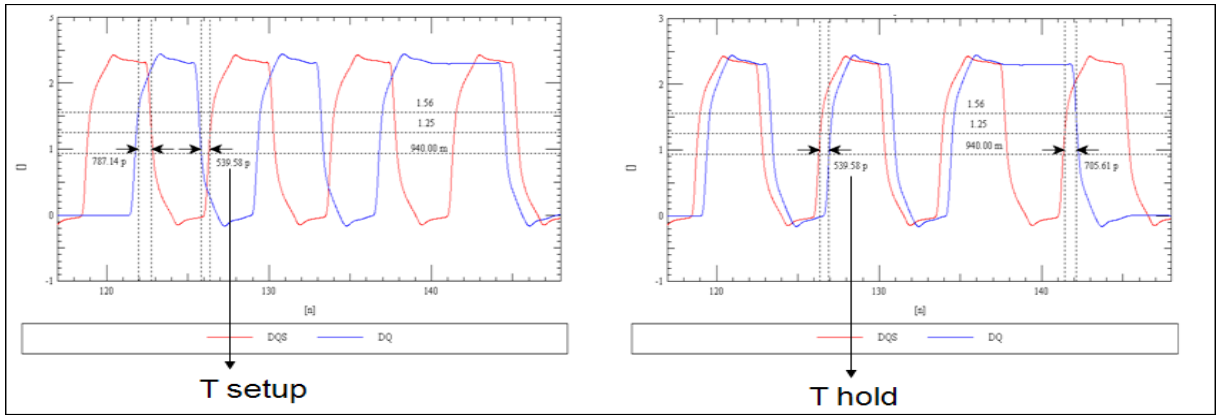
TOP NAME	DDR3_DATA_WRITE	DDR3_DATA_READ	DDR3_ADDR_CK
Timing	NODES NAME1	NODES NAME1	NODES NAME3
From:	CPU	DDR3（HYNIX）	CPU
To:	DDR3（HYNIX）	CPU	DDR3（HYNIX）
Vil/Vih	0.925/0.575	0.925/0.575	
Tsetup	0.2	0.3	0.3
Thold	0. 2	0. 15	0. 3
Vmeas	0. 75	0. 75	0. 75
Tva_min	0. 3	0.36	0.95
Testload@Tcomin			
Tvb_min	0. 3	0. 36	0. 95



Traditional Timing Design for DDRx System

- Using Simulations



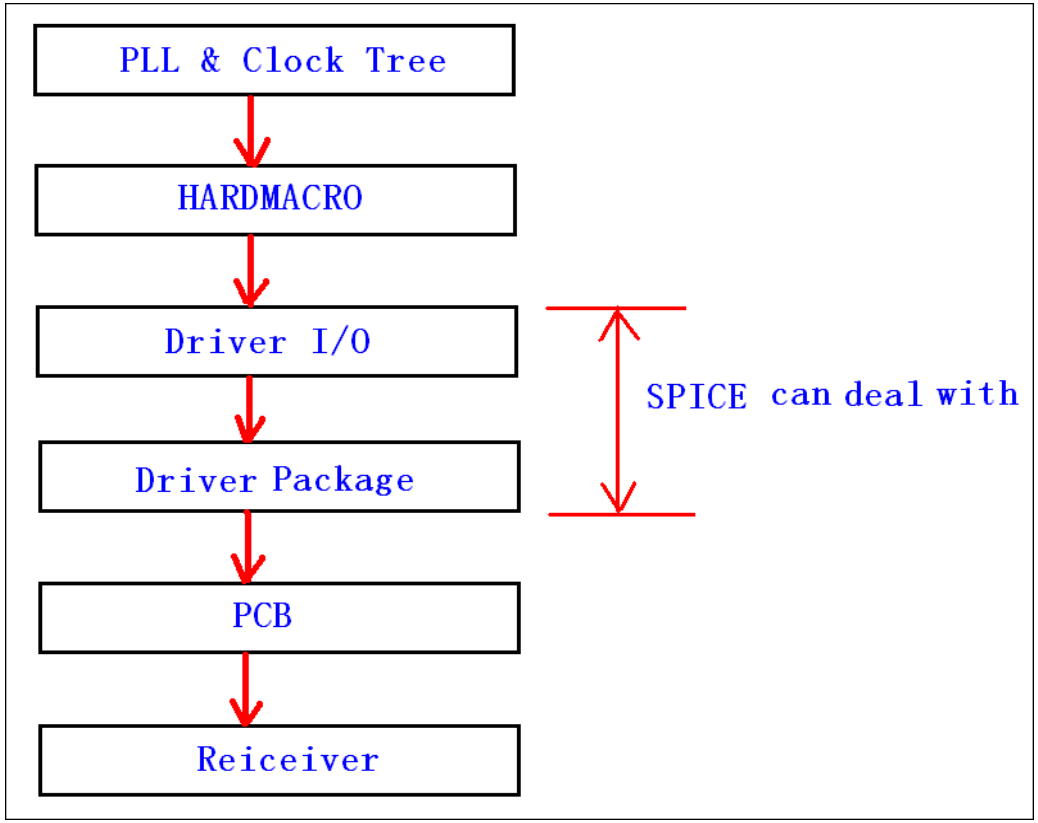


Traditional Timing Design for DDRx System

- Disadvantages of Traditional Methods:
  - It doesn't consider the influences of follow list:
    - SSN of PDN
    - Many Kinds of Jitter, Such as DQS Jitter…
    - Xtalk of Package and PCB

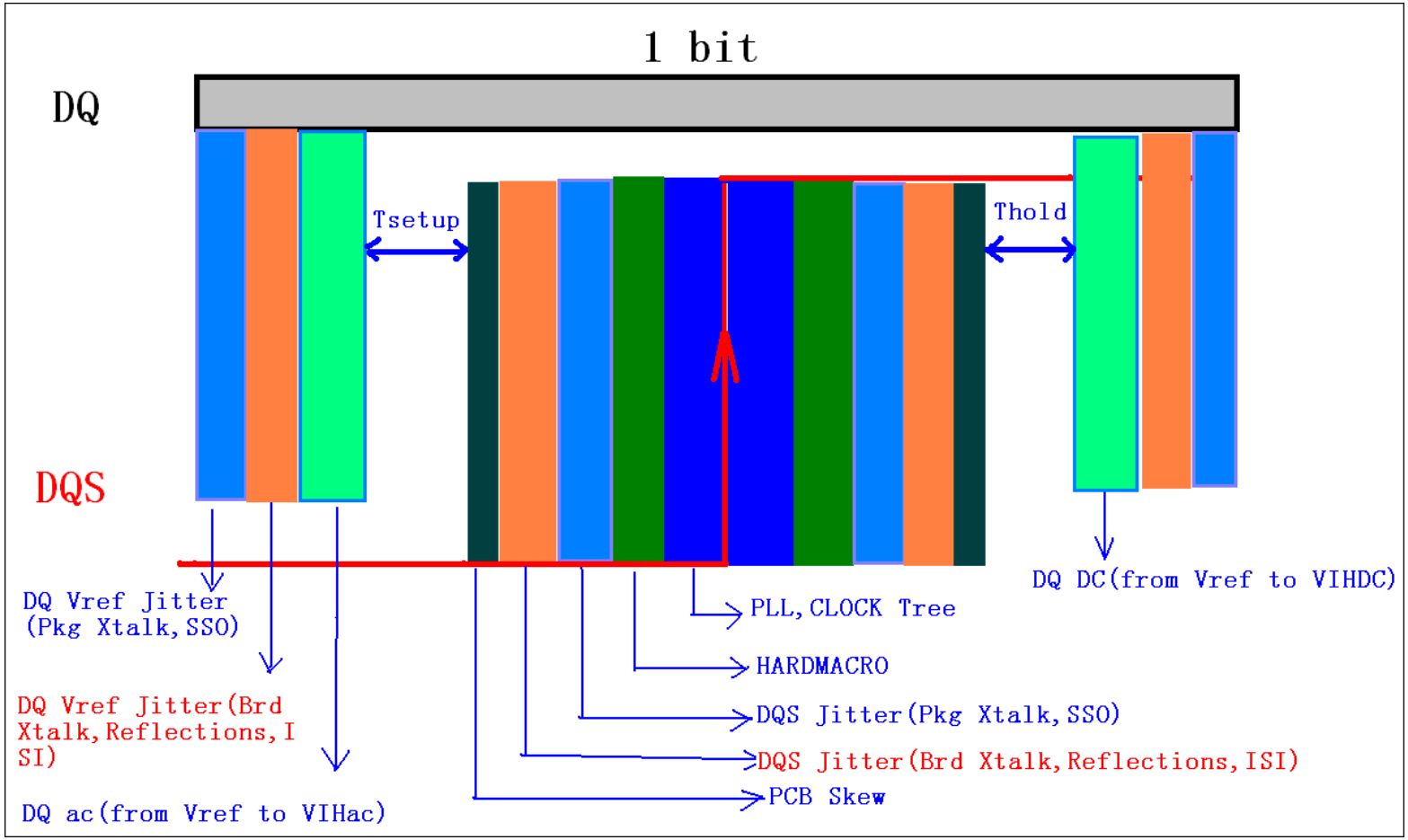
Methods for DDR3 System Timing Budget Analysis

- The DDR3 timing budget consists of observing timing margins and signal integrity of the entire interconnect
- Summarized as follows in the diagram below:



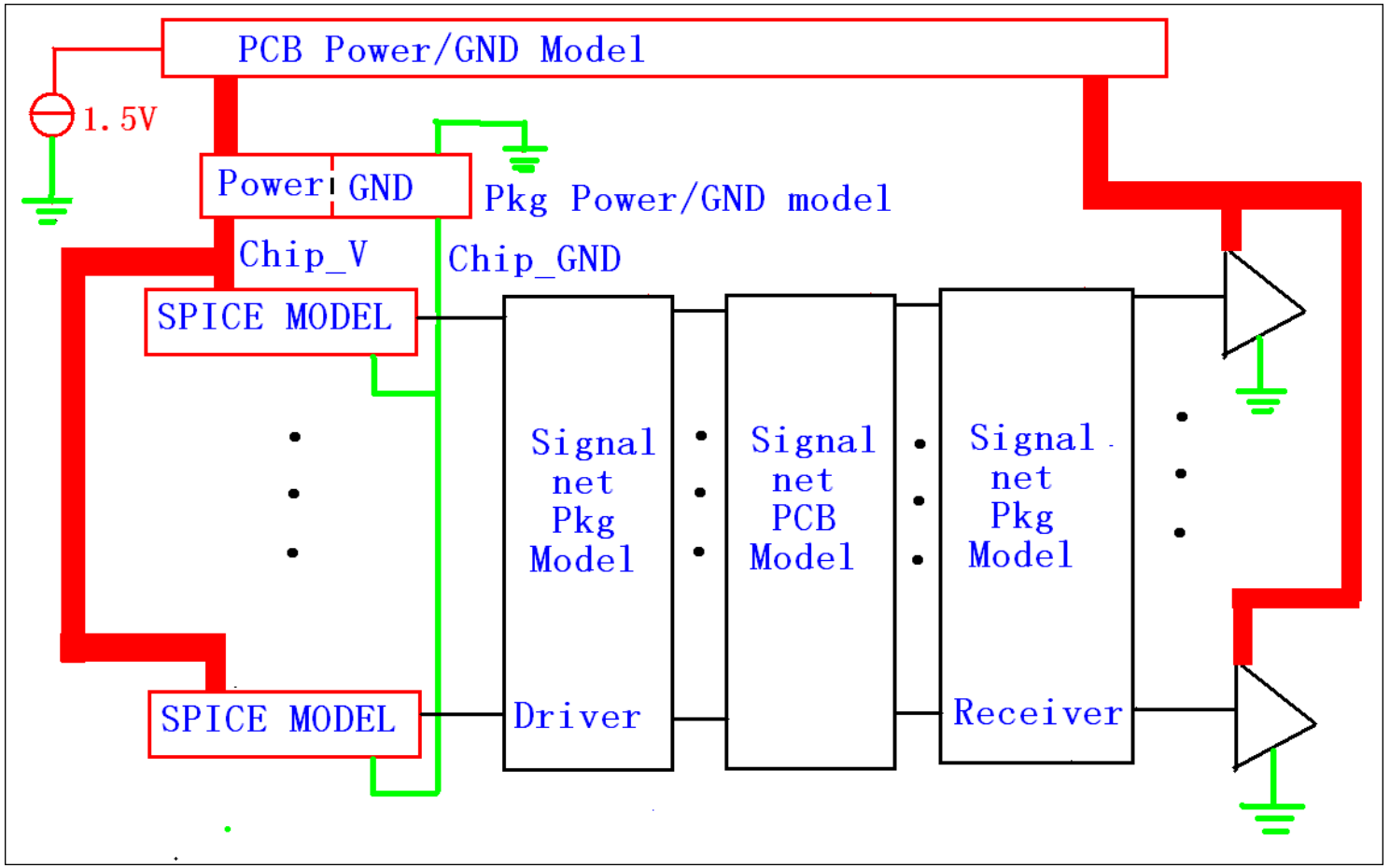
Methods for DDR3 System Timing Budget Analysis

- Timing Calculation method:

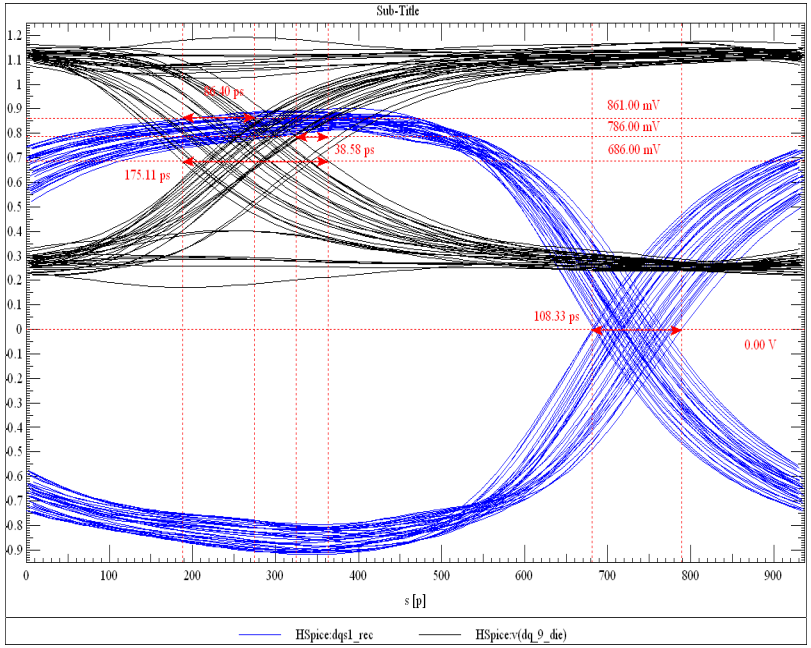


Methods for DDR3 System Timing Budget Analysis

- The Topology of DDR3 System Timing Simulation Using SPICE Models



Methods for DDR3 System Timing Budget Analysis



- An Example of DDR3 Simulation
  - Twc_io_dqs_jitter+Tbrd_io_dqs_jitter= 108.33 ps
  - Twc_io_dq_jitter_vref+Tbrd_io_dq_jitter_vref=175.11 ps
  - Tbrd_io_dq_jitter_ac=86.40 ps
  - Tbrd_io_dq_jitter_dc=38.58 ps

- Cuting all Timing Uncertainties：
  - Tsetup_min_margin=21ps
  - Thold_min_margin=32ps

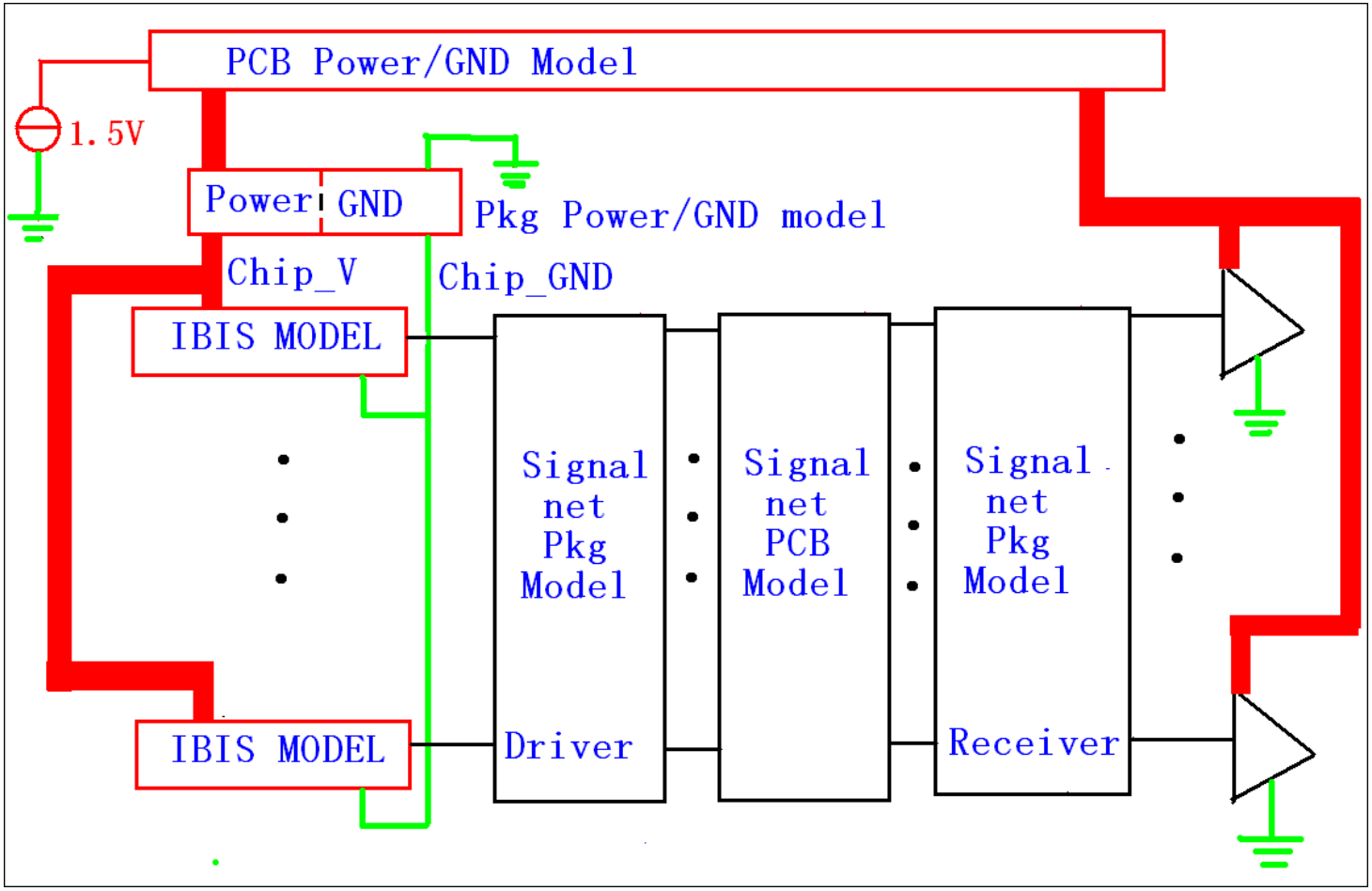
Methods for DDR3 System Timing Budget Analysis

- Analysis sources of uncertainties

Uncertainty	Source
PLL, CLOCK Tree	IC Manufacturer
HARDMACRO	IC Manufacturer
DQS Jitter(Pkg Xtalk, SSO)	IC Manufacturer
DQS Jitter(Brd Xtalk, Reflection, ISI)	Simulation Using SPICE model
DQ Vref Jitter(Pkg Xtalk, SSO)	IC Manufacturer
DQ Vref Jitter(Brd Xtalk, Reflection, ISI)	Simulation Using SPICE model
PCB Skew	PCB file
DQ ac(from Vref to VIHac)	Simulation Using SPICE model
DQ DC(from Vref to VIHDC)	Simulation Using SPICE model

Methods for DDR3 System Timing Budget Analysis

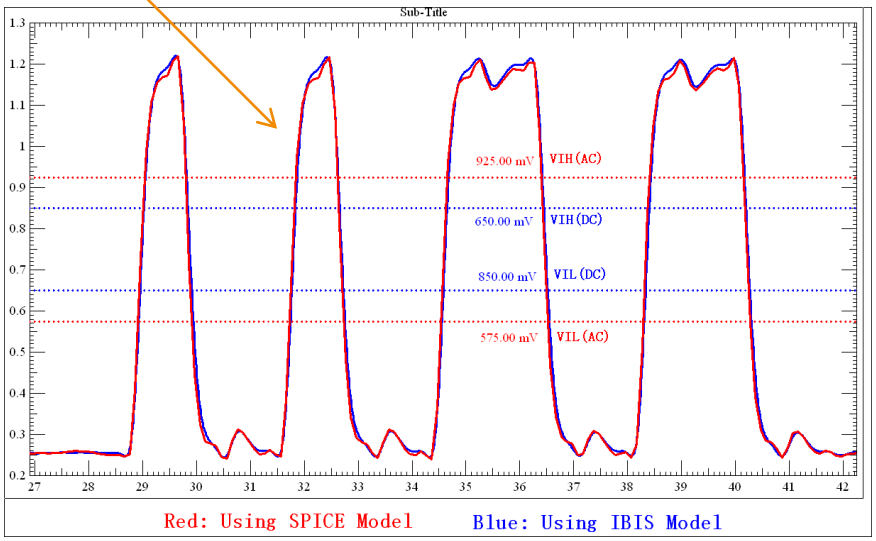
- The Topology of DDR3 System Timing Simulation Using IBIS Models



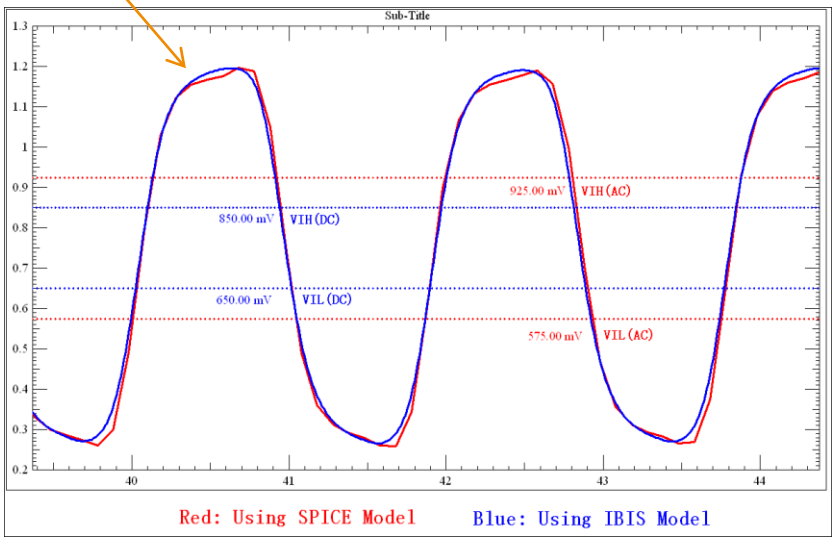
Comparison of Two Simulation Results

- Analysis Precision
  - Waveforms comparison

DQ

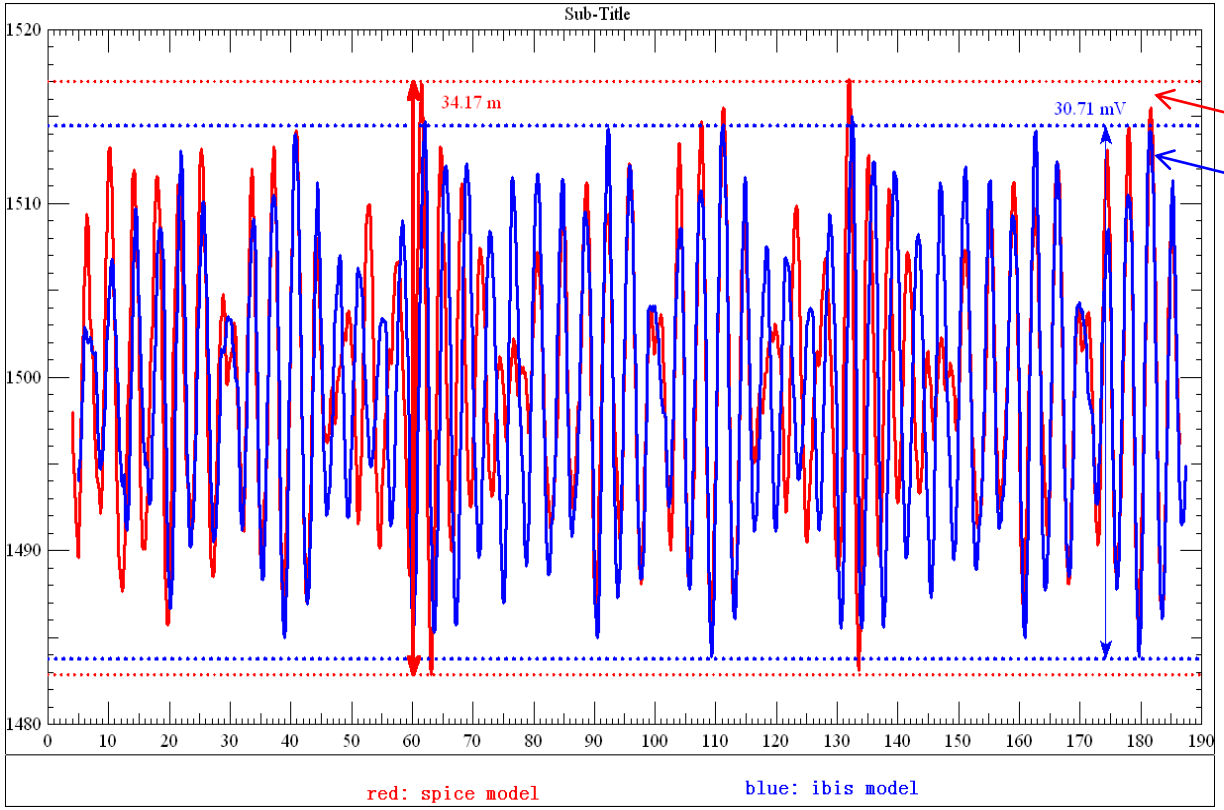


DQS



Comparison of Two Simulation Results

- Analysis Precision
  - △Vpp comparison



Spice: 34.17mV
IBIS: 30.71mV

Comparison of Two Simulation Results

- Comparison Time Consuming

Workstation	2*Intel Xeon X5680,3.33GHz,12MB Cache,6.4GT/s; 96GB (12x8GB) DDR3 RDIMM , 1333MHz	Intel Core™ 2 Duo CPU 3.00GHz 3.37GB
Simulation Time	**40 h** **128bits**	**1 min** **128bits**

- Using IBIS model is very effective in DDR3 system timing simulation .

Summary

- Choosing an appropriate modeling method is critical for simulation. Otherwise simulation may not be accurate enough or too complex and time consuming.
- The traditional way to simulate DDR3 system timing is not precise enough, because DDR3 Timing simulations need to consider all the uncertainties.
- Using the SPICE model in DDR3 timing simulation is precise, but time consuming. It’s not a very effective way to work.
- IBIS model is appropriate for what-if analysis due to its relative short run time and sufficient accuracy.

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