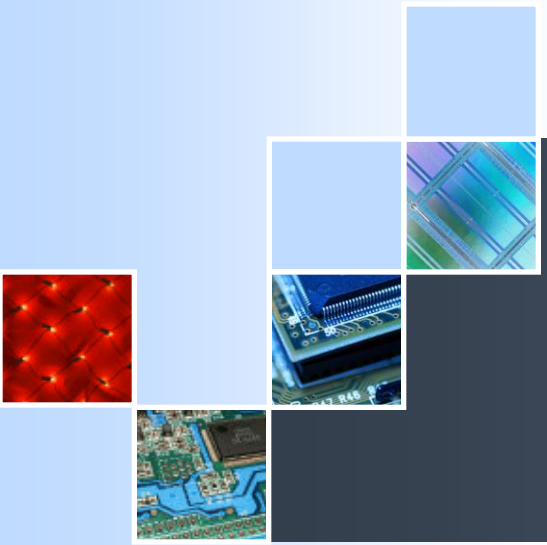

Power-aware I/O Modeling for High-speed Parallel Bus Simulation

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Shanghai China
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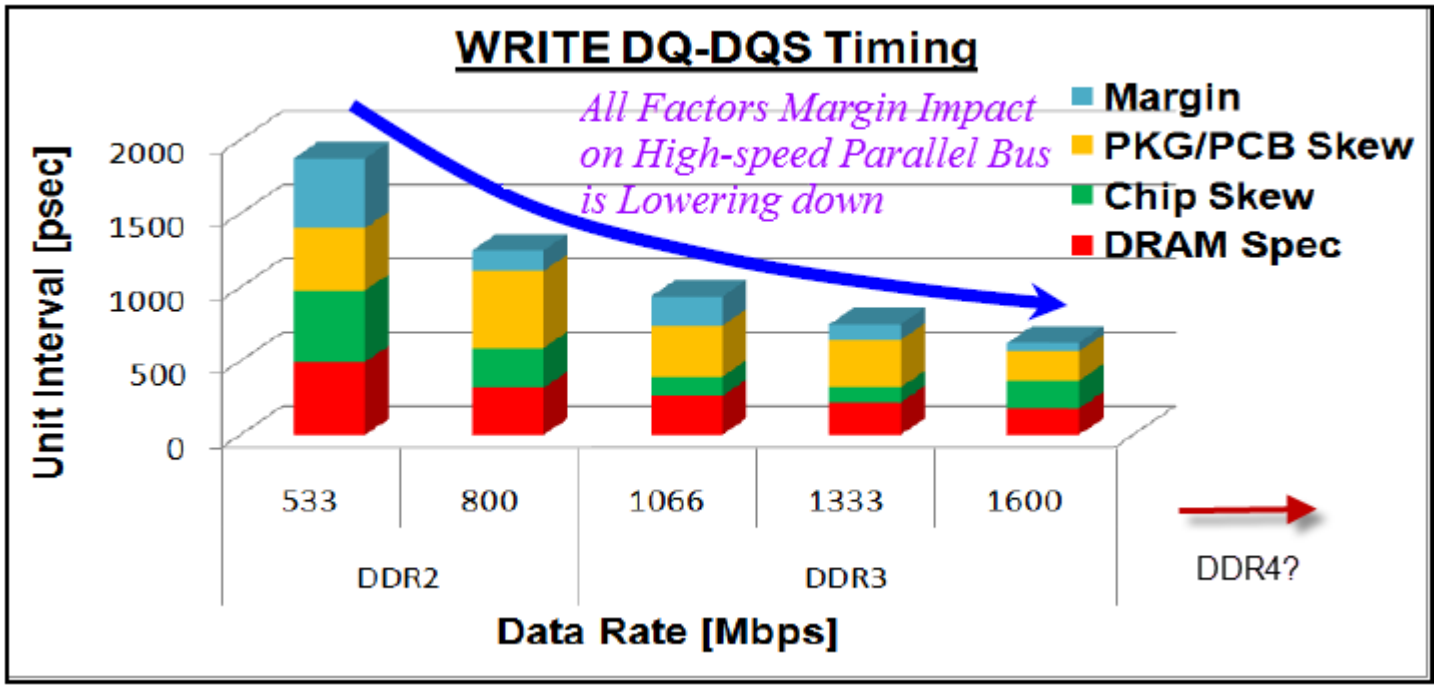
SIGRITY

Outline

- Challenge of High-speed Parallel Bus Simulation
- Power-aware I/O Modeling Progress
  - Necessity of Power-aware I/O Modeling
  - IBIS5.0 Enhancement (BIRD95/BIRD98)
  - Go beyond with IBIS5.0 – IBIS Plus
- Apply Power-aware I/O Model in Parallel Bus SSO Simulation
  - Power noise correlation
  - Signal output correlation
- Summary

Challenge of High-speed Parallel Bus Simulation

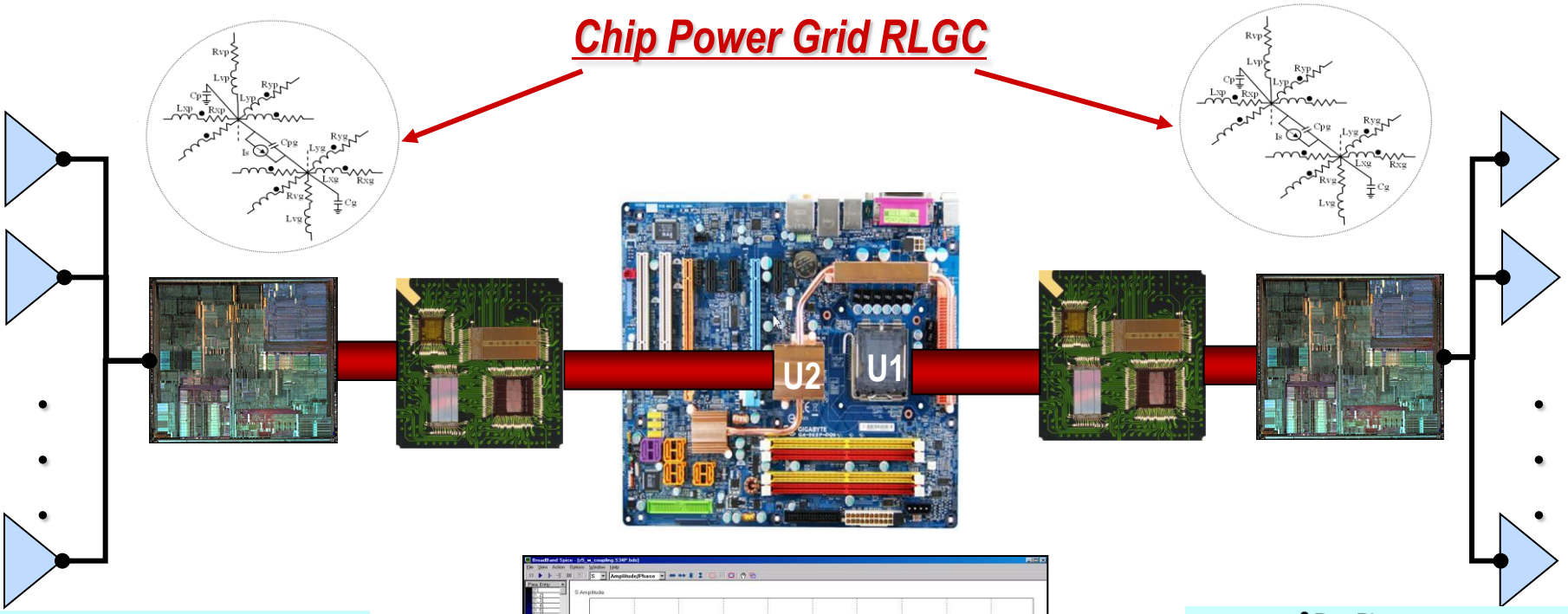
Challenge for High-speed Parallel Bus Design

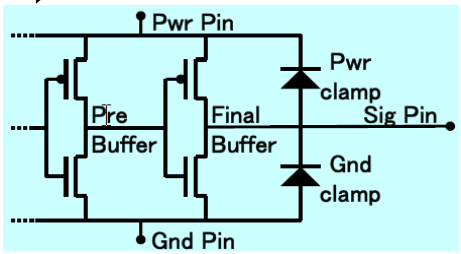


- The margin for jitter/skew is getting more smaller in current high-speed parallel bus design
- The power/ground noise has became a dominate reason that cause parallel bus failure
- Power/ground to signal EM coupling should be considered in system level SSO analysis for current high-speed parallel bus timing sign-off

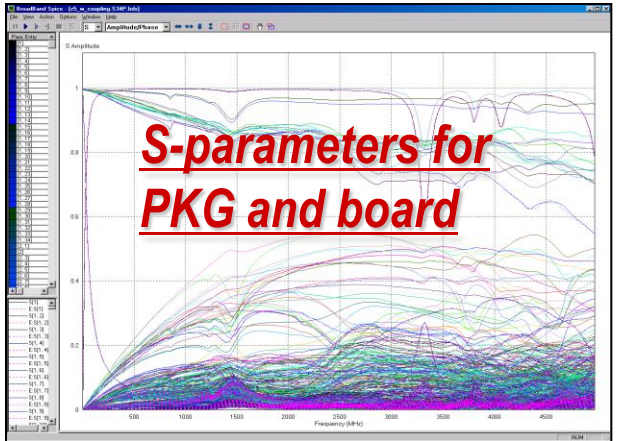
Challenge for High-speed Parallel Bus SSO Simulation

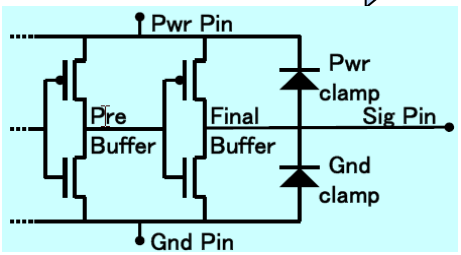
- If this is a 32 bits data SSN analysis, how long will this SPICE DECK run? will the waveform be converged?





Transistor model

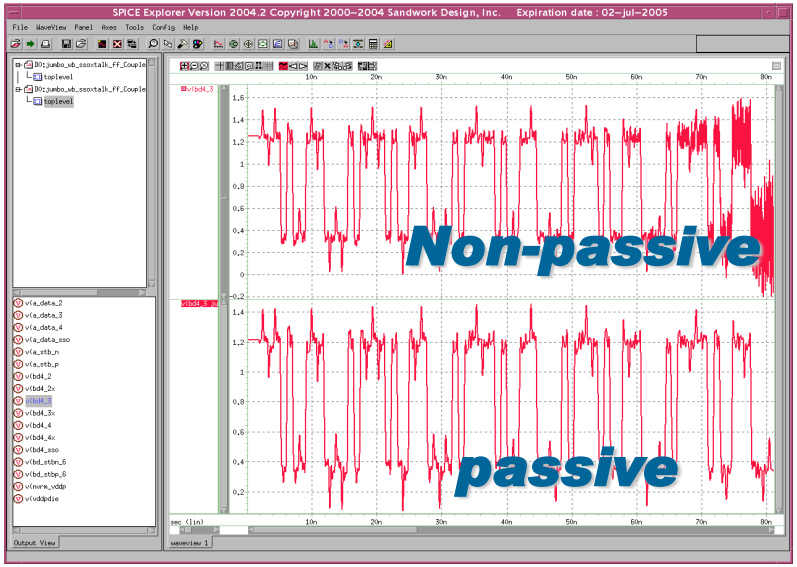




Transistor model

Problems in High-speed Parallel Bus SSO Simulation

- The complex manual task for the nodes linkage between circuits.
- No guaranteed for passivity and causality on each circuit block especially that model is from measurement
- Non-linearity of the whole system circuit network which including drivers and receivers transistor models
- Lost DC accuracy without low frequency data from EM solver, especially for SI analysis with power aware
- Long run time
- Waveforms are non-convergence
- …….



I/O Transistor vs. IBIS Modeling

Summary

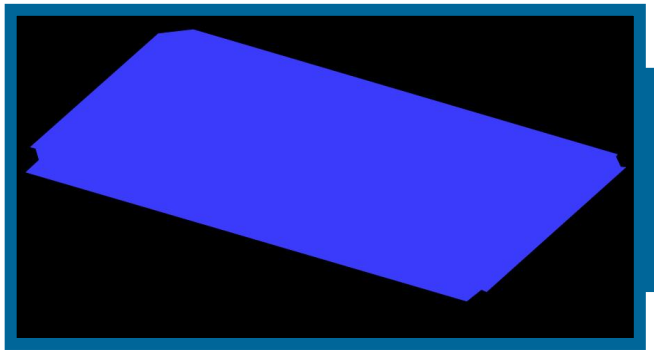
I/O Transistor Netlist	IBIS Model
▪ Extracted from complete design topology, all parasitics and device library included ▪ Parameters, design information	▪ I-V/V-T tables for the final stage ▪ Pin out information

Trade-off

	I/O Transistor Netlist	IBIS Model
Accuracy (SI)	Good	Good
Accuracy (PI)	Good	Enhanced in Ver5.0
Simulation Time	Slow (Usually 10X than IBIS)	Fast
Supported by EDA Tool	Not good	Good (Many EDA tool supported)
Ease of distribution	Bad (IP Consideration)	Good (IP Protection)

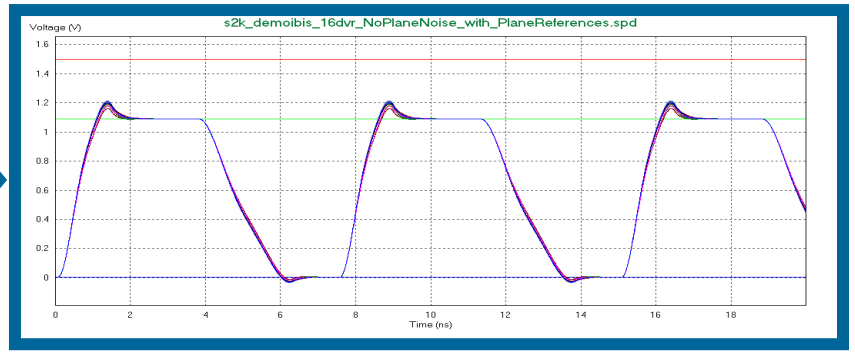
Power-aware I/O Modeling Progress

The Importance of Power-aware Analysis

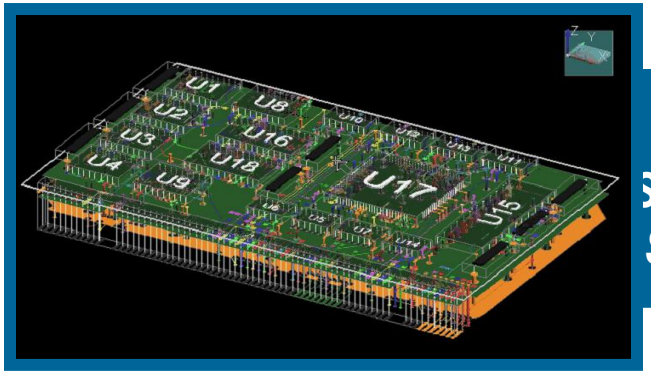


Signal data only

Predicts No SSN

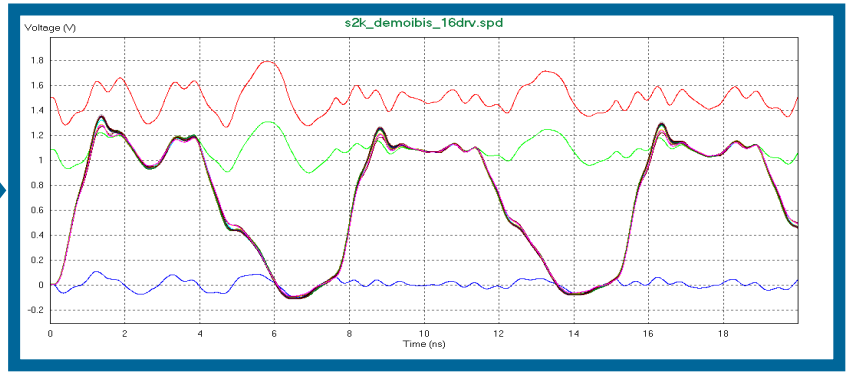


Simulation assuming ideal power delivery network



Signals, accurate planes, vias

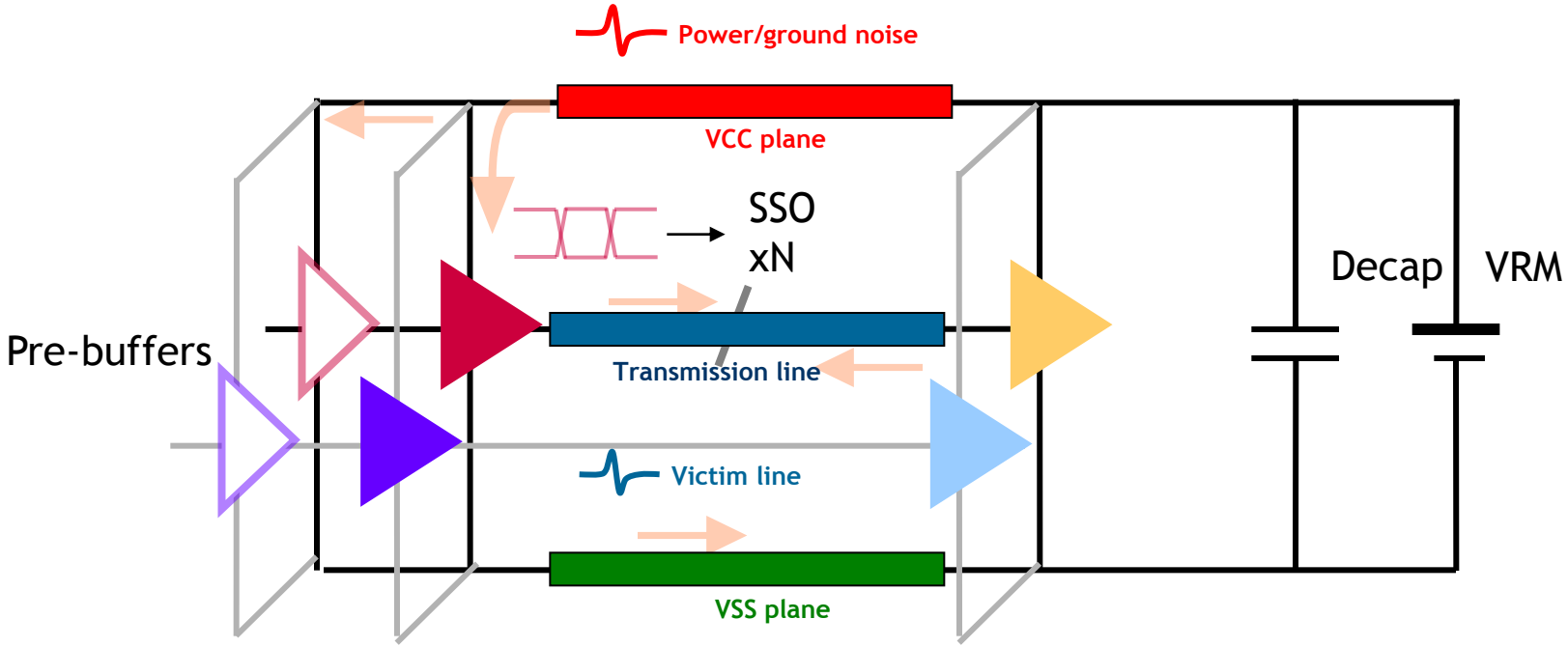
Predicts Significant SSN Risk

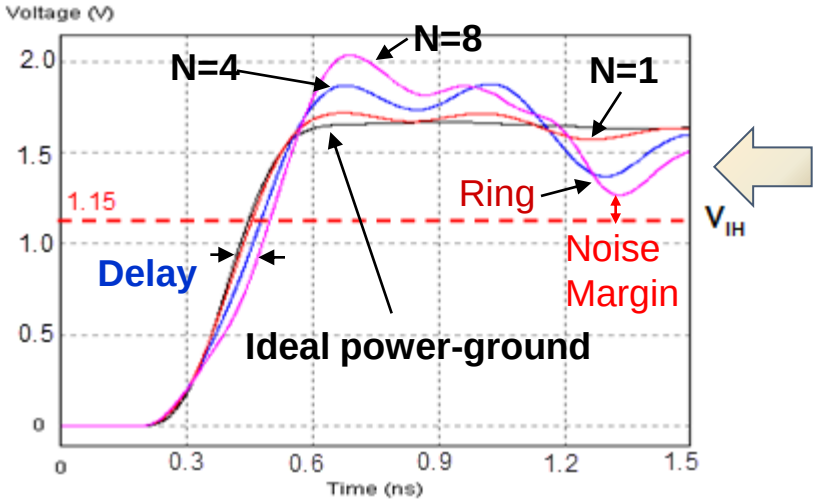


Simulation with all power delivery effects

- Transmission line only analysis can't reveal the real signaling among ICs in current high speed parallel bus design.
- High-speed parallel bus with power-aware analysis can help to identify design defect and find out the root cause behind the problem.

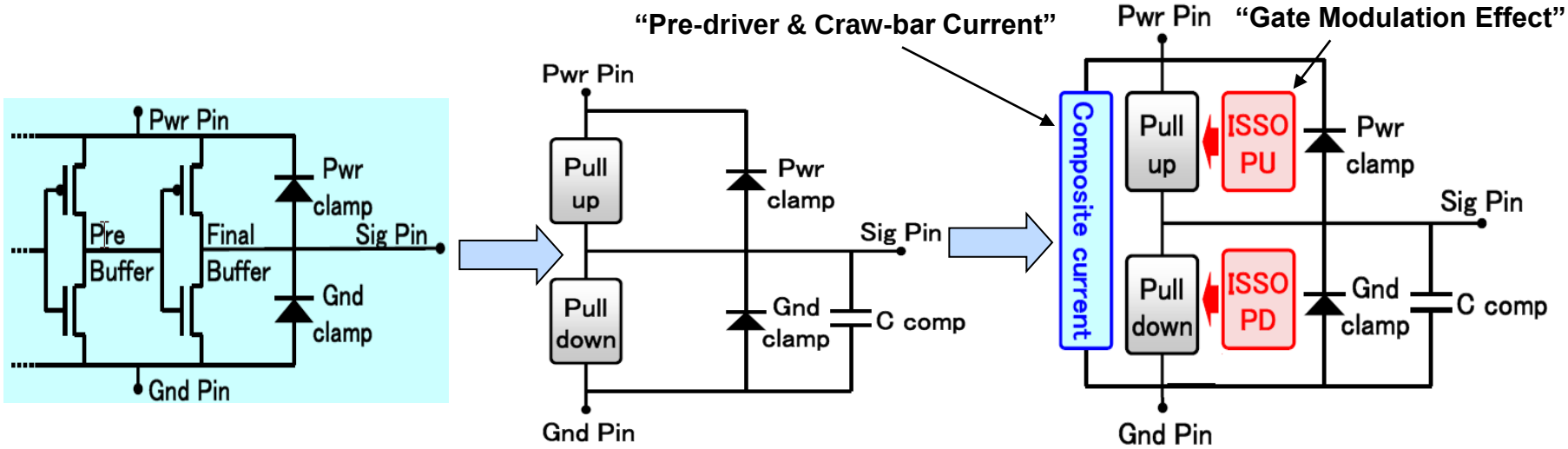
How SSN Noise Impact on Signal Quality





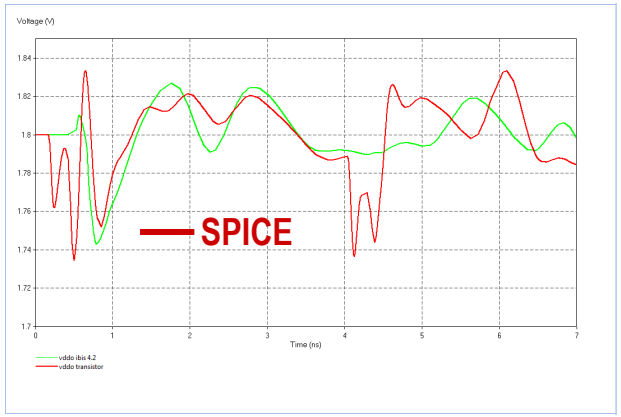
- **SSN noise greatly reduce the noise margin at receiver bump**
- ***SSN noise increase the buffer output delay and finally the jitter, which may cause error-sampling at receiver side***

Power-aware Solution in IBIS5.0 (BIRD95/BIRD98)

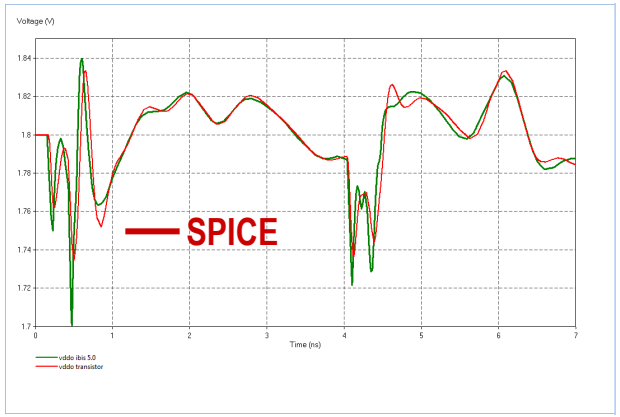


Ideal Power **Power-aware (BIRD95 & 98)**

Accuracy is always concerned while using behavior model. Is it good enough for IBIS5.0?



IBIS4.2 vs. Transistor



IBIS5.0 vs. Transistor

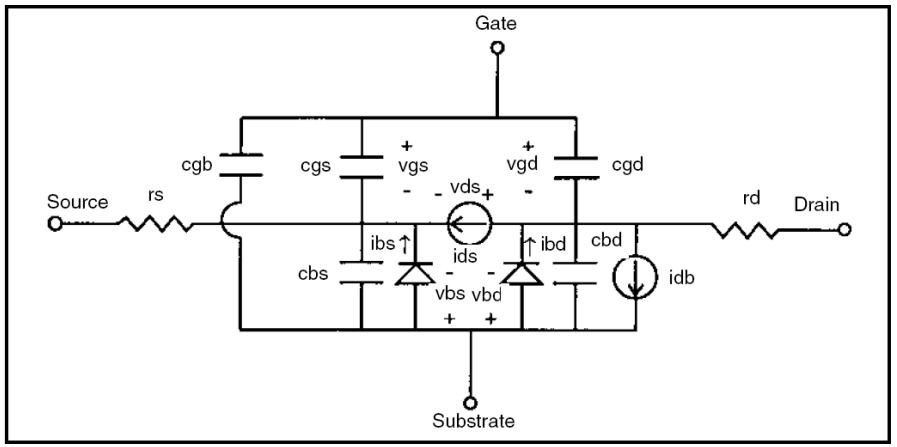
Go Beyond with IBIS5.0

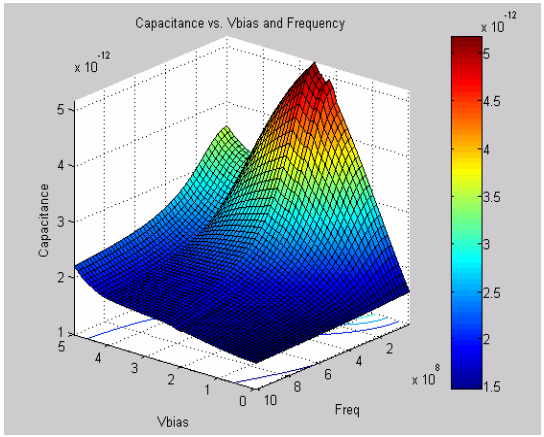
Advantage

- IBIS5.0 is designed for more accurate SI simulation with non-ideal power distribution system (PDS)
- IBIS5.0 greatly improves the correlation accuracy with transistor model with simple but effective methodology
  - By including composite current, more accurate power noise simulation can be performed to have better power/signal integrity evaluation
  - Dynamic power noise impact on signal output waveform is considered in IBIS5.0, which greatly improve the efficiency of using IBIS model in high-speed parallel bus timing sign-off

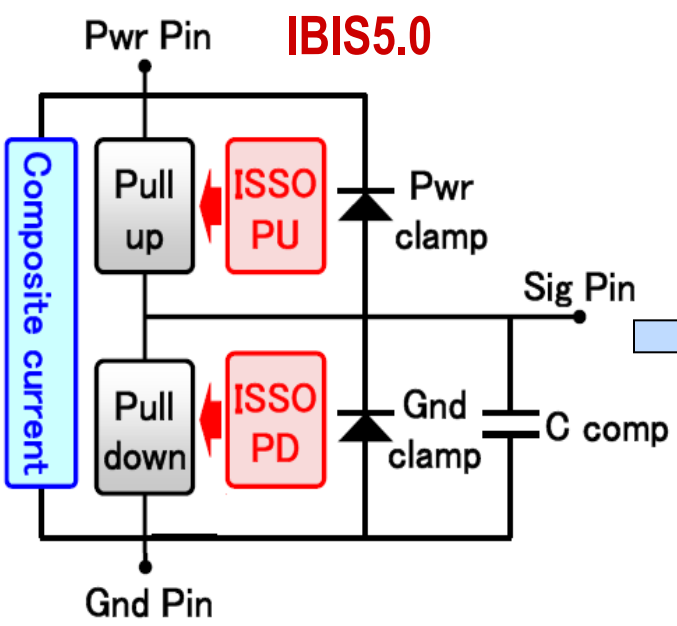
But it's good enough?

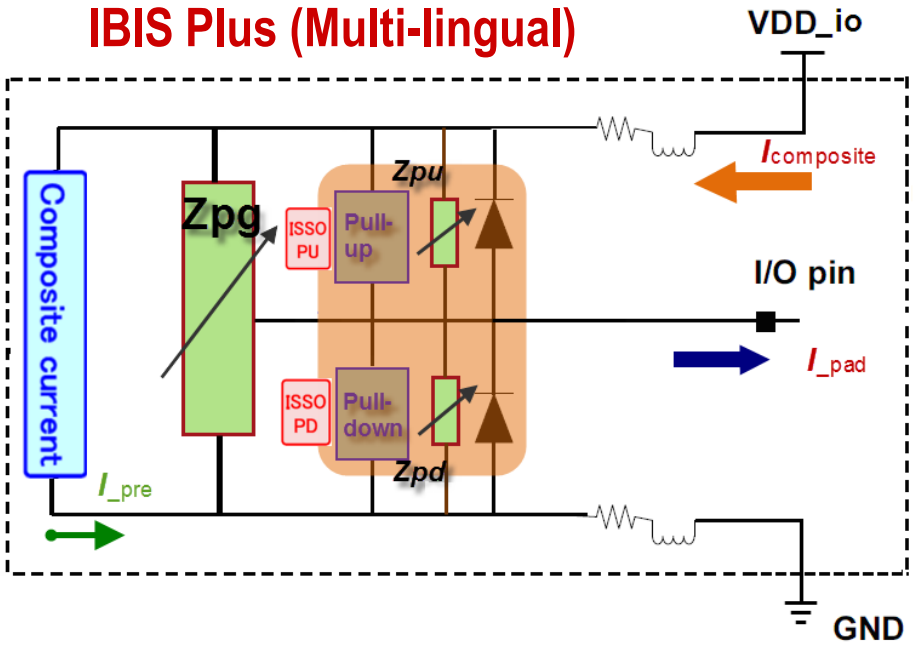
- On-die power/ground impedance is omitted
- The state-dependent non-linear output impedance is modeled with single or splited die capacitance, which may over- or under-estimate the buffer AC effects

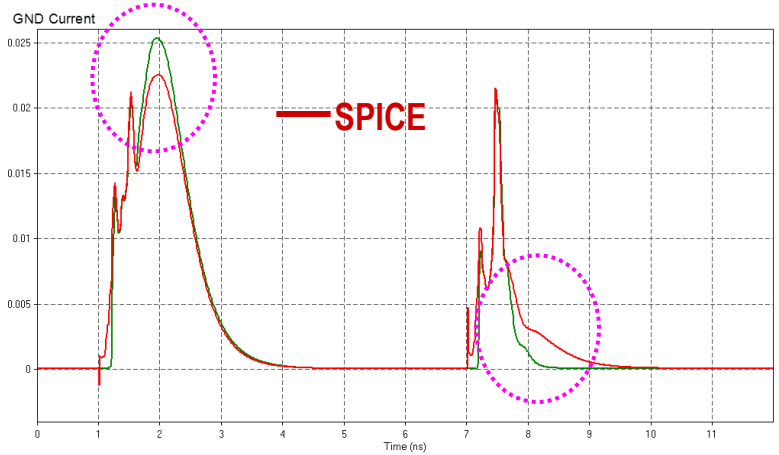




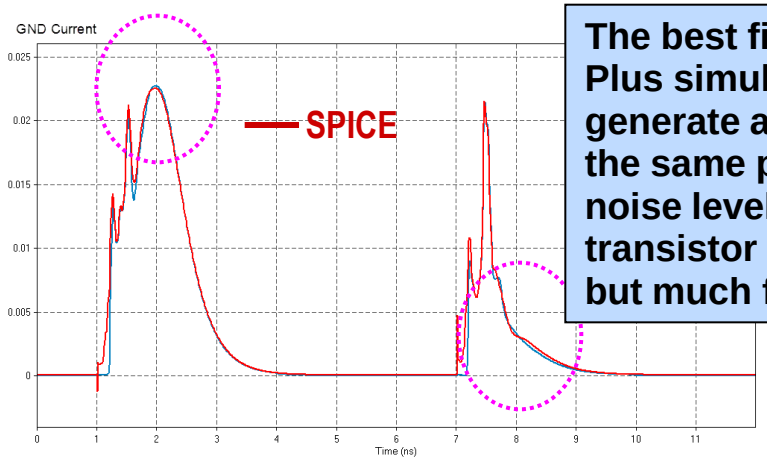
Go Beyond with IBIS5.0







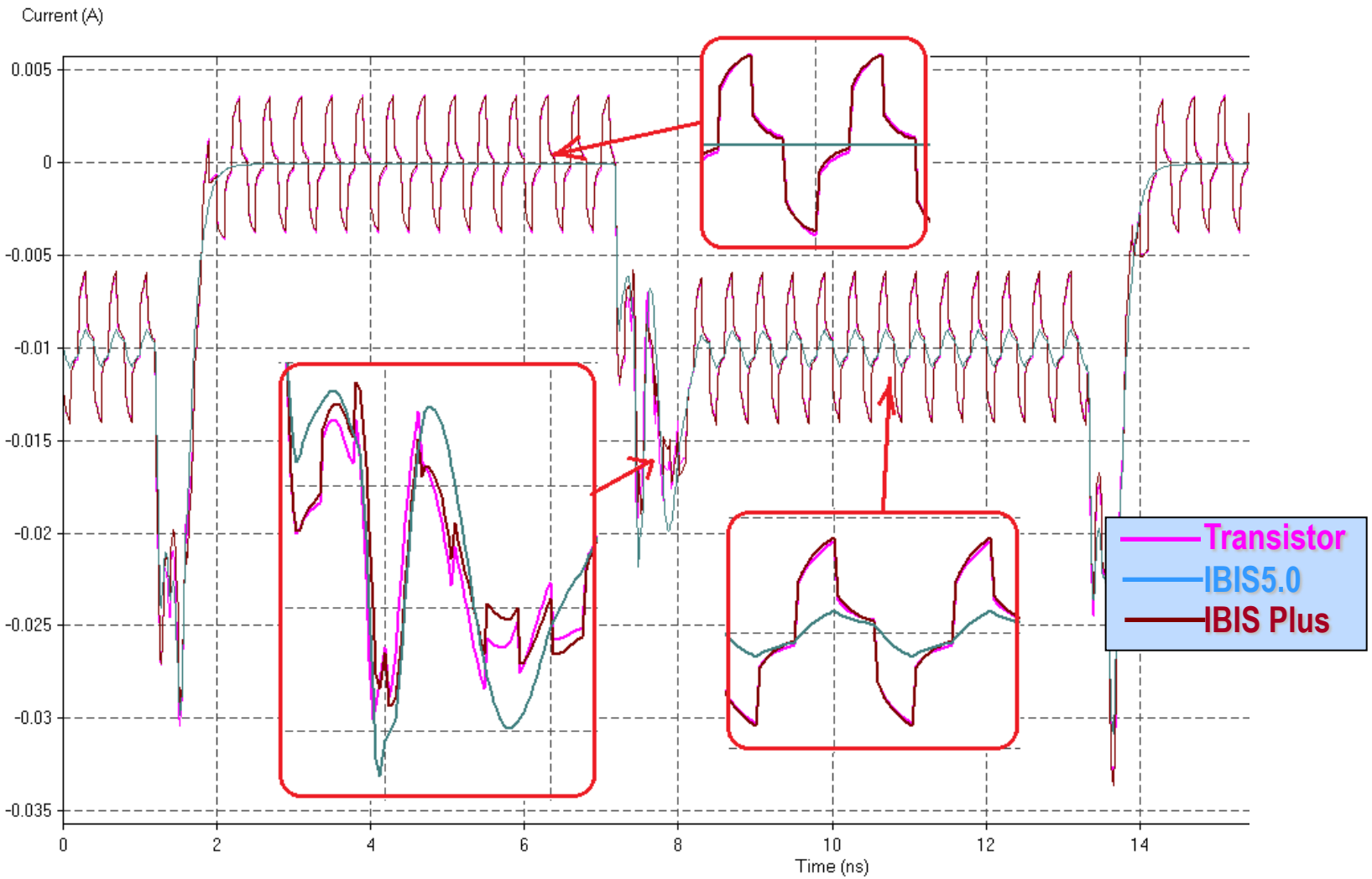
IBIS5.0 vs. Transistor



IBIS Plus vs. Transistor

The best fitted IBIS Plus simulation generate almost the same power noise level with transistor model but much faster

Go Beyond with IBIS5.0 (case study)



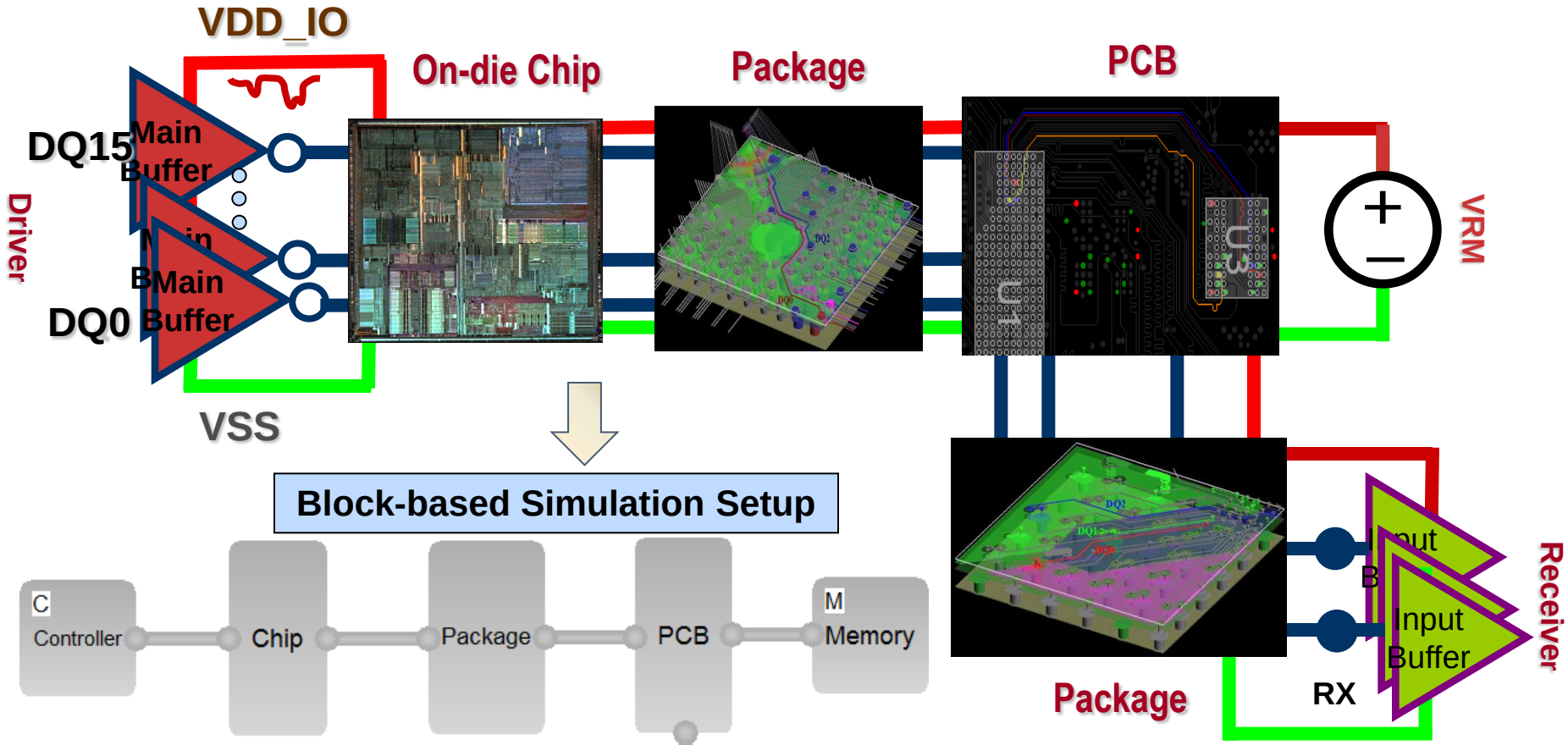
* *HSTL18 I/O, 150 Ohm termination in parallel with 1pF*

VCC=1.8V, 0.05V 2.5GHz AC noise

High-speed Parallel Bus SSO Simulation

DDR3 System-level SSO Simulation (case study)

System-level Correlation to consider all power fluctuation effects (IR-Drop, SSN, Delta-I …)



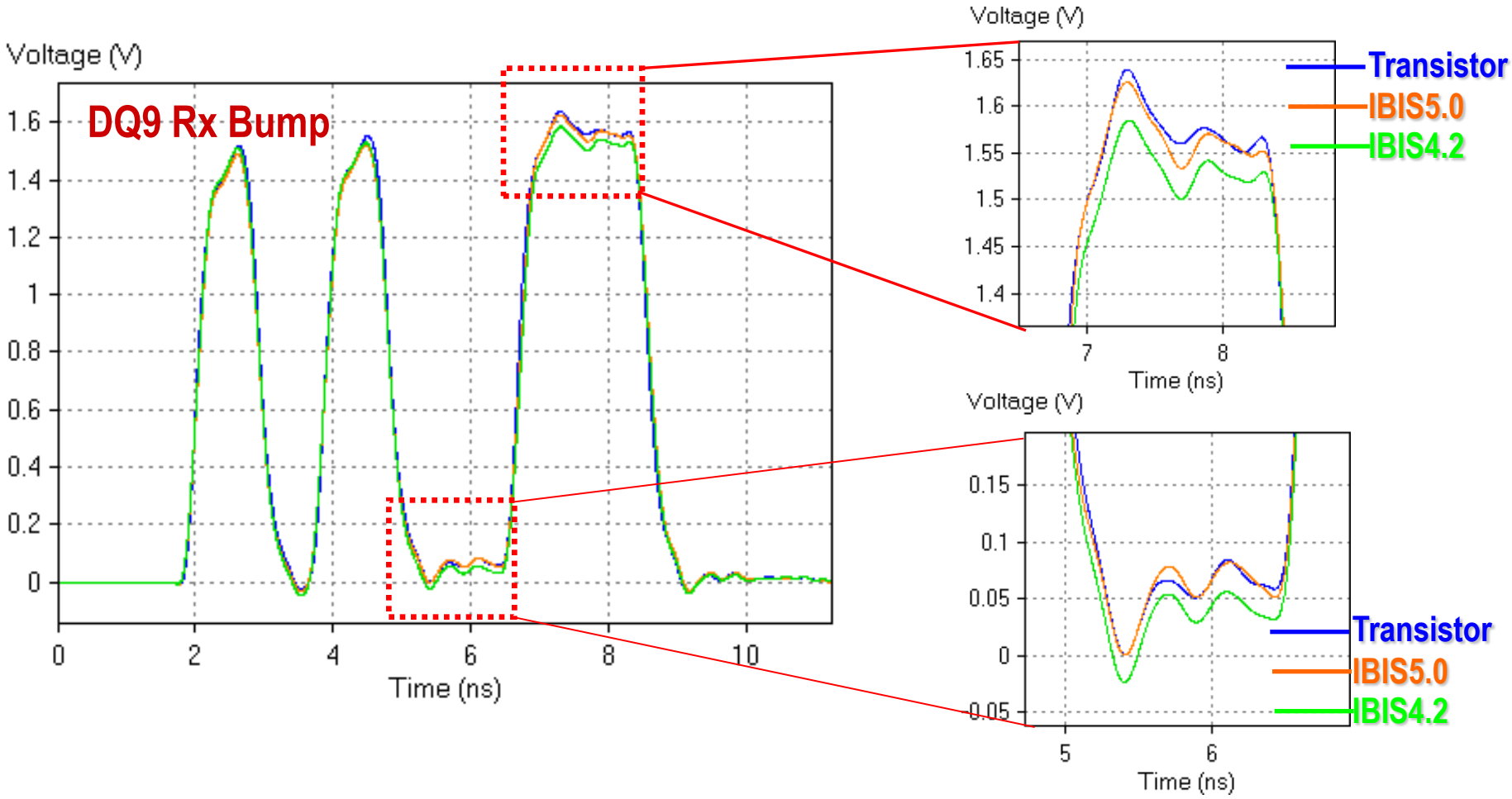
- package, board and on-die power grid model are considered in system-level view
- On-die power grid chip model is extracted in distributed format with all MOS caps included

- Non-ideal power/ground noise is accurately predicted by use of IBIS 5.0 buffer model
- To improve the convergence for time domain analysis, broadband PKG/board S-parameter model are converted into broadband SPICE circuit

DDR3 System-level SSO Simulation (case study)

Signal Output Waveform Comparison (IBIS4.2 vs. IBIS5.0)

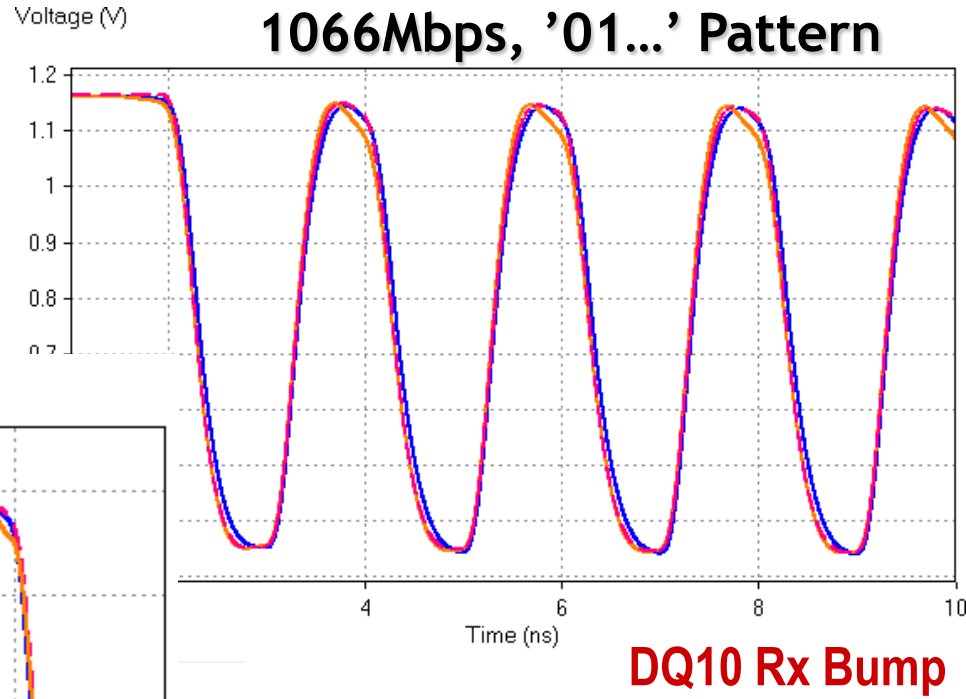
1066Mbps, “10100110” Input Pattern

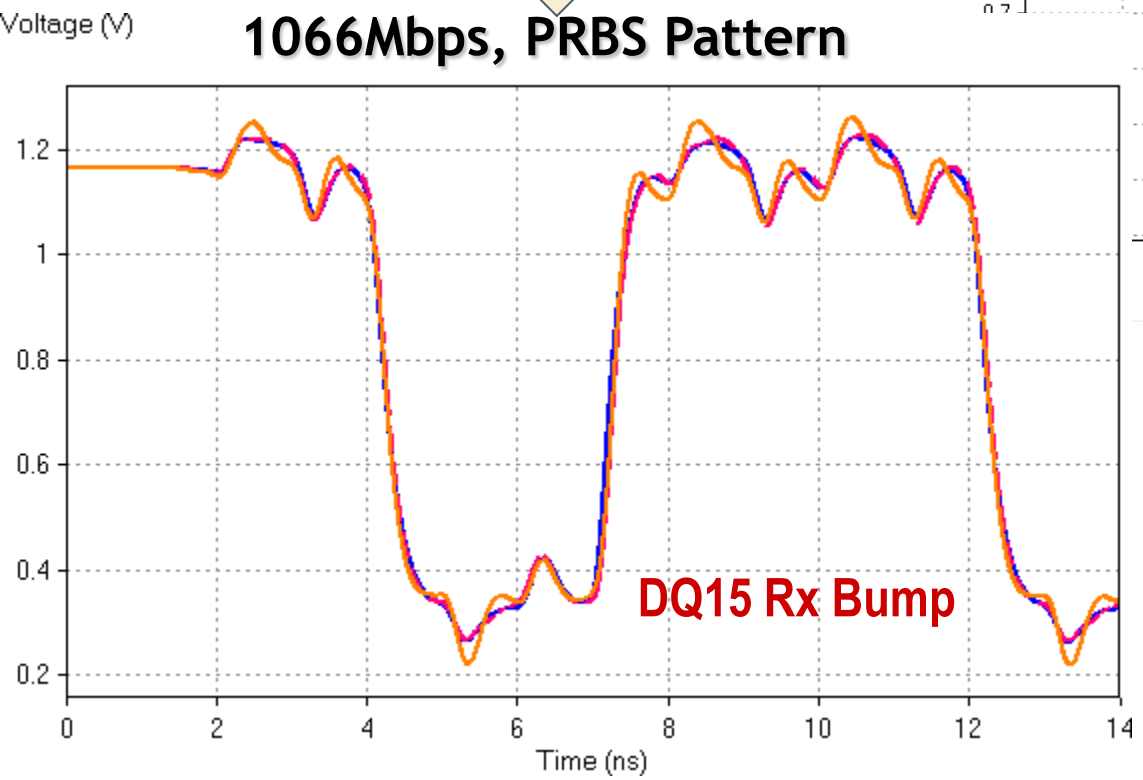


DDR3 System-level SSO Simulation (case study)

Signal Output Waveform Comparison (IBIS5.0 vs. IBIS Plus)

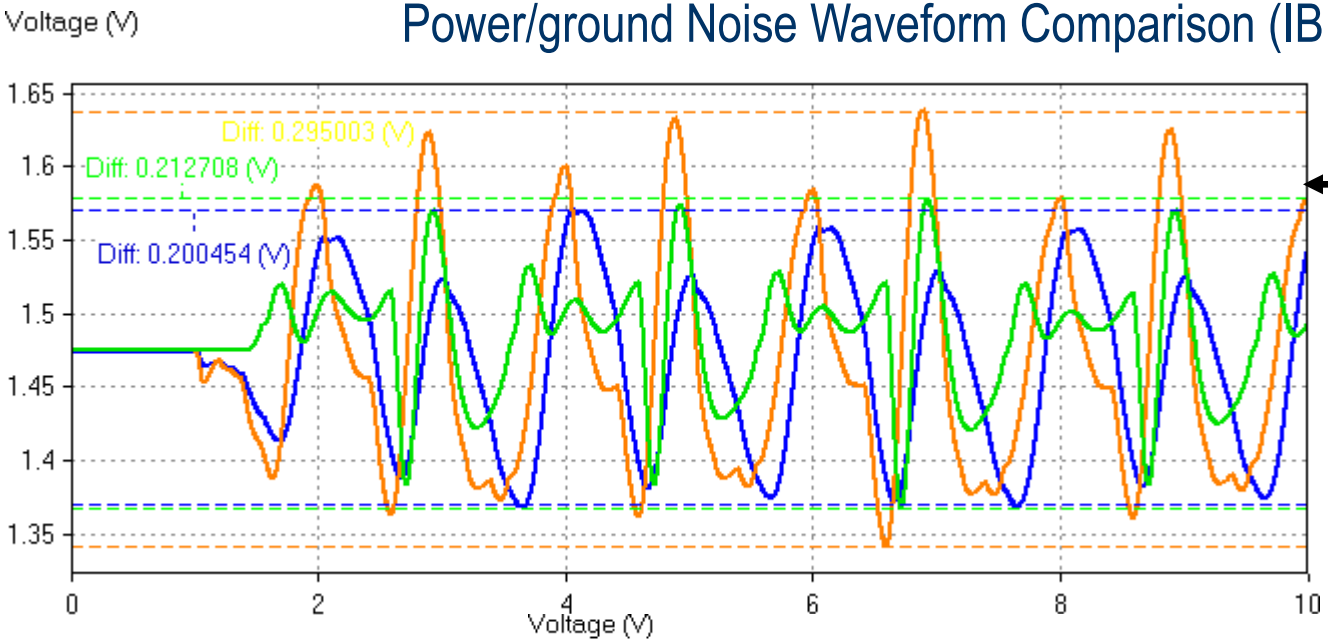
IBIS Plus model perfectly tracked the transistor model in signal output waveforms correlation





DDR3 System-level SSO Simulation (case study)

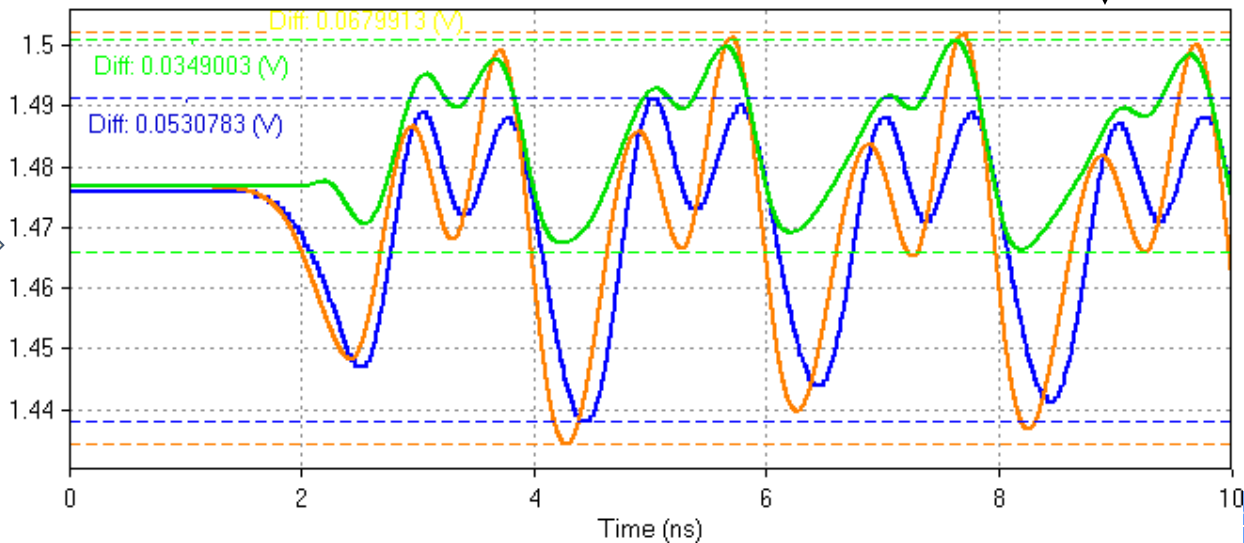
Power/ground Noise Waveform Comparison (IBIS4.2 vs. IBIS5.0)



Tx VDDQ~VSSQ Bump

Rx VDDQ~VSSQ Bump

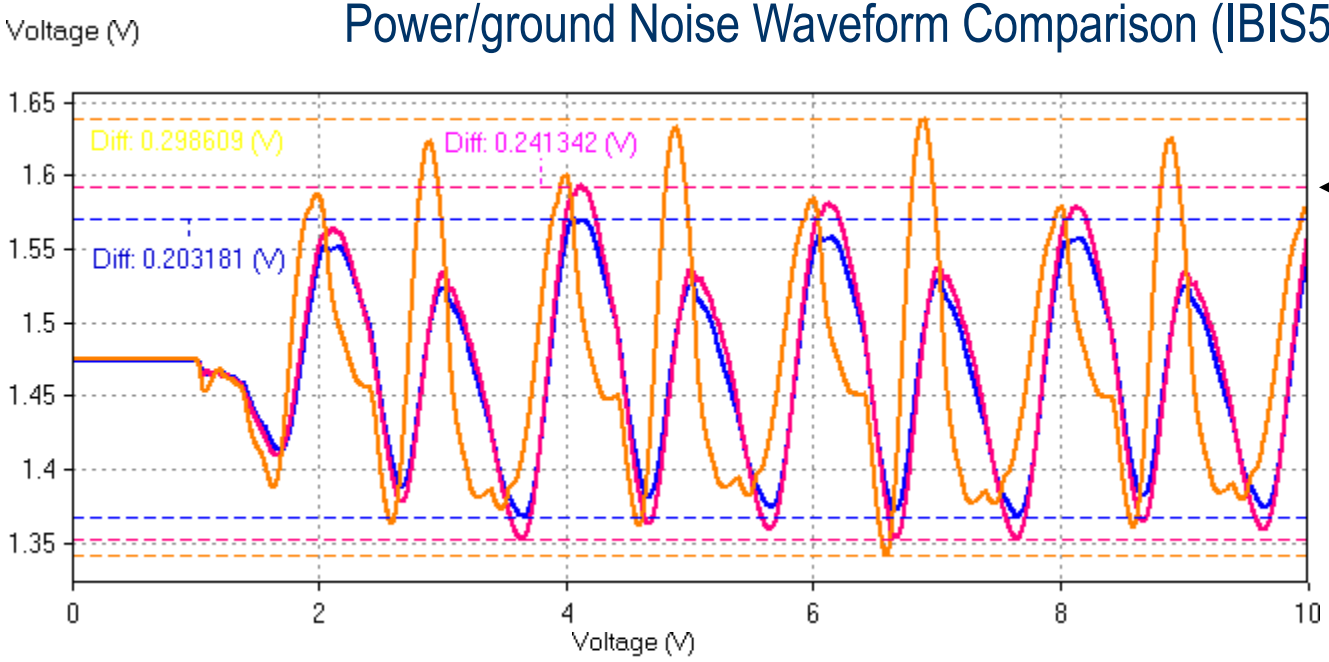
Transistor
IBIS 5.0
IBIS4.2



IBIS4.2 under-estimate but IBIS5.0 over-estimate the power/ground noise in this case

DDR3 System-level SSO Simulation (case study)

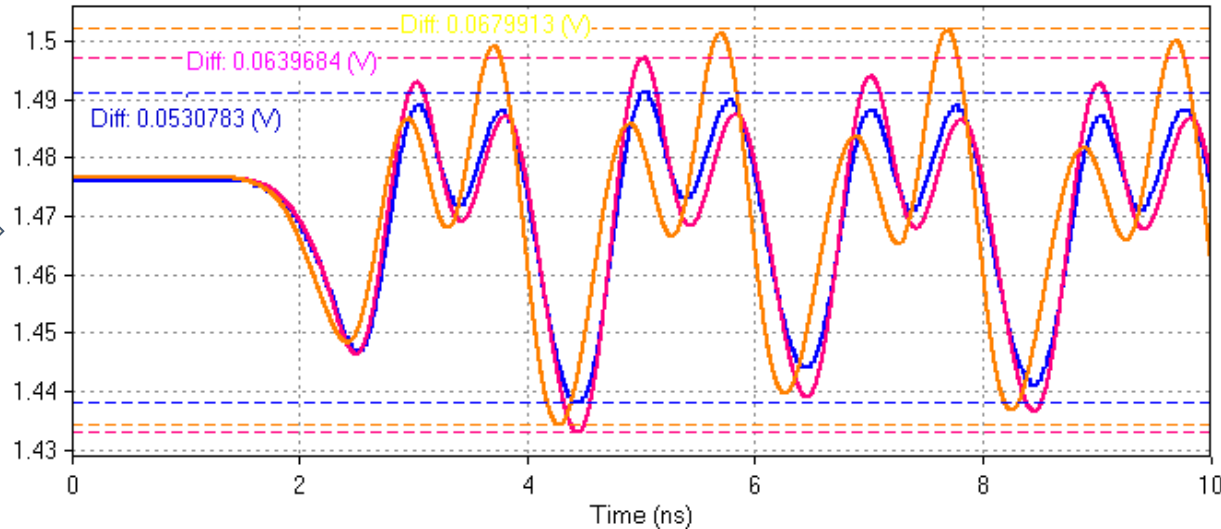
Power/ground Noise Waveform Comparison (IBIS5.0 vs. IBIS Plus)



Tx VDDQ~VSSQ Bump

Rx VDDQ~VSSQ Bump

Transistor
IBIS 5.0
IBIS Plus



IBIS Plus perfectly estimated the power/ground noise on Tx/Rx both sides

Summary

- Current high-speed parallel-bus and serial-link SI analysis require power-aware I/O model to run accurate SI analysis
- Latest IBIS5.0 improve on power-aware I/O buffer modeling with accuracy correlated in system-level SSO simulation
- Demonstrate a new method to generate more accurate behavioral circuit model (IBIS Plus) based on frequency-domain response fitting and can be delievered in IBIS compatible multi-lingual external model
- Both IBIS5.0 and IBIS Plus model show trustable accuracy in system level high-speed parallel bus simulation with non-ideal Power Distribution Network considered
- Block-level system-level simulation automation tool ease the simulation platform setup
- Need to expand the buffer modeling technology to differential (true/half) I/O and more complex I/O design

Thank You!