AMI Applications in High-speed Serial Channel Analysis and Measurement Correlation

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Agenda

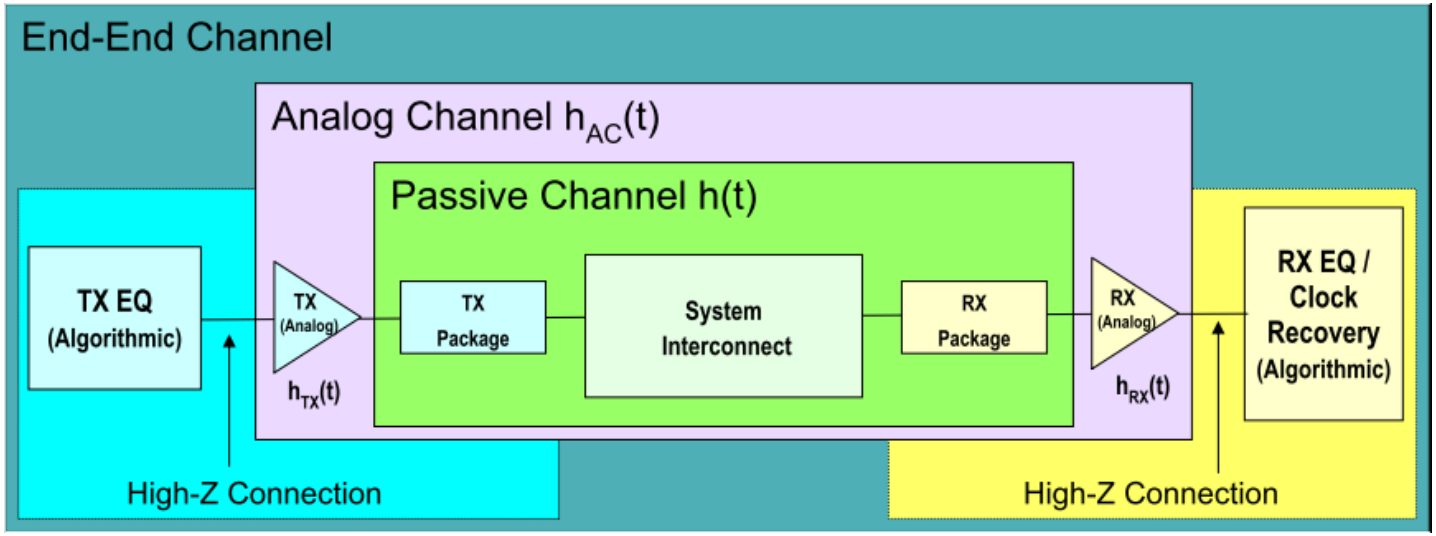
- IBIS-AMI Model versus Transistor-Level Model
- AMI Applications in High-speed Serial Channel Analysis
- AMI Model Accuracy Verification
- Summary and Suggestions

IBIS-AMI Model versus Transistor-Level Model

- **IBIS-AMI Model**
  - Accuracy simulation and fast run time
  - IP Protection
  - Supported by most EDA tools
  - AMI model to provide adaptive DFE, CDR, jitter and other simulation
- **Transistor-Level Model**
  - Good accuracy
  - models are derived from transistor-level netlist and layout
  - Relatively long simulation time and sometimes convergence problems
  - Intellectual property protection concerns

IBIS-AMI Model

- Combination of analog & algorithmic elements
- Analog part can be condidered linear and time-invariant
- Equalization and CDR can be modeled at the algorithmic part



Picture reference from"IBIS-AMI Terminology Overview"at DAC 2009 IBIS Summit

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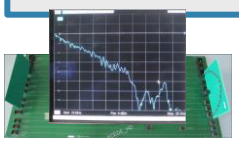
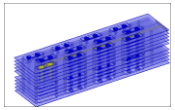
AMI Applications in High-speed Serial Channel Analysis

Methods in10Gbps serial channel analysis

Passive simulation& Test

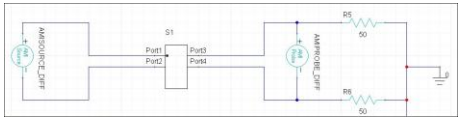
- Breadboard test
- 3D Model and Simulation





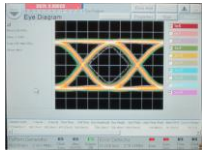
Active simulation

- Hspice Model
- IBIS-AMI Model

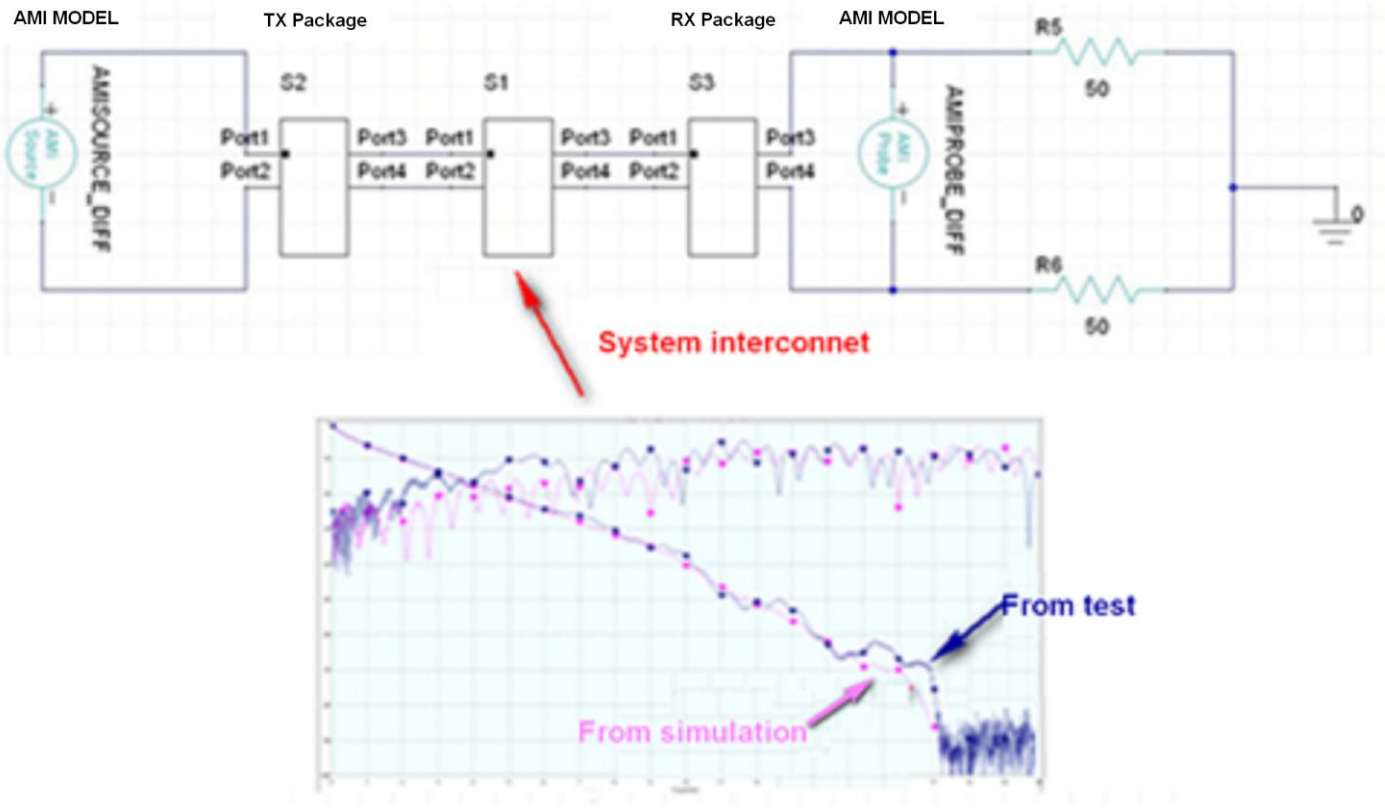


Active Test

- Chip and backplane interconnect system
- Eye test
- BER test



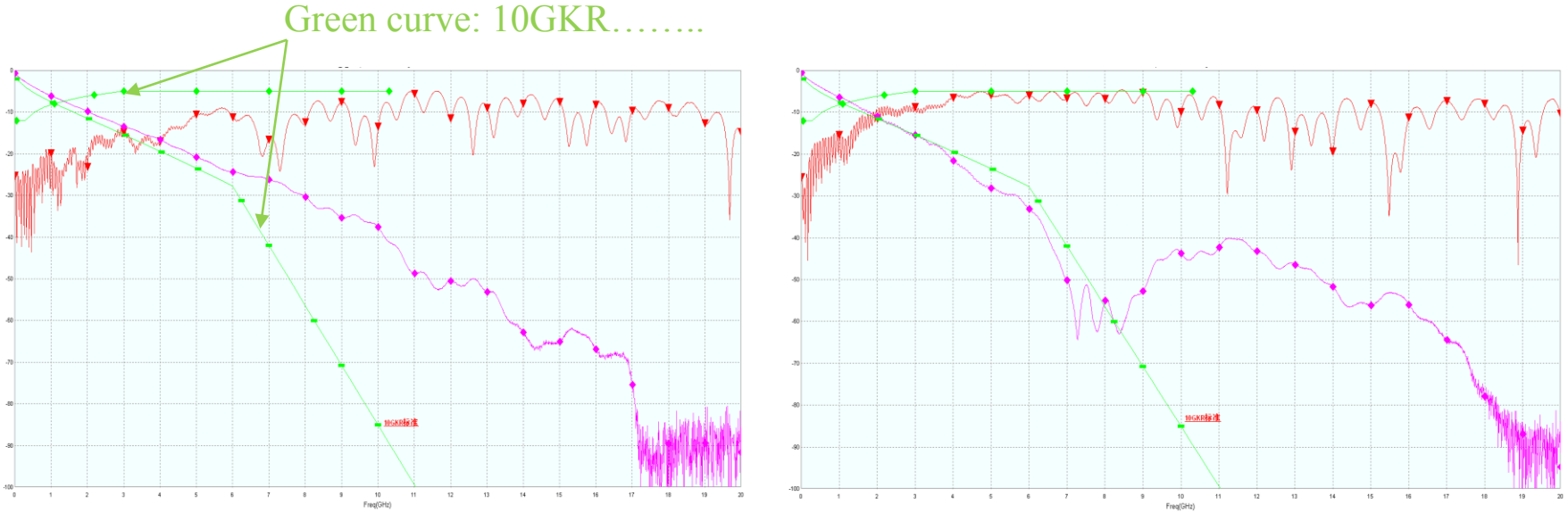
AMI Applications in High-speed Serial Channel Analysis



IBIS-AMI Model Validation Setup

AMI Applications in High-speed Serial Channel Analysis

- IBIS-AMI models for performance evaluation of two different channel



Channel 1：
Backplane traces 40inch 、 Two connectors ， Two test fixture、test cable. Backplane side over the hole stubs 37mil.

Channel 2：
Backplane traces 40inch 、 Two connectors ， Two test fixture、test cable. Backplane side over the hole stubs 150mil.

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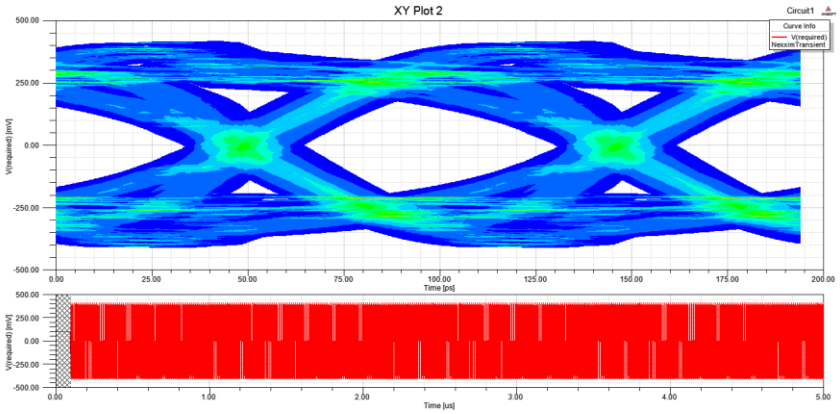
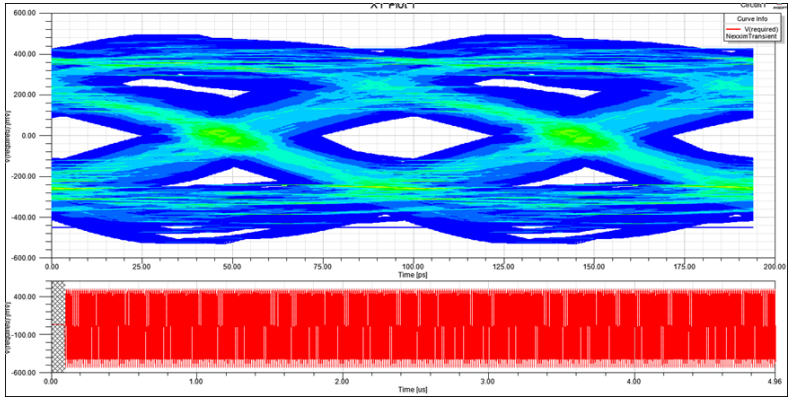
- Channel 1 and Channel 2 Simulation results compare(PRBS31) :





Eye Height	239.11mv
Jitter (pp)	32.40ps
Rise time	45.84ps

Eye Height	53.61mv
Jitter (pp)	51.98ps
Rise time	58.42ps

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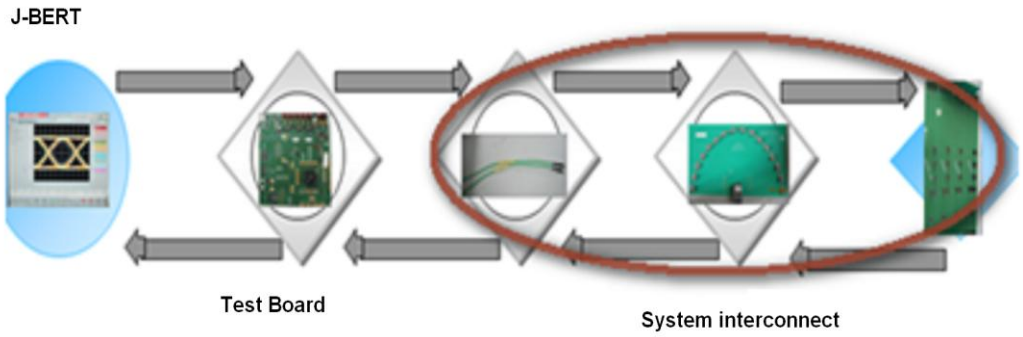
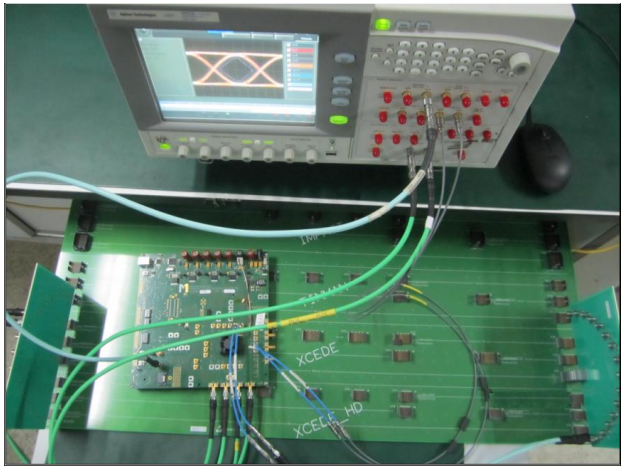
BER Test

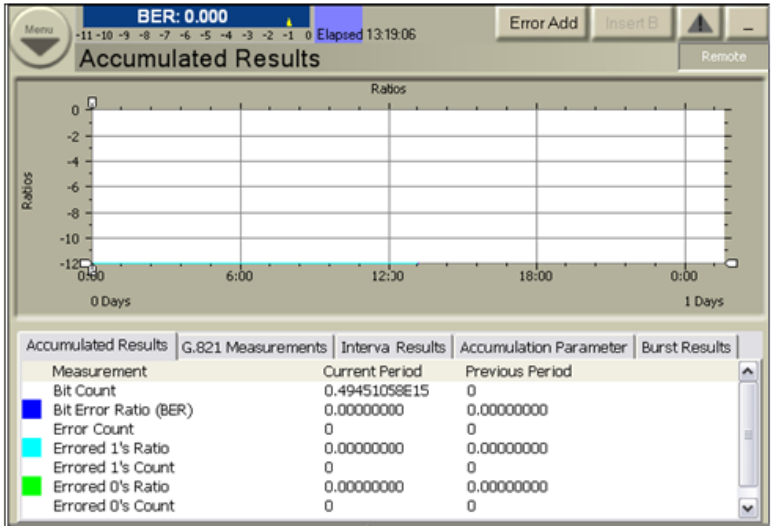
- Use BERT and chip test board for channels 1 and 2 bit error rate test.
- BERT Generates the source signal and also receives the loopback signal for ber test.

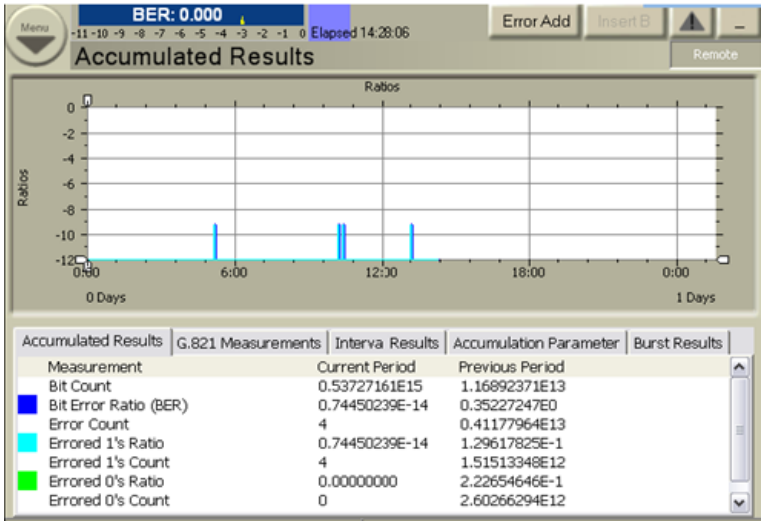




AMI Applications in High-speed Serial Channel Analysis

BER test results





More than 12 hours of the bit error rate test, there was no error.

More than 12 hours of the bit error rate test, the emergence of four errors.

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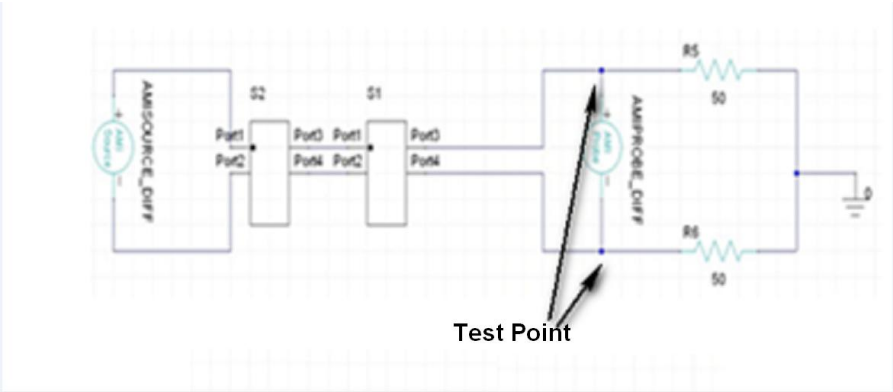
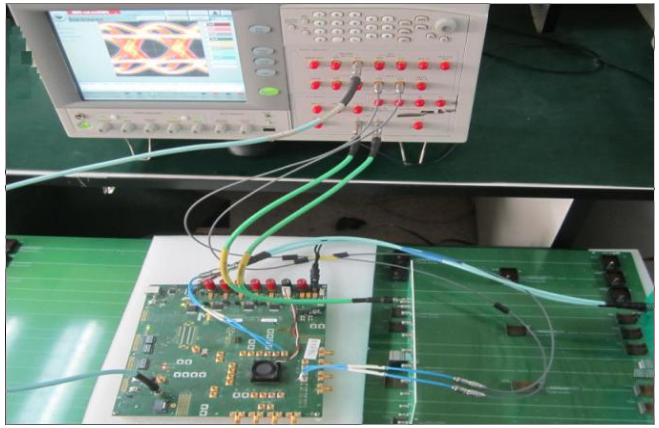
AMI model accuracy verification

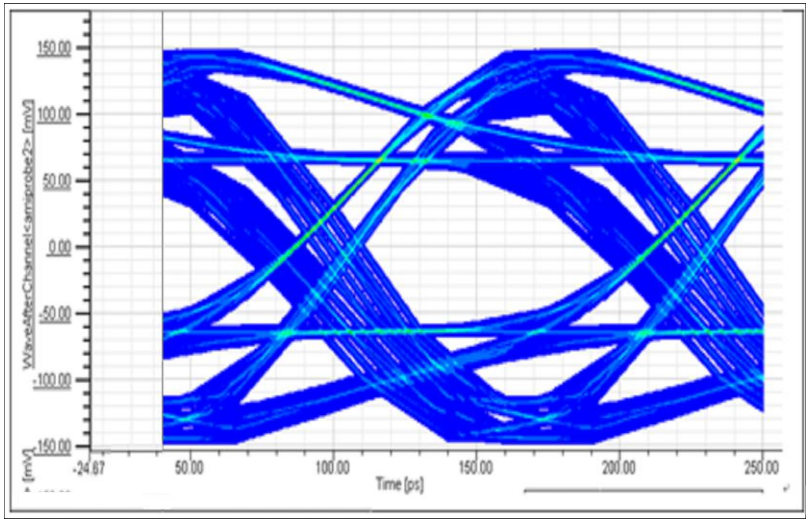
- Simulation channel： Transmitter package parameters、 Backplane traces 10inch、 Two connectors、 Two test fixture、 Connection cable.
- The chip emits a signal after transmission through backplanes direct access to the BERT test in the eye .
- Simulation and test using the same pattern PRBS15 ， Rate 8Gbps，The same pre-emphasis settings (10dB).

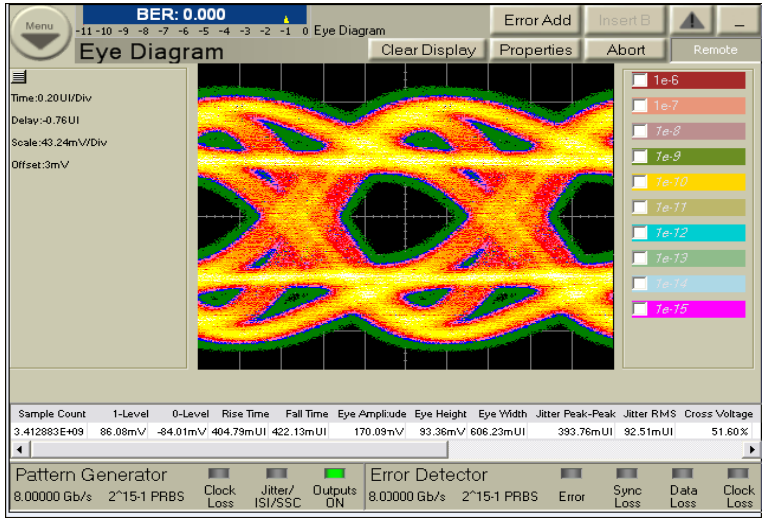




AMI model accuracy verification

- Simulation results compared with test results——Output 600mv





	Simulation	Test
EyeAmplitude	196.17mv	170.09mv
jitter (pp)	46.00ps	49.22ps
EyeRiseTime	61.7ps	50.60ps

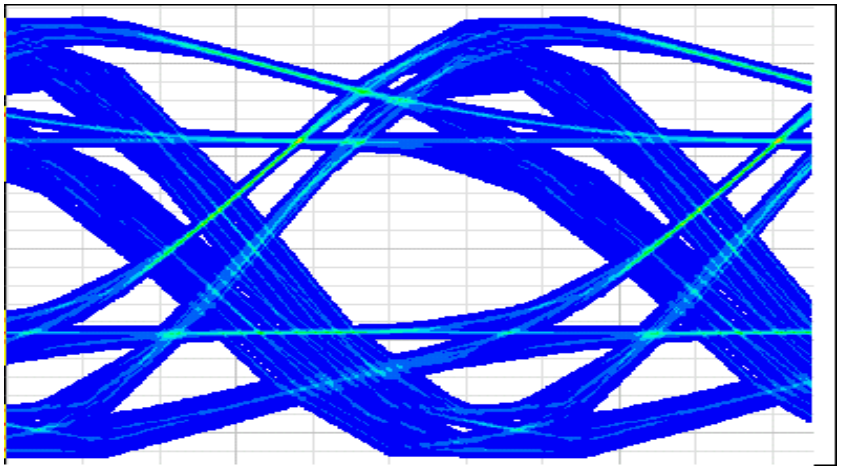
Conclusions ：

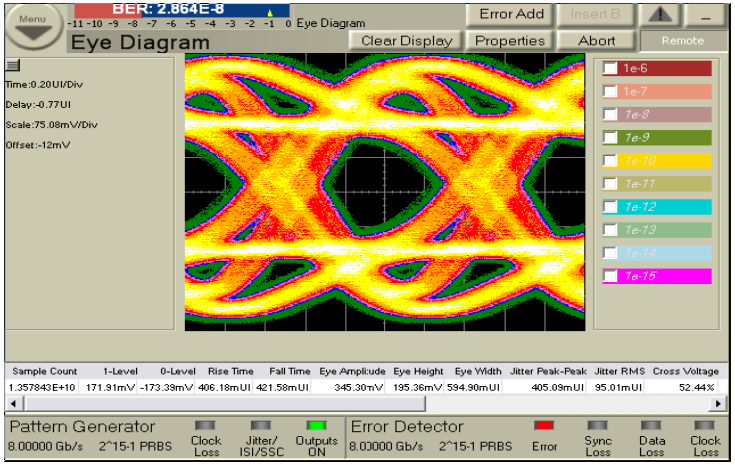
1、 Good Correlation in total eye.

2、 A little defference in rise edge .

AMI model accuracy verification

- Simulation results compared with test results——Output 1200mv





	Simulation	Test
EyeAmplitude	392.34mv	345.30mv
jitter (pp)	46.00ps	50.64ps
EyeRiseTime	61.54	50.77ps

Conclusions ：
Same as output 600mv .

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Summary

- Serial channel analysis using the AMI model simulation can provide good guidance for the design.
- AMI model can be applied to more signal integrity assessment such as crosstalk, jitter, high-speed connector performance analysis.
- The work of AMI model simulation Verification need to be improved, We hope to get more and better ways.

Suggestions

IBIS-AMI model can greatly improve the efficiency of high-speed serial signal simulation ,howeverwe still have encountered the following problems:

- AMI model is currently not uniform and IC vendors supply various models, so it is difficult for users to run them with right EDA tools.
- Some EDA tools supported AMI models are not perfect in function. For example the setting is not convenient to use , TX&RX AMI models can not be simulated alone etc.
- Some AMI models can not support adaptive DFE fuction perfectly. Users need to manually set the value or adaptive DFE operating results are not correct.

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Thanks!

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