# Introduction of FEC IL Gain Estimation Method In High Speed Link

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# Abbreviations

| Abbreviation | Explanation |
| --- | --- |
| FEC | Forward Error Correction |
| DFE | Decision Feedback Equalizer |
| IL | Insertion Loss |
| BER | Bit Error Rate |
| SNR | Signal to Noise Ratio |
| KR | Short for 10GBASE-KR standard |

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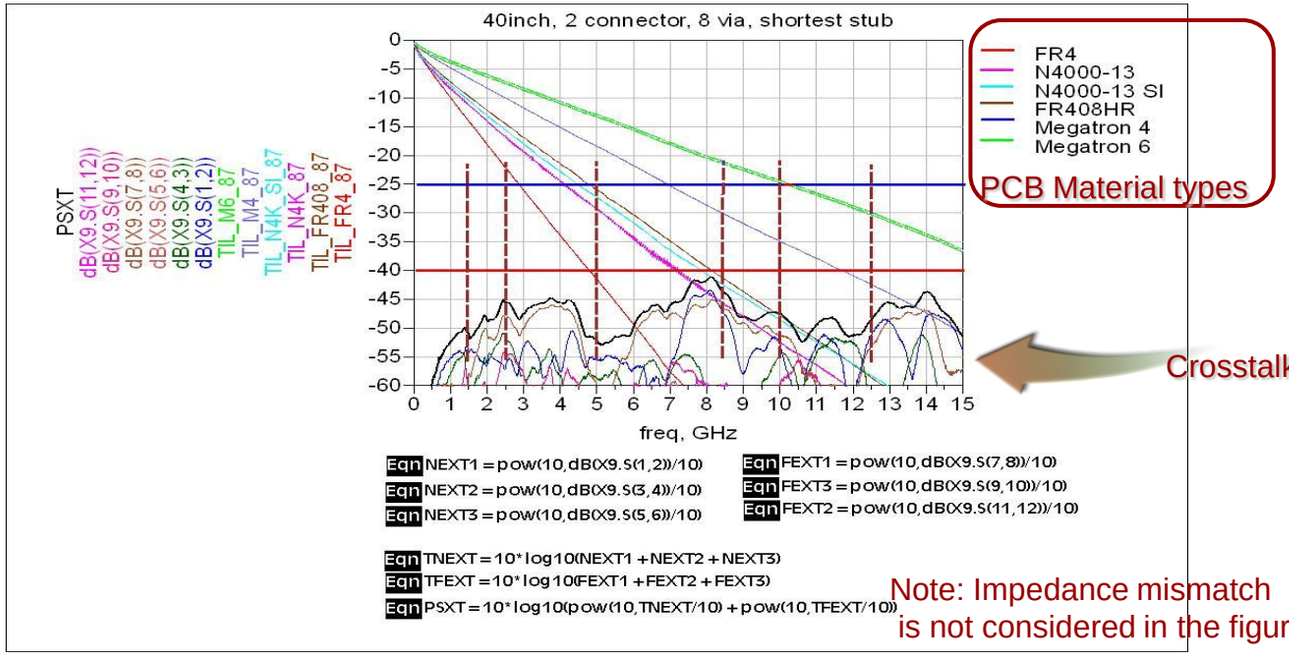
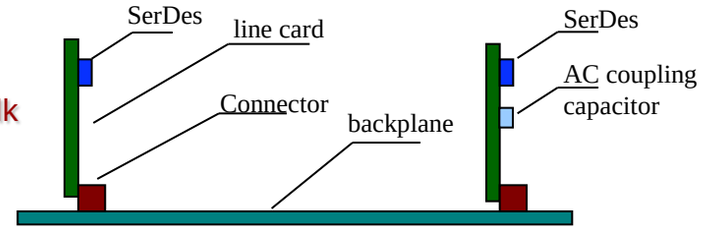
# Backgrounds – Loss Dominated Link Performance

- **Insertion Loss is the top 1 design factor which dominates the performance and cost of a 10Gbps+ high-speed long reach system.**
  - The length of 25Gbps high-speed link may achieve 40inch, regardless of OIF CEI-25G recommendation of 27” length. Even with the Megtron6 material now available, it is not possible to meet the 25dB insertion loss requirement of OIF CEI-25G standard for link length above 27inch.
  - Even for 10Gbps data rate, using lower cost PCB material requires that high-speed system tolerates much more insertion loss by seeking for additional IL gain.

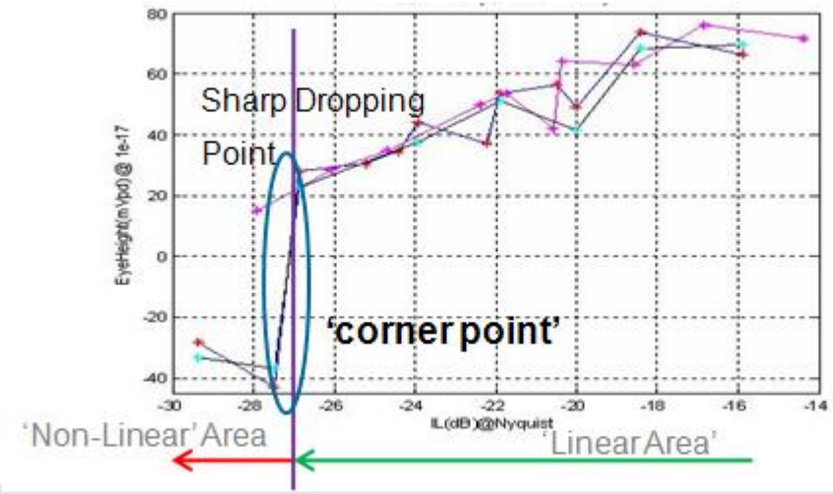


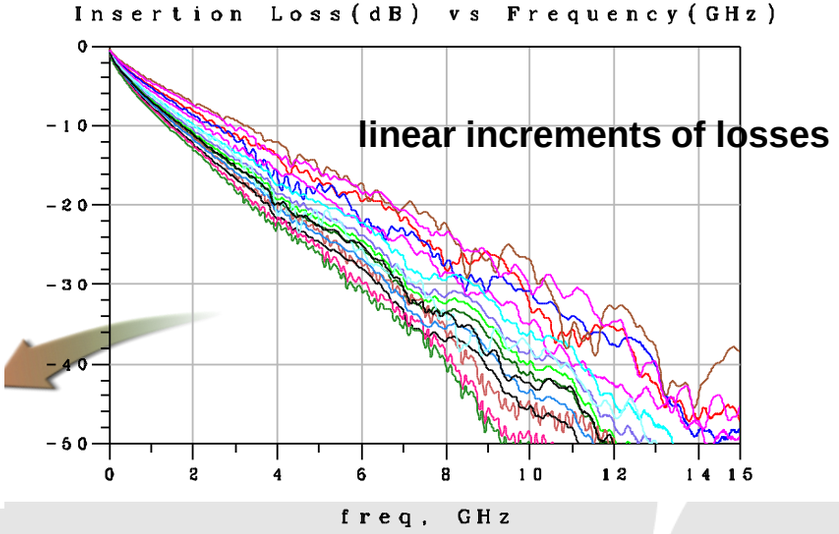




Note: Impedance mismatch is not considered in the figure

# Backgrounds – Basic Viewpoints on FEC

- **FEC is normally used to solve the link reliability issues. Within the SerDes driving capability, Designing proper FEC can improve link SNR and BER performance.**
- **FEC does improve SNR and can also tolerate additional channel losses. It is believed that strong FEC can help meet the 1m objective length requirement of 25Gbps channels.**
- **But, it does depend on:**
  - From both simulation and lab measurement, the BER performance of SerDes degrades sharply at the ‘corner point’ of channels, even with the insertion loss changes with approximate linear increments.
  - FEC can extend the SerDes driving capability by several dB, but it is fact that using ordinary FEC is hard to improve the driving capability from the ‘corner frequency’ by another several dB.

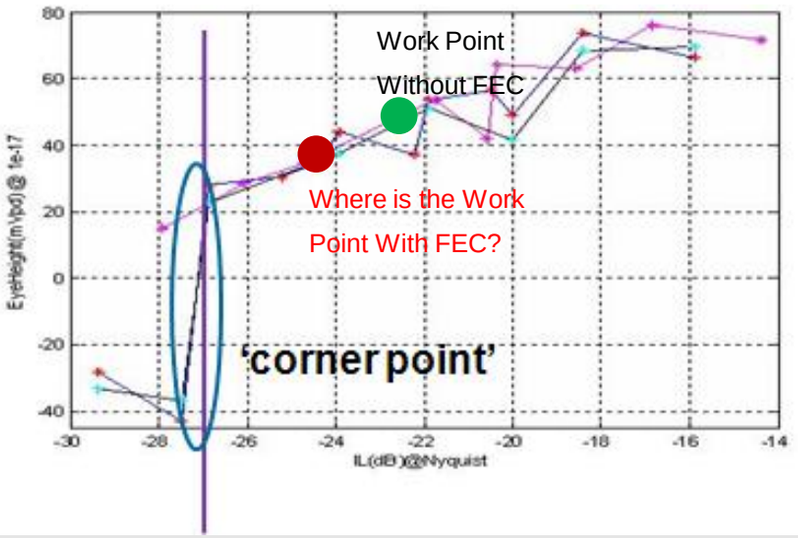


# Backgrounds – Needs for FEC Capability Estimation

- **FEC is more and more often used in 10Gbps+ links:**
  a) For the driving distance's sake: to extend the driving distance of SerDes in long reach channels is often required to meet the system design target. FEC is a useful 'soft' way to extend chip driving distances.
  b) For the reliability's sake: Noises and burst errors happen almost all the time in high-speed link systems, FEC can help in certain degree to reduce errors that induced by these factors, to enhance the link immunity to noises, and thus to enhance the reliability of links.

- **In high speed link specification evaluating phase, detailed FEC performance measurement is not feasible, and valid method to roughly estimate the FEC driving capability is in immediate need.**



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# Issues: Additional IL Gain Equation

- **Traditionally, theoretical relationship between FEC coding gain and the additional driving insertion loss due to FEC is:**

  *additional IL gain = 2*FEC_Coding_Gain, where the IL gain factor is 2*

  **Examples: 6dB FEC coding gain means KR insertion loss limit can be extended to 23+6*2=35dB**

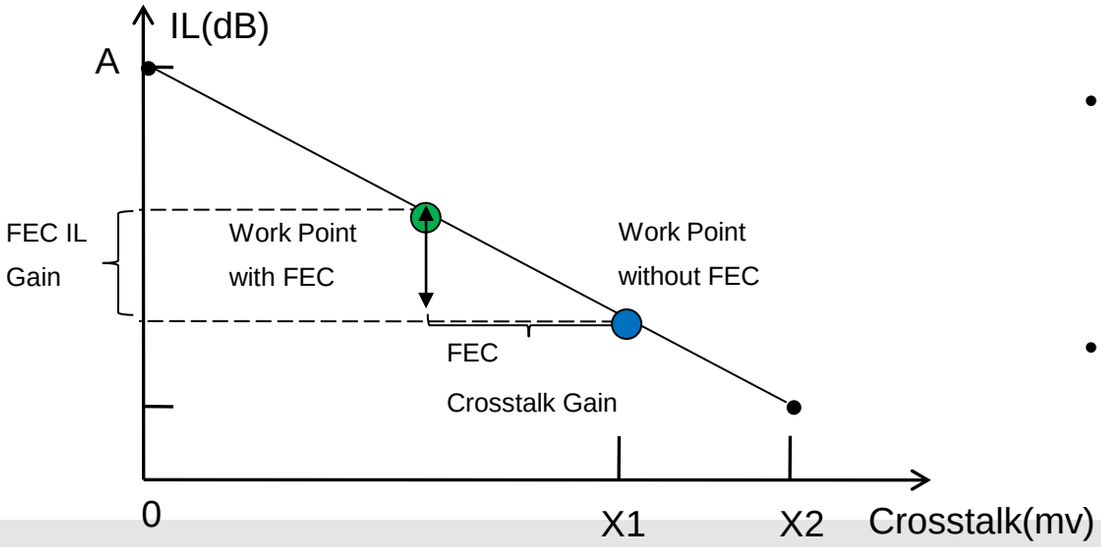
- **From Huawei internal experimental results, the additional IL gain is about 1 with regards to the coding gain, not 2 listed above. According to the testing capability of KR FEC, the additional IL gain is about 2dB, as we all know that KR FEC coding gain is 2~3dB, it is believed that the reasonable value of IL gain factor due to coding gain for this case is about 1.**

  *additional IL gain = FEC_Coding_Gain*

- **Note that if SerDes is working in the area that is beyond the corner point, 'non-linear' area does affect the additional IL gain, so this equation is invalid in estimating SerDes driving capability under this circumstances.**

# Modified Method of Estimating FEC IL Gain

- **There's certain linearity relationship between the maximum tolerable crosstalk and maximum tolerable insertion loss of a high speed link, insertion loss and crosstalk restrict each other, when one gets to certain value, the other will not exceed certain 'mask'.**
- **FEC can enhance link SNR through solving the BER problem induced by crosstalk, so, assuming signal is kept unchanged, the SNR enhancement of FEC is equivalent to the improvement of crosstalk induced BER. Then the work point with FEC could be found by the point of reduced crosstalk.**
- **In the following figure, the horizontal axis represents link crosstalk, the vertical axis represents the link insertion loss. The slope gives the variation of insertion loss gain with regards to the crosstalk variation.**




- Assuming FEC coding Gain is X dB, and Y is crosstalk gain factor

$$Y = 10^{-\frac{X}{20}}$$

- The slope of the line is K, then additional FEC IL gain is $ILGain = K * Y * X1$

# Example of Additional FEC IL Estimation

- **We use this modified method to estimate additional IL gain value. We may get the idea that the IL gain from KR FEC is about 1dB~2dB. However, the theoretical equation tells that 4dB IL gain would come from KR FEC.**
- **From measurement, we got the additional 1~2dB IL gain from KR FEC.**

| Link name | Crosstalk (mV) | Slope (dB/mV) | KR FEC Gain (dB) | Theoretical Equation (dB) | Additional IL Gain (dB) |
|---|---|---|---|---|---|
| Connector 1 | 28 | 0.29 | 2 | 4 | 1.67 |
| Connector 2 | 24 | 0.30 | 2 | 4 | 1.48 |
| Connector 3 | 23 | 0.26 | 2 | 4 | 1.23 |

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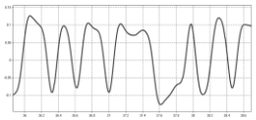
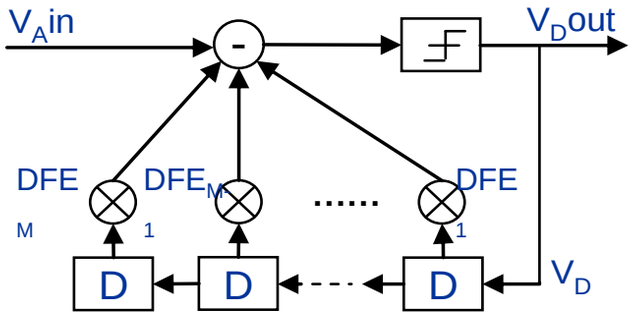
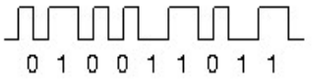
# Error Propagation Mechanism

- **High speed serial links have a mixed error mechanism of random errors and burst errors.**
- **DFE can introduce burst errors due to the feedback mechanism:**

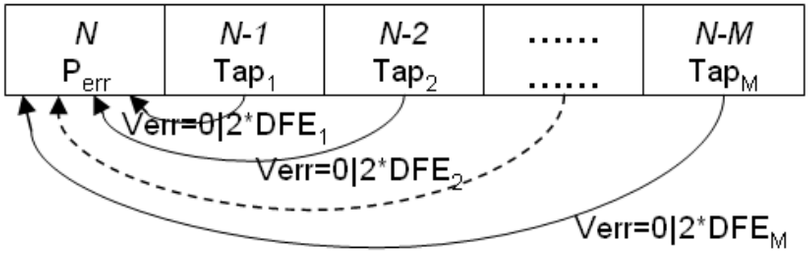





$$V_D out(t_0) = V_A in(t_0) - DFE_1 \cdot V_D(t_{-1}) - DFE_2 \cdot V_D(t_{-2}) - ... - DFE_M \cdot V_D(t_{-M})$$

- **Once errors occur, they change the output voltage of the equalized bits that follow, and thus impact the judgments of the bits that follow.**



# Error Propagation Equation

- **The previous estimation method is a rough estimation for IL Gain due to FEC. More accurate analysis should use Error Propagation Equation to analyze link BER.**
- **The BER performance of Error Propagation of DFE:**

$$BER = \sum_{i=1}^{rll_{\max}} \sum_{allE} p(rll = i, E) \cdot W(E) \cdot p_1 \cdot (1 - p_1)^{n - rll_{\max} - i}$$

- $p_1$: random error probability
- $W(E)$: the probability that $i$ bits in error among a $n$ bit block
- $E$: all the combinations of the error pattern when error propagation length is $i$
- $rll_{\max}$: maximum error propagation length

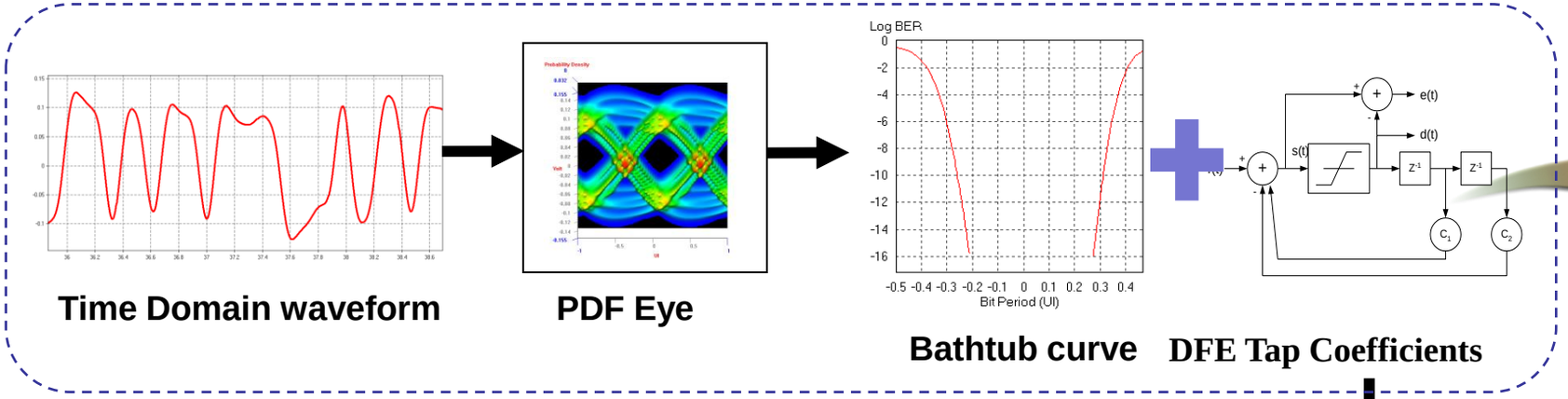
- **The Total BER with error propagation is:**

$$BER_{total} = \frac{1}{N} \sum_{allP} \sum_{i=0}^{H} P_{pkt}(i+1 \mid i)$$

- a function of the vector $Err\_DFE$
- The $(i+1)th$ burst error rate in a packet under the condition that the $ith$ burst error occurs in the same packet
- When $i$ equals to 0, $P_{pkt}$ is simply the probability vector of the 1st burst error in the packet.

# Error Propagation Equation Analysis Method

- **The total Error Propagation Analysis flow:**

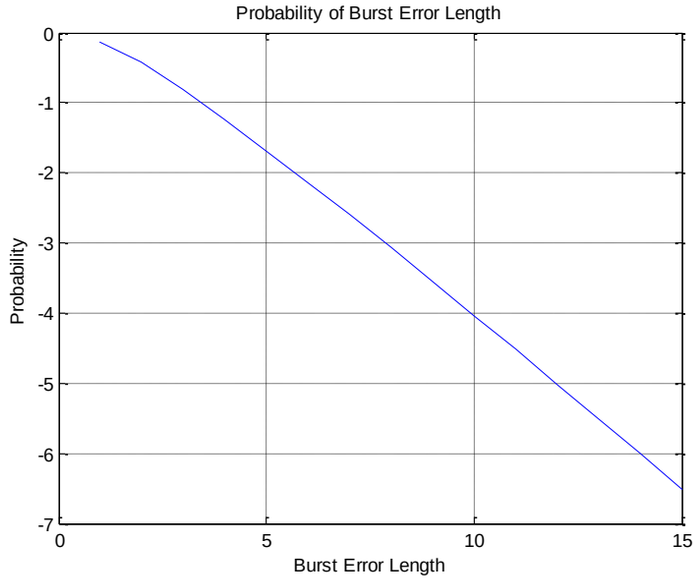


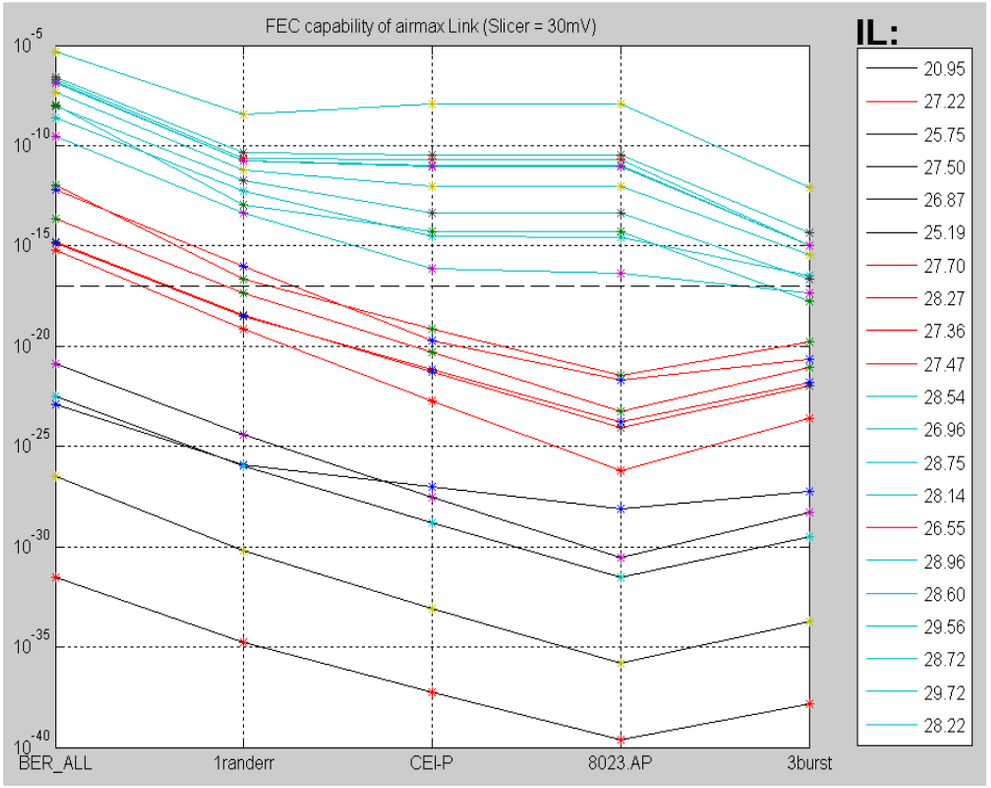

- **The whole process of estimating FEC capability can be divided into two stages, the first stage can be processed in current EDA platforms, but the second stage is now processed by the users.**

# Example of the Error Propagation Equation Analysis Method

- **We use Error Propagation Equation method to estimate BER gain and additional IL gain value. We may get the idea of that the IL gain from current FEC in use is about 1.9dB.**
- **The data correlates well with the 1~2dB measurement results.**

Demo: Probabilities of 1~15 Burst Error Lengths



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# Summary

- **As introduced previously, FEC will play more and more important role in 10Gbps+ high-speed serial links.**

- **A rough IL gain estimation method is summarized and the Error propagation Equation Analysis method is introduced here, and it has been verified to be an very efficient way in system link specification analysis phase for estimating FEC capabilities in terms of additional IL gain.**

- **Current EDA tools can process time domain and statistical analysis very well, but the lack of DFE coefficients outputting function and lack of voltage bathtub sometimes  makes FEC analysis inconvenient.**

- **FEC gain analysis method is recommended to be supported by EDA tools(IBIS specification), including error propagation analysis function.**

# Thank you

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