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IBIS VT Waveform and Over Clocking

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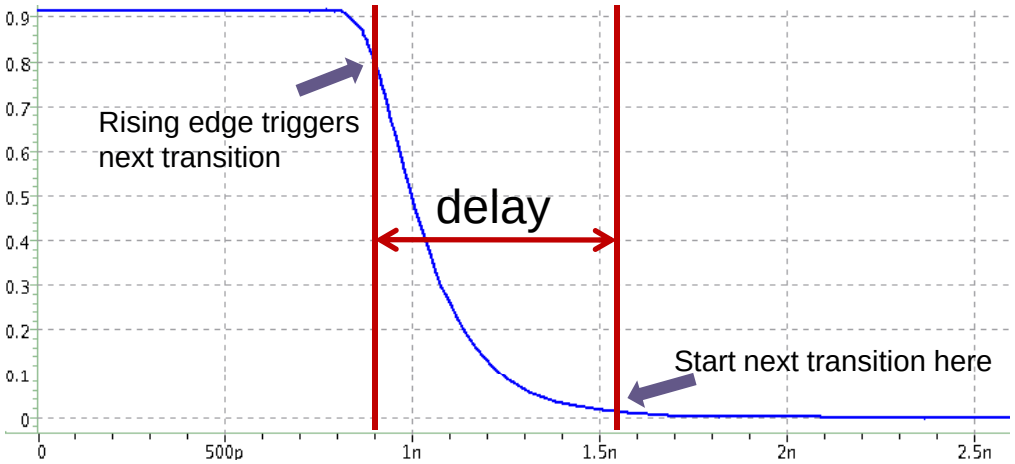
Outline

- Introduction to over clocking
- Adjust VT waveform for better simulation
- Suggestion of new IBIS keyword
- Conclusions

Introduction to over clocking

- **Over clocking:**
  Next transition is triggered when this transition is not finished.

- **Transistor level buffer behavior for over clocking:**
  This transition will continue with a delay time, and then start new transition. (Refer :http://www.vhdl.org/pub/ibis/summits/jun03b/muranyi2.pdf)



- **IBIS buffer behavior for over clocking:**
  Difference exists for different tools.

Introduction to over clocking(Cont.)

- Some research for over clocking in IBIS summit meetings:
  - http://www.vhdl.org/pub/ibis/summits/jun03b/muranyi2.pdf
    - research over clocking by behavior of transistor level buffer
    - provide two algorithm ideas
  - http://www.vhdl.org/pub/ibis/summits/sep05/haller2.pdf
    - add VT offset in IBIS model
    - may loose FF to SS timing relationship
  - http://www.vhdl.org/pub/ibis/summits/jun07/wang.pdf
  - http://www.vhdl.org/pub/ibis/summits/feb07/wang.pdf
    - compare behavior of transistor level buffer and IBIS buffer
    - provide relation of bit width and over clocking
    - provide algorithm enhancement in the simulation equation with PU&PD scaling coefficients.

Adjust VT waveform for Better Over Clocking Simulation

• This presentation is focused on the detailed adjustment method of two kinds of VT waveform truncations for better over clocking simulation (especially the first one):

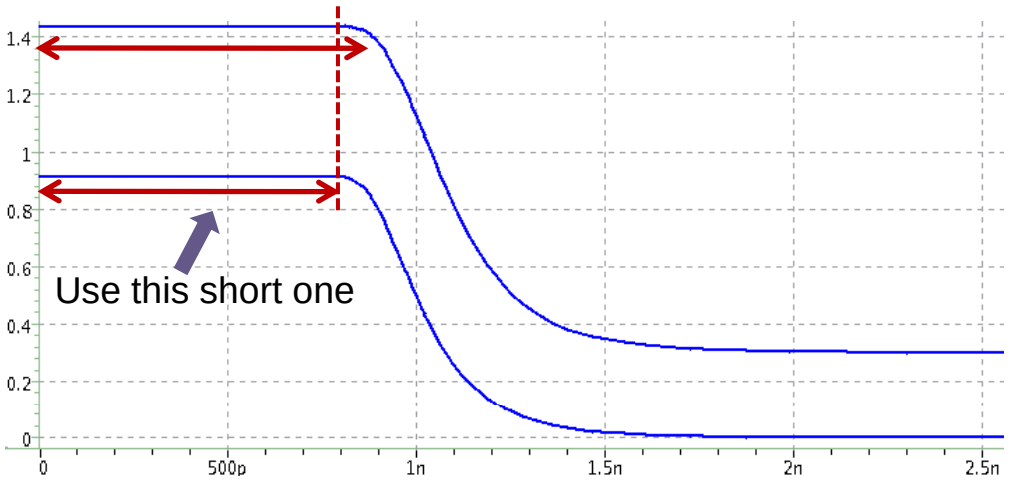
1. **Remove initial delay**

2. **Remove flat tail**

Remove Initial Delay for Better Over Clocking Simulation

Definition of Falling/Rising Initial Delay :

- Usually, there are two falling VT waveforms.
- The falling initial delay is defined to be the minimum of initial flat part.



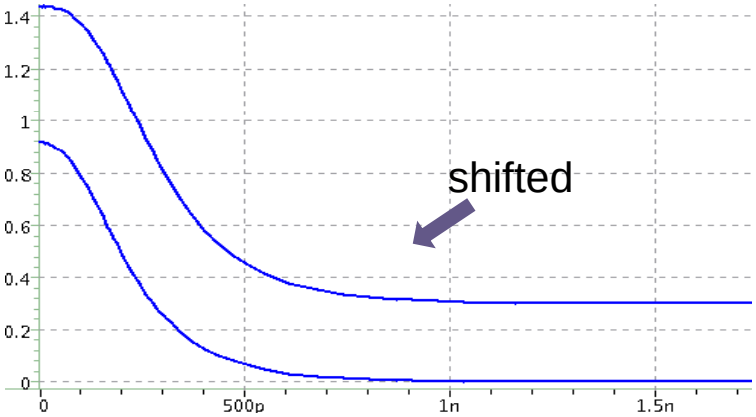
(VT waveform in IBIS model)

- The value of rising initial delay is defined in a similar way.

Remove Initial Delay for Better Over Clocking Simulation(Cont.)

Simulation with Initial Delay Removed VT:

• After remove initial delay, VT waveforms are shifted and time span(i.e. last T value) is shortened. So over clocking maybe "**avoided**".



(VT waveform in IBIS model)

• **Issue:**

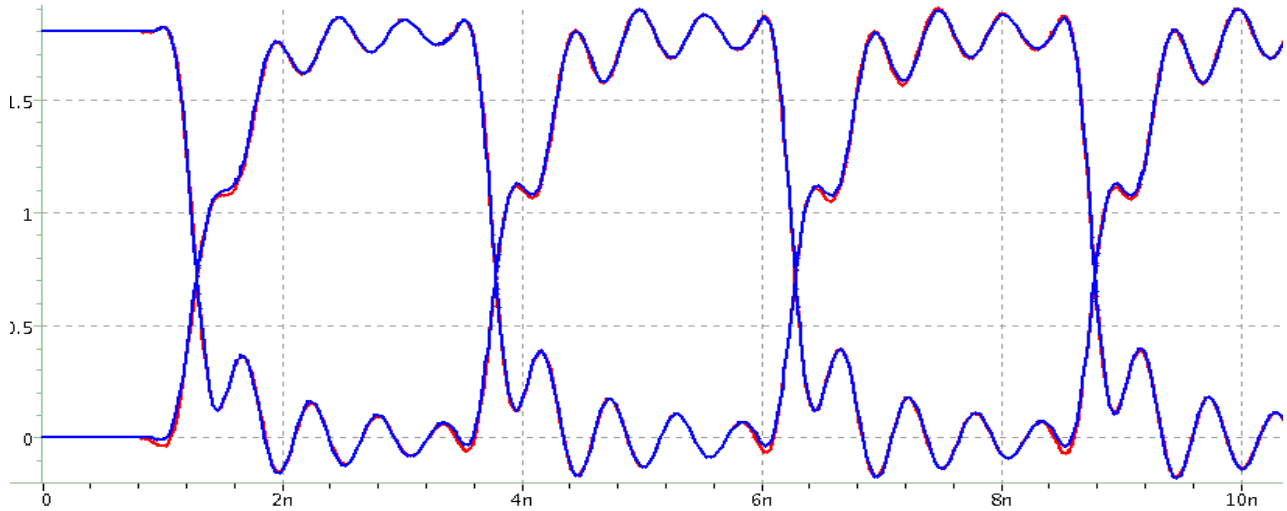
1) The output waveform will be shifted too.
2) Loss timing relation of rising and falling for different falling and rising initial delays. Obviously, it's important for cross point of differential outputs.
3) Loss timing relation of corners of 'Typ', 'Min', 'Max'

Remove Initial Delay for Better Over Clocking Simulation(Cont.)

Solution of No Timing Impact Simulation:

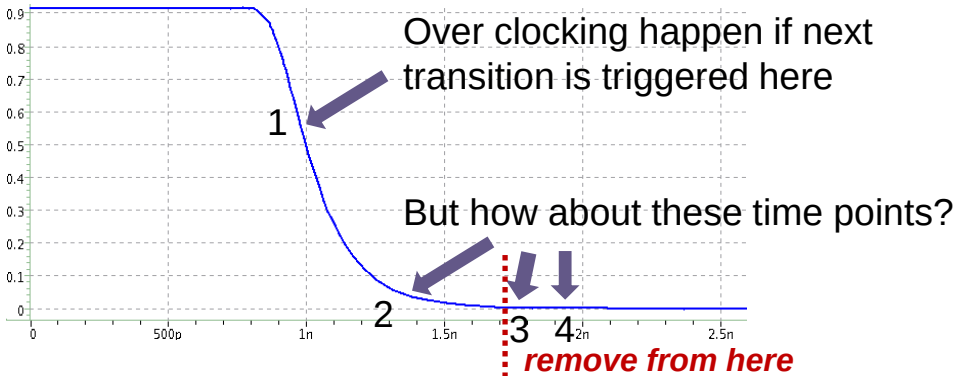
For simulator, add falling and rising delay in input stimulus respectively.

Example: output buffers + T line + input buffers (differential)



blue: result at receivers by this solution
red: result at receivers of no VT adjustment

Remove Flat Tail for Better Over Clocking Simulation



- It's for algorithm stability(although few cases show improvement)
  - ➢ For real over clocking, buffer does not start from initial stable state of next transition. Instead, it starts from one middle state(i.e. Kpu&Kpd are not 0 or 1).
  - ➢ If remove the flat tail, then the time span is shortened. Simulator is easy to detect that current transition is finished for trigger points of 3,4.
- It seems conflicting with IBIS cookbook.
  - ➢ Cookbook suggests to extract VT with long enough time for stable state.
  - ➢ But experiments show removing flat tail is not sensitive to simulation result

Suggestion of New Keyword in IBIS Spec. for Preceded Solution

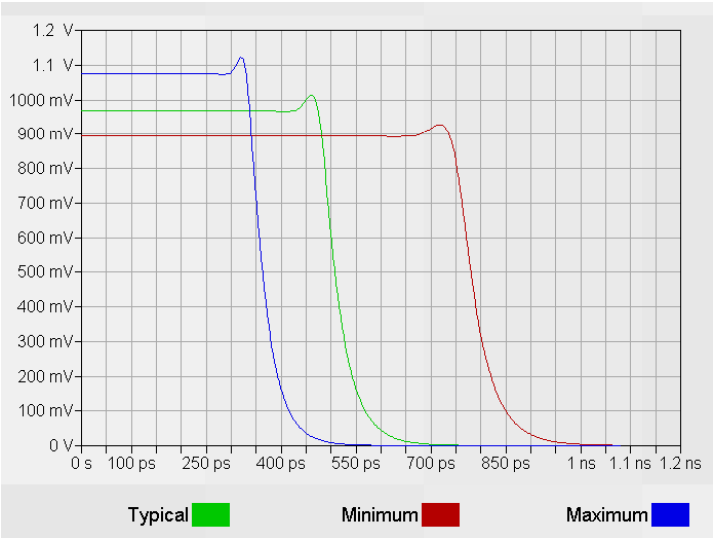
• Add keywords of “[Fall Initial Delay]” and “[Rising Initial Delay]” with values of typ, min, and max in IBIS model.

• VT waveforms in model are truncated with above initial delays, and start from new time zero point.

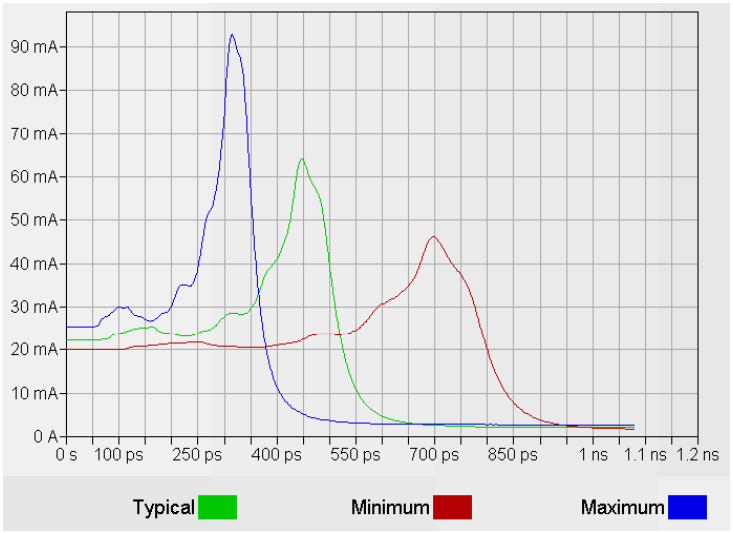
• Advantages for using such keywords:

- There is no impact for timing relation between falling and rising or different corners.
- For over clocking cases, simulator difference will be decreased.

New Challenge for [Composite Current]



(Falling VT waveforms)



(Related Composite Current)

- Only removing initial delay of VT will lost useful data of composite current. (A simple solution is to use the minimum of initial flat part of VT and IT)

- Need much more research on behavior of transistor level buffer for composite current when over clocking happens.

Conclusions

- This presentation provides a detailed solution of VT adjustment with new IBIS keywords for better over clocking simulation.
- Suggest to use a common solution to decrease simulator difference on this aspect.
- There is new challenge for over clocking case simulation with new IBIS feature – [Composite Current]

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