WELCOME FROM MICHAEL MIRMAK, INTEL CORPORATION

On behalf of the I/O Buffer Information Specification (IBIS) Open Forum, I would like to welcome our presenters and guests to the Asian IBIS Summit in Shanghai.

Seven is a lucky number in some parts of the world, and we are happy to be celebrating seven years of annual Summits in the People's Republic with this event. The IBIS Open Forum is certainly lucky and thankful for the opportunity to see our friends and colleagues again, and for such a very detailed and thought-provoking technical program.

We are especially grateful to our sponsors Huawei Technologies, Agilent Technologies, Ansys, Cadence Design Systems, Intel Corporation, IO Methodology Inc., Sigrity, Synopsys and ZTE Corporation, for making this Summit possible.

Our thanks to you for participating and best wishes for a successful summit!

Sincerely,

Michael Mirmak
Chair, IBIS Open Forum

在这里我仅代表的 IBIS 公开论坛，欢迎我们的各位演讲者和嘉宾前来参加在上海举行的第七届亚洲 IBIS 技术研讨会。

在世界上一些地区，七是一个幸运的数字。在这里我很高兴与大家一起来庆祝这第七年度 IBIS 亚洲峰会。 IBIS 开放论坛是幸运的。我感谢再次有机会见到我们的朋友和同事，一起来研讨这个值得人深思的技术问题。

我们特别感谢我们的赞助商华为技术有限公司，安捷伦科技公司，ANSYS，Cadence 设计系统公司，英特尔公司，IO Methodology 公司，Sigrity 公司，Synopsys 公司和中兴通讯股份有限公司，是他们使得本次峰会成为可能。

感谢您的参与，并祝愿本次峰会圆满成功！

此致

马梦宽
IBIS 开放论坛主席

WELCOME FROM LI JINJUN, HUAWEI TECHNOLOGIES

Ladies and Gentleman,

On behalf of Huawei Technologies, welcome to the seventh annual Asian IBIS Summit (China). I would like to express my appreciation to IBIS Open Forum and all the sponsors for co-organizing this event.

Since 2005, IBIS Asian Summit in China has been the top-level international conference in high speed digital design society in China. I am looking forward to work with IBIS members in China, and to expand our participations in the region.

Huawei has actively involved in all IBIS society's events. We hope to resolve high speed link issues with IBIS Open Forum, EDA vendors and IC vendors. Your comments and suggestions will be deeply appreciated!

Welcome all of you to Shanghai! Hope you will enjoy all the technical discussions and sharing throughout the meeting, and have a nice journey!

Thank you!
Li Jinjun
Huawei Technologies

各位专家，各位来宾：

我代表华为公司，欢迎大家来参加第 7 届亚洲 IBIS 技术研讨会，衷心地感谢 IBIS 协会组织本次会议。

自从 2005 年以来，IBIS 技术研讨会已经成为了中国高速设计领域的一次盛会。我很高兴有机会与 IBIS 协会一起促进和扩大在该领域的分享。

华为积极参与各项 IBIS 活动，希望与 IBIS 协会、EDA 软件、芯片公司一道来共同解决许多高速链路设计上的挑战，欢迎大家会上讨论和建议。

欢迎 IBIS 专家来到上海，希望你们能够喜欢所有的技术讨论和会议分享，度过美好一天。

谢谢大家
华为公司 厉进军

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

8:15 REFRESHMENTS & SIGN IN
- Vendor Tables Open at 8:30

9:15 **Welcome**
- Li, JinJun
  (Huawei Technologies, China)
- Mirmak, Michael
  (Chair, IBIS Open Forum, Intel Corporation, USA)

9:00 **IBIS Status and Future Direction** **5**
Mirmak, Michael (Intel Corporation, USA)

9:15 **IBIS Model as De-Facto Standard** **10**
Kusunoki, Kazuhiko* and Dai, WenLiang**
(*Wadow Co., Japan and **Xpeedic, China)

9:40 **IBIS VT Waveform and Over Clocking** **18**
Chen, XueFeng (Synopsys, China)

10:10 BREAK (Refreshments and Vendor Tables)

10:30 **IBIS Parsers** **25**
Ross, Bob (Teraspeed Consulting Group, USA)

11:00 **DDR3 System Timing Budget Analysis by SI&PI Co-Simulation** **33**
Yi, Bi; Wang, Ping; and Zhu, Shunlin (ZTE Corporation, China)

11:30 **Modeling the On-die De-cap of IBIS 5.0 PDN-aware Buffers** **41**
Wang, Lance* and Wolff, Randy**
(*IO Methodology, and **Micron Technology, USA)

12:00 FREE BUFFET LUNCH (Hosted by Sponsors)
- Vendor Tables

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

IBIS Status and Future Direction

Michael Mirmak
Intel Corp.
Chair, IBIS Open Forum

马梦宽
英特尔公司
IBIS 委员会主席

Asian IBIS Summit (Shanghai)
November 15, 2011

亚洲 IBIS 技术研讨会（中国上海）
2011 年 11 月 15 日

Agenda

- IBIS as Organization and Standard
- IBIS 5.0
- Touchstone 2.0
- IBIS-ISS 1.0
- Timeline for Changes
- Call to Action

Specifications and Technologies

- IBIS: both an organization and a standard
- IBIS – I/O Buffer Information Specification
  - Version 5.0 today (includes IBIS-AMI support)
- Touchstone 2.0
  - Ratified April 2009
  - TSCHK2 parser also offered
- IBIS-ISS: Interconnect SPICE Subcircuit
  - Version 1.0 ratified October 2011

IBIS Specification Direction

- 5.1: Clarifications and Style Improvements
  - New, more readable format
  - Significant changes to IBIS-AMI
    - *Version control, plus clarifications to clocking, tables, crosstalk*
  - Support for weak tie-up/tie-down definitions
  - Clarifications to [Composite Current]
  - Fixes to EBD format
  - Fixes to [Test Data] and [Test Load]
- 5.2: Major features, still under discussion
  - Support for repeaters
  - Links to IBIS-ISS, Touchstone
  - C_comp clarifications

Touchstone 2.x

- Description/format for network parameters
  - Primary use in industry is for S-parameters
  - 2.0 introduces mixed-mode support and per-port impedance
- Touchstone 2.1/3.0 Approved Changes
  - Sparse Matrix format
  - Binary file representation (compression)
- Change under discussion
  - Support for explicit port-node mapping

IBIS-ISS 1.0

- Interconnect SPICE Subcircuit Specification
- Universal SPICE format for interconnects
  - Packages, cables, connectors, traces, etc.
- Basic SPICE elements supported
  - R, L, G, C, some sources
- Supports Touchstone, W-element data
  - Both frequency and time domains supported

Long-term successor to PKG, EBD, ICM

Timeline for Changes

- IBIS 5.1
  - Expecting changes to close by end of 2011
  - Draft complete and in approval cycle in Q1'12
- Touchstone 2.1
  - Q1'12 for approved changes
- Touchstone 3.0 & IBIS-ISS 1.0
  - Does IBIS-ISS resolve port-node mapping issue?

Key challenge:
smoothly linking all three specifications

Call to Action

- For tool vendors…
  - Are you planning to support these improvements?
- For system designers
  - Can you use these to improve your design margins?
- For IC vendors
  - Can these help you better specify your devices?

Please become familiar with the specifications and provide feedback!

For More Information...

- IBIS 5.0
  - http://www.eda.org/ibis/ver5.0/
- IBIS-ISS 1.0
  - http://www.eda.org/ibis/ibis-iss_ver1.0/
- Touchstone 2.0
  - http://www.eda.org/ibis/touchstone_ver2.0

Q/A

IBIS Model as De-Facto Standard

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wenliang.dai@xpeedic.com

Prologue

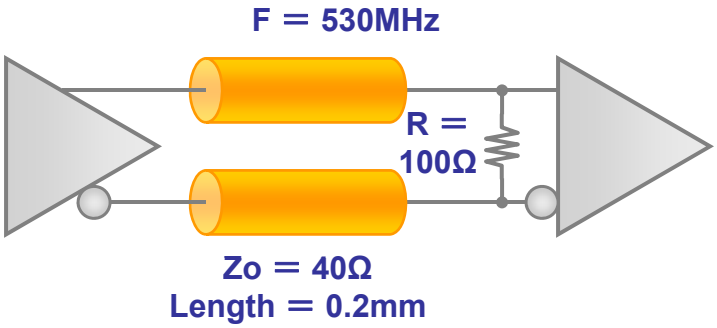
When do you do SI simulation by using same IBIS model but different SI simulators,

do you think the results will be same?

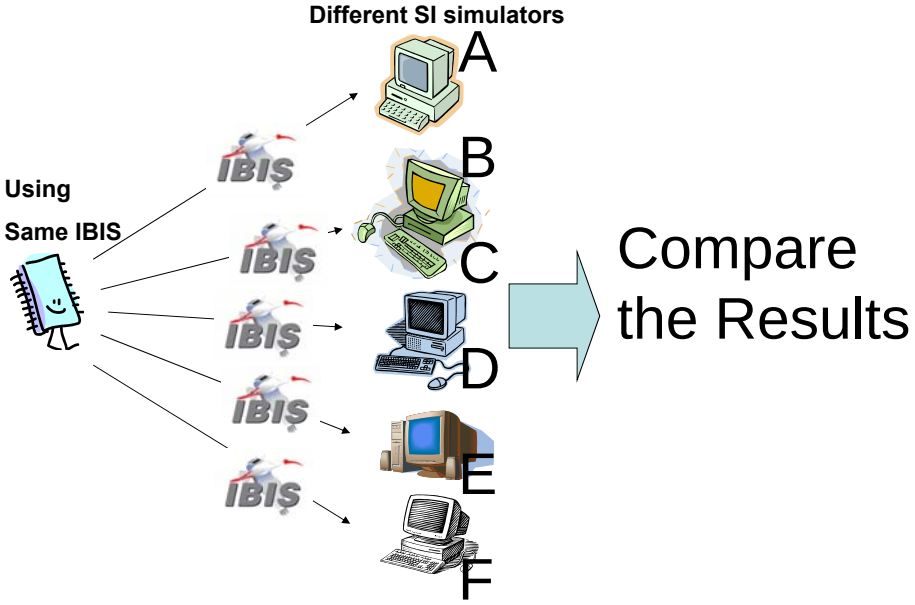
I did an experiment.

The experiments.

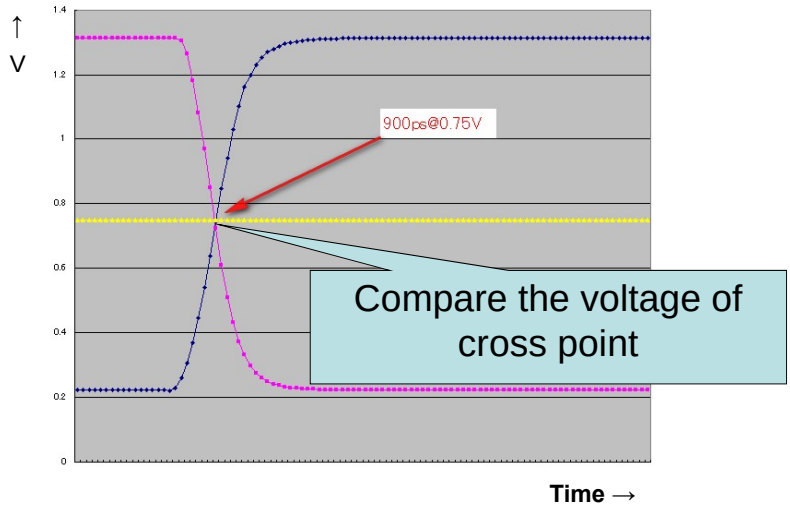
Using Same circuit



The experiments.



Compare point



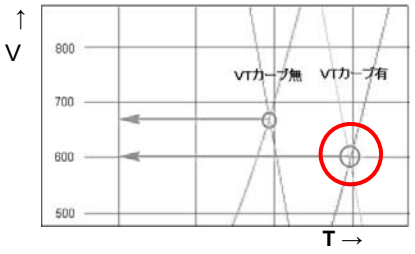
The Results

SI simulator	Cross Point Voltage
A	**600 mV**
B	**730 mV**
C	**620 mV**
D	**750 mV**
E	**764 mV**
F	**705 mV**

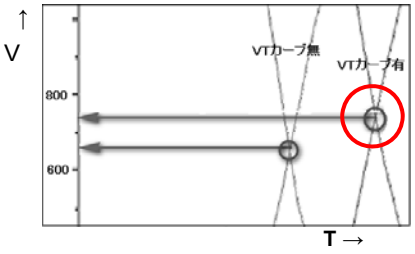
The results are all different

The Results

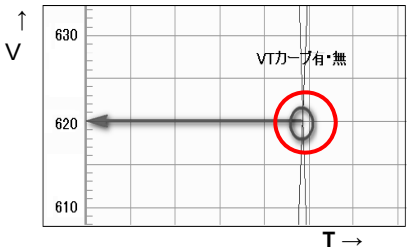
Simulator A



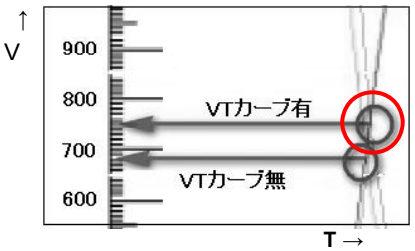
Simulator B



Simulator C

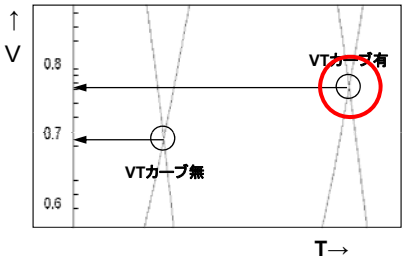


Simulator D

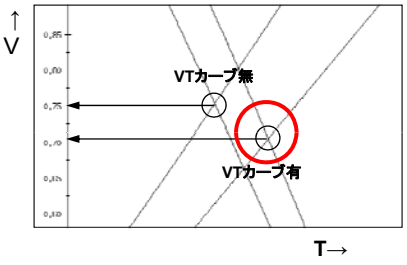


The Results

Simulator E



Simulator F



All of 6 simulator's results are different!!

(MAX 160mV difference)

SI simulator	Cross Point Voltage
A	**600 mV**
B	**730 mV**
C	**620 mV**
D	**750 mV**
E	**764 mV**
F	**705 mV**

What can I believe?

We are in era of

Can get IBIS model easily

Can trust IBIS model

Many Thanks for JEITA

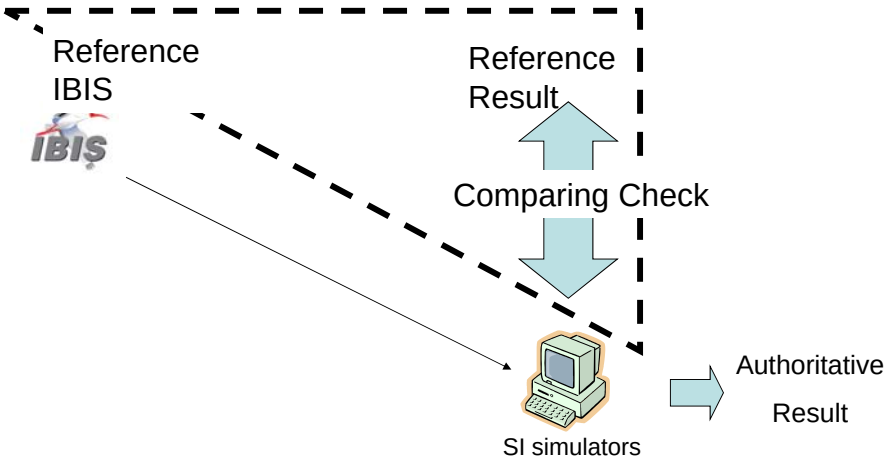
***IBIS Quality* Framework**

But,
In order to use IBIS model as real **de-facto standard,**

Now, we may need to have

The quality framework for SI simulators

The quality framework for SI simulators



Many thanks for helping to do the experiment.

IBITECH Co., LTD
BOARD TECHNOLOGY Ltd
TOWA Electronics Co., Ltd
Cedar-Creek Co., Ltd
Xpeedic Technology, Inc.

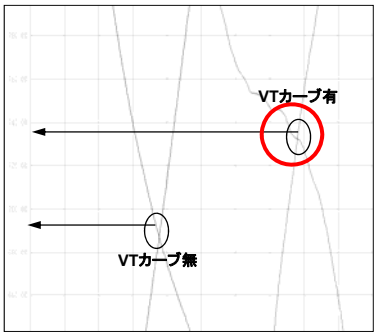
Epilogue

I did another experiment.

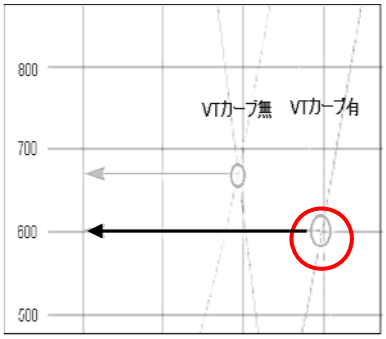
Same IBIS and same SI simulator but different Engineer.

The result was……

The result was…… **Different!** ?



Engineer Mr. A



Engineer Mr. B

Engineer's skill makes the result difference

Today, IBIS model is getting to be real de-facto standard.

Every body can get good IBIS.

So many engineers (From beginner to expert) are using IBIS model.

But, SI simulator is not magical tool yet.

It still depends on engineer's skill.

We need

- GOOD IBIS and GOOD TOOL
- GOOD Engineer and GOOD support.

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IBIS VT Waveform and Over Clocking

Xuefeng Chen
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SYNOPSYS
Asian IBIS Summit Meeting
Shanghai, China
November 15, 2011

Outline

- Introduction to over clocking
- Adjust VT waveform for better simulation
- Suggestion of new IBIS keyword
- Conclusions

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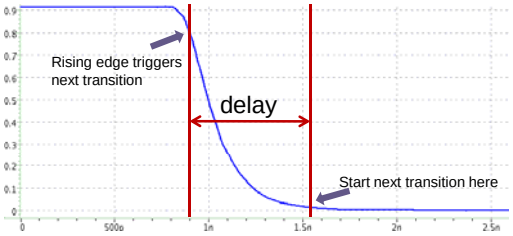
Introduction to over clocking

- **Over clocking:**
  Next transition is triggered when this transition is not finished.

- **Transistor level buffer behavior for over clocking:**
  This transition will continue with a delay time, and then start new transition. (Refer :http://www.vhdl.org/pub/ibis/summits/jun03b/muranyi2.pdf)



- **IBIS buffer behavior for over clocking:**
  Difference exists for different tools.

Introduction to over clocking(Cont.)

- Some research for over clocking in IBIS summit meetings:
  - http://www.vhdl.org/pub/ibis/summits/jun03b/muranyi2.pdf
    - research over clocking by behavior of transistor level buffer
    - provide two algorithm ideas
  - http://www.vhdl.org/pub/ibis/summits/sep05/haller2.pdf
    - add VT offset in IBIS model
    - may loose FF to SS timing relationship
  - http://www.vhdl.org/pub/ibis/summits/jun07/wang.pdf
  - http://www.vhdl.org/pub/ibis/summits/feb07/wang.pdf
    - compare behavior of transistor level buffer and IBIS buffer
    - provide relation of bit width and over clocking
    - provide algorithm enhancement in the simulation equation with PU&PD scaling coefficients.

Adjust VT waveform for Better Over Clocking Simulation

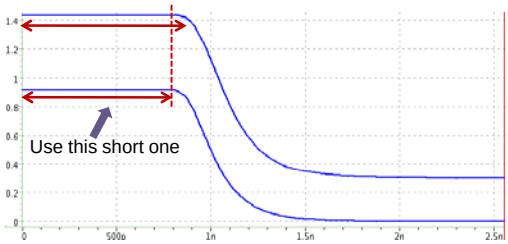
• This presentation is focused on the detailed adjustment method of two kinds of VT waveform truncations for better over clocking simulation (especially the first one):

1. **Remove initial delay**
2. **Remove flat tail**

Remove Initial Delay for Better Over Clocking Simulation

Definition of Falling/Rising Initial Delay :

• Usually, there are two falling VT waveforms.
• The falling initial delay is defined to be the minimum of initial flat part.



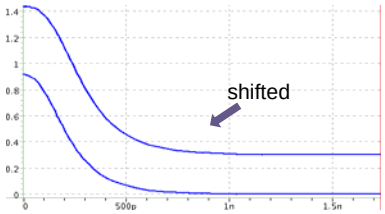
(VT waveform in IBIS model)

• The value of rising initial delay is defined in a similar way.

Remove Initial Delay for Better Over Clocking Simulation(Cont.)

Simulation with Initial Delay Removed VT:

• After remove initial delay, VT waveforms are shifted and time span(i.e. last T value) is shortened. So over clocking maybe "**avoided**".



(VT waveform in IBIS model)

• **Issue:**

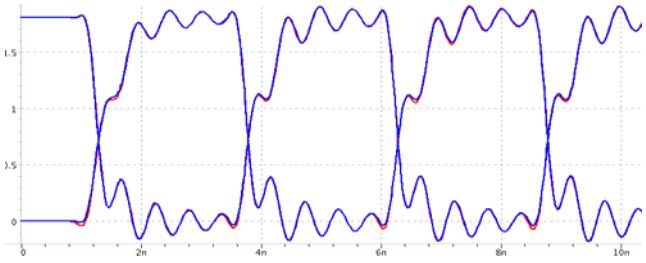
1) The output waveform will be shifted too.
2) Loss timing relation of rising and falling for different falling and rising initial delays. Obviously, it's important for cross point of differential outputs.
3) Loss timing relation of corners of 'Typ', 'Min', 'Max'

Remove Initial Delay for Better Over Clocking Simulation(Cont.)

Solution of No Timing Impact Simulation:

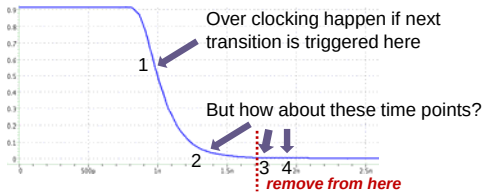
For simulator, add falling and rising delay in input stimulus respectively.

Example: output buffers + T line + input buffers (differential)



blue: result at receivers by this solution
red: result at receivers of no VT adjustment

Remove Flat Tail for Better Over Clocking Simulation

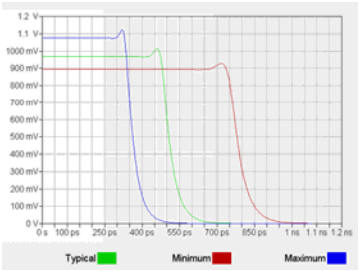


- It's for algorithm stability(although few cases show improvement)
  - For real over clocking, buffer does not start from initial stable state of next transition. Instead, it starts from one middle state(i.e. Kpu&Kpd are not 0 or 1).
  - If remove the flat tail, then the time span is shortened. Simulator is easy to detect that current transition is finished for trigger points of 3,4.
- It seems conflicting with IBIS cookbook.
  - Cookbook suggests to extract VT with long enough time for stable state.
  - But experiments show removing flat tail is not sensitive to simulation result

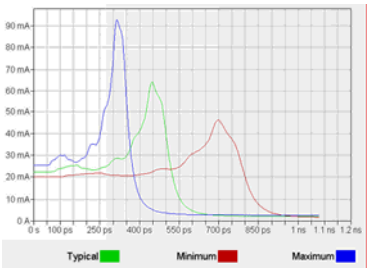
Suggestion of New Keyword in IBIS Spec. for Preceded Solution

- Add keywords of "[Fall Initial Delay]" and "[Rising Initial Delay]" with values of typ, min, and max in IBIS model.
- VT waveforms in model are truncated with above initial delays, and start from new time zero point.
- Advantages for using such keywords:
  - There is no impact for timing relation between falling and rising or different corners.
  - For over clocking cases, simulator difference will be decreased.

New Challenge for [Composite Current]



(Falling VT waveforms)



(Related Composite Current)

- Only removing initial delay of VT will lost useful data of composite current. (A simple solution is to use the minimum of initial flat part of VT and IT)
- Need much more research on behavior of transistor level buffer for composite current when over clocking happens.

Conclusions

- This presentation provides a detailed solution of VT adjustment with new IBIS keywords for better over clocking simulation.
- Suggest to use a common solution to decrease simulator difference on this aspect.
- There is new challenge for over clocking case simulation with new IBIS feature – [Composite Current]

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IBIS Parsers

Bob Ross
Asian IBIS Summit
Shanghai, China
November 15, 2011
bob@teraspeed.com

TERASPEED CONSULTING GROUP

Presentation Topics

- ibischk5
  - Operation
  - Spread sheet for messages
  - Some new checks
- tschk2
  - Operation
  - Messages
- Conclusions

TERASPEED CONSULTING GROUP

"ibischk5" Parser

- Ibischk5, Version 5.0.7
  - Free executables: http://www.eda.org/ibis/ibischk5/
  - Supports IBIS Version 5.0 (ratified 2008)
    - Algorithmic model interface for Serdes analysis
    - Power delivery system SSO and gate modulation
    - EMI parameters
    - Other – (area based thresholds)
- Checks all [IBIS Ver]s of IBIS files
  - (1.1, 2.1, 3.2, 4.2, 5.0)
- Over $114,000 of contracted work since 1993
- Supports .ibs, .pkg, .ebd, and .ami formats
  - directly or through linkages from top level file

TERASPEED CONSULTING GROUP

New Flags in ibischk5

```
Usage: ibischk5       <IBS filename>
     : ibischk5  -ebd <EBD filename>
     : ibischk5  -pkg <PKG filename>
     : ibischk5  -ami <AMI filename>
Usage: ibischk5  -caution -numbered      <IBS filename>
     : ibischk5  -caution -numbered -ebd <EBD filename>
     : ibischk5  -caution -numbered -pkg <PKG filename>
     : ibischk5  -caution -numbered -ami <AMI filename>
The flags prior to the file name can be in any order,
and the -caution and/or -numbered flags are optional.
```

- **–ami** for <file_name>.ami (algorithmic model interface control file)
- **–numbered** for numbered **E**rror, **W**arning, **N**otes and **C**aution messages

TERASPEED CONSULTING GROUP

ibischk5 {–numbered} –ami file4.ami

```
Checking file4.ami for IBIS 5.0 Compatibility...

ERROR - Illegal Usage value A specified for Param1
ERROR - Illegal Type value B specified for Param1
ERROR - Illegal Format value C specified for Param1
ERROR - No Reserved_Parameters found

Errors  : 4

File Failed
```

```
Checking file4.ami for IBIS 5.0 Compatibility...

E4627 - Illegal Usage value A specified for Param1
E4627 - Illegal Type value B specified for Param1
E4627 - Illegal Format value C specified for Param1
E4622 - No Reserved_Parameters found

Errors  : 4

File Failed
```


New: Message Number File (1155 unique message strings)

	Number	Symbol in Code	Message string	Parameters	Comment	Category	Clasification
2	100	MDL_ERR_0	Unable to Allocate Memory: %s %d	filename, line number	The code failed to allocate memory in <filename> at <linenumber>	Internal Error	E
3	101	MDL_ERR_1	Unable to get IBIS structure		Program data structures are corrupt	Internal Error	E
4	102	MDL_ERR_2	Orphan Model keyword.		Model keyword found but not within a Model declaration	Error with IBIS file Line number	E
5	103	MDL_ERR_3	Illegal Digital Port <%s> (not allowed in SPICE Ports section)	portname	Improper use of Digital port <portname>	Error with IBIS file Line number	E
6	104	MDL_ERR_4	D_switch not allowed with (D_drive,D_receive,or D_enable) in		Improper use of D_switch	Error with IBIS file Line number	E
7	105	MDL_ERR_5	%s not allowed with D_switch in Ports/A2D/D2A Section			Error with IBIS file Line number	E
8	106	MDL_ERR_6	Reserved Digital Port <%s> used as	portname	Improper use of Reserved Digital port <portname>	Error with IBIS file Line number	E
9	107	MDL_ERR_7	Orphan data line keyword.		A Model related data line was found where none was expected	Error with IBIS file Line number	E
10	108	MDL_ERR_8	TTgnd Typical value should be > 0		Improper TTgnd typical value	Error with IBIS file Line number	E
11	109	MDL_ERR_9	TTgnd Min value should be > 0		Improper TTgnd minimum value	Error with IBIS file Line number	E
12	110	MDL_ERR_10	TTgnd Max value should be > 0		Improper TTgnd maximum value	Error with IBIS file Line number	E
13	111	MDL_ERR_11	TTgnd typ value is not in between		Improper range for TTgnd	Warning	W
14	112	MDL_ERR_12	TTpower Typical value should be > 0		Improper TTpower typical value	Error with IBIS file Line number	E
15	113	MDL_ERR_13	TTpower Min value should be > 0		Improper TTpower minimum value	Error with IBIS file Line number	E
16	114	MDL_ERR_14	TTpower Max value should be > 0		Improper TTPower maximum value	Error with IBIS file Line number	E
17	115	MDL_ERR_15	TTpower typ value is not in between		Improper range for TTPower	Warning	W
18	116	MDL_ERR_16	[Model Spec] should be specified immediately after all the subparameters of a model and		Improper positioning of [Model Spec]	Error with IBIS file Line number	
19	117	MDL_ERR_17	[Receiver Thresholds] should not be specified for model type %s	modeltype	Receiver thresholds are not allowed for a <modeltype> which is not an Input or I/O model type	Warning with IBIS file Line number	W
20	118	MDL_ERR_18	[Add Submodel] should be specified before other keywords for a model		Improper positioning of [Ad Submodel]	Error with IBIS file Line number	E
21	119	MDL_ERR_19	%s Already Defined For Model '%s'	sub parameter/keyword, modelname	A model <sub-parameter or keyword> was already defined for <modelname>	Error with IBIS file Line number	E
22	120	MDL_ERR_20	[Receiver Thresholds] should be specified immediately after all the subparameters of a model and before the other keywords of a		Improper positioning of [Receiver Thresholds] keyword	Error with IBIS file Line number	E
23	121	MDL_ERR_21	Expecting Keyword. Invalid Line		An invalid line was found where a keyword was expected	Error with IBIS file Line number	E

Message Columns (for documentation and sorting)

- **Number** (printed message number)
- **Symbol in Code** (by module grouping)
  - Example: ALGMODERR_25 (message 25 of 36 AMI module messages)
- **Message String** (all unique message strings)
- **Parameters** (if applicable for printed % arguments)
  - For line numbers, keywords, subparameters, etc.
- **Comment** (brief description)
- **Category** (Error, Warning Notes, Caution, etc.)
- **Classification** (E, W, N, C added for easier sorting)

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Recent ibischk5 Fixes

- dV of [Ramp] dV/dt_r, dV/dt_f Caution checks
  - BUG104, BUG123, BUG130 (case-sensitivity crash)
  - Can be used to find the exact dV values based on I-V tables and specified ramp load conditions
  - Calculated value reported if wrong value entered
- [Model Spec] timing test load entries
  - BUG122 for waveform crossing Vmeas test
- [ISSO PU] and [ISSO PD] table time entry mismatches
  - BUG115, BUG116
  - BUG129 time alignment test from Error to Caution

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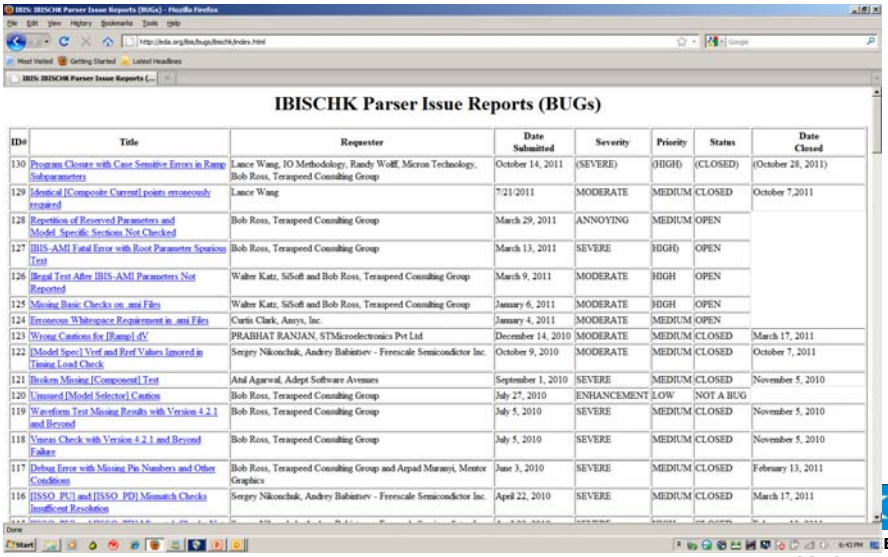
Bug List for Filed BUG Reports

http://www.eda.org/ibis/bugs/ibischk/



IBISCHK Parser Issue Reports (BUGs)

ID#	Title	Requester	Date Submitted	Severity	Priority	Status	Date Closed
130	Program Closure with Case Sensitive Errors in Ramp Subparameters	Lance Wang, IO Methodology; Randy Wolff, Micron Technology; Bob Ross, Teraspeed Consulting Group	October 14, 2011	(SEVERE)	(HIGH)	(CLOSED)	(October 28, 2011)
129	Identical [Composite Current] points erroneously required	Lance Wang	7/21/2011	MODERATE	MEDIUM	CLOSED	October 7,2011
128	Repetition of Reserved Parameters and Model_Specific Sections Not Checked	Bob Ross, Teraspeed Consulting Group	March 29, 2011	ANNOYING	MEDIUM	OPEN	
127	IBIS-AMI Fatal Error with Root Parameter Spurious Text	Bob Ross, Teraspeed Consulting Group	March 13, 2011	SEVERE	HIGH)	OPEN	
126	Illegal Text After IBIS-AMI Parameters Not Reported	Walter Katz, SiSoft and Bob Ross, Teraspeed Consulting Group	March 9, 2011	MODERATE	HIGH	OPEN	
125	Missing Basic Checks on .ami Files	Walter Katz, SiSoft and Bob Ross, Teraspeed Consulting Group	January 6, 2011	MODERATE	HIGH	OPEN	
124	Erroneous Whitespace Requirement in .ami Files	Curtis Clark, Ansys, Inc.	January 4, 2011	MODERATE	MEDIUM	OPEN	
123	Wrong Cautions for [Ramp] dV	PRABHAT RANJAN, STMicroelectronics Pvt Ltd	December 14, 2010	MODERATE	MEDIUM	CLOSED	March 17, 2011
122	[Model Spec] Vref and Rref Values Ignored in Timing Load Check	Sergey Nikonchuk, Andrey Babintsev - Freescale Semiconductor Inc.	October 9, 2010	MODERATE	MEDIUM	CLOSED	October 7, 2011
121	Broken Missing [Component] Test	Atul Agarwal, Adept Software Avenues	September 1, 2010	SEVERE	MEDIUM	CLOSED	November 5, 2010
120	Unused [Model Selector] Caution	Bob Ross, Teraspeed Consulting Group	July 27, 2010	ENHANCEMENT	LOW	NOT A BUG	
119	Waveform Test Missing Results with Version 4.2.1 and Beyond	Bob Ross, Teraspeed Consulting Group	July 5, 2010	SEVERE	MEDIUM	CLOSED	November 5, 2010
118	Vmeas Check with Version 4.2.1 and Beyond Failure	Bob Ross, Teraspeed Consulting Group	July 5, 2010	SEVERE	MEDIUM	CLOSED	November 5, 2010
117	Debug Error with Missing Pin Numbers and Other Conditions	Bob Ross, Teraspeed Consulting Group and Arpad Muranyi, Mentor Graphics	June 3, 2010	SEVERE	MEDIUM	CLOSED	February 13, 2011
116	[ISSO_PU] and [ISSO_PD] Mismatch Checks Insufficient Resolution	Sergey Nikonchuk, Andrey Babintsev - Freescale Semiconductor Inc.	April 22, 2010	SEVERE	MEDIUM	CLOSED	March 17, 2011

"tschk2" Parser

- Checks Touchstone Version 1.0 (TS1) and Version 2.0 (TS2)
  - Error and Warning numbers
  - Free executables: http://www.eda.org/ibis/tschk2/
- Converts TS1 to TS2, TS2 to TS1 where practical with **-canonical*** flags
- Provides comment headers and real, imaginary format (RI) with **-describe** flag
- Source code package includes 440+ test cases
- C++, well documented
- Thanks to contractor Agilent Technologies

tschk2 {-canonical*} FILE

- **{-canonical | -canonical-v2}**
  - **TS1, TS2 → TS2**
  - Provides number of ports, frequencies and other information
  - Un-normalizes TS1 Y-, Z-, G- and H-parameters and effective noise resistance
- **{-canonical-v1}**
  - **TS1, TS2 → TS1** where practical
  - Applies column formatting rules and 2-port 21_12 ordering
  - Normalizes TS2 Y-, Z-, G- and H-parameters and effective noise resistance
  - No mixed mode or selectable reference resistance processing

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tschk2 {-describe} FILE (header comments, RI format)

```
[Network Data]
! freq  S11re  S11im  S12re  S12im  S13re  S13im  S14re  S14im
        S15re  S15im  S16re  S16im
!       S21re  S21im  S22re  S22im  S23re  S23im  S24re  S24im
        S25re  S25im  S26re  S26im
!       S31re  S31im  S32re  S32im  S33re  S33im  S34re  S34im
        S35re  S35im  S36re  S36im
!       S41re  S41im  S42re  S42im  S43re  S43im  S44re  S44im
        S45re  S45im  S46re  S46im
!       S51re  S51im  S52re  S52im  S53re  S53im  S54re  S54im
        S55re  S55im  S56re  S56im
!       S61re  S61im  S62re  S62im  S63re  S63im  S64re  S64im
        S65re  S65im  S66re  S66im
10000   -0.665574600466     -0.00066097512141300 01  0.333068101839
    0.000663504688568   0.333100908672      -0.0006633295929
    Etc.
```

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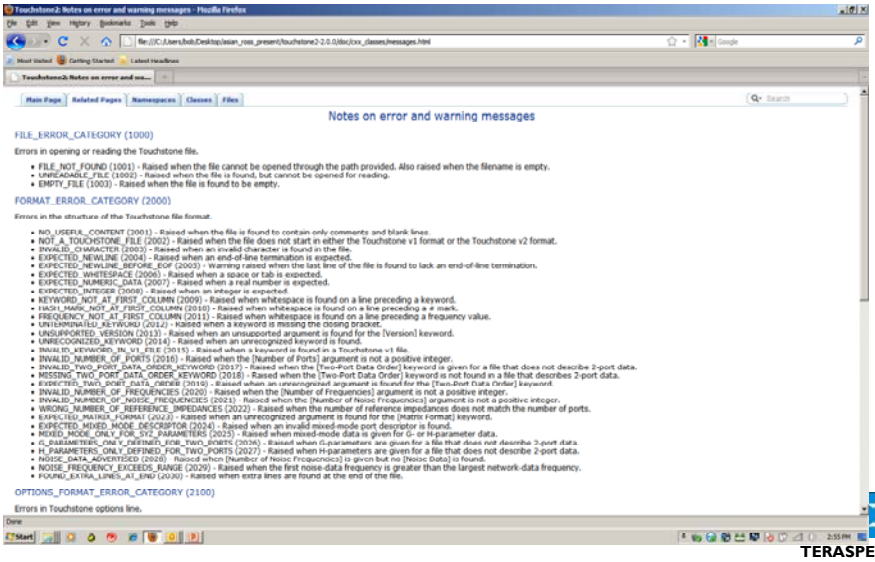
71 tschk2 Messages



Message Groupings

- Message chart in source code package
- Message categories (starting number)
  - **Full Error** (1000)
  - **Format Error** (2000)
  - **Options Error** (2100)
  - **Keyword Order** (2200)
  - **Data Format** (2300)

Conclusions

- ibischk5 and tschk2 parsers - free to **officially** check files for specification compliance
- Parser development also checks specification for accuracy and clarity
- BUG process helps maintain integrity of parsers with latest fixes

- **Parsers are critical to IBIS success**

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Useful Links Under IBIS Home Page: www.eda.org/ibis/

ver5.0/ ibischk5/	**IBIS Version 5.0** (August 29, 2008) **ibischk5 Version 5.0.7** (Pending 2011)
touchstone_ver2.0/ tschk2/	**Touchstone Version 2.0** (April 24. 2009) **tschk2 Version 2.0.0** (December 2009)
quality_ver2.0/ ibis-iss_ver1.0/	**IBIS Quality Specification** (Oct. 30, 2009) **Interconnect SPICE Subcircuit Specification Version 1.0** (New - October 7, 2011)
editorial_wip/ interconnect_wip/ macromodel_wip/ quality_wip/	**Editorial Task Group** (wip) **Interconnect Task Group** (wip) - suspended **Advanced Technology Task Group (**wip) **Quality Task Group** (wip)

(wip: work in progress)

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DDR3 System Timing Budget Analysis by SI&PI Co-Simulation

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Wang Ping, wang.ping@zte.com.cn;
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Bringing you closer

Asian IBIS Summit
Shanghai, China
November 15, 2011

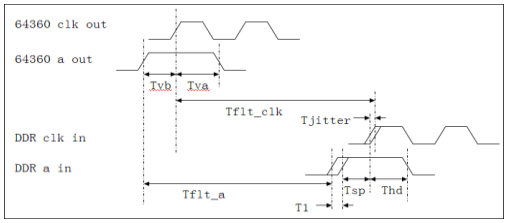
Agenda

- Traditional Timing Design for DDRx System
- Methods for DDR3 System Timing Budget Analysis
- Comparison of Two Simulation Results
- Summary

Traditional Timing Design for DDRx System

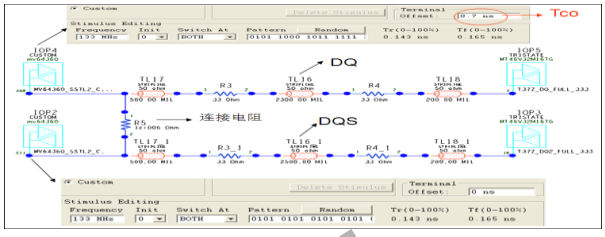
- Using Tables

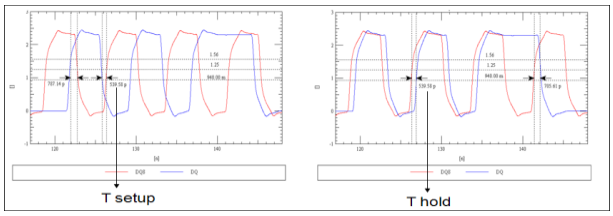
TOP NAME	DDR3_DATA_WRITE	DDR3_DATA_READ	DDR3_ADDR_CK
Timing	NODES NAME1	NODES NAME1	NODES NAME3
From:	CPU	DDR3（HYNIX）	CPU
To:	DDR3（HYNIX）	CPU	DDR3（HYNIX）
Vil/Vih	0.925/0.575	0.925/0.575	
Tsetup	0.2	0.3	0.3
Thold	0. 2	0. 15	0. 3
Vmeas	0. 75	0. 75	0. 75
Tva_min	0. 3	0.36	0.95
Testload@Tcomin			
Tvb_min	0. 3	0. 36	0. 95



Traditional Timing Design for DDRx System

- Using Simulations



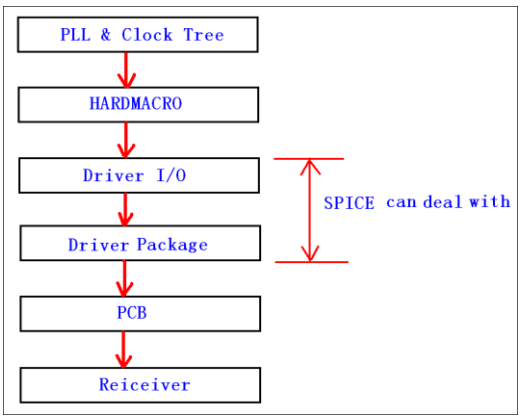


Traditional Timing Design for DDRx System

- Disadvantages of Traditional Methods:
  - It doesn't consider the influences of follow list:
    - SSN of PDN
    - Many Kinds of Jitter, Such as DQS Jitter…
    - Xtalk of Package and PCB

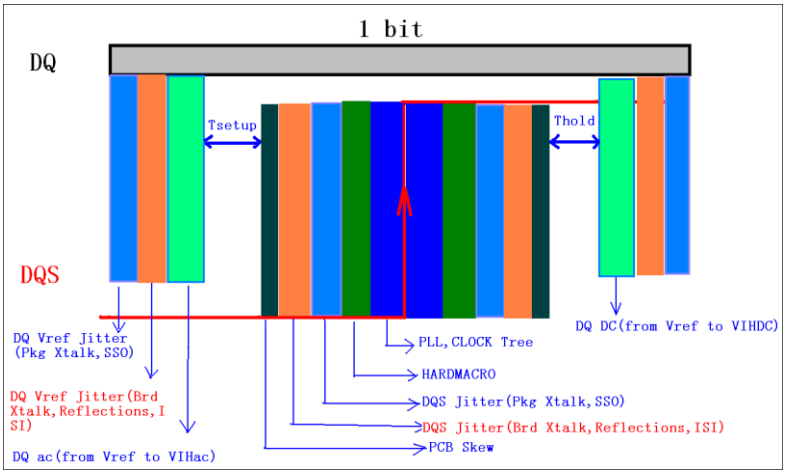
Methods for DDR3 System Timing Budget Analysis

- The DDR3 timing budget consists of observing timing margins and signal integrity of the entire interconnect
- Summarized as follows in the diagram below:



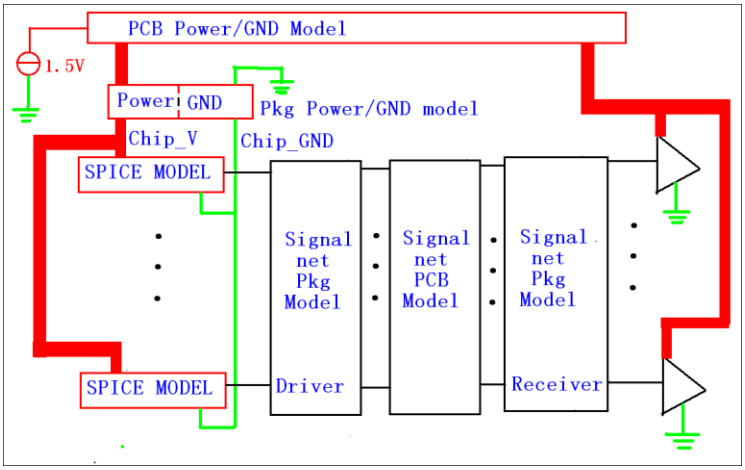
Methods for DDR3 System Timing Budget Analysis

- Timing Calculation method:

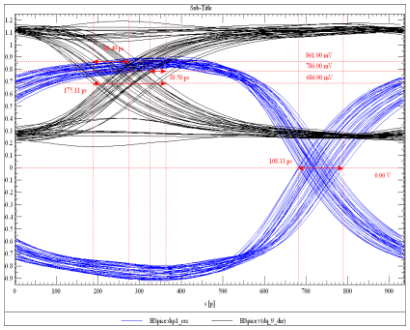


Methods for DDR3 System Timing Budget Analysis

- The Topology of DDR3 System Timing Simulation Using SPICE Models



Methods for DDR3 System Timing Budget Analysis



- An Example of DDR3 Simulation
  - Twc_io_dqs_jitter+Tbrd_io_dqs_jitter= 108.33 ps
  - Twc_io_dq_jitter_vref+Tbrd_io_dq_jitter_vref=175.11 ps
  - Tbrd_io_dq_jitter_ac=86.40 ps
  - Tbrd_io_dq_jitter_dc=38.58 ps
- Cuting all Timing Uncertainties:
  - Tsetup_min_margin=21ps
  - Thold_min_margin=32ps

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Methods for DDR3 System Timing Budget Analysis

- Analysis sources of uncertainties

Uncertainty	Source
PLL, CLOCK Tree	IC Manufacturer
HARDMACRO	IC Manufacturer
DQS Jitter(Pkg Xtalk, SSO)	IC Manufacturer
DQS Jitter(Brd Xtalk, Reflection, ISI)	Simulation Using SPICE model
DQ Vref Jitter(Pkg Xtalk, SSO)	IC Manufacturer
DQ Vref Jitter(Brd Xtalk, Reflection, ISI)	Simulation Using SPICE model
PCB Skew	PCB file
DQ ac(from Vref to VIHac)	Simulation Using SPICE model
DQ DC(from Vref to VIHDC)	Simulation Using SPICE model

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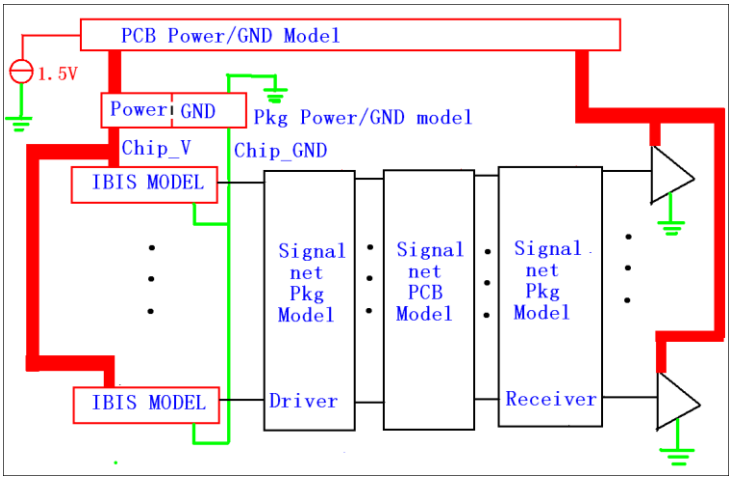
Methods for DDR3 System Timing Budget Analysis

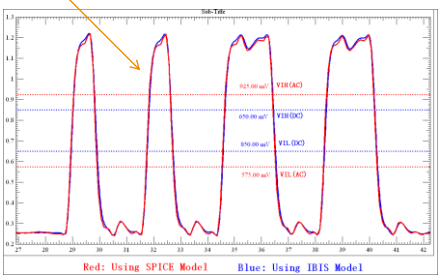
- The Topology of DDR3 System Timing Simulation Using IBIS Models



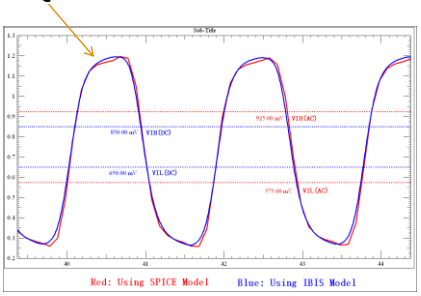
Comparison of Two Simulation Results

- Analysis Precision
  - Waveforms comparison

DQ

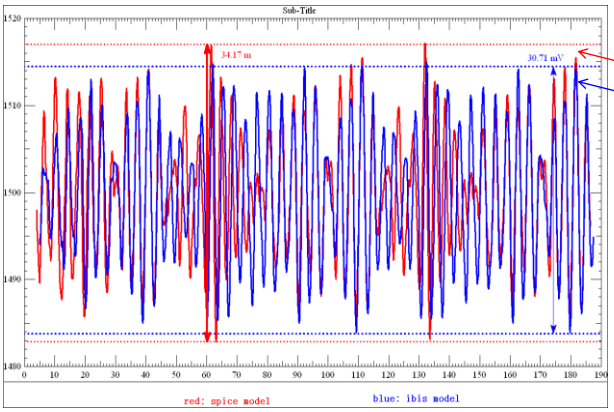


DQS



Comparison of Two Simulation Results

- Analysis Precision
  - △Vpp comparison



Spice: 34.17mV
IBIS: 30.71mV

Comparison of Two Simulation Results

- Comparison Time Consuming

Workstation	2*Intel Xeon X5680,3.33GHz,12MB Cache,6.4GT/s; 96GB (12x8GB) DDR3 RDIMM , 1333MHz	Intel Core™ 2 Duo CPU 3.00GHz 3.37GB
Simulation Time	**40 h** **128bits**	**1 min** **128bits**

- Using IBIS model is very effective in DDR3 system timing simulation .

Summary

- Choosing an appropriate modeling method is critical for simulation. Otherwise simulation may not be accurate enough or too complex and time consuming.
- The traditional way to simulate DDR3 system timing is not precise enough, because DDR3 Timing simulations need to consider all the uncertainties.
- Using the SPICE model in DDR3 timing simulation is precise, but time consuming. It's not a very effective way to work.
- IBIS model is appropriate for what-if analysis due to its relative short run time and sufficient accuracy.

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Thanks!

Bringing you closer

Modeling the On-die De-cap of IBIS 5.0 PDN-aware Buffers

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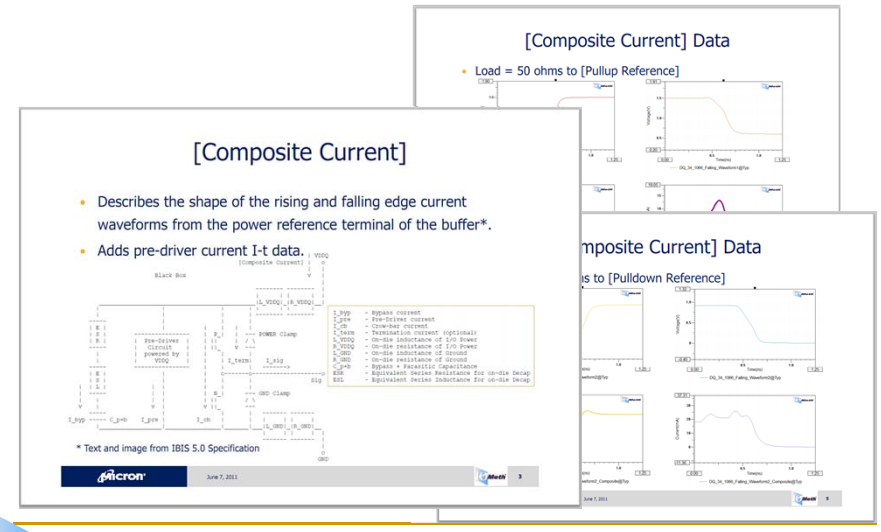
IO Methodology Inc.
Randy Wolff, rrwolff@micron.com
Micron Technology
IBIS Summit (Shanghai) Nov. 15th, 2011

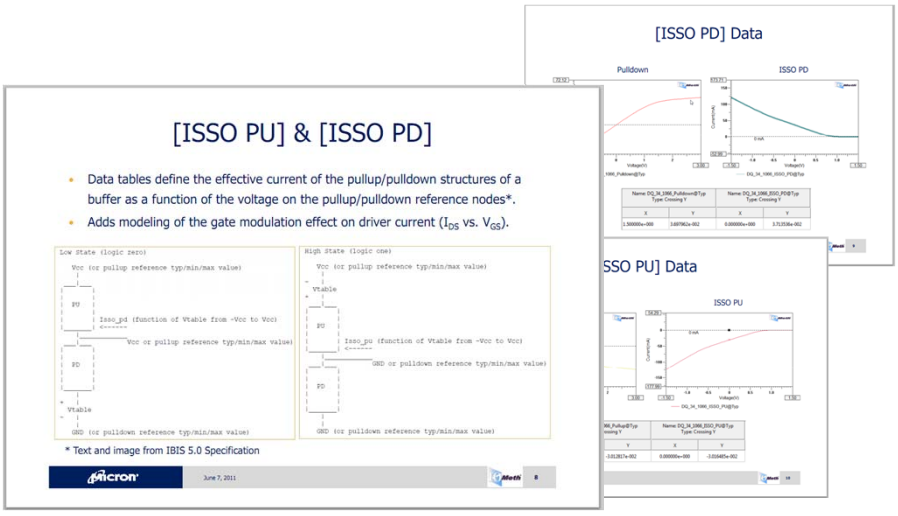
Outline

- Introduction to IBIS 5.0 PDN modeling
- On-die de-coupling circuit
- A test case and workaround
- An issue?
- Conclusions

Introduction to IBIS 5.0 PDN Modeling



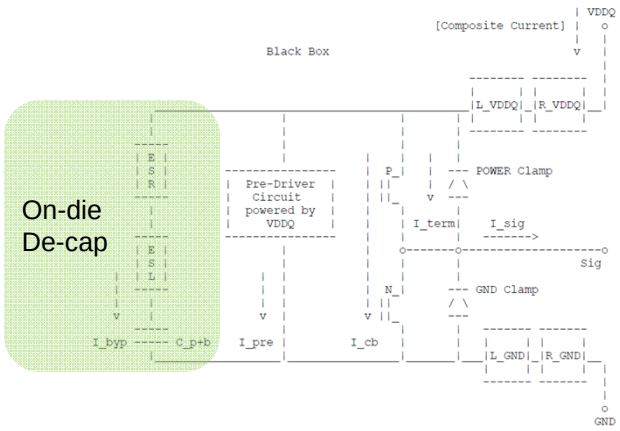
Introduction to IBIS 5.0 PDN Modeling



Introduction to IBIS 5.0 PDN Modeling

- IBIS 5.0 PDN modeling features are useful for SSN sensitive system designs
  - Parallel interfaces, Low power systems
  - Standard compliance models are interoperable and IP protected
- IBISCHK5 is up-to-date
  - Version 5.0.7 fixes BUG129
- At least 4 EDA simulators have implemented IBIS 5.0 PDN features
  - And more coming …

On-Die De-Coupling Circuit

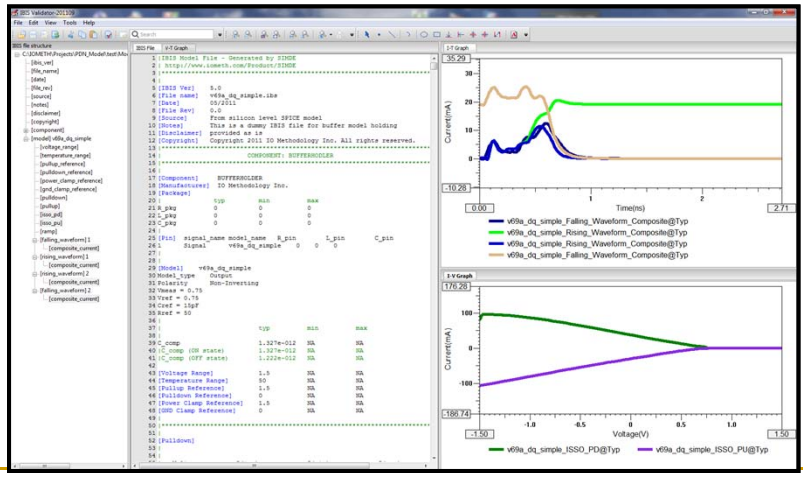


- De-cap may be on the order of 500pF per buffer

* Image from IBIS 5.0 Specification

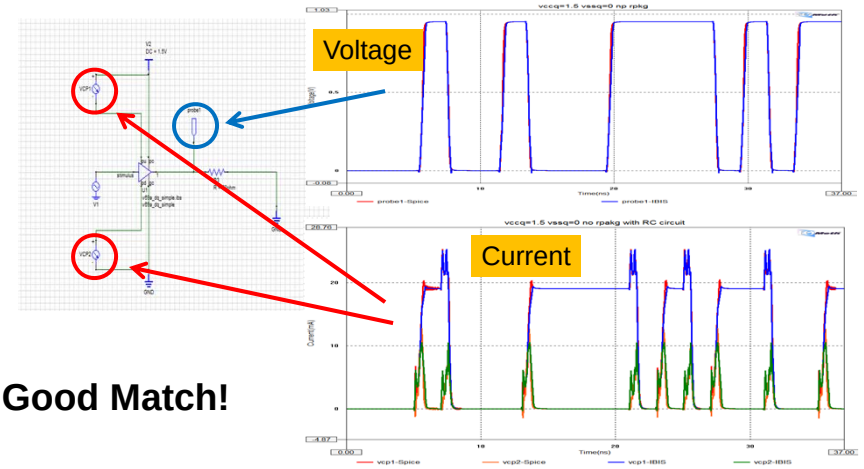
Test Case – IBIS Model

Extracted IBIS 5.0 Model – no on-die de-cap model



Test Case – IBIS vs. SPICE

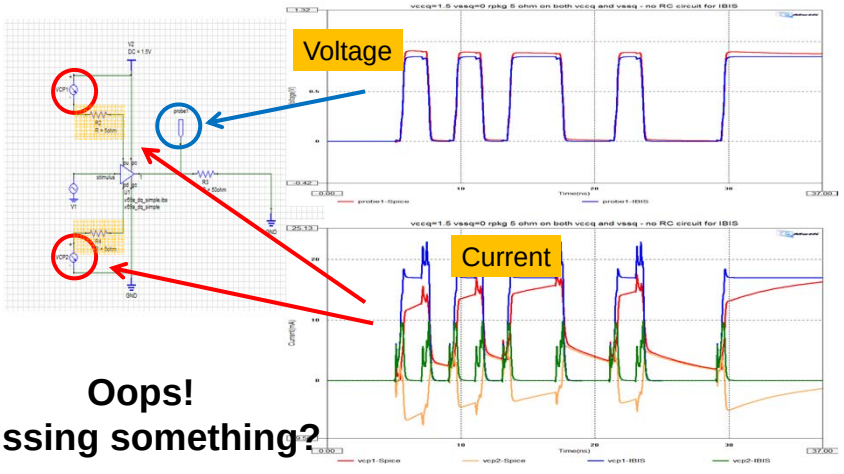
Validation with perfect power supply



Good Match!

Test Case – IBIS vs. SPICE

Validation with large R_pkg on power/gnd pins

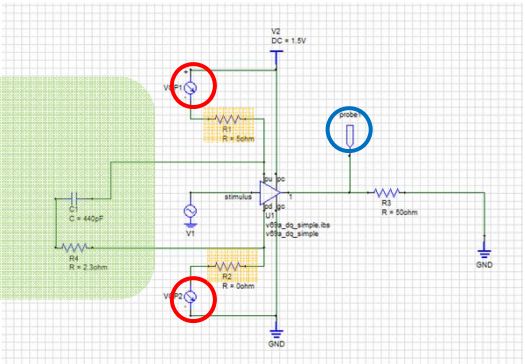


Oops!
Missing something?

Workaround

Validation with R_pkg on power/gnd pins

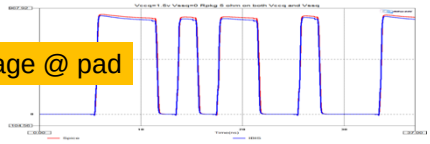
RC De-coupling circuit added into IBIS simulations



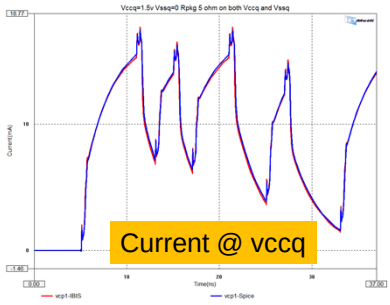
Workaround

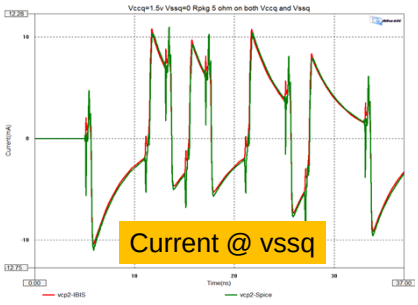
Validating with R_pkg on power/gnd pins
– added RC de-coupling circuit

Voltage @ pad



Now they match!





Modeling On-Die De-Cap

- IBIS 5.0 model extracted using the static power supply
  - IBIS model data doesn't contain any info about de-coupling circuit between Vccq and Vssq
  - There is no place for us to add this info into the [Model] section
- Solution within existing IBIS Specification
  - Use IBIS "Series" Model type (e.g. [C Series], [Rc Series]) to model de-coupling circuit
  - Use [Series Pin Mapping] to connect with Power and GND pins

There is a problem!

What is the issue?

- The Series Model de-coupling circuit attaches at the [Component] Pin level, not inside the [Model]
  - On-Die de-coupling circuit belongs to each buffer
  - In most cases, multiple buffers share one power/gnd rail
  - The only way to model per-buffer de-cap is with a per-power bus model. This might not be the desired de-cap model.

Conclusion

- IBIS 5.0 [Model] does not contain any info about decoupling between Power and GND nodes
- On-die de-coupling circuit can be added outside of IBIS [Model] to achieve accuracy requirement
- Be careful using IBIS [Series Pin Mapping] feature for On-die De-coupling Circuit modeling
- BIRD145 might provide a solution
  - Would allow complex on-die de-cap model attached to each [Model] and modeling of other important PDN parasitics


Thank You
Micron
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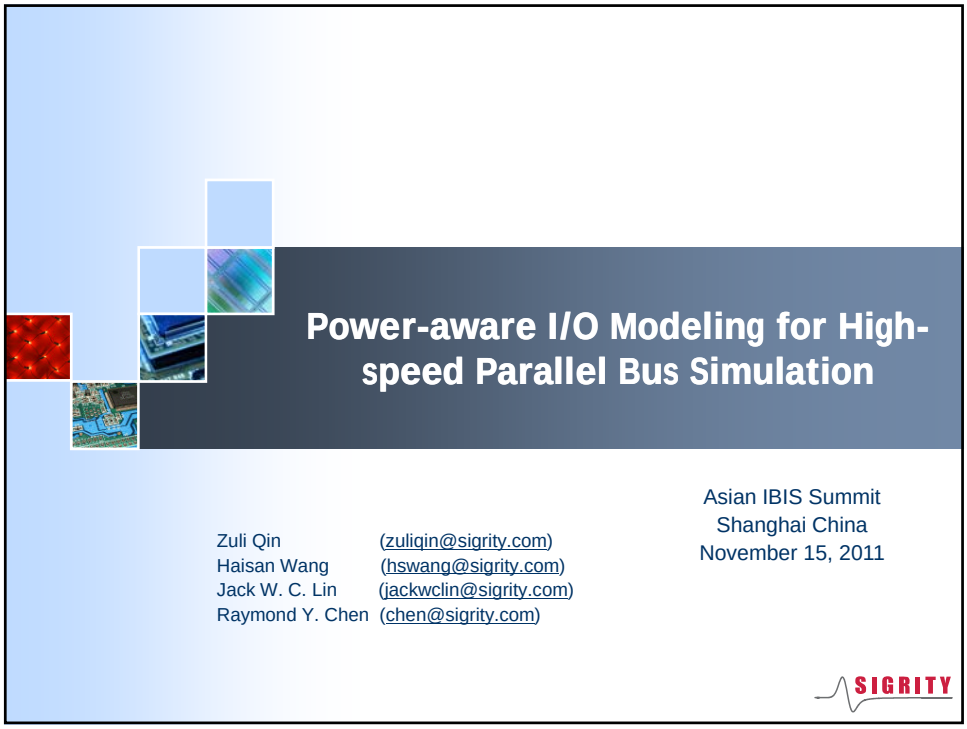
15



Power-aware I/O Modeling for High-speed Parallel Bus Simulation

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Asian IBIS Summit
Shanghai China
November 15, 2011

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Outline

- Challenge of High-speed Parallel Bus Simulation
- Power-aware I/O Modeling Progress
  - Necessity of Power-aware I/O Modeling
  - IBIS5.0 Enhancement (BIRD95/BIRD98)
  - Go beyond with IBIS5.0 – IBIS Plus
- Apply Power-aware I/O Model in Parallel Bus SSO Simulation
  - Power noise correlation
  - Signal output correlation
- Summary

2

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Challenge of High-speed Parallel Bus Simulation

3

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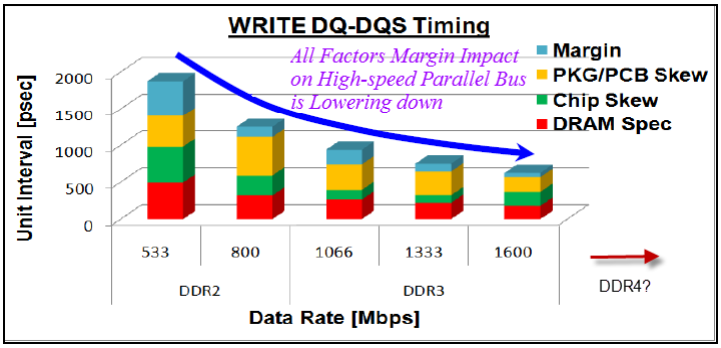
Challenge for High-speed Parallel Bus Design



- The margin for jitter/skew is getting more smaller in current high-speed parallel bus design
- The power/ground noise has became a dominate reason that cause parallel bus failure
- Power/ground to signal EM coupling should be considered in system level SSO analysis for current high-speed parallel bus timing sign-off

4

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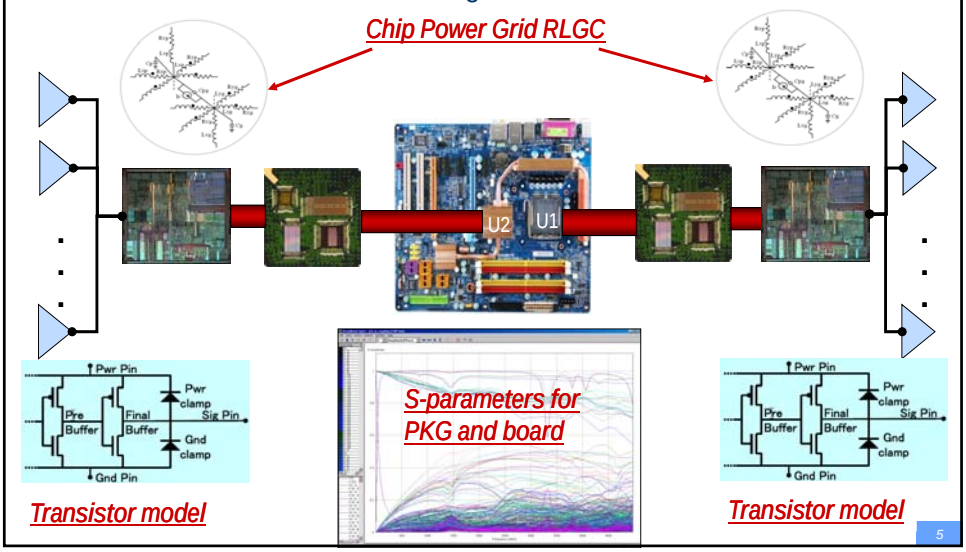
Challenge for High-speed Parallel Bus SSO Simulation

- If this is a 32 bits data SSN analysis, how long will this SPICE DECK run? will the waveform be converged?



5

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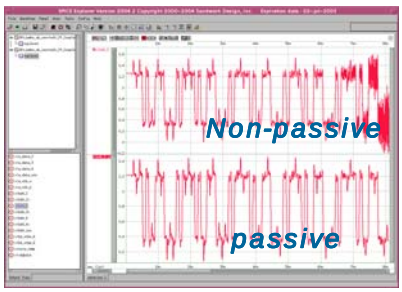
Problems in High-speed Parallel Bus SSO Simulation

- The complex manual task for the nodes linkage between circuits.
- No guaranteed for passivity and causality on each circuit block especially that model is from measurement
- Non-linearity of the whole system circuit network which including drivers and receivers transistor models
- Lost DC accuracy without low frequency data from EM solver, especially for SI analysis with power aware
- Long run time
- Waveforms are non-convergence
- …….



6

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I/O Transistor vs. IBIS Modeling

- **Summary**

I/O Transistor Netlist	IBIS Model
▪ Extracted from complete design topology, all parasitics and device library included ▪ Parameters, design information	▪ I-V/V-T tables for the final stage ▪ Pin out information

- **Trade-off**

	I/O Transistor Netlist	IBIS Model
Accuracy (SI)	Good	Good
Accuracy (PI)	Good	Enhanced in Ver5.0
Simulation Time	Slow (Usually 10X than IBIS)	Fast
Supported by EDA Tool	Not good	Good (Many EDA tool supported)
Ease of distribution	Bad (IP Consideration)	Good (IP Protection)

7

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Power-aware I/O Modeling Progress

8

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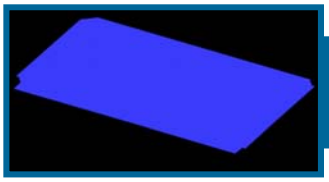
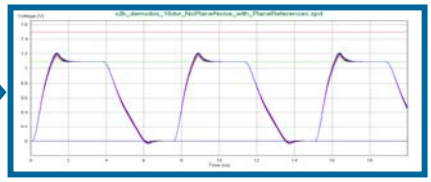
The Importance of Power-aware Analysis

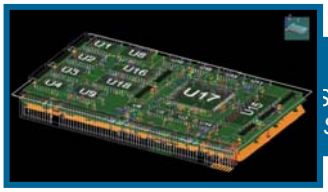


Predicts No SSN

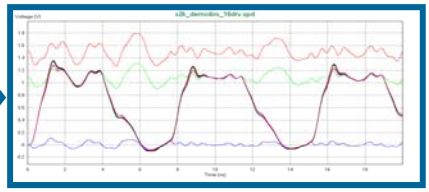


Signal data only

Simulation assuming ideal power delivery network



Predicts Significant SSN Risk



Signals, accurate planes, vias

Simulation with all power delivery effects

- Transmission line only analysis can't reveal the real signaling among ICs in current high speed parallel bus design.
- High-speed parallel bus with power-aware analysis can help to identify design defect and find out the root cause behind the problem.

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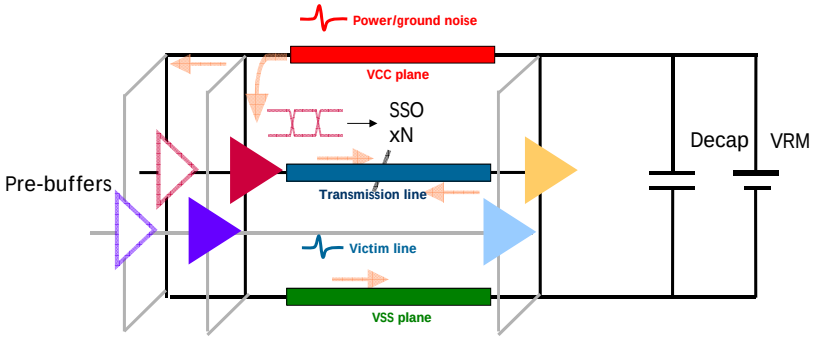
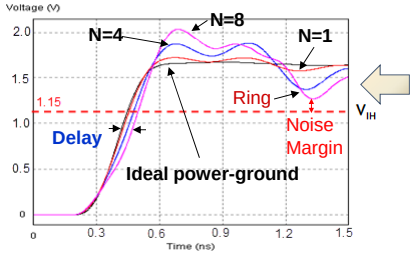
How SSN Noise Impact on Signal Quality





- **SSN noise greatly reduce the noise margin at receiver bump**
- ***SSN noise increase the buffer output delay and finally the jitter, which may cause error-sampling at receiver side***

10

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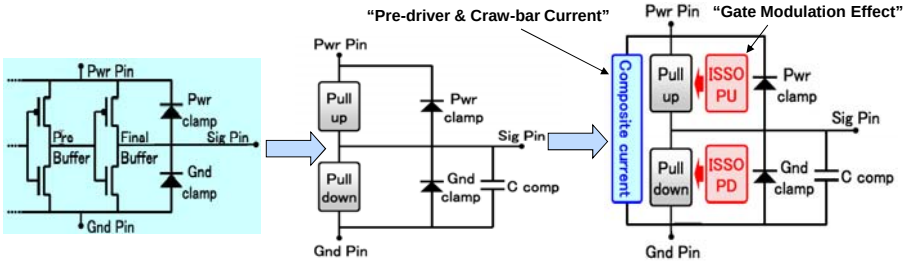
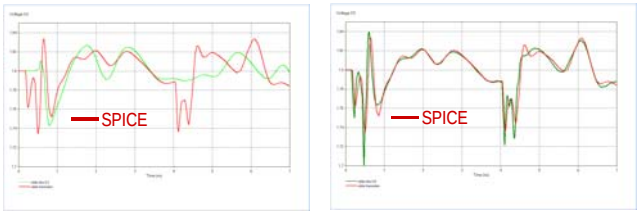
Power-aware Solution in IBIS5.0 (BIRD95/BIRD98)



Ideal Power | Power-aware (BIRD95 & 98)

Accuracy is always concerned while using behavior model. Is it good enough for IBIS5.0?



IBIS4.2 vs. Transistor | IBIS5.0 vs. Transistor

11

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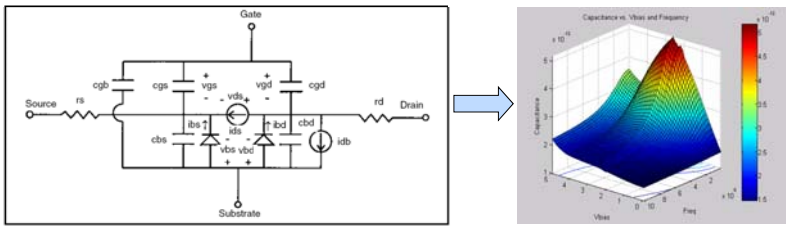
Go Beyond with IBIS5.0

Advantage

- IBIS5.0 is designed for more accurate SI simulation with non-ideal power distribution system (PDS)
- IBIS5.0 greatly improves the correlation accuracy with transistor model with simple but effective methodology
  - By including composite current, more accurate power noise simulation can be performed to have better power/signal integrity evaluation
  - Dynamic power noise impact on signal output waveform is considered in IBIS5.0, which greatly improve the efficiency of using IBIS model in high-speed parallel bus timing sign-off

But it's good enough?

- On-die power/ground impedance is omitted
- The state-dependent non-linear output impedance is modeled with single or splited die capacitance, which may over- or under-estimate the buffer AC effects



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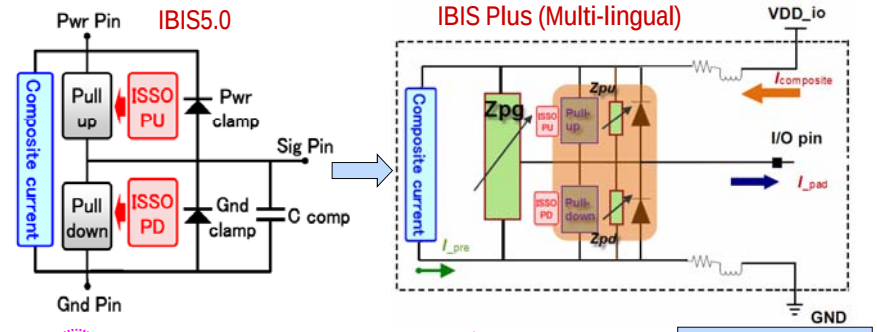
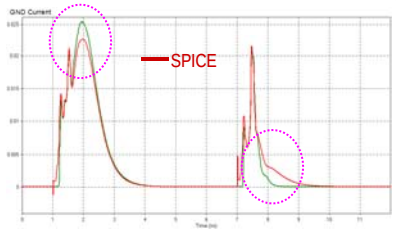
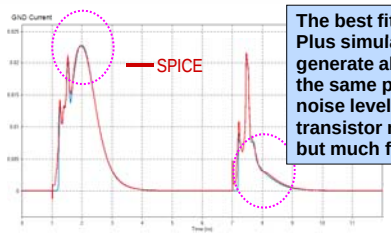
Go Beyond with IBIS5.0





IBIS5.0 vs. Transistor



IBIS Plus vs. Transistor

The best fitted IBIS Plus simulation generate almost the same power noise level with transistor model but much faster

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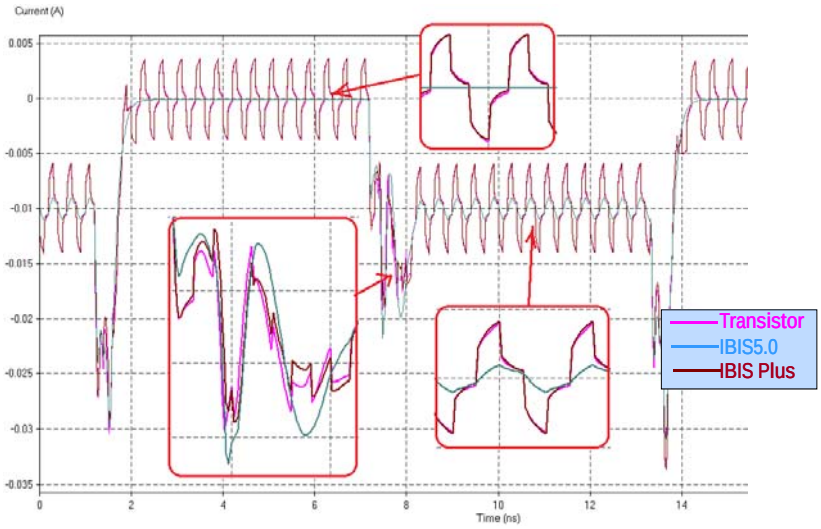
Go Beyond with IBIS5.0 (case study)



** HSTL18 I/O, 150 Ohm termination in parallel with 1pF*

VCC=1.8V, 0.05V 2.5GHz AC noise

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High-speed Parallel Bus SSO Simulation

15

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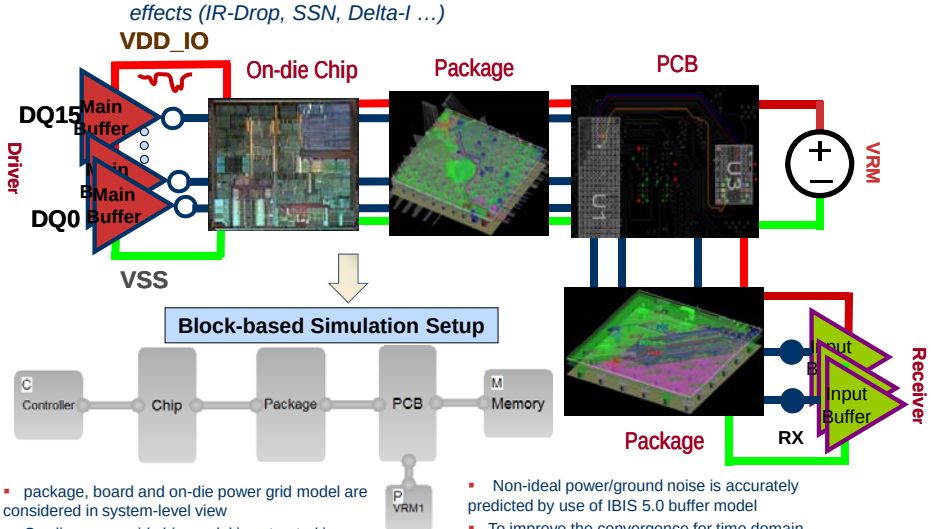
DDR3 System-level SSO Simulation (case study)

System-level Correlation to consider all power fluctuation effects (IR-Drop, SSN, Delta-I …)



- package, board and on-die power grid model are considered in system-level view
- On-die power grid chip model is extracted in distributed format with all MOS caps included

- Non-ideal power/ground noise is accurately predicted by use of IBIS 5.0 buffer model
- To improve the convergence for time domain analysis, broadband PKG/board S-parameter model are converted into broadband SPICE circuit

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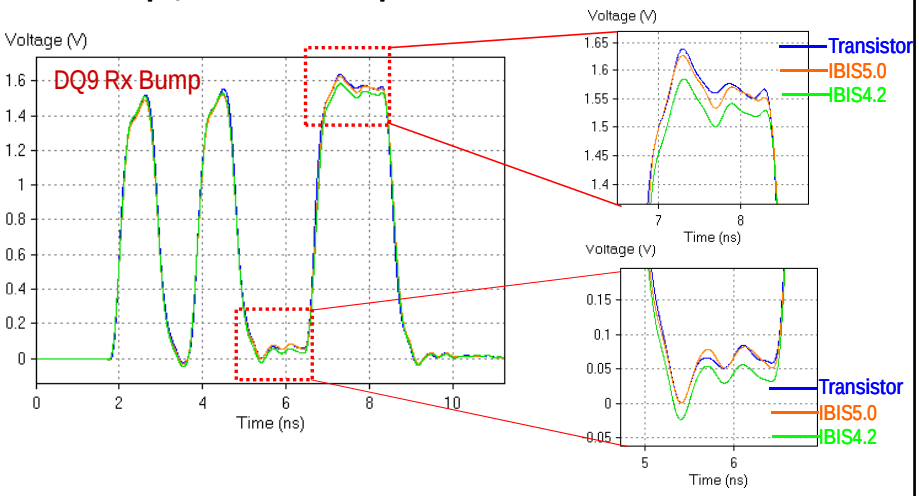
DDR3 System-level SSO Simulation (case study)

Signal Output Waveform Comparison (IBIS4.2 vs. IBIS5.0)

1066Mbps, "10100110" Input Pattern



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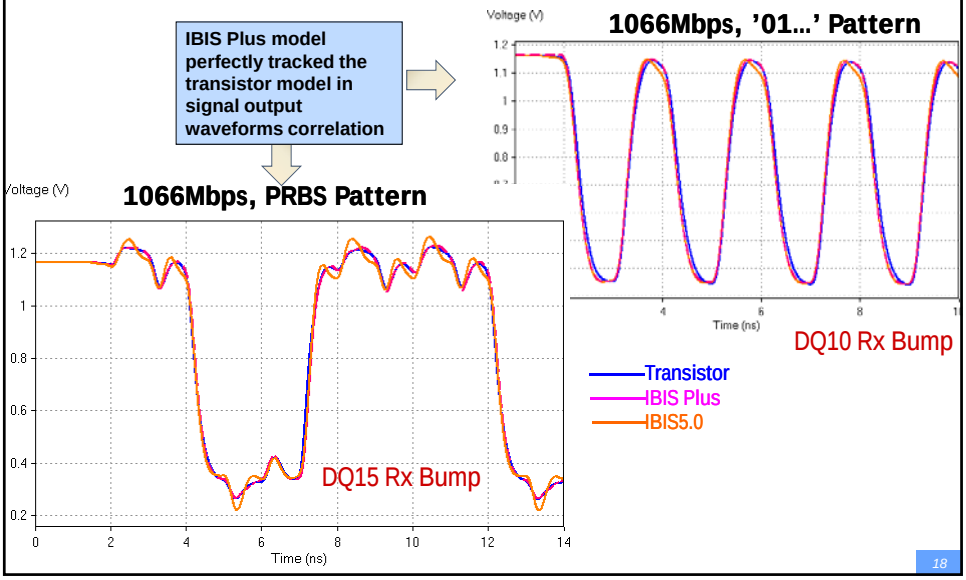
DDR3 System-level SSO Simulation (case study)

Signal Output Waveform Comparison (IBIS5.0 vs. IBIS Plus)

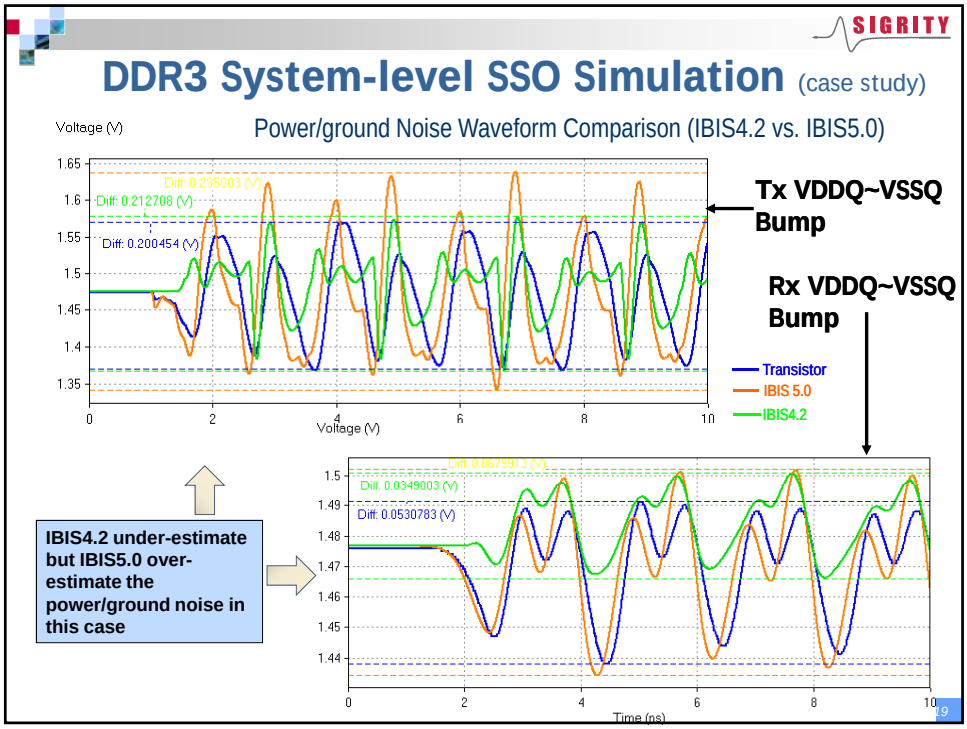
IBIS Plus model perfectly tracked the transistor model in signal output waveforms correlation

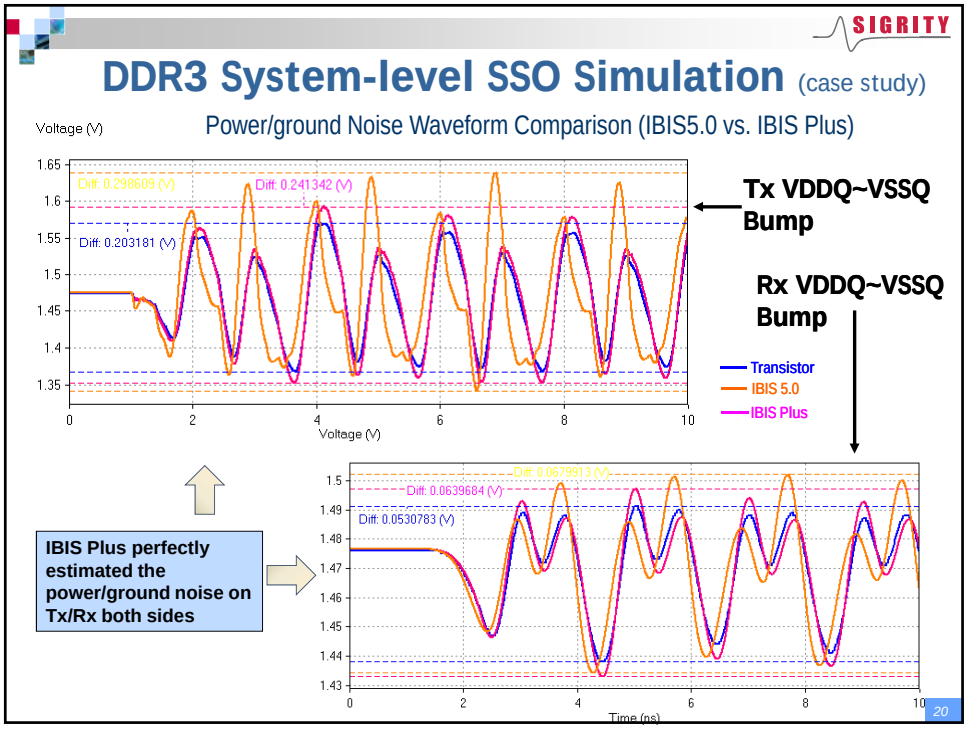
1066Mbps, '01…' Pattern

1066Mbps, PRBS Pattern



18


SIGRITY
DDR3 System-level SSO Simulation (case study)
Power/ground Noise Waveform Comparison (IBIS4.2 vs. IBIS5.0)
Voltage (V)
Diff: 0.295003 (V)
Diff: 0.212708 (V)
Diff: 0.200454 (V)
Tx VDDQ~VSSQ Bump
Rx VDDQ~VSSQ Bump
Transistor
IBIS 5.0
IBIS4.2
Diff: 0.0679813 (V)
Diff: 0.0349003 (V)
Diff: 0.0530783 (V)
IBIS4.2 under-estimate but IBIS5.0 over-estimate the power/ground noise in this case
Time (ns)
19


SIGRITY
DDR3 System-level SSO Simulation (case study)
Power/ground Noise Waveform Comparison (IBIS5.0 vs. IBIS Plus)
Voltage (V)
Diff: 0.298609 (V)
Diff: 0.241342 (V)
Diff: 0.203181 (V)
Tx VDDQ~VSSQ Bump
Rx VDDQ~VSSQ Bump
Transistor
IBIS 5.0
IBIS Plus
Diff: 0.0679813 (V)
Diff: 0.0639684 (V)
Diff: 0.0530783 (V)
IBIS Plus perfectly estimated the power/ground noise on Tx/Rx both sides
Time (ns)
20

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Summary

- Current high-speed parallel-bus and serial-link SI analysis require power-aware I/O model to run accurate SI analysis
- Latest IBIS5.0 improve on power-aware I/O buffer modeling with accuracy correlated in system-level SSO simulation
- Demonstrate a new method to generate more accurate behavioral circuit model (IBIS Plus) based on frequency-domain response fitting and can be delievered in IBIS compatible multi-lingual external model
- Both IBIS5.0 and IBIS Plus model show trustable accuracy in system level high-speed parallel bus simulation with non-ideal Power Distribution Network considered
- Block-level system-level simulation automation tool ease the simulation platform setup
- Need to expand the buffer modeling technology to differential (true/half) I/O and more complex I/O design

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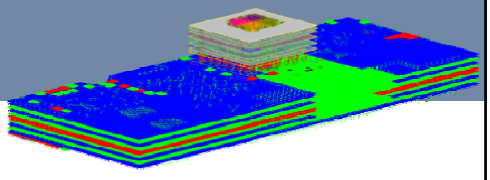
Thank You!



22

The Application of IBIS-AMI Model Cascaded Simulation for 10 Gigabit Repeater Serial Link Analysis

www.huawei.com

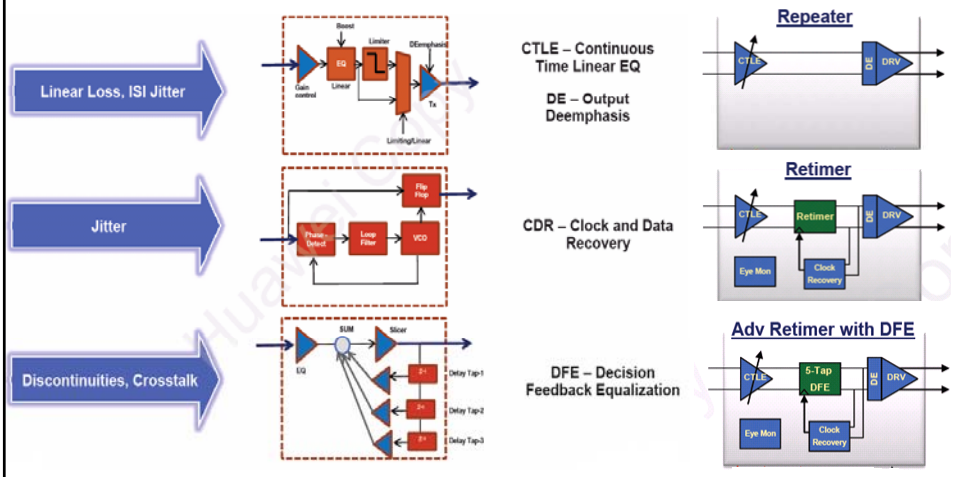
Asian IBIS Summit, Shanghai China, November 15, 2011

Zhengrong Xu, Huawei
Luyu Ma, Huawei
Ken Willis, Sigrity
Haisan Wang, Sigrity
Lee Sledjeski, TI
Nate Unger, TI
HUAWEI TECHNOLOGIES CO., LTD.

Agenda

- Where repeaters might be applied
- The application of repeater in 10G channel
- Needs for repeater simulation
- Repeater topology
- IBIS-AMI data flow and APIs
- Test and simulation correlation
- How to select the repeater parameter
- Summary

Where repeaters might be Applied



Note: All these devices are referred as "repeaters" in this presentation

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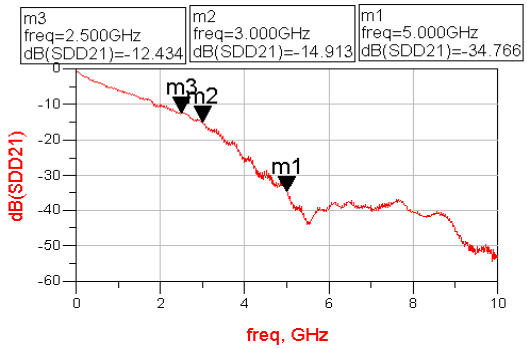
The application of repeater in 10G channel

- **Insertion loss increase with data rate up to 10G at the same channel**
- **Need repeater to enhance the transmission distance for 10G-SR SerDes IP**



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The application of repeater in 10G channel (cont.)

- SFF 8431 defines 10G SFP+ module electrical interface specification
- Hardly meet the channel spec. if FR4 trace is longer than 5 inch
- Repeater reduce ISI jitter to meet the eye mask requirement when trace length is longer than 5 inch

Table 25 SFI Host Interconnect Budget

Parameter	Symbol	Conditions	Min	Max	Units
Channel Transfer Including Connector measured with Host Compliance Board (see Appendix C)	SDD21	at 5.5 GHz, see 1	-6.5	-2.25	dB

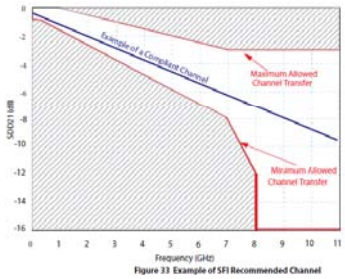

Figure 33 Example of SFI Recommended Channel

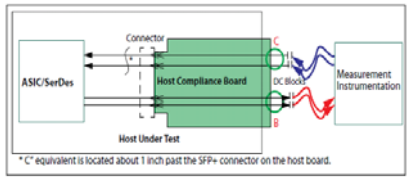

Figure 13 Host Compliance Board

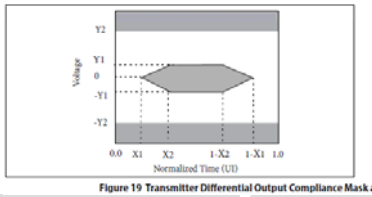

Figure 19 Transmitter Differential Output Compliance Mask at B and B*

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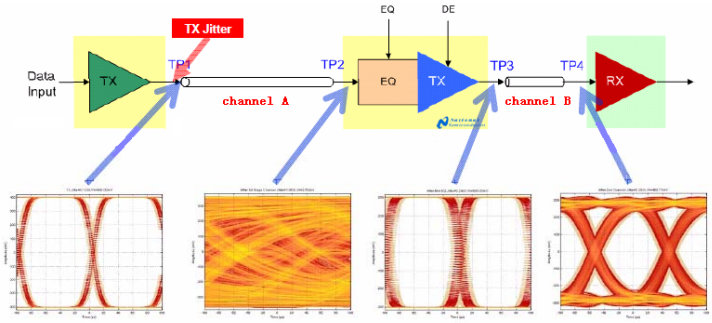
Needs for repeater simulation

- Industry high speed specification just for point to point application, not suitable for repeater channel
- Jitter transfer in the whole channel and need simulation to estimate
- Parameter setting and combination for the whole channel become more complicated. Simulation is a good assistance to select parameter



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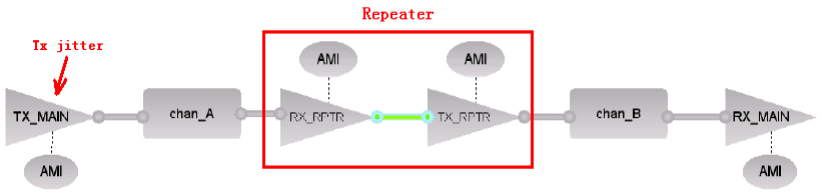
Repeater topology

- There's four IBIS-AMI model in the whole channel
- Model repeater by adding intermediate Rx and Tx models between channels "A" and "B"
- Need EDA tools to support cascaded "N" channels simulation together



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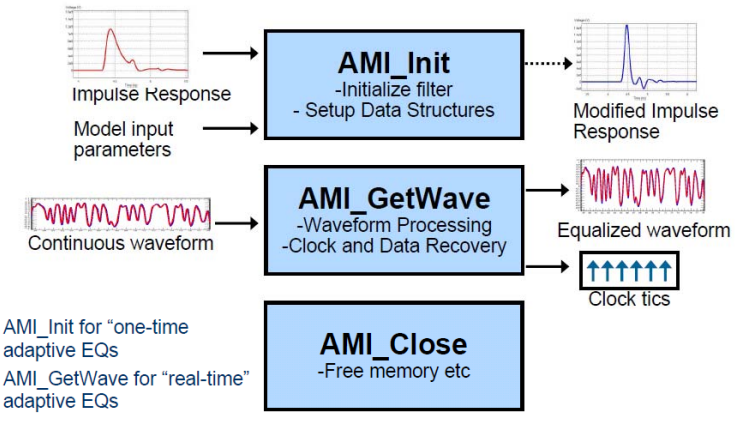
IBIS-AMI data flow and APIs



- AMI_Init for "one-time adaptive EQs
- AMI_GetWave for "real-time" adaptive EQs

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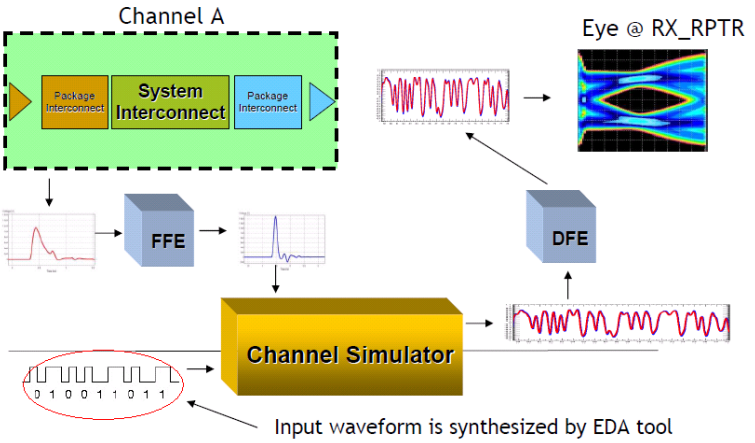
Channel "A" simulation



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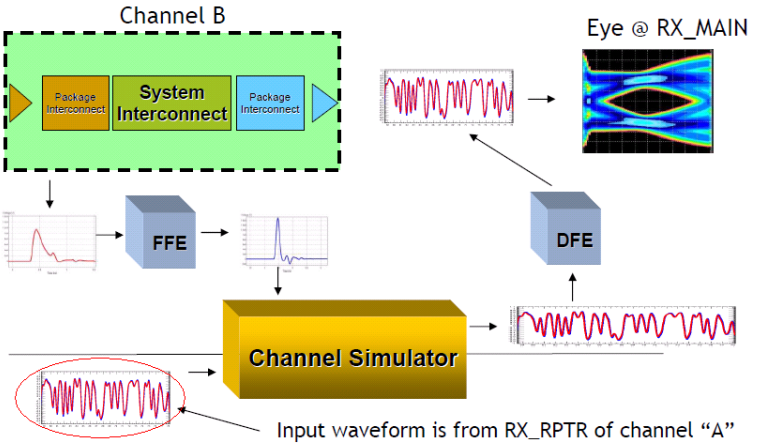
Channel "B" simulation



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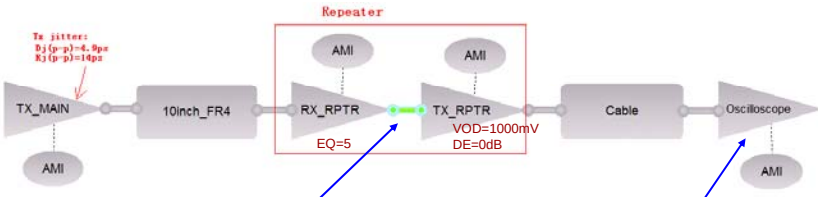
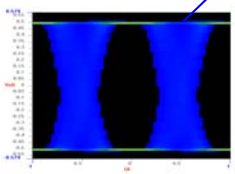
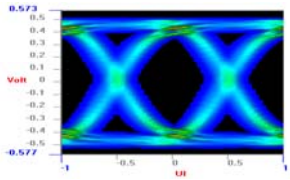
Test and simulation correlation

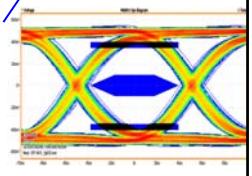




Eye diagram after EQ and limiter



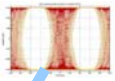
Tj=0.31UI
Height=696mV

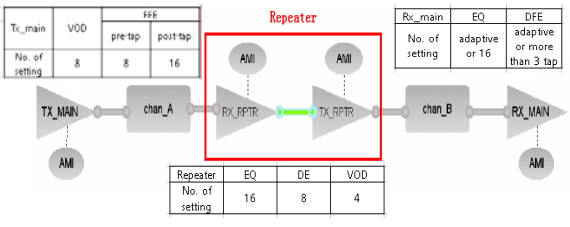


Tj=0.33UI
Height=719mV

How to select repeater parameter

- **Sweeping all parameter in simulation is still a time-consuming work for large number of combinations**
- **Methods need to simplify the combinations**
- **Retimer can be treated as an independent receiver**
- **Repeater: limiting mode vs. non-limiting mode**
- Limiting mode cut the relationship between channel “A” and “B” just compensating for the loss of channel “A”
- Non-limiting mode still connect “A” and “B” , so setting depends on the whole channel loss budget

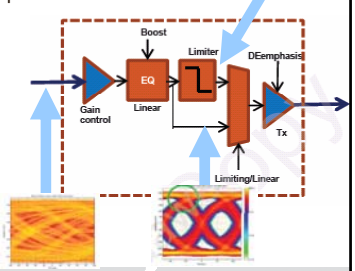




Tx_main	VOD	FFE	
		pre-tap	post-tap
No. of setting	8	8	16

Rx_main	EQ	DFE
No. of setting	adaptive or 16	adaptive or more than 3 tap

Repeater	EQ	DE	VOD
No. of setting	16	8	4



Summary

- Repeater is a good solution for 10G over-spec. application
- Standard IBIS-AMI models can be used for modeling repeaters. No additional change in IBIS-AMI expression
- The IBIS-AMI models must contain all repeater functionally like EQ, linear/limiting, DE, VOD, DFE, CDR and so on. Accurate IBIS-AMI models are important for analysis results
- EDA tools can handle the cascading of multiple channels during simulation
- Knowledge about repeater help select parameters more efficiently. Simulation is a good assistance

Thank you!

AMI Applications in High-speed Serial Channel Analysis and Measurement Correlation

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High-Speed System Lab，ZTE Corporation

Bringing you closer

Asian IBIS Summit

Shanghai, China
November 15, 2011

Agenda

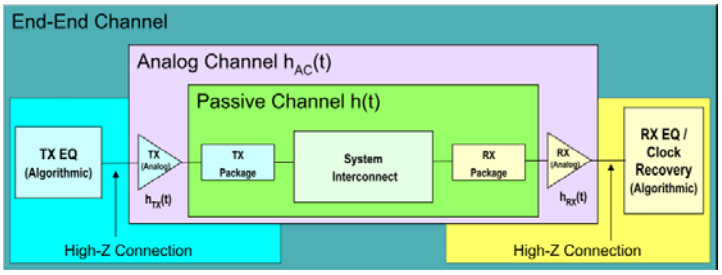
- IBIS-AMI Model versus Transistor-Level Model
- AMI Applications in High-speed Serial Channel Analysis
- AMI Model Accuracy Verification
- Summary and Suggestions

IBIS-AMI Model versus Transistor-Level Model

- **IBIS-AMI Model**
  - Accuracy simulation and fast run time
  - IP Protection
  - Supported by most EDA tools
  - AMI model to provide adaptive DFE, CDR, jitter and other simulation
- **Transistor-Level Model**
  - Good accuracy
  - models are derived from transistor-level netlist and layout
  - Relatively long simulation time and sometimes convergence problems
  - Intellectual property protection concerns

IBIS-AMI Model

- Combination of analog & algorithmic elements
- Analog part can be condidered linear and time-invariant
- Equalization and CDR can be modeled at the algorithmic part



Picture reference from"IBIS-AMI Terminology Overview"at DAC 2009 IBIS Summit

Agenda

- IBIS-AMI Model versus Transistor-Level Model
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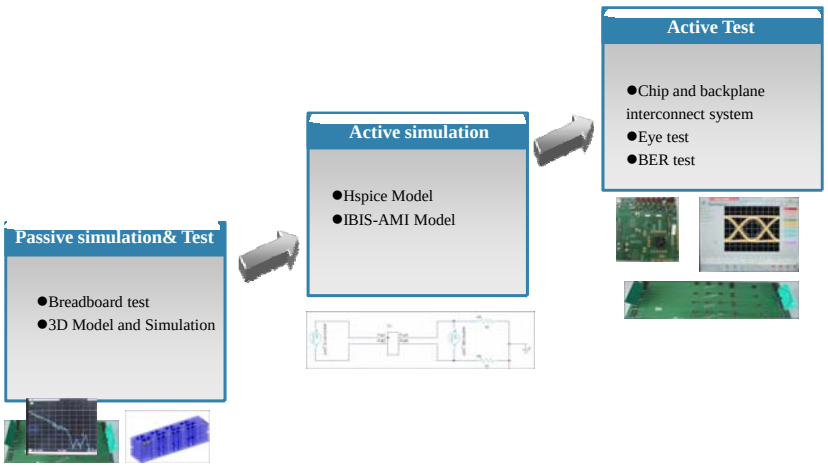
AMI Applications in High-speed Serial Channel Analysis

Methods in10Gbps serial channel analysis



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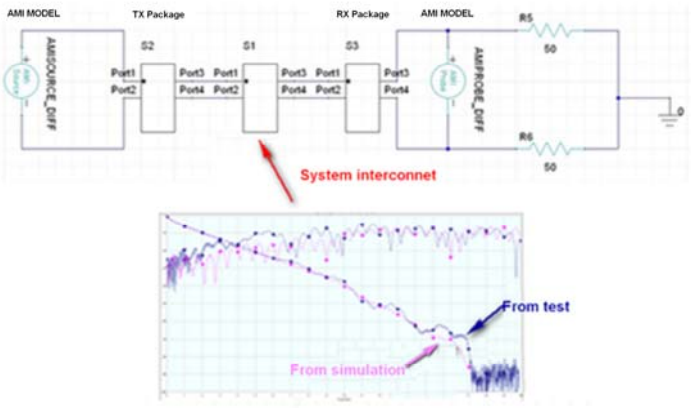
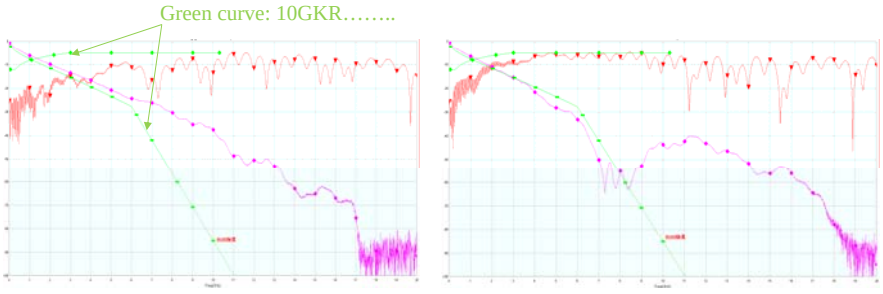
AMI Applications in High-speed Serial Channel Analysis



IBIS-AMI Model Validation Setup

AMI Applications in High-speed Serial Channel Analysis

- IBIS-AMI models for performance evaluation of two different channel

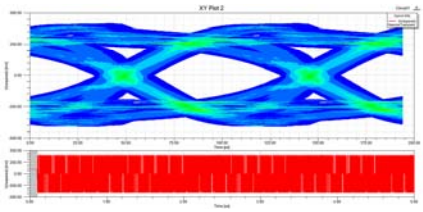


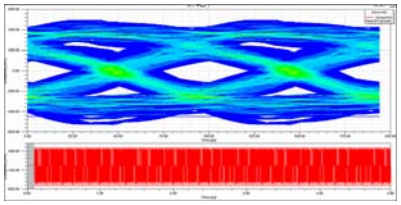
Channel 1：
Backplane traces 40inch 、 Two connectors ， Two test fixture、test cable. Backplane side over the hole stubs 37mil.

Channel 2：
Backplane traces 40inch 、 Two connectors ， Two test fixture、test cable. Backplane side over the hole stubs 150mil.

AMI Applications in High-speed Serial Channel Analysis

- Channel 1 and Channel 2 Simulation results compare(PRBS31) :





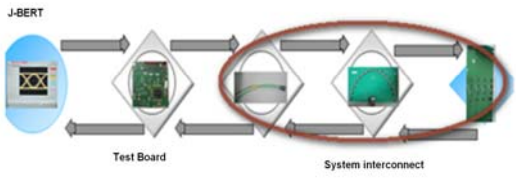
Eye Height	239.11mv
Jitter (pp)	32.40ps
Rise time	45.84ps

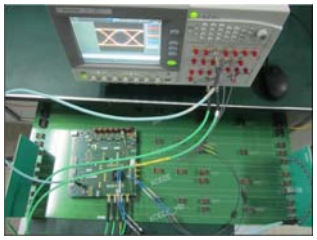
Eye Height	53.61mv
Jitter (pp)	51.98ps
Rise time	58.42ps

AMI Applications in High-speed Serial Channel Analysis

BER Test

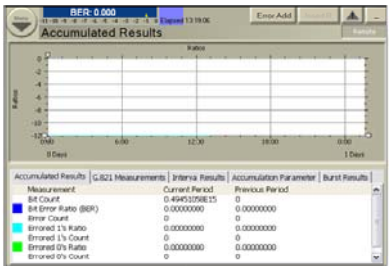
- Use BERT and chip test board for channels 1 and 2 bit error rate test.
- BERT Generates the source signal and also receives the loopback signal for ber test.



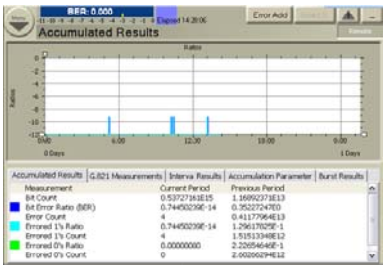


AMI Applications in High-speed Serial Channel Analysis

BER test results



More than 12 hours of the bit error rate test, there was no error.



More than 12 hours of the bit error rate test, the emergence of four errors.

Agenda

- IBIS-AMI Model versus Transistor-Level Model
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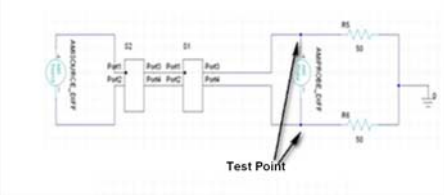
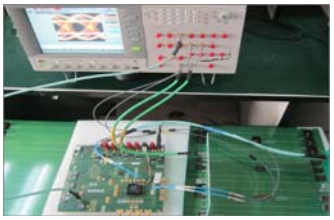
AMI model accuracy verification

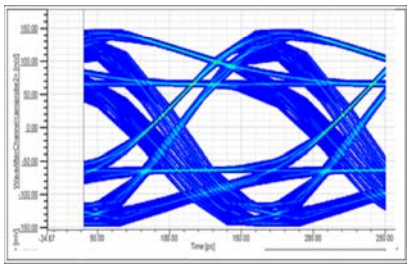
- Simulation channel： Transmitter package parameters 、 Backplane traces 10inch 、 Two connectors 、 Two test fixture、 Connection cable.
- The chip emits a signal after transmission through backplanes direct access to the BERT test in the eye .
- Simulation and test using the same pattern PRBS15 ， Rate 8Gbps ， The same pre-emphasis settings (10dB).

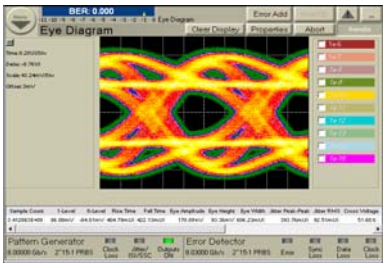




AMI model accuracy verification

- Simulation results compared with test results——Output 600mv





	Simulation	Test
EyeAmplitude	196.17mv	170.09mv
jitter (pp)	46.00ps	49.22ps
EyeRiseTime	61.7ps	50.60ps

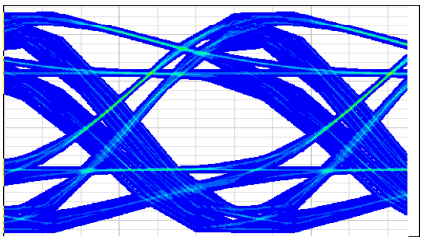
Conclusions ：

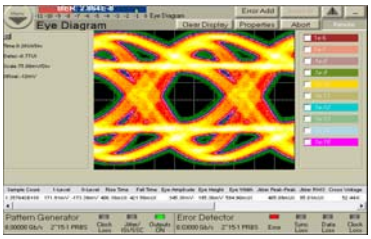
1、 Good Correlation in total eye.

2、 A little defference in rise edge .

AMI model accuracy verification

- Simulation results compared with test results——Output 1200mv





	Simulation	Test
EyeAmplitude	392.34mv	345.30mv
jitter (pp)	46.00ps	50.64ps
EyeRiseTime	61.54	50.77ps

Conclusions ：
Same as output 600mv .

Agenda

- IBIS-AMI Model versus Transistor-Level Model
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Summary

- Serial channel analysis using the AMI model simulation can provide good guidance for the design.
- AMI model can be applied to more signal integrity assessment such as crosstalk, jitter, high-speed connector performance analysis.
- The work of AMI model simulation Verification need to be improved, We hope to get more and better ways.

Suggestions

IBIS-AMI model can greatly improve the efficiency of high-speed serial signal simulation ,howeverwe still have encountered the following problems:

- AMI model is currently not uniform and IC vendors supply various models, so it is difficult for users to run them with right EDA tools.
- Some EDA tools supported AMI models are not perfect in function. For example the setting is not convenient to use , TX&RX AMI models can not be simulated alone etc.
- Some AMI models can not support adaptive DFE fuction perfectly. Users need to manually set the value or adaptive DFE operating results are not correct.


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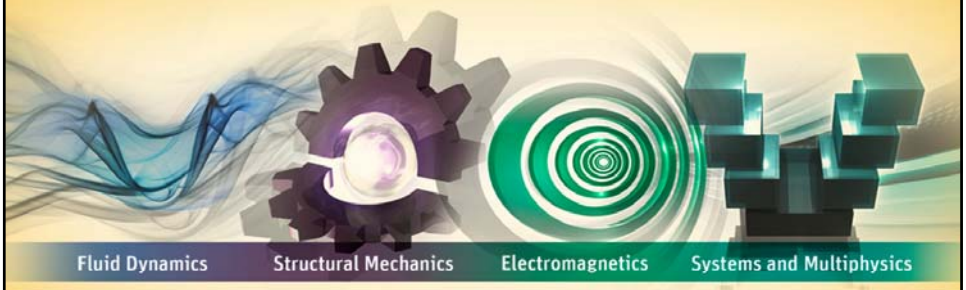
Pseudo transient eye analysis by convolution method



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IBIS Asia Summit 2011. Nov.15th 2011 , Shanghai, China

ANSYS

Background

- **In IBIS Asia summit 2008, we have first introduced statistical analysis method for GHz analysis**

http://www.eda.org/ibis/summits/nov08a/li.pdf

- **Statistical analysis used convolution method for fast SSE (Solution Space Explorer), but it has limits**
  - **Suitable for LTI system**
  - **Not as accurate as SPICE transient eye**
- **Today, we'll discuss the convolution method for Non-LTI system and introduce pseudo transient eye analysis by convolution method**

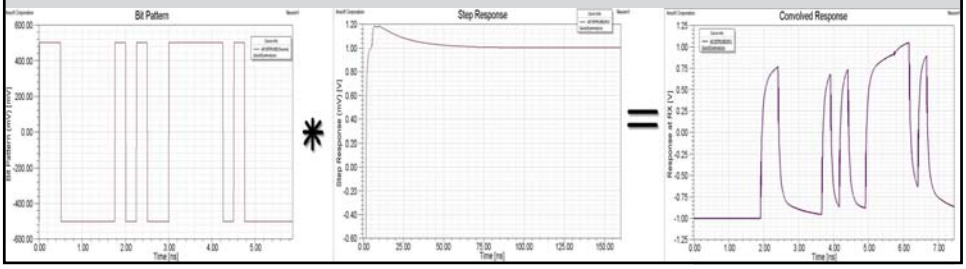
Convolution and LTI system

$X_1(t) \Rightarrow Y_1(t)$
$X_2(t) \Rightarrow Y_2(t)$ Input yields output

$X_1(t) + X_2(t) \Rightarrow Y_1(t) + Y_2(t)$ Additive property

$aX_1(t) \Rightarrow aY_1(t)$ Homogeneity property

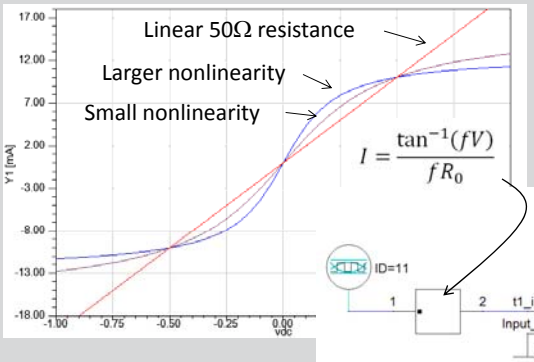
$X_1(t-\tau) \Rightarrow Y_1(t-\tau)$ Time invariant property



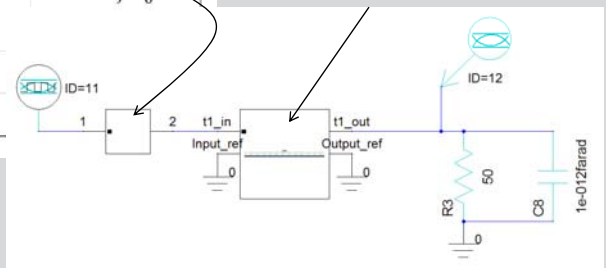
How About Non-linear System?

Simple channel with driver that has a nonlinear self impedance:

- **3 curves tested for driver impedance**



10 inch microstrip trace



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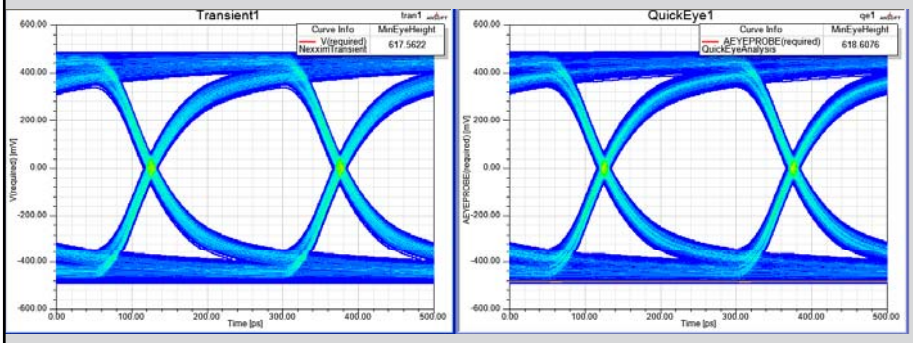
Transient vs. Convolution for Linear network

Transient Eye Height = 618 mV

Convolution Eye Height = 619 mV



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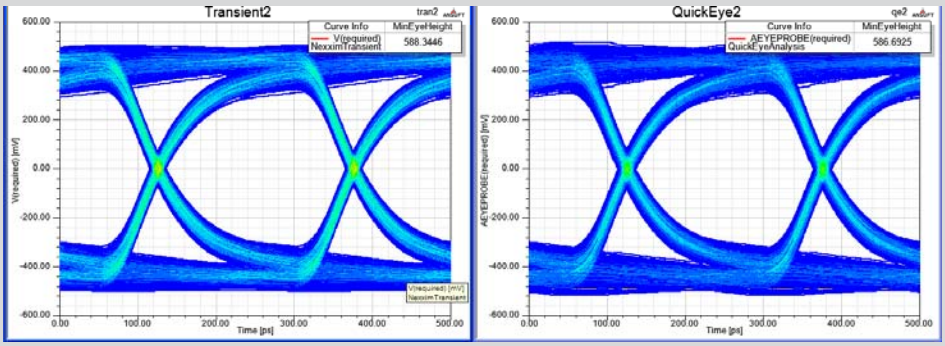
Transient vs. Convolution for Small Nonlinearity

Transient Eye Height = 588 mV

Convolution eye Height = 587 mV



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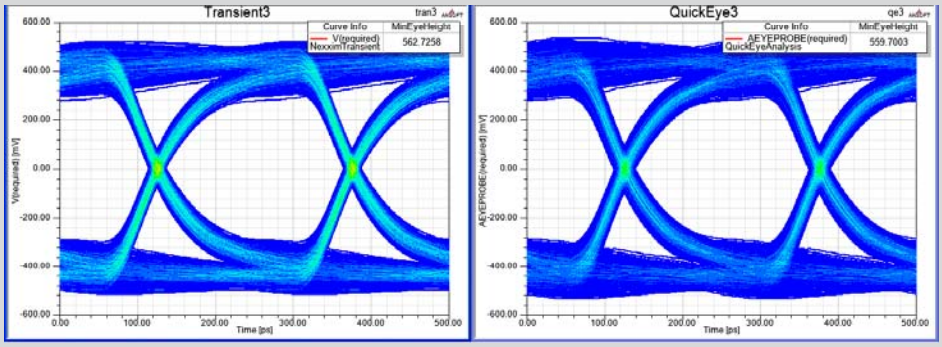
Transient vs. Convolution for Larger Nonlinearity

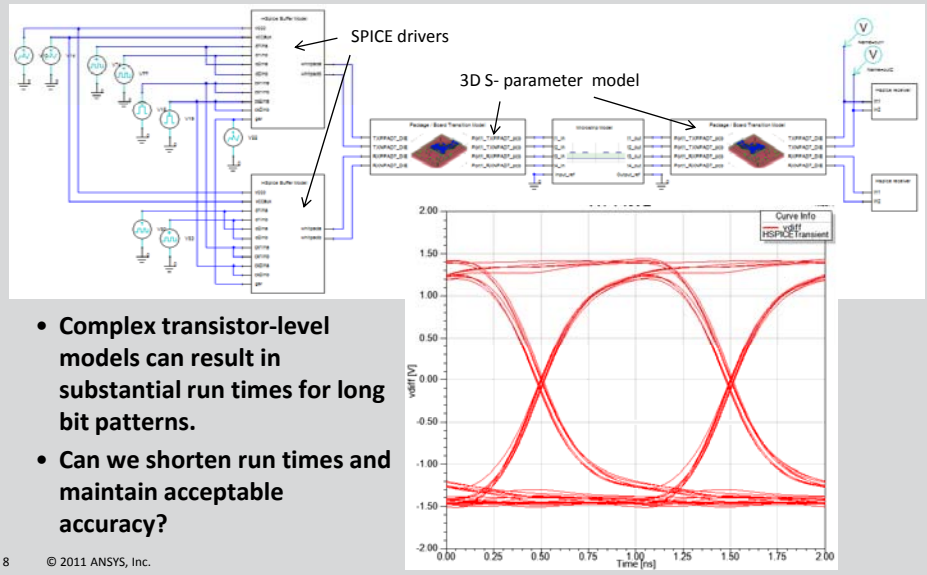
Transient Eye Height = 563 mV

Convolution Height = 560 mV



- **Test cases show that even Convolution make an assumption of linearity, accuracy is often excellent for moderately nonlinear drivers**

Typical GHz Transient simulation

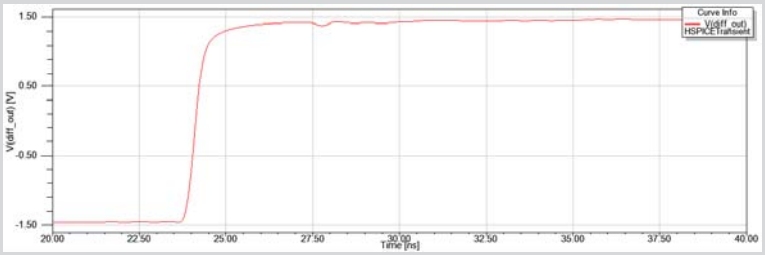


- **Complex transistor-level models can result in substantial run times for long bit patterns.**
- **Can we shorten run times and maintain acceptable accuracy?**

Pseudo transient eye analysis

Pseudo transient like IBIS' V-T curve:

- Run transient simulations using SPICE to capture the step response of the channel, Store step responses in text files
- Separate rising and falling responses can be specified
- Run convolution using these external step responses
- Theory is based on LTI assumption



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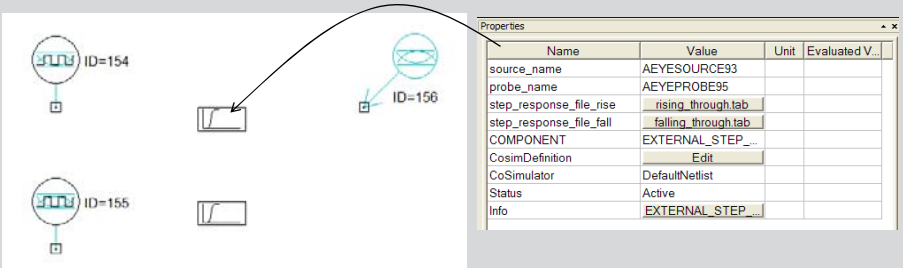
Pseudo transient eye analysis(cont.)

Pseudo transient eye results will closely match transient if buffers are approximately linear



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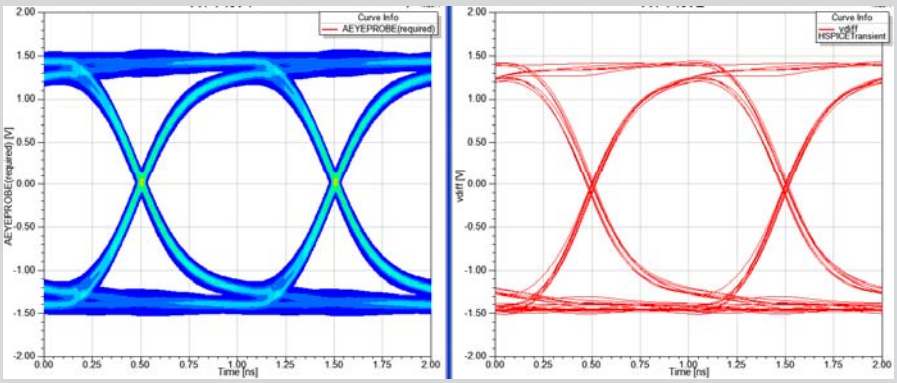
Pseudo transient eye vs. SPICE transient eye

Pseudo transient and SPICE transient

- After capturing 100ns transient step response for rising, falling, and crosstalk edges, 100,000 bits run in seconds by convolution
- Results consistent with SPICE transient



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Conclusion

- Even Statistical eye analysis by using convolution method is assumption LTI system, sometimes it also can be used for Non-Linear system, but the simulator must be tested
- SPICE transient step response can also be used in Statistical analysis for Pseudo transient
- Chip vendor maybe supply typical channel's step response for end user evaluation. EDA vendor also can give the comparison of pseudo transient and SPICE transient for user reference.

12

Introduction of FEC IL Gain Estimation Method In High Speed Link

Dong Xiaoqing, Huang Chunxing

Asian IBIS Summit
Shanghai, China
November 15, 2011

HUAWEI

Abbreviations

Abbreviation	Explanation
FEC	Forward Error Correction
DFE	Decision Feedback Equalizer
IL	Insertion Loss
BER	Bit Error Rate
SNR	Signal to Noise Ratio
KR	Short for 10GBASE-KR standard

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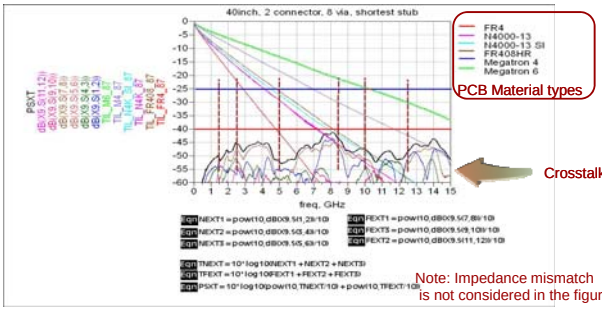
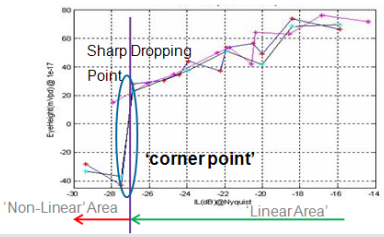
Backgrounds – Loss Dominated Link Performance

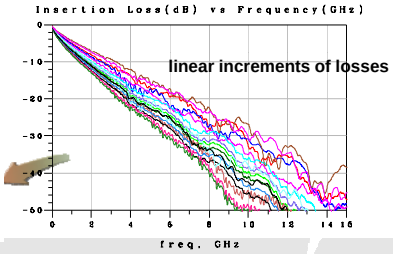
- **Insertion Loss is the top 1 design factor which dominates the performance and cost of a 10Gbps+ high-speed long reach system.**
  - The length of 25Gbps high-speed link may achieve 40inch, regardless of OIF CEI-25G recommendation of 27" length. Even with the Megtron6 material now available, it is not possible to meet the 25dB insertion loss requirement of OIF CEI-25G standard for link length above 27inch.
  - Even for 10Gbps data rate, using lower cost PCB material requires that high-speed system tolerates much more insertion loss by seeking for additional IL gain.



Backgrounds – Basic Viewpoints on FEC

- **FEC is normally used to solve the link reliability issues. Within the SerDes driving capability, Designing proper FEC can improve link SNR and BER performance.**
- **FEC does improve SNR and can also tolerate additional channel losses. It is believed that strong FEC can help meet the 1m objective length requirement of 25Gbps channels.**
- **But, it does depend on:**
  - From both simulation and lab measurement, the BER performance of SerDes degrades sharply at the 'corner point' of channels, even with the insertion loss changes with approximate linear increments.
  - FEC can extend the SerDes driving capability by several dB, but it is fact that using ordinary FEC is hard to improve the driving capability from the 'corner frequency' by another several dB.

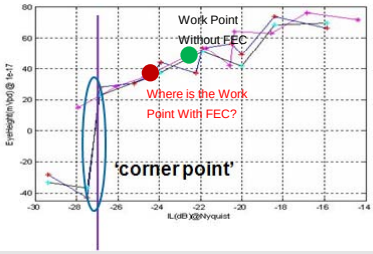




Backgrounds – Needs for FEC Capability Estimation

- **FEC is more and more often used in 10Gbps+ links:**
  a) For the driving distance's sake: to extend the driving distance of SerDes in long reach channels is often required to meet the system design target. FEC is a useful 'soft' way to extend chip driving distances.
  b) For the reliability's sake: Noises and burst errors happen almost all the time in high-speed link systems, FEC can help in certain degree to reduce errors that induced by these factors, to enhance the link immunity to noises, and thus to enhance the reliability of links.

- **In high speed link specification evaluating phase, detailed FEC performance measurement is not feasible, and valid method to roughly estimate the FEC driving capability is in immediate need.**



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Issues: Additional IL Gain Equation

- **Traditionally, theoretical relationship between FEC coding gain and the additional driving insertion loss due to FEC is:**

  *additional IL gain = 2*FEC_Coding_Gain, where the IL gain factor is 2*

  Examples: 6dB FEC coding gain means KR insertion loss limit can be extended to 23+6*2=35dB

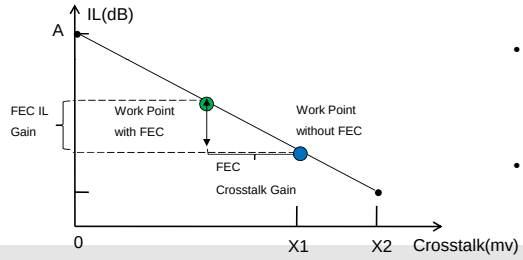
- **From Huawei internal experimental results, the additional IL gain is about 1 with regards to the coding gain, not 2 listed above. According to the testing capability of KR FEC, the additional IL gain is about 2dB, as we all know that KR FEC coding gain is 2~3dB, it is believed that the reasonable value of IL gain factor due to coding gain for this case is about 1.**

  additional IL gain = FEC_Coding_Gain

- **Note that if SerDes is working in the area that is beyond the corner point, 'non-linear' area does affect the additional IL gain, so this equation is invalid in estimating SerDes driving capability under this circumstances.**

Modified Method of Estimating FEC IL Gain

- **There's certain linearity relationship between the maximum tolerable crosstalk and maximum tolerable insertion loss of a high speed link, insertion loss and crosstalk restrict each other, when one gets to certain value, the other will not exceed certain 'mask'.**
- **FEC can enhance link SNR through solving the BER problem induced by crosstalk, so, assuming signal is kept unchanged, the SNR enhancement of FEC is equivalent to the improvement of crosstalk induced BER. Then the work point with FEC could be found by the point of reduced crosstalk.**
- **In the following figure, the horizontal axis represents link crosstalk, the vertical axis represents the link insertion loss. The slope gives the variation of insertion loss gain with regards to the crosstalk variation.**



- Assuming FEC coding Gain is X dB, and Y is crosstalk gain factor $Y = 10^{-\frac{X}{20}}$
- The slope of the line is K, then additional FEC IL gain is $ILGain = K * Y * X1$

Example of Additional FEC IL Estimation

- **We use this modified method to estimate additional IL gain value. We may get the idea that the IL gain from KR FEC is about 1dB~2dB. However, the theoretical equation tells that 4dB IL gain would come from KR FEC.**
- **From measurement, we got the additional 1~2dB IL gain from KR FEC.**

Link name	Crosstalk (mV)	Slope (dB/mV)	KR FEC Gain (dB)	Theoretical Equation (dB)	Additional IL Gain (dB)
Connector 1	28	0.29	2	4	1.67
Connector 2	24	0.30	2	4	1.48
Connector 3	23	0.26	2	4	1.23

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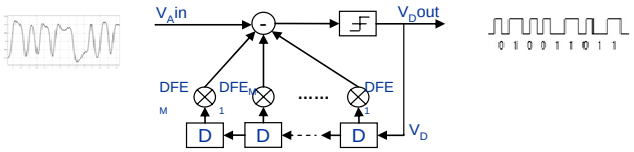
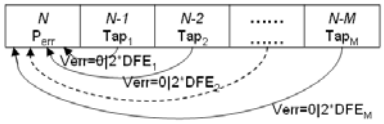
Error Propagation Mechanism

- **High speed serial links have a mixed error mechanism of random errors and burst errors.**
- **DFE can introduce burst errors due to the feedback mechanism:**



$$V_D out(t_0) = V_A in(t_0) - DFE_1 \cdot V_D(t_{-1}) - DFE_2 \cdot V_D(t_{-2}) - ... - DFE_M \cdot V_D(t_{-M})$$

- **Once errors occur, they change the output voltage of the equalized bits that follow, and thus impact the judgments of the bits that follow.**



Error Propagation Equation

- **The previous estimation method is a rough estimation for IL Gain due to FEC. More accurate analysis should use Error Propagation Equation to analyze link BER.**
- **The BER performance of Error Propagation of DFE:**

$$BER = \sum_{i=1}^{rll_{max}} \sum_{allE} p(rll = i, E) \cdot W(E) \cdot p_1 \cdot (1 - p_1)^{n - rll_{max} - i}$$

- p_1: random error probability
- $W(E)$: the probability that i bits in error among a n bit block
- E: all the combinations of the error pattern when error propagation length is i
- rll_{max}: maximum error propagation length

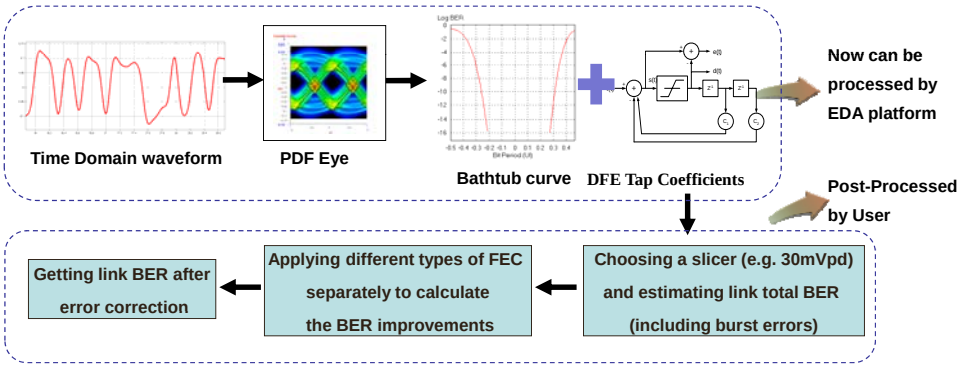
- **The Total BER with error propagation is:**

$$BER_{total} = \frac{1}{N} \sum_{allP} \sum_{i=0}^{H} P_{pkt}(i+1 \mid i)$$

- P_{pkt}: a function of the vector Err_DFE
- $P_{pkt}(i+1 \mid i)$: The $(i+1)th$ burst error rate in a packet under the condition that the ith burst error occurs in the same packet
- When i equals to 0, P_{pkt} is simply the probability vector of the 1st burst error in the packet.

Error Propagation Equation Analysis Method

- **The total Error Propagation Analysis flow:**

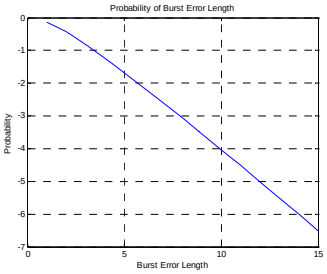


- **The whole process of estimating FEC capability can be divided into two stages, the first stage can be processed in current EDA platforms, but the second stage is now processed by the users.**

Example of the Error Propagation Equation Analysis Method

- **We use Error Propagation Equation method to estimate BER gain and additional IL gain value. We may get the idea of that the IL gain from current FEC in use is about 1.9dB.**
- **The data correlates well with the 1~2dB measurement results.**

Demo: Probabilities of 1~15 Burst Error Lengths



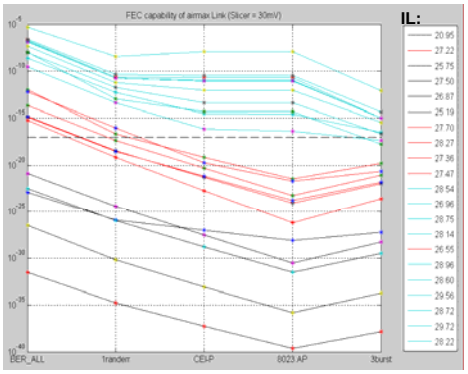


Table of Contents

Summary

- **As introduced previously, FEC will play more and more important role in 10Gbps+ high-speed serial links.**
- **A rough IL gain estimation method is summarized and the Error propagation Equation Analysis method is introduced here, and it has been verified to be an very efficient way in system link specification analysis phase for estimating FEC capabilities in terms of additional IL gain.**
- **Current EDA tools can process time domain and statistical analysis very well, but the lack of DFE coefficients outputting function and lack of voltage bathtub sometimes makes FEC analysis inconvenient.**
- **FEC gain analysis method is recommended to be supported by EDA tools(IBIS specification), including error propagation analysis function.**

Thank you

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Supporting External circuit as Spice or S-parameters in conjunction with I-V/V-T tables

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Asian IBIS Summit
Shanghai, China
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Agenda

- **Requirement**
- **Current Limitations of [External Circuit]**
- **Solution**
  - **Supporting S-parameters in [External Circuit] (BIRD144)**
  - **Simulating [External Circuit] in conjunction with I-V/V-T tables (BIRD145)**
- **Summary**

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Agenda

- **Requirement**
- Current Limitations of [External Circuit]
- Solution
  - Supporting S-parameters in [External Circuit]
  - Simulating [External Circuit] in conjunction with I-V/V-T tables
- Summary

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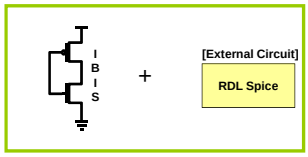
Requirement

- **At high frequencies, we need ways over and above I-V, V-T tables and AMI to model the buffer.**
  - On DIE Terminations (ODT) that vary with frequencies need to be expressed as S-parameters or RLGC Spice files
  - On DIE Re-distribution layer (RDL) parasitics become significant and vary with frequencies and hence have to be expressed as S-parameters
  - Analog portion of IO-buffer get expressed as Spice as against I-V/V-T curve; S-parameters get used to describe transfer characteristics of linear IO-buffer amplifiers.

Requirement

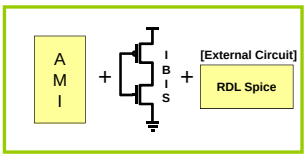
- **At high frequencies, we need ways over and above I-V, V-T tables and AMI to model the buffer.**
  - Some algorithmic portion of IO-buffer model could be expressed as behavioral Spice to augment AMI code
    - Example: 'if-then-else kind of spice' to pick right sub-circuit based on parameter values/processes
    - Example: Modeling continuous filters as behavioral spice to augment digital filters in AMI code

Requirement
- Various Cases that need to be covered



Simulating RDL parasitics in conjunction with I-V/V-T tables

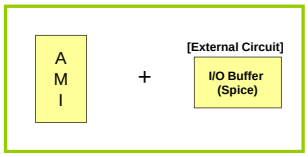
Case 1



Simulating RDL parasitics in conjunction with I-V/V-T tables and AMI

Case 2

Simulating AMI with IO-buffer expressed as Spice



Case 3

Agenda

- Requirement
- **Current Limitations of [External Circuit]**
- Solution
  - Supporting S-parameters in [External Circuit]
  - Simulating [External Circuit] in conjunction with I-V/V-T tables
- Summary

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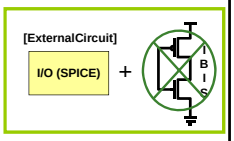
Current Limitations - [External Circuit]

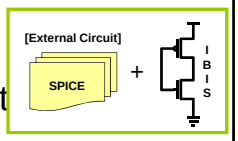
- Today, S-parameters have to be wrapped into Spice models (vendor specific) and then used under [External Model/Circuit] Keyword.
  - On similar lines, BIRDs 116-118 propose that Touchstone file name can be parameterized for the IBIS-ISS sub-circuit, which means that IBIS-ISS wrapper could be written for the S-parameter element.
- **NEED**: Extend support for direct usage of S-parameters

Current Limitations - [External Circuit]

- The current [External Circuit] and [Circuit Call] usage rules do not allow the direct interconnection and instantiation of existing IBIS I/O models with the rest of the [External Circuit] blocks. Traditionally, users either use Spice or I-V/V-T tables.



- **NEED**: Extend use of [External Circuit] keyword to point to Spice sub-circuits that augment I-V/V-T data for complete characterization of IO-buffer.



Current Limitations - [External Circuit]

- In order for a model developer to use an IBIS I/O model in an [External Circuit] the following steps need to be followed:
  - Develop SPICE like wrappers in which the corresponding typ, min, and max IBIS I/O sub-circuits are instantiated
  - Develop an [External Circuit] to point to the wrapper sub-circuits
  - Use the [Circuit Call] keyword to call the [External Circuit].
- These usage rules are cumbersome especially when the developer can just directly call the desired IBIS I/O model without the need to develop a SPICE like wrapper as well as an [External Circuit] section.

Agenda

- Requirement
- Current Limitations of [External Circuit]
- **Solution**
  - **Supporting S-parameters in [External Circuit] (BIRD144)**
  - Simulating [External Circuit] in conjunction with I-V/V-T tables
- Summary

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Solution: Leveraging [External Model/Circuit] to Support Package S-parameters

- For support of package S-parameters:
  - IBIS model should have Keywords to support Touchstone S-parameters under Package section, with fields to
    - Point to Touchstone file from the Package section
    - Provide port-mapping of IO-buffer pins to S-parameter ports
    - R/L/C values should be ignored by SI tools if S-parameter file is used
- For support of S-parameters when representing elements beyond package parasitics: This can be achieved through use of [External Model] keyword that directly instantiates Touchstone file

Solution: Leveraging [External Model/Circuit] to Support S-parameters (beyond Package)

- Positioning S-parameters as a method to completely define IO-buffer model or portions of IO-buffer requires support for:
  - Direct support of S-parameters without the need for wrapping
  - Port mapping of S-parameters
  - Corners beyond typ/min/max to provide flexibility of choosing various S-parameter files under different conditions

Solution: Leveraging [External Model/Circuit] to Support S-parameters (beyond Package)

- Support for Language 'Touchstone' with port-map

```
|-----------------------------------------------------------------
| Example of True Differential [External Model] using TOUCHSTONE:
|-----------------------------------------------------------------
|
[Model] Ext_TOUCHSTONE,_Diff_Buff
Model_type I/O_diff
Rref_diff = 100
|
| other model subparameters are optional
|
                  typ      min      max
[Voltage Range]   3.3      3.0      3.6
|
[Ramp]
dV/dt_r         1.57/0.36n   1.44/0.57n   1.73/0.28n
dV/dt_f         1.57/0.35n   1.46/0.44n   1.68/0.28n
|
[External Model]
Language TOUCHSTONE
|
| Corner corner_name file_name    circuit_name (.subckt name)
Corner    Typ          diff1o.s8p   NA
Corner    Min          diff1o.s8p   NA
Corner    Max          diff1o.s8p   NA
|
| Ports List of port names (in same order as in TOUCHSTONE)
Ports A_signal_pos A_signal_neg my_receive my_drive my_enable
Ports A_puref A_pdref A_pcref A_gcref A_extref my_ref A_gnd
|
| D_to_A d_port    port1       port2     vlow vhigh trise tfall corner_name
D_to_A    D_drive  my_drive    my_ref     0.0  3.3   0.5n  0.3n  Typ
D_to_A    D_drive  my_drive    my_ref     0.0  3.0   0.6n  0.3n  Min
D_to_A    D_drive  my_drive    my_ref     0.0  3.6   0.4n  0.3n  Max
D_to_A    D_enable my_enable   my_ref     0.0  3.3   0.5n  0.3n  Typ
D_to_A    D_enable my_enable   my_ref     0.0  3.0   0.6n  0.3n  Min
D_to_A    D_enable my_enable   my_ref     0.0  3.6   0.4n  0.3n  Max
|
| A_to_D d_port     port1        port2          vlow   vhigh corner_name
A_to_D    D_receive  A_signal_pos  A_signal_neg  -200m  200m  Typ
A_to_D    D_receive  A_signal_pos  A_signal_neg  -200m  200m  Min
A_to_D    D_receive  A_signal_pos  A_signal_neg  -200m  200m  Max
|
[End External Model]
```

Solution: Leveraging [External Model/Circuit] to Support S-parameters (beyond Package)

- Picking different S-parameter files for different corners

```
|-------------------------------------------------------------
| Example of True Differential [External Model] using TOUCHSTONE:
|-------------------------------------------------------------
|
[Model] Ext_TOUCHSTONE,_Diff_Buff
Model_type I/O_diff
Rref_diff = 100
|
| other model subparameters are optional
|
                typ      min      max
[Voltage Range]   3.3      3.0      3.6

[Ramp]
dV/dt_r         1.57/0.36n   1.44/0.57n   1.73/0.28n
dV/dt_f         1.57/0.35n   1.46/0.44n   1.68/0.28n
|
[External Model]
Language TOUCHSTONE
|
| Corner corner_name file_name    circuit_name (.subckt name)
Corner     Typ          diff1o.s8p   NA
Corner     Min          diff1o.s8p   NA
Corner     Max          diff1o.s8p   NA
|
| Ports List of port names (in same order as in TOUCHSTONE)
Ports A_signal_pos A_signal_neg my_receive my_drive my_enable
Ports A_puref A_pdref A_pcref A_gcref A_extref my_ref A_gnd
|
| D_to_A d_port    port1       port2     vlow vhigh trise tfall corner_name
D_to_A     D_drive  my_drive    my_ref     0.0  3.3    0.5n  0.3n  Typ
D_to_A     D_drive  my_drive    my_ref     0.0  3.0    0.6n  0.3n  Min
D_to_A     D_drive  my_drive    my_ref     0.0  3.6    0.4n  0.3n  Max
D_to_A     D_enable my_enable   my_ref     0.0  3.3    0.5n  0.3n  Typ
D_to_A     D_enable my_enable   my_ref     0.0  3.0    0.6n  0.3n  Min
D_to_A     D_enable my_enable   my_ref     0.0  3.6    0.4n  0.3n  Max
|
| A_to_D d_port      port1          port2          vlow   vhigh corner_name
A_to_D     D_receive  A_signal_pos   A_signal_neg  -200m  200m  Typ
A_to_D     D_receive  A_signal_pos   A_signal_neg  -200m  200m  Min
A_to_D     D_receive  A_signal_pos   A_signal_neg  -200m  200m  Max
|
[End External Model]
```

Solution: Leveraging [External Model/Circuit] to Support S-parameters (beyond Package)

- Supporting user-defined corners – each user-defined corner maps to typ/min/max IBIS corners

```
|-------------------------------------------------------------
| Example [External Model] using TOUCHSTONE with 2 userdef corners:
|-------------------------------------------------------------
|
[Model] ExLinearBufferTouchstoneWithTwoUserDefCorners
Model_type Output
|
| Other model subparameters are optional
|
                typ      min      max
[Voltage Range]   3.3      3.0      3.6
|
[Ramp]
dV/dt_r         1.57/0.36n   1.44/0.57n   1.73/0.28n
dV/dt_f         1.57/0.35n   1.46/0.44n   1.68/0.28n
|
[External Model]
Language TOUCHSTONE
|
| Corner corner_name file_name         circuit_name
Corner     Typ          buffer_typ.s2p   NA
Corner     Min          buffer_min.s2p   NA
Corner     Max          buffer_max.s2p   NA
|
| Parameters List of parameters
Parameters MinNumber MaxNumber
|
| User_defined_corner user_defined_corner_name parameter_name parameter_value file_name corner_name
User_defined_corner     Min1     MinNumber    1     buffer_min1.s2p  Min
User_defined_corner     Max1     MaxNumber    1     buffer_max1.s2p  Max
|
```

Solution: Leveraging [External Model/Circuit] to Support S-parameters (beyond Package)

- Use in [External Model] and [External Circuit]

```
|-------------------------------------------
| Example [External Model] using TOUCHSTONE:
|-------------------------------------------
|
[Model] ExBufferTOUCHSTONE
Model_type I/O
Vinh = 2.0
Vinl = 0.8
|
| Other model subparameters are optional
|
                  typ     min     max
[Voltage Range]   3.3     3.0     3.6
|
[Ramp]
dV/dt_r         1.57/0.36n   1.44/0.57n   1.73/0.28n
dV/dt_f         1.57/0.35n   1.46/0.44n   1.68/0.28n
|
[External Model]
Language TOUCHSTONE
|
| Corner corner_name file_name       circuit_name (.subckt
Corner    Typ          buffer_typ.s7p  NA
Corner    Min          buffer_min.s7p  NA
Corner    Max          buffer_max.s7p  NA
|
| Ports List of port names (in same order as in TOUCHSTONE)
Ports A_signal my_drive my_enable my_receive my_ref
Ports A_puref A_pdref A_pcref A_gcref A_extref
|
| D_to_A d_port   port1     port2    vlow vhigh trise tfall
D_to_A   D_drive  my_drive   my_ref   0.0  3.3  0.5n  0.3n
D_to_A   D_enable my_enable  A_gcref  0.0  3.3  0.5n  0.3n
|
| A_to_D d_port    port1       port2       vlow  vhigh  corner_name
A_to_D   D_receive  my_receive  my_ref  0.8   2.0    Typ
|
| Note: A_signal might also be used instead of a user-defined interface port
| for measurements taken at the die pads
|
[End External Model]|
```

```
|-------------------------------------------
| Example [External Circuit] using TOUCHSTONE:
|-------------------------------------------
|
[External Circuit] BUFF-TOUCHSTONE
Language TOUCHSTONE
|
| Corner corner_name file_name       circuit_name (.subckt name)
Corner    Typ          buffer_typ.s9p  NA
Corner    Min          buffer_min.s9p  NA
Corner    Max          buffer_max.s9p  NA
|
| Ports List of port names (in same order as in TOUCHSTONE)
Ports A_signal int_in int_en int_out A_control
Ports A_puref A_pdref A_pcref A_gcref
|
| D_to_A d_port   port1  port2    vlow vhigh trise tfall corner_name
D_to_A   D_drive  int_in  my_gcref 0.0  3.3   0.5n  0.3n  Typ
D_to_A   D_drive  int_in  my_gcref 0.0  3.0   0.6n  0.3n  Min
D_to_A   D_drive  int_in  my_gcref 0.0  3.6   0.4n  0.3n  Max
D_to_A   D_enable int_en  my_gnd   0.0  3.3   0.5n  0.3n  Typ
D_to_A   D_enable int_en  my_gnd   0.0  3.0   0.6n  0.3n  Min
D_to_A   D_enable int_en  my_gnd   0.0  3.6   0.4n  0.3n  Max
|
| A_to_D d_port     port1    port2     vlow vhigh corner_name
A_to_D   D_receive  int_out  my_gcref  0.8  2.0   Typ
A_to_D   D_receive  int_out  my_gcref  0.8  2.0   Min
A_to_D   D_receive  int_out  my_gcref  0.8  2.0   Max
|
[End External Circuit]
```

Agenda

- Requirement
- Current Limitations of [External Circuit]
- **Solution**
  - Supporting S-parameters in [External Circuit]
  - **Simulating [External Circuit] in conjunction with I-V/V-T tables(BIRD145)**
- Summary

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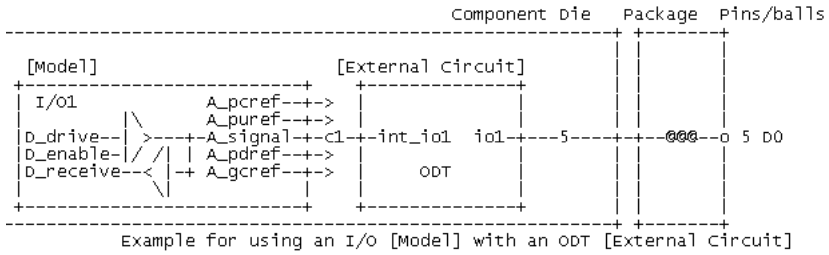
Solution: Include IBIS I/O table model in an [External Circuit] using the new [Model Call]

- Ability to connect External Circuit to IBIS I/O model. The External Circuit could represent RDL parasitics, portion of active I/O buffer, some algorithmic part of I/O buffer.



Example for using an I/O [Model] with an ODT [External Circuit]

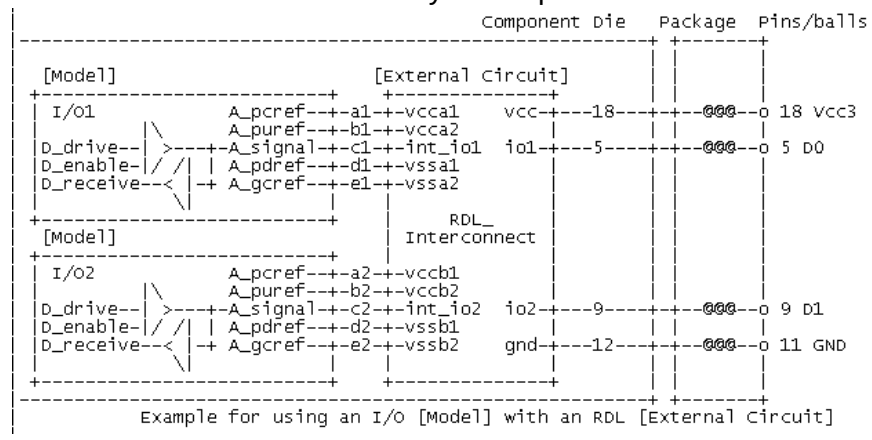
Solution: Include IBIS I/O table model in an [External Circuit] using the new [Model Call]

- [Pin] signal_name model_name R_pin L_pin C_pin
- 1 RAS0# Buffer1 200.0m 5.0nH 2.0pF
- 2 RAS1# Buffer2 209.0m NA 2.5pF
- 3 EN1# Input1 NA 6.3nH NA
- 4 A0 3-state
- **5 D0 I/O1**
- 6 RD# Input2 310.0m 3.0nH 2.0pF
- 7 WR# Input2
- 8 A1 I/O2
- **9 D1 I/O2**
- 10 GND GND 297.0m 6.7nH 3.4pF
- 11 RDY# Input2
- 12 GND GND 270.0m 5.3nH 4.0pF

HERE DO, D1 are to be modeled as I/O1, I/O2 buffers followed by RDL Spice and represent a differential buffer

Solution: Include IBIS I/O table model in an [External Circuit] using the new [Model Call]

- I/O1 and I/O2 are followed by RDL Spice model



Solution: Include IBIS I/O table model in an [External Circuit] using the new [Model Call]

- **[Node Declarations]** **| Must appear before any [Circuit Call] or [Model Call] keyword**
- |
- | Die nodes
- a1 b1 c1 d1 e1 | List of die nodes representing signals that connect models
- a2 b2 c2 d2 e2
- |
- **[End Node Declarations]**
- |
- | NOTE:
- | A [Model] named "I/O1" must be present in the IBIS file in order to enable
- | the tool to instantiate and connect the called model "as usual" based on
- | the I-V and T-V curves as well as the subparameters under the corresponding
- | [Model] section.
- |
- **[Model Call] I/O1** **| Instantiates [Model] named "I/O1"**
- |
- | mapping port pad/node
- |
- Port_map A_pcref a1 | Port to internal node connection
- Port_map A_puref b1 | Port to internal node connection
- Port_map A_signal c1 | Port to internal node connection
- Port_map A_pdref d1 | Port to internal node connection
- Port_map A_gcref e1 | Port to internal node connection
- |
- **[End Model Call]**
- |

Solution: Include IBIS I/O table model in an [External Circuit] using the new [Model Call]

```
| NOTE:
| A [Model] named "I/O2" must be present in the IBIS file in order to enable
| the tool to instantiate and connect the called model "as usual" based on
| the I-V and T-V curves as well as the subparameters under the corresponding
| [Model] section.
|

[Model Call] I/O2              | Instantiates [Model] named "I/O2"
|
| mapping  port         pad/node
|
Port_map   A_pcref       a2       | Port to internal node connection
Port_map   A_puref       b2       | Port to internal node connection
Port_map   A_signal      c2       | Port to internal node connection
Port_map   A_pdref       d2       | Port to internal node connection
Port_map   A_gcref       e2       | Port to internal node connection
|
[End Model Call]
|
```

Solution: Include IBIS I/O table model in an [External Circuit] using the new [Model Call]

```
[Circuit Call] RDL_Interconnect   | Instantiates [External Circuit] named    "RDL_Interconnect"
|
| mapping  port         pad/node
|
Port_map   vcc          18       | Port to implicit pad connection
Port_map   gnd          12       | Port to implicit pad connection
Port_map   io1          5        | Port to implicit pad connection
Port_map   io2          9        | Port to implicit pad connection
Port_map   vcca1        a1       | Port to internal node connection
Port_map   vcca2        b1       | Port to internal node connection
Port_map   int_io1      c1       | Port to internal node connection
Port_map   vssa1        d1       | Port to internal node connection
Port_map   vssa2        e1       | Port to internal node connection
Port_map   vccb1        a2       | Port to internal node connection
Port_map   vccb2        b2       | Port to internal node connection
Port_map   int_io2      c2       | Port to internal node connection
Port_map   vssb1        d2       | Port to internal node connection
Port_map   vssb2        e2       | Port to internal node connection
|
[End Circuit Call]
```

Agenda

- Requirement
- Current Limitations of [External Circuit]
- Solution
  - Supporting S-parameters in [External Circuit]
  - Simulating [External Circuit] in conjunction with I-V/V-T tables
- **Summary**

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Summary

- With increase in frequencies, we need enhanced usage of External Model / Circuit
  - S-parameters are becoming common way to model portions of I/O buffers and package parasitics; Hence need to have direct support of S-parameter model under [External Model/Circuit]. *This has been proposed as BIRD144*
  - Significant portion of I/O buffer gets modeled as Spice/S-parameters to augment the main analog buffer to capture the high frequency behavior; Hence need to have easy way to connect External Circuit to I-V/V-T table-model. *This has been proposed as BIRD145*

Summary

- BIRD144 and BIRD145 can be accessed at
  http://www.eda.org/pub/ibis/birds/
  - The BIRDs would be considered and discussed by the IBIS open forum
  - Other BIRDs will also be considered that might be alternatives or add-on to this proposal

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Board-only Power Deliver Prediction for Voltage regulator and Mother Board Designs

Intel Corporation
Data Center Platform Application Engineering
November 15, 2011

Asian IBIS Summit
Shanghai, China

Jiangqi He
Y.L. Li

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Agenda

- Introduction
- Simplified SPICE Model
- Case Study and Its Application
- Validation
- Summary and Next Steps

Agenda

- ✓ Introduction
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Introduction

Power delivery performance prediction typically is using full wave solvers to extract board, socket, package, and on-chip interconnect. There are many tools and approaches across industries.

However, this typical approach is usually focusing on high frequency noise, involving many piece of software and has certain limitations:

- Very high frequency oriented analysis. Typically looking for many 100s MHz or GHz range
- Extracted full wave S parameters needs macro-modeling for transient analysis
- All full wave solvers has accuracy limitation at low frequency and board analysis needs very accurate low frequency prediction
- Full wave extraction and its associated analysis do not have full explicit information on return path (GND) which is critically important for board design and optimizations.
- Typically full wave approach takes much more time to complete an analysis cycle and also needs electro-magnetics background for many uncertain scenarios during modeling/sims
- Due to its complexity, some OEM/ODM skip prediction step and go directly for testing vehicles
- Therefore, a method that involves less steps, easy to understand, good low frequency accuracy and high efficiency is highly desired!

Introduction (cont'd)

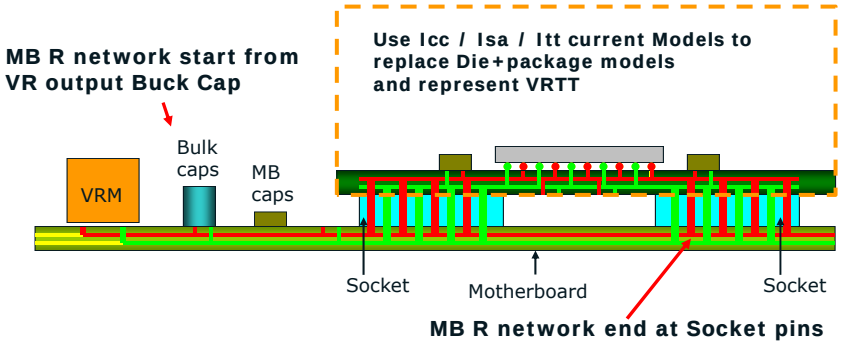
A new methodology is called 'Simplified SPICE Model'. It allows companies to conduct simulations focused on the follows:

- Determine # of MB layers and stack-up
- Choose MB cap types, numbers and locations
- Check the coupling noise due to imperfect common ground
- Validate MB and VR performance in early development stage
- Reduce design cycle time due to faster simulations
- A lot more accurate at low frequency regions.
- Explicitly know exactly return currents
- Least software involvement
- An entry engineer can conduct modeling/simulations

Agenda

- Introduction
- ✓Simplified SPICE Model
- Case Study and Its Application
- Validation
- Summary and Next Steps

A Typical Network for MB Power Delivery Analysis



Conventional PD Models :
Die (on-die caps) + Package(with caps) + socket + MB + MB/Bulk caps + VR

Simplified SPICE Model for OEMs/ODMs:
VRTT (Icc/Isa/Itt) + socket + MB + MB/Bulk Caps + VR

Simplified SPICE Model Workflow

Step 1. Create MB model

- Create R-network using EDA tool.
- Set up port locations for cap terminations and Vcore, Vsa, Vtt, and socket locations.

Step 2. Socket model

- Get socket pin map from supplier.
- Get R & L values of each socket pin from supplier.
- Group socket pins and scale R & L values.

Step 3. Icc, Isa, Itt models

- Get I (t) model from supplier

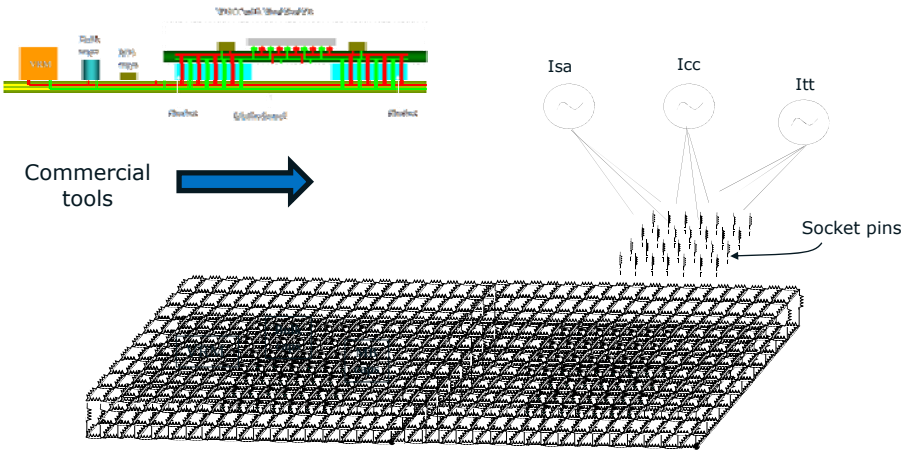
Step 4. VR model

- Use simple VR model from supplier.

Step 5. Connect all models together and run transient simulations

- Vcore(t), Vsa(t), Vtt(t) separately

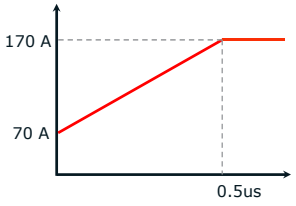
Step 6. Compare V(t) with DC and Transient Requirements



For VR design: we'll provide current models of Vcore, Vsa, and Vtt and indicate the locations of the socket pins to connect your MB. MB models will only include R from Power/Ground planes and vias.

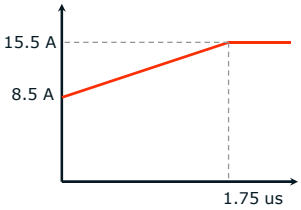
I(t) Models of Vcc/Vsa/Vtt

A server CPU
150 W PVCCP (8 core)



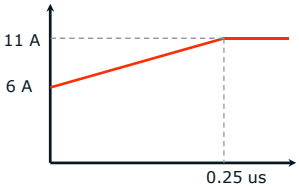
Max step load size = 100 A
Max step load slew rate di/dt ≤ 200 A/µs

A server CPU PVSA



Max step load size = 7A (Current pulse duration <1µs)
Max step load slew rate di/dt ≤ 4.0 A/µs

A server CPU PVTT



Max step load size = 5 A
Max step load slew rate di/dt = 20 A/µs

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Socket Connections (Top MB Layer, 1 of 5)

MB nodes	PKG nodes
VCCU pins	
AB33	bx11y20
AA33	bx11y21
Y33	bx11y22
W33	bx11y23
V33	bx11y24
U33	bx11y25
T33	bx11y26
R33	bx11y27
BA28	bx16y1
AY28	bx16y2
AW28	bx16y3
AV28	bx16y4
AU28	bx16y5
AT28	bx16y6
AR28	bx16y7
AP28	bx16y8
AN28	bx16y9
AM28	bx16y10
AL28	bx16y11
AK28	bx16y12
BA27	bx17y1
AY27	bx17y2
AW27	bx17y3
AV27	bx17y4
AU27	bx17y5
AT27	bx17y6
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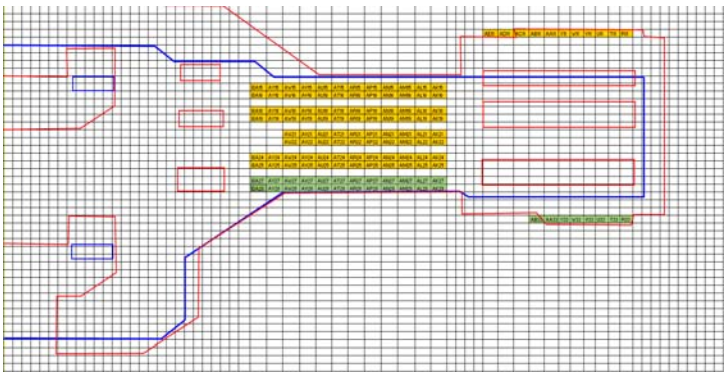
AP27	bx17y8
AN27	bx17y9
AM27	bx17y10
AL27	bx17y11
AK27	bx17y12



You may need to lump several pins as one node.

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Stackup (6 layer)

Layer Name	Plane Description	Layer Thickness (mil)	Copper Weight (oz)	Dielectric (eR)	tand (max)
	solder mask	0.50		3.8	0.022
Signal 1	SIGNAL	1.90	1.5		
	prepreg and/or Core	2.70		4.0	0.022
Plane 2	GND	1.30	1.0		
	Prepreg	4.00		4.1	0.022
Signal 3	SIGNAL	1.30	1.0		
	core	39.00		4.0	0.022
Signal 4	SIGNAL	1.30	1.0		
	Prepreg	4.00		4.1	0.022
Plane 5	GND / VDD	1.30	1.0		
	prepreg and/or Core	2.70		4.0	0.022
Signal 6	SIGNAL	1.90	1.5		
	solder mask	0.50		3.8	0.022
	Total	62.40	(+8/-5)		

You may want to get MB resistivity value from MB suppliers.

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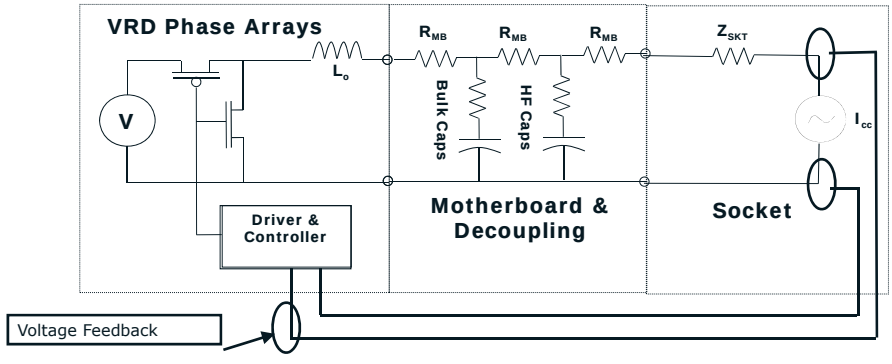
Simplified SPICE Model

Simplified Multiphase VRD (P1~P4) with Socket LoadLine

Simplified MB R network include Bulk Caps & Decoupling HF Caps

Icc / Isa / Itt current SPICE Model

Sensing at CPU Socket



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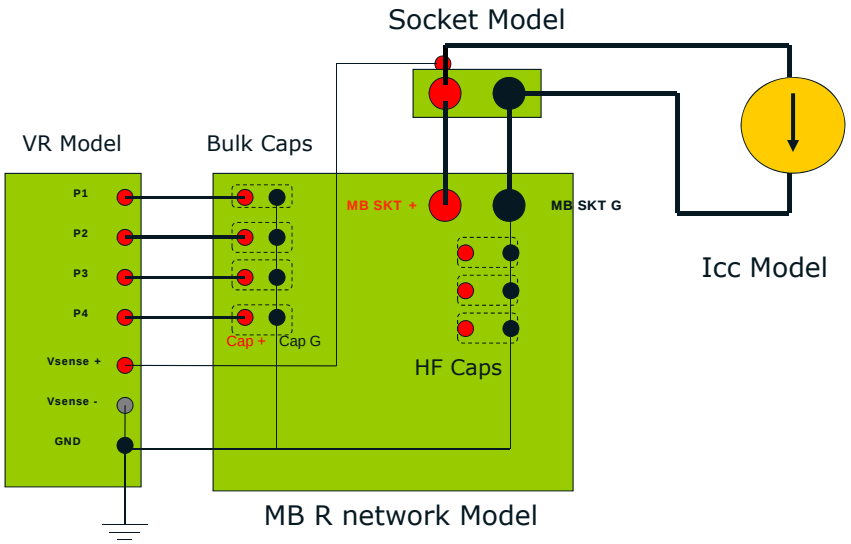
SPICE Model Connection Block Diagram



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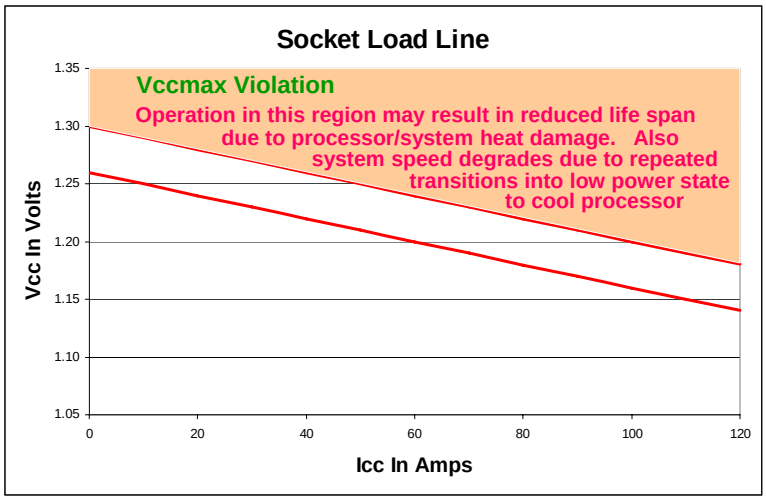
DC Requirements



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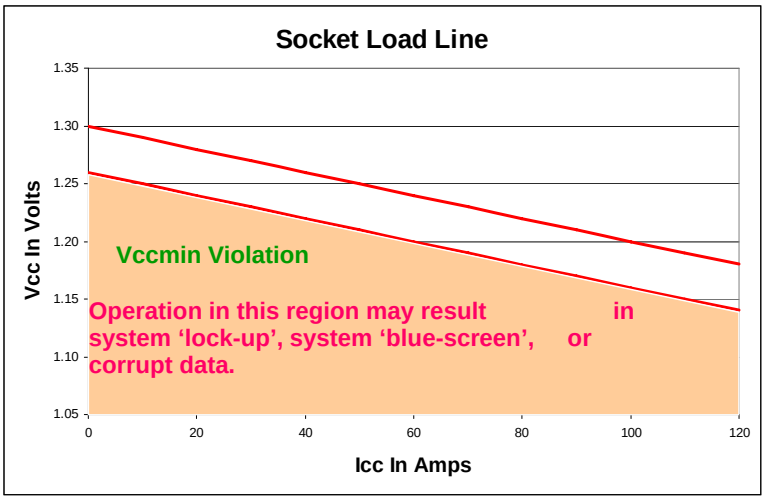
DC Requirements (cont'd)



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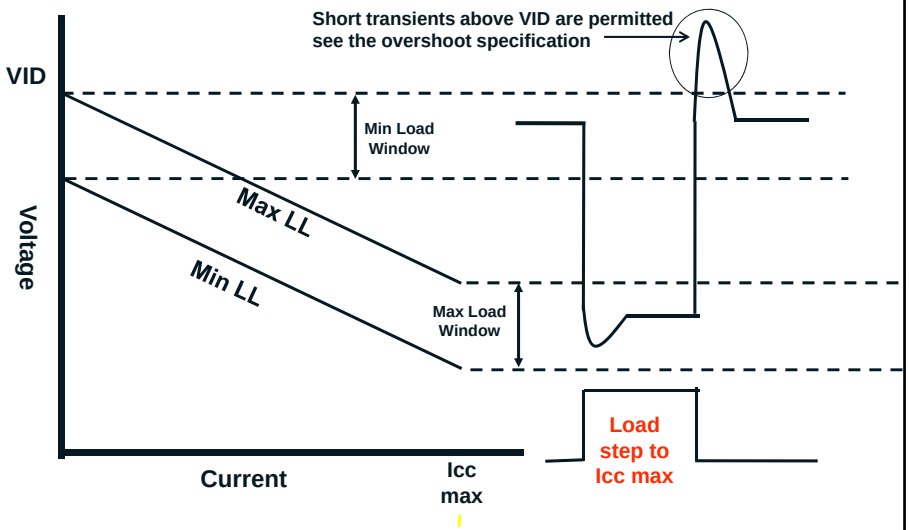
Dynamic or Transient Requirements



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Agenda

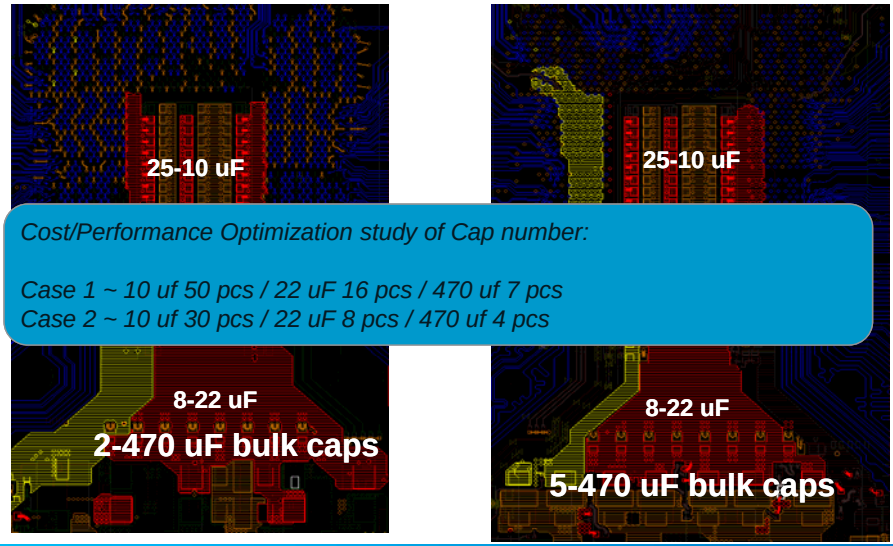
- Introduction
- Simplified SPICE Model
- ✓ Case Study and Its Application
- Validation
- Summary & Next Steps

Case Study –

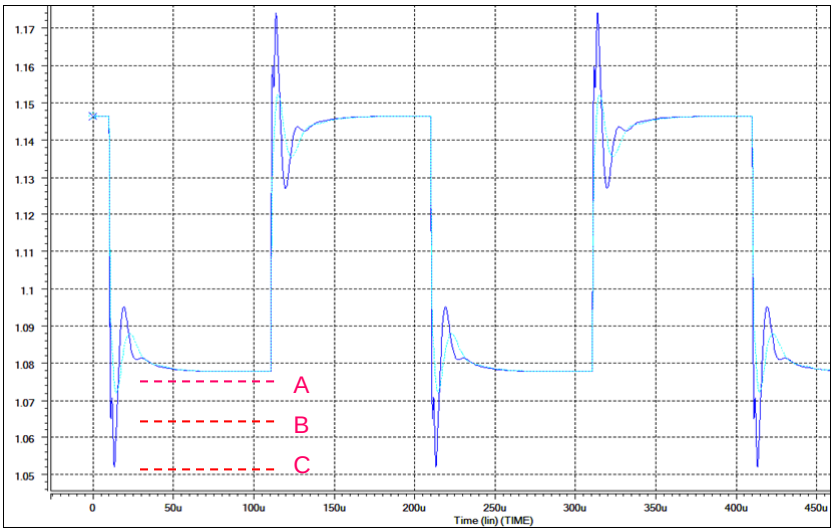
Cost/Performance Optimization of Cap number

Top caps

Bottom caps



Case Study – *Cost/Performance Optimization of Cap number*



If transient design target is A, both Cases 1 and 2 fail.
If transient design target is B, Case 1 is fine but Case 2 fail.
If transient design target is C, both Cases 1 and 2 are fine.

Agenda

- Introduction
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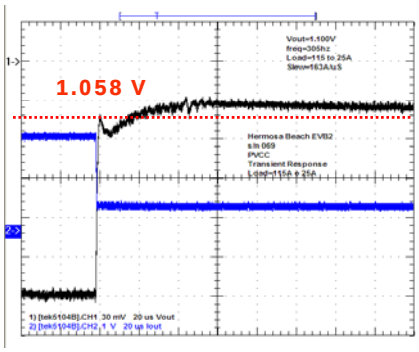
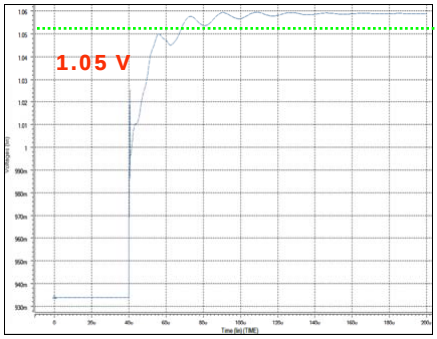
XYZ CRB
Simulation Result vs. VRTT Test Result

Loading frequency = 305 Hz

Slew=163 A/uS





1st spike reading:

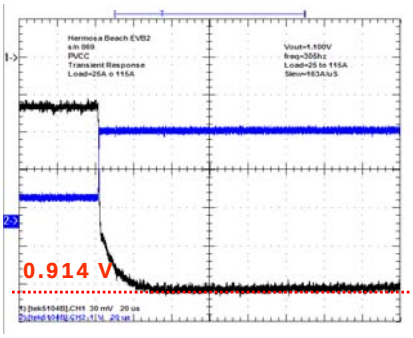
1.058 V vs. 1.05 V @ 115 A to 25 A **8 mV** difference only → **99.24% Accuracy**

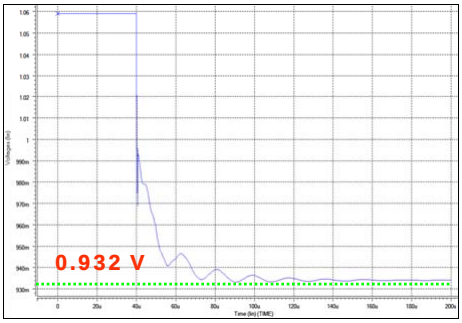
- Including more sophisticated VR model with FETs may be able to reduce Waveform Δ.
- Adding MB parasitic C & L should be helpful in reduction of waveform Δ as well.

XYZ CRB
Simulation Result vs. VRTT Test Result

Loading frequency = 305 Hz

Slew=163 A/uS





1st spike reading:

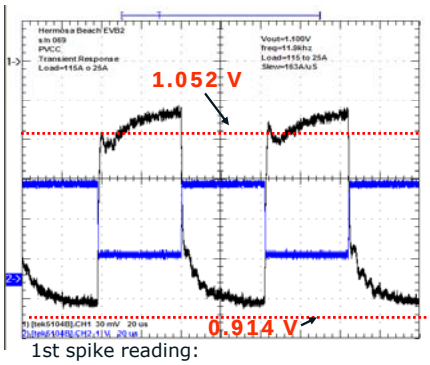
0.914 V vs. 0.932 V @ 25 A to 115 A **18 mV** difference only → **98.07% Accuracy**

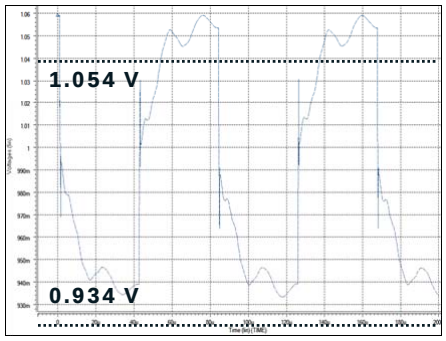
- Including more sophisticated VR model with FETs may be able to reduce Waveform Δ.
- Adding MB parasitic C & L should be helpful in reduction of waveform Δ as well.

XYZ CRB
Simulation Result vs. VRTT Test Result

Loading frequency = 12K

Slew=163A/uS





1st spike reading:

1.052 V vs. 1.054 V @ **115** A to 25 A **2 mV** difference only → **99.8% Accuracy**

0.914 V vs. 0.934 V @ 25 A to 115 A **20 mV** difference only → **97.85% Accuracy**

- Including more sophisticated VR model with FETs may be able to reduce Waveform Δ.
- Adding MB parasitic C & L should be helpful in reduction of waveform Δ as well.

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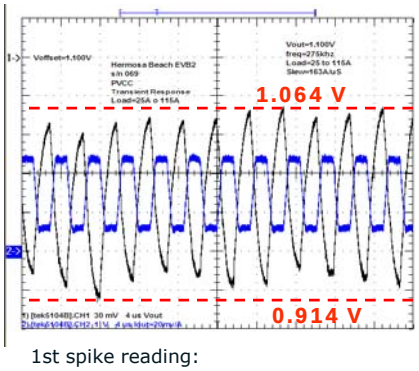
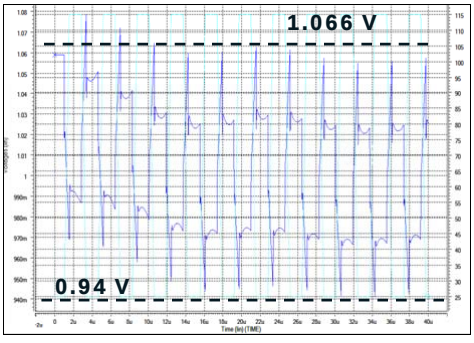
XYZ CRB
Simulation Result vs. VRTT Test Result

Loading frequency = 275K

Slew=163 A/uS





1st spike reading:

1.064 V vs. 1.066 V @ 115 A to 25 A **2 mV** difference only → **99.8% Accuracy**

0.914 V vs. 0.94 V @ 25 A to 115 A **26 mV** difference only → **97.63% Accuracy**

- Including more sophisticated VR model with FETs may be able to reduce Waveform Δ.
- Adding MB parasitic C & L should be helpful in reduction of waveform Δ as well.

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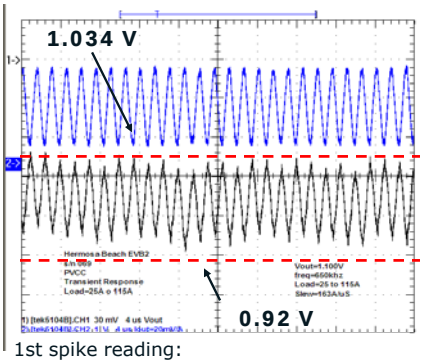
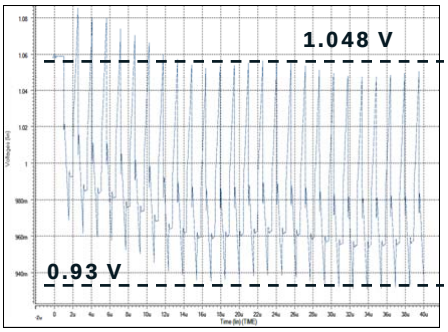
XYZ CRB
Simulation Result vs. VRTT Test Result

Loading frequency = 650K

Slew=163 A/uS





1st spike reading:

1.034 V vs. 1.048 V @ 115 A to 25 A **14 mV** difference only → **98.66% Accuracy**

0.92 V vs. 0.93 V @ 25 A to 115 A **10 mV** difference only → **98.9% Accuracy**

- Including more sophisticated VR model with FETs may be able to reduce Waveform Δ.
- Adding MB parasitic C & L should be helpful in reduction of waveform Δ as well.

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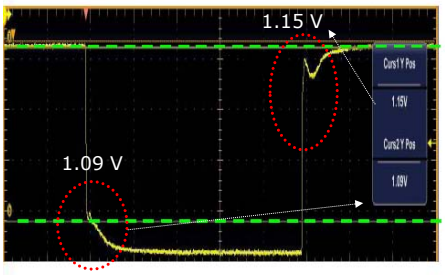
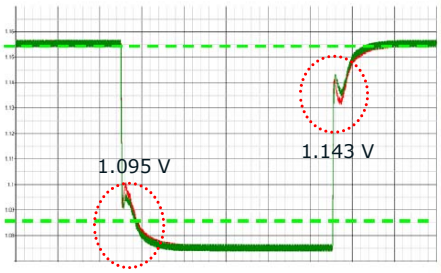
Simulation Result vs. Real VRTT Test Result





— MB model is a Resistance network
— MB model is a SPICE lump circuit

1st spike reading:

1.15 V vs. 1.143 V @ 165 A to 59 A **7 mV** difference only

1.09 V vs. 1.095 V @ 59 A to 165 A **5 mV** difference only

Simulation Result Accuracy higher then 99%
*** (This case used a very sophisticated VR model from VR Vender.)**

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Agenda

- Introduction
- Simplified SPICE Model
- Case Study & Its Application
- Methodology Validation
- ✓Summary and Next Steps

Summary and Next Steps

Simplified SPICE model has been validated by companies

Using the collaterals, companies can

- ❑ optimize their own designs & make their own decisions before Gerber Out to achieve the best cost/performance trade-off in
  - ➢ Determine # of MB layers & stack-up
  - ➢ Choose MB cap types, numbers & locations
- ❑ reduce risk of common ground noise coupling among Vcc, Vsa, Vtt, and Vddq
- ❑ validate their own designs after Gerber Out

Next Steps

- ❑ Obtain more sophisticated VR model from venders
- ❑ Include thermal impact to more accurately predict Maximum Current can be carried.