



IBIS-ISS: What It Is and What It Means to You

Michael Mirmak
Intel Corporation
Chair, IBIS Open Forum

マイケルマーマク
インテルコーポレーション
会長, アイビス

IBIS Summit Tokyo
November 15, 2010

Originally presented in Shenzhen on Nov. 9, 2010

Legal Disclaimer

Notice: This document contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information. Contact your local Intel sales office or your distributor to obtain the latest specification before placing your product order.

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO SALE AND/OR USE OF INTEL PRODUCTS, INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, or life sustaining applications. Intel may make changes to specifications, product descriptions, and plans at any time, without notice.

All products, dates, and figures are preliminary for planning purposes and are subject to change without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The Intel products discussed herein may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or by visiting Intel's website at <http://www.intel.com>.

Intel and the Intel logo are trademarks of Intel Corporation in the U. S. and other countries.

Copyright © 2010, Intel Corporation. All rights reserved.

*Other names and brands may be claimed as the property of others.

Agenda

- The Problem of SPICE* Model Portability
- The Concept of IBIS-ISS
- What Is and Isn't Supported
- IBIS-ISS and Good SPICE Usage
- Status and Future Work
- Summary and Call for Action!

* Other names and brands may be claimed as the property of others



A Standard SPICE* Does Not Exist

- What does the following SPICE* statement do?

Example 1 2 I=sin(V(3,0))

- Results depend on the SPICE tool you use
 - IBIS or non-linear dependent source?
- Some elements are not supported or do not share a common meaning in all SPICE variants
 - Other non-universal elements include P, W, Y, Z

How do you ensure a model works in your tool or your customers' tools?

A Solution for SI/PI Interconnects

- SPICE* netlists include interconnects, devices and engine commands
 - e.g., .tran analysis for a driver and receiver on a PCB trace
- IBIS supports portable device models directly
- Engine commands are specific to EDA tools
- How to ensure interconnect models are portable?
 - Package, via, connector, PCB trace, on-die PDN...

IBIS-ISS: an industry baseline for interconnect modeling in SPICE

IBIS-ISS in Simple Terms

- IBIS-ISS: IBIS Interconnect SPICE* Subcircuits
- Defines a limited set of common, basic elements useful for SI interconnect modeling
- Based on documents and concepts donated by Synopsys as seen in Synopsys HSPICE*
- Developed with SI community through IBIS Interconnect Task Group
 - EDA vendors, IC vendors and system vendors

What Is (and Is Not) Supported

- Fundamental circuit elements
 - Resistors, Inductors, Capacitors: R, L, K, C
 - Dependent Sources: E, F, G, H
 - Transmission Lines: T, W (including tabular, Foster, etc.)
 - S-parameters: S
- Subcircuit definitions and instantiation
 - .subckt, .ends, X element
- Other basic commands
 - .include, .end, .param

... but no engine commands, no active device support, and no field solver

Usage Model

- IBIS-ISS consists entirely of subcircuits and subcircuit definitions
 - IBIS-ISS does not define netlists
 - Subcircuits may be nested or independent
- All parameters are local, and passed explicitly
- Multiple files are supported (.include)
- Compliant tools simply accept IBIS-ISS files
 - Meaning, properly apply IBIS-ISS assumptions within the scope of the top-level subcircuit

How Does It Work?

```
.subckt my_trace_group 1 2 3 4 5 6 7 8 ref length=5e-3
* Units are meters
* This is a top-level subcircuit
* The user/system designer will instantiate this circuit in a netlist
```

```
Xtrace_a 1 ref 2 ref single_trace local_length=length
Xtrace_b 3 ref 4 ref single_trace local_length=length
Xtrace_c 5 ref 6 ref single_trace local_length=length
Xtrace_d 7 ref 8 ref single_trace local_length=length
```

```
* This circuit assumes no crosstalk
```

```
.subckt single_trace in local_ref out local_ref local_length=1
```

```
Wsingle in local_ref out local_ref N=1 L='local_length'
+ TABLEMODEL='single_line_table'
```

```
.include 'single_line_table.inc'
```

```
* This file defines the tabular data using .MODEL
```

```
* This file should also be written using ISS rules
```

```
.ends
```

```
.ends
```

Using SPICE* Correctly

- Good SPICE* habits will make IBIS-ISS adoption and use easier
 - Pass parameters explicitly and sparingly
 - Do not rely on global parameter definitions
 - Avoid using global nodes
 - Use modular circuit design
 - Make node, parameter and element names clear and unique
 - Avoid setting engine options in subcircuits
 - Avoid ambiguous units and multipliers (e.g., amps vs. atto-)

Practice using IBIS-ISS rules in your circuits today

Status and Future Work

- Draft v0.7 now in review
- Once drafts are complete, the document will be provided to the IBIS Open Forum for approval
- A parser is under consideration
- Documents and background materials on-line:
 - http://www.eda.org/ibis/interconnect_wip/
- Mailing list available for updates and discussion:
 - <http://www.freelists.org/list/ibis-interconn/>

Questions and comments are welcome!

Summary

- If you model interconnects, IBIS-ISS can help ensure usability across SPICE* tools
- If you use SPICE of any kind, IBIS-ISS will be familiar to you
- Following principles of good SPICE circuit construction makes IBIS-ISS easy to use

Please study, learn, discuss and comment
on the IBIS-ISS draft.

Your contributions are important!