IBIS Open Forum Minutes

Meeting Date: **November 15, 2010**
Meeting Location: **Tokyo, Japan**

VOTING MEMBERS AND 2010 PARTICIPANTS

Agilent	Radek Biernacki, Ming Yan, Fangyi Rao, Gilbert Berger, Amolak Badeasa, Jose Pino, Junaid Khan, Charles Lu, Xuliang Yuan, Ming-Chih Lin, David Huang, Avery Chung
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Ansys (Ansoft Corporation)	Danil Kirsanov, Baolong Li
Apple Computer	(Matt Herndon)
Applied Simulation Technology	(Fred Balistreri)
ARM	(Nirav Patel)
Cadence Design Systems	Terry Jernberg, Wenliang Dai, Ambrish Varma Shisheng Wu, Lanbing Chen, Daisy Cheung, Fang Li, Sammi (Rong) Fu, William Fu, Weichun Ke, Ciron Wu, Jun Wu, Thunder Lay, Yukio Masuko*
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Ericsson	Anders Ekholm*, Pete Tomaszewski
Freescale	Jon Burnett, Om Mandhana
Green Streak Programs	Lynne Green
Hitachi ULSI Systems	Yutaka Uematsu, Sadahiro Nonoyama*
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LSI	Brian Burdick
Mentor Graphics	Arpad Muranyi, Neil Fernandes, Zhen Mu, Jack Yang, Sophia Yang
Micron Technology	Randy Wolff
Nokia Siemens Networks GmbH	Eckhard Lenski
Samtec	(Corey Kimble)
Signal Integrity Software	Walter Katz, Mike Steinberger, Todd Westerhoff,

	Barry Katz
Sigrity	Brad Brim, Kumar Keshavan, Srdjan Djordjevic, Ben Franklin, Zhangmin Zhong, Raymond Y. Chen, Xianfeng Li, Haisan Wang, Polin Chi, Jack Lin, Joshua Luo
Synopsys	Ted Mido, Paul Lo, Geoffrey Ying, Frank Lee, Xuefeng Chen, Deng Shi
Teraspeed Consulting Group	Bob Ross*, Tom Dagostino
Texas Instruments	Bonnie Baker
Toshiba (Toshiba I.S. Corp.)	Yoshihiro Hamaji*, Yasutaka Oodake*, Yasuki Torigoshi*, Atsuko Baba*
Xilinx	Mike Jenkins
ZTE	Jian Pang, Ping Wang, Shunlin Zhu, Zhiwei Yang, Jinku Guan, Wei Jia, Nan Jian, Guanghui Li, Xian Lu, Yingxin Wang, Bi Yi, Wei Zhou, Shunlin Zhu
Zuken (ZSAS)	Michael Schaeder, Ralf Bruening, Hirohiko Matsuzawa*, Yuichi Nakajima*, Seikou Go*

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Altera	John Oh, Hui Fu
Apache Design Solutions	Shulong Wu
ASE Group	Marco Cheng, AlexCC Wang, Paddy Wu
ASUSTek Computer	David Chou, Yu-Ching Liao, Vincent Lu
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Avago	Razi Kaw
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China Fastprint	Matthew Li, Mark Long
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Delta Network	Skipper Liang, Min-Hong Tsai
ECL, Inc.	Tom Iddings

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Etron	Chunmu Lin, Stu Tsai
eSilicon	Hanza Rahmai
EVOC Intelligent Technology	ChangQian Yu
Exar Corp.	Helen Nguyen
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(Fujitsu Semiconductors)	Motoaki Matsumura*
(Fujitsu VLSI Limited)	Yuji Nakagawa*, Kyota Shimizu*
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Giga Hertz Technology	Ryuji Kawamura*
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Ili Technology	Chia-Cheng (Trevor) Wu
Inventec	Ian Chen, Elien Tseng
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KEI Systems	Shinichi Maeda*
Layout Technology	Ken Chen
Leading Edge	Pietro Vergine
Lenovo	Mandy Yang, Lu Zhang
Magna Design Automation	Anand Ramalingram
Mindspeed	Bobby Altaf
Nanya Technology	Cheyen Huang, Yuwei Chen, Ching-Feng Chen, Yumin Chen, Argy Cheng, Raphael Huang, Chun-Huang Yu
National Semiconductor	Hsinho Wu
National Chao Tung University (NCTU)	Cheng-Yuan Chin, Pan-Shine Wang
National University of Kaohsiung (NUK)	Ming Haei Huang, Kao-Yi Wang
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NXP Semiconductors	Gerald Krasemann
Pegatron Corp.	Stanley Chu, Lawrence Ting
Politecnico di Torino	Igor Stievano, Stefano Grivet-Talocia, Piero Triverio, Flavio Canavero
Portwell	Michael Chang
Propogate Group Corp. (PGC)	Wayne Tsai, Mage Wang
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Ralink Technology	Wilbur Hsu, Dean Yang
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TDK	Yoshikazu Fujishiro*
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Towa Electronics	Yoshikazu Suzuki*
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Vitesse Semiconductor	Bob McDonough
Winbond Electronics Corp.	Jein-Cherng Lin
Wistron Corp.	Denis Chen, Passor Ho, Dirack Lai, Edward Pan
YanHua Technology	Xiuchun Peng
ZyXEL Communications Corp.	Frank Chang
Independent	AbdulRahman (Abbey) Rafiq, Robert Badal

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 19, 2010	204 170 411	IBIS

For teleconference dial-in information, use the password at the following website:

https://cisco.webex.com/cisco/j.php?J=204170411

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The IBIS Open Forum summit was held in Tokyo, Japan at the Japan Electronics and Information Technology Industries Association (JEITA) headquarters. About 38 people representing 22 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/pub/ibis/summits/nov10c/

Bob Ross (on behalf of Michael Mirmak) opened the fifth Asian IBIS Summit - Tokyo meeting at 1:30 PM.

Yasutaka Oodake (JEITA EC Working Group Chair and Toshiba Corporation) welcomed everyone and thanked the international attendees: Bob Ross and Anders Ekholm for coming. He also thanked the sponsors, ATE Service (Sigrity), Cadence Design Systems, and Zuken for their support. Yasutaka indicated that the JEITA EC Working Group remains active in IBIS and that an IBIS model quality website will be hosted by JEITA by the end of the year.

Bob Ross provided some brief remarks noting that this was the fifth meeting and that cooperation with JEITA has been strong over the years. He thanked JEITA for arranging the meeting and providing excellent facilities.

IBIS PROJECTS AND ACTIVITIES

Bob Ross (Teraspeed Consulting Group, USA)

Bob described IBIS as an official standards committee under the SSTC (Standards and Technology Council), which itself is under TechAmerica. Bob showed the current IBIS officers and noted that IBIS has been active since 1993 with teleconference/web meetings and with up to six Summits per year in Asia, Europe and the US. Four task groups (Advanced Technology Modeling, Quality, Interconnect, and IBIS Model Review) remain active under IBIS.

Bob identified nine current projects and gave a brief summary to define some terminology and to relate how presentations in this meeting are related to on-going activities. The projects are (1) IBIS-ISS (IBIS - Interconnect Spice Subcircuits), (2) IBIS-AMI (IBIS - Algorithmic Model Interface), (3) possible IBIS multi-lingual linkages with IBIS-ISS, (4) MCP (Model Connection Protocol), (5) Touchstone Version 2.1, (6) IBIS Version 5.1, (7) IBIS Version 5.0 ongoing support, (8) ibischk5 maintenance, and (9) Quality Committee advances. Bob also provided

some IBIS home page links to relevant documents and work-in-progress directories under

http://www.eda.org/ibis

Bob noted that several presentations directly or indirectly related to IBIS issues and methods to simplify the analysis.

MODEL HANDLING AND IBIS FILE SIZES - RECENT EXPERIENCES WITH NEW IBIS FILES

Hirohiko Matsuzawa#, Ralf Bruening## and Michael Schaeder## (Zuken, #Japan and ##Germany)

Hirohiko Matsuzawa started his presentation by telling about the experience from customers that the size of some IBIS files has increased tremendously and that it almost can not be handled. A user who is not working daily with IBIS models is overly challenged; even some [Model Selector]s have up to 30 models. He then talked about the early days of IBIS with just a few I/O models per device and that from time to time the size did grow. But in recent years, the size of IBIS files is exploding. Files with 70 MB to 80 MB including up to 7000 different I/O models appeared. The IBIS parser can handle these big files, although it might take up to 2 minutes for a file to be checked, but some third party tools (especially freeware viewers) have problems with these big files. Some vendors deliver an extra file with a model description, while others are using an almost encrypted model name convention, which is not easy to understand. And there are other models for parts that are even divided by technology or functional block, and the package is delivered as an HSPICE model. So, the user has to do a lot of handwork, which is error prone. Hirohiko concluded that the handling of IBIS data must be improved and more and more users are asking him for help.

POINT REDUCTION METHOD FOR IBIS CURVES

Lance Wang (IO Methodology, USA)

Anders Ekholm (Ericsson, Sweden) on behalf of Lance Wang described how a point reduction system uses algorithms for proper point number reduction with minimum sacrifices to accuracy. A point reduction method is useful in IBIS for representations of I-V curves with only 100 data points. The IBIS cookbook mentions two methods: points selected with a regular interval or using a ‘greatest change’ algorithm. The interval spacing method is easy but may lack enough detail in some areas of the curves. Anders described the methodology of developing a ‘greatest change’ algorithm. The two methods were compared to a Golden Waveform curve to show the superiority of the ‘greatest change’ method. The ‘greatest change’ algorithm works well with IBIS V-t curve point reduction but may still cause inaccuracies in I-V curves. This inaccuracy was demonstrated by showing simulation results to a test circuit. Anders then introduced a ‘Weighted Best Point’ (WBP) method. The WBP method combines the ‘regular interval’ and ‘greatest change’ methods by focusing the ‘greatest change’ method on the working range of the I-V curves. This method improves accuracy.

In response to questions, Anders indicated that the main benefit of the WBP approach is to provide the same accuracy with fewer points than with the other methods.

JEITA IBIS QUALITY WG UPDATE

Yoshihiro Hamaji* and Atsushi Osaki** (Toshiba I.S. Corporation and **Toshiba Corporation, Japan)
Yoshihiro Hamaji indicated that quality issues are confusing. Questions arise between the set maker (user), the EDA vendor, and the chip vendor regarding correct generation of IBIS models, correct simulator algorithms, and correct usage of the simulator. The purpose of the JEITA IBIS Quality WG is to provide a framework so that one can verify IBIS quality. Work began in 2007 and currently includes single-ended and differential IBIS models. A website is being prepared for low-speed IBIS models.

Yoshihiro showed some process slides to qualify IBIS models for different tools and with 12 different test loads. He then showed draft website templates (in Japanese) planned under a future link:

http://www.ec.jeita.or.jp/jp/

On the site, the submitter of IBIS model information is identified and golden results for models are provided for the given test circuits. He hopes companies will use this framework.

IBIS FOR SSO ANALYSIS

Haisan Wang, Joshua Luo, Jack Lin, Zhangmin Zhong (Sigrity, China)
Yutaka Honda (ATE Service (Sigrity), Japan) began with an overview of a traditional I/O SSO analysis investigating PDN noise and crosstalk. He listed fundamentals of SSO mechanisms. Simulations of power supply voltage noise were compared to measurements. SSO simulation requires models of boards, packages and IO buffers. IBIS buffer model accuracy is questionable for Power Integrity (PI) analysis as compared to a SPICE model. SPICE limitations make use of IBIS for PI analysis a requirement. IBIS models of Version 4.2 or older do not model pre-driver currents which can have significantly higher dI/dt than the driver current. Crowbar current can be modeled fairly well when all four sets of V-t curves are in the IBIS model, but pre-driver currents are missing. The BIRD95 [Composite Current] keyword found in IBIS 5.0 adds pre-driver current characteristics to the IBIS model. Using [Composite Current] results in significantly improved correlation to SPICE results. A BIRD95 model is still missing the on-die decoupling capacitor between power and ground. Adding an RC circuit for this capacitance in parallel with the IBIS driver improves the model accuracy: oscillations occur at the proper frequencies and the SSO magnitude is correct. Simulations were compared to measurements with good correlation. IBIS 5.0 improves accuracy in SSO simulation.

EXTENDING/LEVERAGING IBIS CONSTRUCTS TO MODEL HIGH-SPEED I/O'S AND PACKAGES USING AMI, SPICE, AND S-PARAMETERS

John Lin*, Feras Al-Hawari**##, Taranjit Kukal**# and Ambrish Varma**## (*Flextronics, China and **Cadence Design Systems, #India and ##USA)
Yukio Masuko (Cadence Design Systems, Japan) delivered the presentation. With current IBIS constructs, RDL and/or pin parasitic are lumped into pin R/L/C values. At high frequencies, IO buffers could have portions that need to be modeled using Spice files such as On-die termination with frequency dependence. Multiple Spice subcircuits could be used to model different process corners, buffer configurations or dynamic ODT. There are many limitations to current inclusion of Spice subcircuits with [External Model]. [External Model] could be leveraged to support S-parameter package modeling. Long term, IBIS could have keywords to support S-parameters under the Package section to provide port mapping and prompt SI tools

to ignore RLC values. An example was shown of using [External Model] to include an S-parameter package model. Package RLC values were zeroed out when doing this to avoid double-counting. Yukio proposed extending [External Model] to point to Spice sub-circuits that augment V-I and V-t data for complete characterization of the IO buffer. [External Model] would also be extended to allow dynamic switching of subcircuits for corners and parametric variations. AMI models should also work in conjunction with [External Model].

IBIS-ISS: WHAT IS IT AND WHAT IT MEANS TO YOU

Michael Mirmak (Intel Corporation, USA)

Bob Ross (Teraspeed Consulting Group,USA) on behalf of Michael noted that the problem with SPICE model portability is that a standard SPICE does not exist. IBIS-ISS (Interconnect SPICE Subcircuits) establishes an industry standard baseline for interconnect modeling in SPICE. It defines a limited set of common, basic elements useful for SI interconnect modeling. It is based on documents and concepts donated by Synopsys as seen in Synopsys HSPICE. IBIS-ISS was developed with the SI community through the IBIS Interconnect task group. IBIS-ISS supports fundamental circuit elements, subcircuit definitions and instantiation and some other basic commands, but no engine commands, no active device support and no field solver.

IBIS-ISS consists entirely of subcircuits, so it does not define netlists. All parameters are local and passed explicitly. Multiple files are supported. Good SPICE habits will make IBIS-ISS adoption and use easier. Bob listed several IBIS-ISS rules to follow. Draft 0.7 is now in review and a parser is under consideration. He encouraged questions and comments.

Tadashi Arai and others questioned and commented about the omission of voltage and current sources. Bob commented that this was a restriction to keep the IBIS-ISS focused on interconnect issues.

FIRST PRACTICAL EXPERIENCES WITH ICEM (IC EMISSION) MODELS IN ECAD ANALYSIS TOOLS

Hirohiko Matsuzawa# and Ralf Bruening## (Zuken, #Japan and ##Germany)

Hirohiko Matsuzawa noted that the demand for ICEM models arises since IBIS does not model the core switching behavior. The need for IC emission analysis arises mostly from the automotive and aerospace industry. Emissions from printed circuit boards can be separated into four major root causes: differential mode (from transmission lines), common mode radiation, radiation from the power bus, and IC noise. Hirohiko wondered if ICEM models could close the gap, since they are very close to SPICE. Normally a large netlist with a large number of elements is needed for core switching. ICEM documents a reduced structure. Most of the ICEM work is still very research oriented, and Hirohiko provided a list of modeling challenges such as internal coupling effects. He explained that only a few vendors are supporting ICEM models, and a lot of work is necessary such as for getting information about the current profile of the die and the coupling between functional blocks. This results in a long SPICE netlist. He pointed out that a reduction process for this large netlist is under development. Correlation is difficult and problems exist to get the netlist to run at all. For even the one that worked, it took days to finish the simulation. The current challenge is to create a model that has a frequency dependency for the current. It appears that ICEM is used more in IC-design rather than for PCB design.

MODEL CONNECTION PROTOCOL EXTENSIONS FOR MIXED SIGNAL SIP

Taranjit Kukal*#, WenLiang Dai*##, Brad Brim** and Eiji Fujine*** (*Cadence Design Systems, #India, ##China, **Sigrity, USA and ***Fujitsu VLSI Limited, Japan)

Yukio Masuko (Cadence, Japan) described how chip/package/board connections can have 100s to 1000s of physical connections, but not all electrical nodes can have per-pin resolution. A method is needed to group pins and auto-connect models across the chip/package/board boundaries. Model Connection Protocol (MCP) establishes pin grouping and mapping of physical to electrical nodes. MCP extensions can be used for mixed-signal System-in-Package (SiP) power delivery analysis. Connecting two disparately pin-grouped models is possible by choosing to short together electrical nodes that have overlapping pin domains. Support for modules is needed in MCP as a category for structures drawing power within the package such as RF modules and metal passive structures. Connections by reference designator instead of x-y location are another recommended extension to existing MCP. An optional column showing connection by REFDES makes for easy mapping for mixed-signal modules and pre-layout analysis.

CONCLUDING ITEMS

Bob Ross thanked Atsushi Ishikawa and Yasutaka Oodake of JEITA for their support, the sponsors of the meeting, the presenters for fine presentations, and Yukio Masuko (Cadence Design Systems) and Shinichi Maeda (KEI Systems) for assisting in English-to-Japanese translation. He also thanked the attendees for providing strong support, and he looked forward to another Summit in 2011. The meeting adjourned at approximately 6:05 PM.

NEXT MEETING

The next IBIS Open Forum teleconference will be held November 19, 2010 from 8:00 to 10:00 AM US Pacific Standard Time. A vote on BIRD113 is scheduled.

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NOTES

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This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda.org

In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda.org)
IBIS Users' Group Reflector (ibis-users@eda.org)
State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	October 22, 2010	November 9, 2010	November 12, 2010	November 15, 2010
Advanced Micro Devices	Producer	Inactive	-	-	-	X
Agilent Technologies	User	Active	X	X	X	-
Ansys	User	Inactive	-	X	-	-
Apple Computer	User	Inactive	-	-	-	-
Applied Simulation Technology	User	Inactive	-	-	-	-
ARM	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	X	X	X
Cisco Systems	User	Inactive	X	-	-	-
Ericsson	Producer	Active	X	X	X	X
Freescale	Producer	Inactive	-	-	-	-
Green Streak Programs	General Interest	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	X	-	-
Hitachi ULSI Systems	Producer	Inactive	-	-	-	X
IBM	Producer	Active	X	-	X	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	-
IO Methodology	User	Active	-	X	X	-
LSI	Producer	Inactive	X	-	-	-
Mentor Graphics	User	Inactive	X	X	-	-
Micron Technology	Producer	Active	X	X	X	-
Nokia Siemens Networks	Producer	Inactive	X	-	-	-
Samtec	Producer	Inactive	-	-	-	-
Signal Integrity Software	User	Inactive	X	-	-	-
Sigrity	User	Active	-	X	X	-
Synopsys	User	Inactive	-	X	-	-
Teraspeed Consulting	General Interest	Active	X	X	X	X
Texas Instruments	Producer	Inactive	-	-	-	-
Toshiba	Producer	Inactive	-	-	-	X
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	X	-	-
Zuken	User	Inactive	-	-	-	X

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH TECHAMERICA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.