Extending/Leveraging IBIS Constructs to Model High-Speed I/Os and Packages using AMI, Spice, and S-Parameters

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Note: Previously presented at IBIS Summits in China Nov. 9 and Taiwan Nov. 12

Asian IBIS Summit
Tokyo, Japan
November 15, 2010

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Agenda

- **IBIS Overview**
- **Why extend IBIS to SPICE models**
  - **Current Limitations**
- **Leveraging [External Model] to allow including Package S-Parameters for High Speed simulation**
  - **Example**
- **Extending [External Model] to:**
  - Simulate VI-VT model in conjunction with Spice sub-circuits that represent RDL elements, DSP Spice code, etc.
  - Dynamically switch sub-circuits to take care of corners and parametric variations.
  - Simulate AMI with [External Model] that represents analog IO modeled in Spice or S-parameters.
- **Summary**

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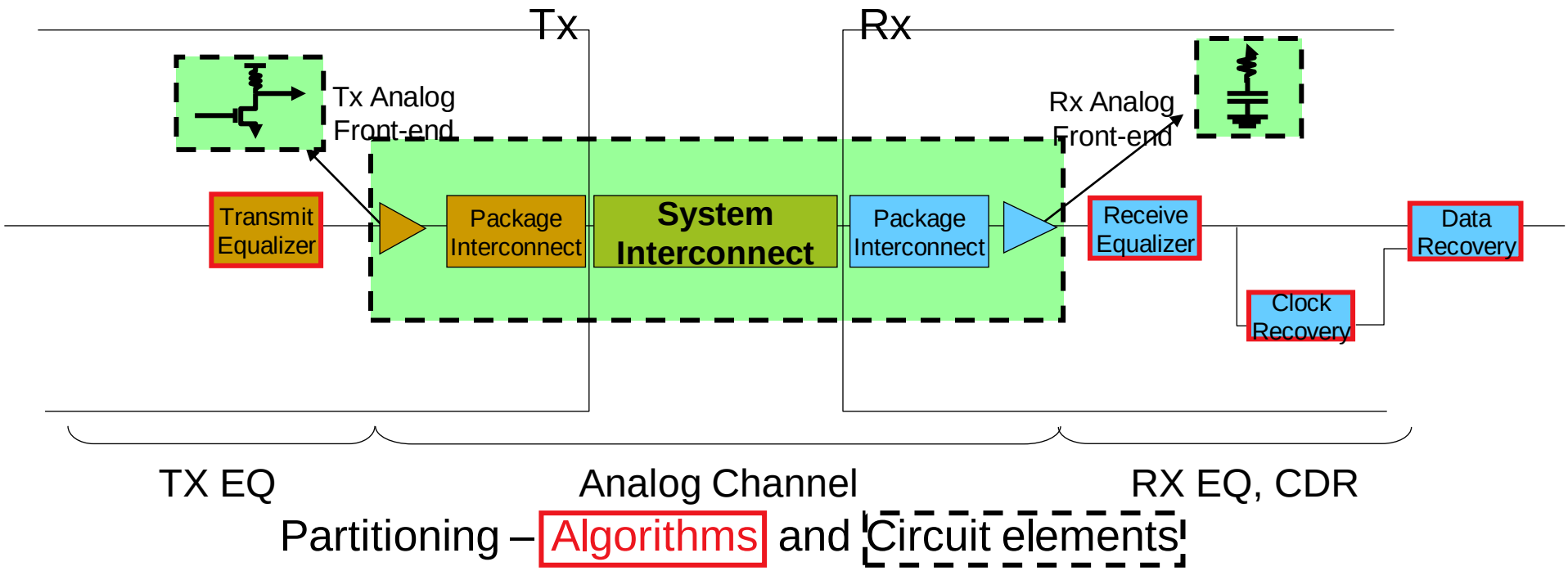
IBIS overview

- Analog IO model is modelled by IBIS VI and VT curves
- Equalization (DSP algorithmic) portion of IO model is modelled by AMI C-code (Algorithmic Model Interface) that is pointed by IBIS model
- RDL and or pin parasitics are lumped into pin R/L/C values



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Why extend IBIS to SPICE models

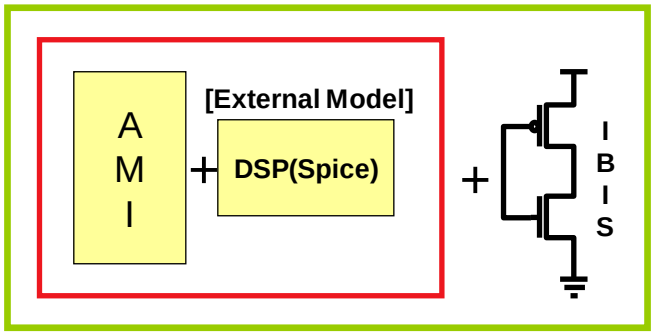
- **At high frequencies, IO buffers could have portions that need to be modeled using Spice files**:
  - On DIE Terminations (ODT) that vary with frequencies need to be expressed as s-parameters or RLGC Spice files
  - On DIE RDL parasitics become significant and vary with frequencies and hence have to be expressed as s-parameters or SPEF
  - Analog portion of IO-buffer is expressed as Spice as against VI-VT curve; s-parameters can also be used to describe transfer characteristics of IO-buffer amplifiers.
  - Some algorithmic portion may be modeled in Spice as against AMI code

Why extend IBIS to SPICE models

- **Multiple Sub-circuits / Spice files**
  - Different Spice sub-circuits could be applicable for different process corners. On-DIE RDL could be expressed as different s-parameter files for typ/min/max conditions.
  - Different Spice sub-circuits could be applicable for different buffer configurations. For example, Pre-emphasis portion could have been modeled as Spice using different sub-circuits for different settings.
  - ODT could be a function of current being drawn out of IO-buffer (Dynamic ODT) and could have been expressed as behavioral Spice, Verilog-A

Current Approach and Limitations

- Package parasitics can be used as S-parameters by including them as part of interconnect network in a way similar to external interconnect parasitics.
  - Limitation
    - RDL parasitics that need to be part of IO-buffer characterization are treated as interconnects and assumed bi-directional.
- Spice IO-buffers can be included as part of IBIS using [External Model] Keyword.
  - Limitations
    - Cannot model DSP (in SPICE) in conjunction with AMI model
      - Use of [External Model] in conjunction with VI-VT (IBIS) is not recommended today
    - Does not directly support s-parameters (Touchstone)
      - For example, it is not easy to model RDL and other elements in conjunction with VI-VT curves cannot take care of process corners and parametric selection of subcircuits



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Leveraging [External Model] to Support Package S-Parameters

- Long-term: IBIS model should have Keywords to support Touchstone S-parameters under Package section, with fields to
  - point to touchstone file from the Package section
  - provide port-mapping of IO-buffer pins to s-parameter ports
  - R/L/C values should be ignored by SI tools if s-parameter file is used
- Short-term: This can be achieved through use of [External Model] keyword
  - Set R/L/C values in package keyword as ZERO (to avoid double counting)
  - Point to the touchstone file of the package inside the Spice subcircuits

Example : Support for S-parameters for package parasitics using [External Model]

- Use IBIS Device with 4 pins (1, 2, 3, and 4)
- Pins 1 and 2 are +ve and -ve diff pins respectively, with a “tx” diff model assigned to both of them
- Pins 3 and 4 are +ve and -ve diff pins respectively, with a “rx” tdiff model assigned to both of them
- Tx and Rx contain corresponding
  - [External Model] section

Example ….

```
[Component]     MyComp
[Manufacturer]  xyz

[Package]
| variable      typ             min             max
R_pkg           0.0m            0.0m            0.0m
L_pkg           0nH             0nH             0nH
C_pkg           0pF             0pF             0pF
|
|-------------------------------------------------------------
[Pin]   signal_name     model_name      R_pin   L_pin   C_pin
|
  1     OUT1            tx      NA      NA      NA
  2     OUT2            tx      NA      NA      NA
  3     IN1             rx      NA      NA      NA
  4     IN2             rx      NA      NA      NA
|
[Diff Pin]  inv_pin  vdiff   tdelay_typ tdelay_min tdelay_max
|
 1          2           200mV    0ns        0ns        0ns
 3          4           200mV    0ns        0ns        0ns
|
```

Make values zero or NA

- Set the values of all package parasitics to 0 or NA because in this case we will model the package using an s-parameter that is referenced from the Rx/Tx subckts
- Assign the same model to each diff pin (e.g., tx is assigned to pins 1 and 2)
- Define the diff pins (e.g., 3 and 4) and specify vdiff

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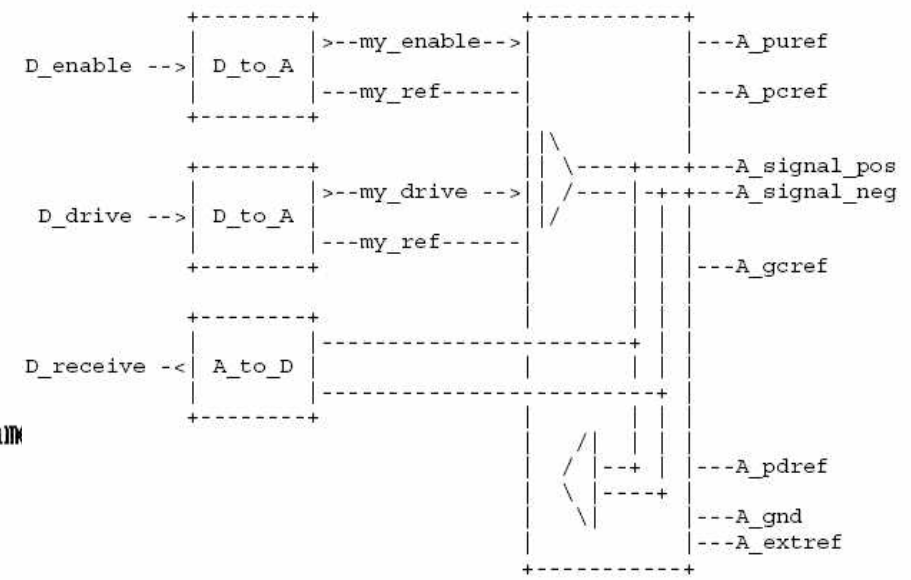
Example ….

```
|
[External Model]
Language SPICE
|
| Corner corner_name file_name   circuit_name (.subckt name)
Corner    Typ         tdiff_tx.spc  tdiff_tx_typ
Corner    Min         tdiff_tx.spc  tdiff_tx_min
Corner    Max         tdiff_tx.spc  tdiff_tx_max
|
| Ports List of port names (in same order as our 8-term macromodel)
Ports A_puref A_signal_pos A_pdref my_drive my_enable
Ports A_pcref A_gcref A_signal_neg my_ref
|
| D_to_A d_port   port1      port2    vlow vhigh trise tfall corner_nam
D_to_A   D_drive  my_drive   my_ref   0.0  3.3   0.5n  0.3n  Typ
D_to_A   D_drive  my_drive   my_ref   0.0  3.0   0.6n  0.3n  Min
D_to_A   D_drive  my_drive   my_ref   0.0  3.6   0.4n  0.3n  Max
|
[End External Model]
|
```



Example SPICE, Verilog-A(MS) or VHDL-A(MS) implementation of a true differential buffer

- Specify language as SPICE
- Specify the SPICE files that contain the subckts for the typ/min/max corners i.e., tdiff_rx.spc in this case;
- tdiff_rx.spc should contains the following subckts tdiff_rx_typ, tdiff_rx_min, and tdiff_rx_max
- Ports can be split on separate lines, but each line is a continuation for the previous one (in this case each subckt has 9 ports)
- Add the D/A or A/D statements (no need for D_enable and D_Drive conversion for input models)

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Example ….

```
.subckt tdiff_tx_typ 1 2 3 my_drive my_enable 6 7 8 my_ref
*  The terminals in an 8-terminal differential MacroModel are as follows:
*       power = 1
*       outp = 2
*       ground = 3
*       input = 4
*       enable = 5
*       power_clamp_reference = 6
*       ground_clamp_reference = 7
*       outn = 8

v1 my_ref 0 0
r1 my_enable 0 1e6
r2 my_drive my_ref 1e6

erx in 0 v='v(my_drive,my_ref)'
einv inv 0 v='v(1) - v(in)'

S1 in 2 inv 8 algorithm=default file=  diff_pkg.s4p

.ends
```

- The SPICE subckt tdiff_tx_typ for the typical corner in tdiff_tx.spc is as shown on the left. Min and Max similar.
- We need to connect the extra IBIS nodes inside the subckt to make sure there are no disconnected nodes in the circuit
- This is a simple pass-through driver that applies the “in” stimulus and its inverted pattern to the package input nodes
- The s-parameter file (diff_pkg.dat) for the package is referenced internally in the subckt and connects the in and inv stimulus to the I/O output nodes i.e. 2 and 8

Similar for Rx

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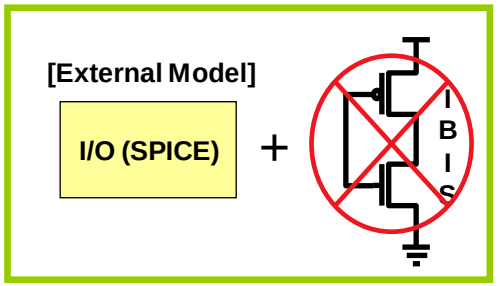
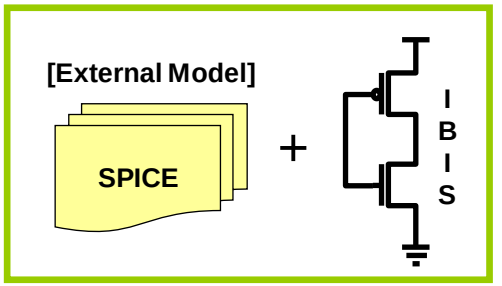
Simulate VI-VT model in conjunction with Spice

- Traditionally [External Model] keyword has been used for IO-buffer that needs to characterized as Spice IO in which case IBIS VI-VT data is not required.



- Extend use of [External Model] keyword to point to Spice sub-circuits that augment VI-VT data for complete characterization of IO-buffer.
  - Model On-DIE RDL parasitics using Spice or S-parameters that connect to Analog IO-buffer characterized as VI-VT data
  - Model DSP algorithm in Spice that works in conjunction with VI-VT data



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Simulate VI-VT model in conjunction with Spice

```
[External Model]
Language SPICE | SPARAM
Type Other
```

(VI-VT tables are required when Type is not I/O, Allowed Types are 'I/O' and 'Other', where 'Other' can be RDL, ODT, DSP, etc or any combination)

```
|corner        file_name                      circuit_name
 Typ           dsp.spc | dsp_typ.s4p          dsp_typ
 Min           dsp.spc | dsp_min.s4p          dsp_min
 Max           dsp.spc | dsp_max.s4p          dsp_max

| Ports List of port names (in same order as in SPICE | SPARAM)
Ports A_signal_pos A_signal_neg my_receive my_drive my_enable
Ports A_puref A_pdref A_pcref A_gcref A_extref my_ref A_gnd
```


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Dynamically switch sub-circuits to take care of corners and parametric variations.

[External Model]
Language SPICE

|corner	file_name	circuit_name	switch_param	switch_param_val
Typ	tdiff.spc	tdiff_txrx_typ	temp	50,100,150
Typ	tdiff.spc	tdiff_txrx_typ	freq	1,2,5
Min	tdiff.spc	tdiff_txrx_min	temp	-50,-100,-150
Max	tdiff.spc	tdiff_txrx_max	temp	70, 120, 200

Parameterized subcircuit selection

Allowed values with 1st as default

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Using AMI in conjunction with [External Model]

- Analog IO buffers in some cases could be modeled as s-parameters or as Spice sub-circuits. These models then work in conjunction with AMI code that represents DSP portion of IO-buffers. There could be even situations where IO-core itself becomes part of this AMI code.

- Hence we need to support AMI model simulation in absence of VI-VT data.
  - AMI model + Analog buffer represented as Spice-IO
  - AMI model + VI-VT Analog buffer + RDL (etc) in [External Model] (Case 1)
  - AMI model + Analog buffer represented as S-parameter-IO (Case 2)
  - AMI model (contains Analog-IO buffer coded as in AMI itself) + S-parameter/Spice RDL (Case 3)

```
[External Model]
Language SPARAM
Type I/O
```

(VI-VT tables are not required as S-Params represent the analog I/O buffer or RDL etc + I/O buffer)

```
|corner              file_name
 Typ                 io_typ.s4p
 Min                 io_min.s4p
 Max                 io_max.s4p

| Ports List of port names (in same order as in SPICE | SPARAM)
Ports A_signal_pos A_signal_neg my_receive my_drive my_enable
Ports A_puref A_pdref A_pcref A_gcref A_extref my_ref A_gnd
```


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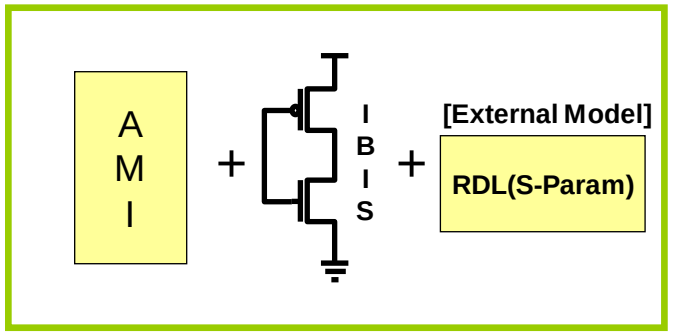
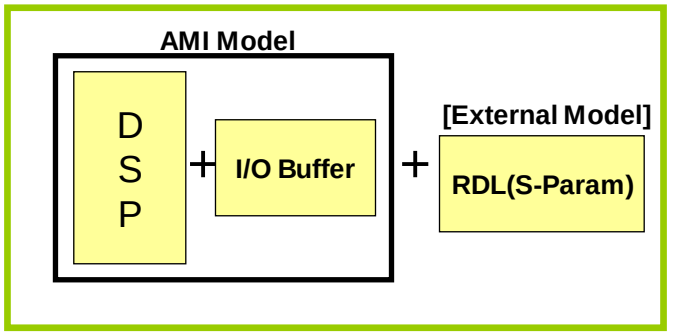
Using AMI in conjunction with [External Model]



Case 1

Case 2



Case 3

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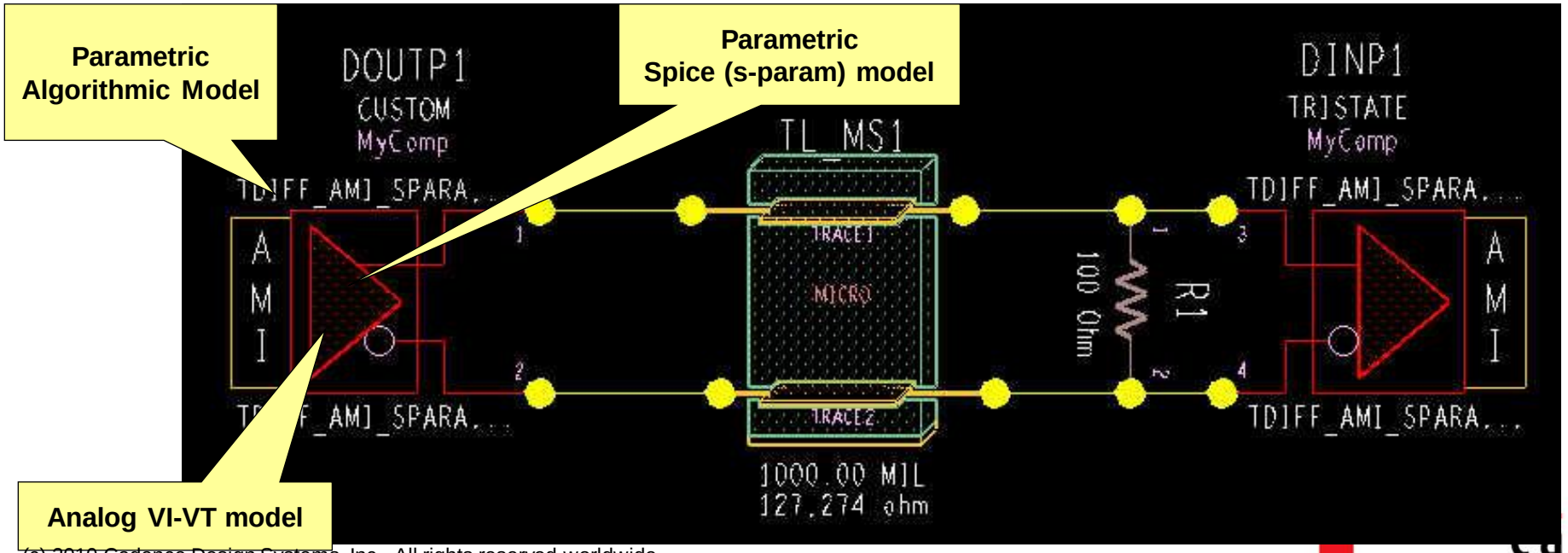
Summary

- Package parasitics can be modeled as SPICE using [External Model]; but we need to support S-parameters and it should be under proper keyword in Package-Section
- [External Model] has been traditionally used as alternate to VI-VT data; but we need to leverage it to use this model in conjunction with VI-VT
- [External Model] should support parameter switching to pick subcircuits dynamically
- AMI model today assumes analog-IO available as VI-VT; AMI model should work in conjunction with [External Model]



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