WELCOME FROM MICHAEL MIRMAK, INTEL CORPORATION

On behalf of the IBIS Open Forum, I would like to welcome you to the first Taipei Asian IBIS Summit. The IBIS Open Forum has long been aware of a significant and growing interest in signal and power integrity analysis here, and we are very happy to finally have an opportunity to meet and interact face-to-face. Our goal is to help build a healthy relationship between IBIS users and providers across the globe through technical exchanges. Summits like these help ensure that IBIS standards and solutions can keep pace with the needs of the IBIS community worldwide.

We are grateful to our generous co-sponsors for their assistance in making these events possible and hope that you will encourage them to continue their support as we plan for future summits here.

These Summits are simply one part of the IBIS Open Forum's ongoing activities. We host on-line discussions over our e-mail reflectors and during our teleconference meetings throughout the year. IBIS and the specifications it manages can only advance through the active involvement of its members and supporters worldwide. We invite and encourage your participation.

We hope that you enjoy the Summit and find the presentations and discussions useful. We wish you success.

Michael Mirmak
Chair, IBIS Open Forum

我謹代表IBIS開放論壇，歡迎您參加這次在台北舉行的亞洲IBIS技術研討會。 IBIS開放論壇的早已知道信號和電源完整性分析技術在這裡正在飛速的發展，我們非常高興終於有機會和大家見面和進行面對面的交流。我們的目標是在全球範圍內，通過技術的交流，從而建立一個完善的IBIS的使用者和提供者之間的關係。這次的技術研討會議將有助於確保IBIS的標準和解決方案能夠跟上全球技術發展的需求。

我們感謝各贊助單位對這個會議的經濟支持，並希望你們將來能繼續支持這個峰會的順利召開。

每年的IBIS峰會僅僅是IBIS開放論壇正在進行的活動的一部分。我們邀請各位能積極參與在我們的電子郵件論壇和電話會議上討論。 IBIS開放論壇和其規範的發展依賴於全世界的工程師在信號和電源完整性的積極參與。

我們希望您能從此次峰會中發現有用的資料和討論。祝大家成功。

馬夢寬
IBIS峰會主席

WELCOME FROM SOGO HSU, FOXCONN TECHNOLOGY GROUP

Welcome to the sixth annual Asian IBIS Summit in Taipei. On behalf of the Foxconn SRDTDC (Server Research and Development Technical Development Committee), it is such an honor to express my deepest appreciation to the IBIS group and the co-sponsors for making this event so successful.

Greater China is the most populous continent in the world, which implies there are many emerging opportunities for technological industries. Since the first Asian IBIS summit meeting back in 2005, this summit has been gathering signal integrity experts and engineers to discuss signal integrity and related technical issues.

As a dominant ODM supplier in server and/or storage product design, Foxconn Technology Group continues to pay close attention to well construction of IBIS standards and related the technical directions, to ensure delivery of high-reliability products. It is encouraging for us to share a topic during the meeting this year about **Enforcement Passivity of S-parameter Sampled Frequency Data**. We hope that the topic will be inspiring, and we also sincerely welcome all your feedback and technical suggestions.

We trust that all the invited members today will find today's meeting to be a rewarding journey.

ShouKuo Sogo Hsu, Ph. D.
Foxconn Technology Group

歡迎參加第六屆台北舉辦之亞洲IBIS開放論壇。在此，謹代表鴻海科技集團伺服器研發技委會，很榮幸能夠對於IBIS協會組織以及各贊助單位，對此次論壇能成功舉行敬致謝忱。

大中華區已然成為全球人口最稠密之區域，而這也意味著對於科技產業的許多新興機會。自 2005 年，亞洲IBIS開放論壇持續每年聚集各界訊號完整性專家以及工程人員一齊探討相關議題。

做為伺服器/儲存器領域的主要 ODM 供應商，鴻海科技集團持續投注心力關注於 IBIS 標準以及科技發展方向，以確保提供高可靠度之產品。很榮幸能夠在今年度會議中，受邀與大家分享有關**散射參數之無源性強制法**之主題。我們冀盼藉由此題目之鼓舞，拋磚引玉，得到來自各位先進之迴響與技術建議。

相信今天的開放論壇議程，會讓各位與會先進，有一趟豐收之旅程。

許壽國 博士
鴻海科技集團

AGENDA AND ORDER OF PRESENTATIONS

(The actual agenda might be modified)

I B I S   S U M M I T   M E E T I N G   A G E N D A

8:15 REFRESHMENTS & SIGN IN
- Vendor Tables Open at 8:30

9:00 Welcome
- Sogo Hsu (Foxconn Technology Group)
- Michael Mirmak (Chair IBIS Open Forum, Intel Corporation)

9:20 **Introducing IBIS 5**
Michael Mirmak (Intel Corporation)

9:35 **Point Reduction Method for IBIS Curves 9**
Lance Wang (IO Methodology)

10:05 BREAK (Refreshments and Vendor Tables)

10:25 **IBIS for SSO Analysis 19**
Haisan Wang, Joshua Luo, Jack Lin, and Zhangmin Zhong (Sigrity)

11:05 **Correlating C_pin Capacitance with Measurements 33**
Randy Wolff (Micron Technology)

11:30 **Enforced Passivity of S-parameter Sampled Frequency Data 41**
Wenliang Tseng, Sogo Hsu, Frank Y.C. Pai, and Scott C.S. Li (Foxconn Technology Group)

12:00 FREE BUFFET LUNCH (Hosted by Sponsors)
- Vendor Tables

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

13:30 **Automated AMI Model Generation & Validaton 51**
Jose Luis Pino*, Amolak Badesha*, Manuel Luschas**,
Antonis Orphanou**; and Halil Civit**
(*Agilent Technologies and **NetLogic Microsystems)

14:10 **Extending/Leveraging IBIS Constructs to Model High-Speed 65**
I/Os and Packages using AMI, Spice, and S-Parameters
John Lin*, Feras Al-Hawari**, Taranjit Kukal**, and
Ambrish Varma** (*Flextronic and **Cadence Design Systems)

14:40 BREAK (Refreshments and Vendor Tables)

15:00 **IBIS-ISS: What Is It and What It Means to You 77**
Michael Mirmak (Intel Corporation)

15:30 **Model Connection Protocol Extensions for Mixed Signal SiP 83**
Taranjit Kukal*, Wenliang Dai*, Brad Brim**, and
Eiji Fujine*** (*Cadence Design Systems, **Sigrity,
and ***Fujitsu VLSI Limited)

16:00 Concluding Items

16:30 END OF IBIS SUMMIT MEETING

Introducing IBIS

Michael Mirmak 馬夢寬
Intel Corporation 英特爾公司
Chair, IBIS Open Forum IBIS 委員會主席

Asian IBIS Summit Taipei 台北 IBIS 技術研討會
November 12, 2010 2010 年 11 月 12 日

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Agenda

- IBIS – A Review
- Specifications and Technologies
- How Changes Are Made
- How to Get Involved
- References

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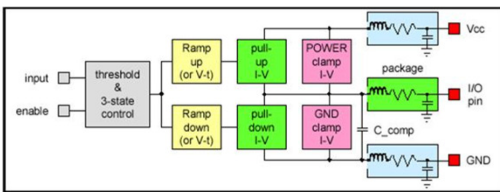
IBIS – A Review

- IBIS – I/O Buffer Information Specification, Ver. 5.0
  - Standardized as ANSI/EIA* 656-B, IEC* 62014
  - Managed by the IBIS Open Forum
  - Originally analog: resistance, transition speed, capacitance
  - Package modeling included in early revisions



- Extended in recent years
  - AMS: Verilog-A, Verilog-AMS, VHDL-AMS support
  - AMI: Algorithmic Modeling Interface for advanced SerDes

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Specifications and Technologies

- IBISCHK5: Free IBIS Syntax Checker and Parser
  - www.eda.org/ibis/ibischk5/
- IBIS Quality Specification
  - Defines a structured rating system for IBIS models
- Touchstone 2.0
  - Network parameter descriptions (e.g., S-parameters)
- IBIS Interconnect Modeling (ICM) Specification
  - Generic transmission line modeling format
  - Also links to S-parameters through Touchstone

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How Changes Are Made

- BIRDs: Buffer Issue Resolution Documents
  - Change proposals for the IBIS specification
  - Submitted by individuals or Task Groups
  - If approved by IBIS Open Forum, included in future IBIS specification versions
- BUGs: IBIS Parser issues
  - Violations of the specification, unexpected behaviors or requests for improvement
  - Usually submitted by individuals
- TSIRDs: Touchstone Issue Resolution Documents
  - Similar to BIRDs, but for Touchstone 2.0

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How to Get Involved

- E-mail Reflectors – Discussion welcome!
  - ibis@eda.org for administration and change updates
  - ibis-users@eda.org for usage questions
  - To subscribe, write to ibis-info@eda.org
- IBIS Open Forum teleconferences every 3 weeks
- Task Groups
  - Advanced Technology Modeling
  - Model Review (EDA vendors)
  - Interconnect
  - Quality

Your participation helps IBIS provide the standard, unified solutions needed by industry!

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References

- IBIS Web site: www.eda.org/ibis/
  - Links to Task Groups available there
- Specifications
  - IBIS 5.0: www.eda.org/ibis/ver5.0/
  - Touchstone: www.eda.org/ibis/touchstone_ver2.0/
  - ICM: www.eda.org/ibis/icm_ver1.1/
- BIRDs
  - www.eda.org/ibis/birds/
- IBIS 4.0 Cookbook
  - www.eda.org/ibis/cookbook/
- Training
  - www.eda.org/ibis/training/

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Point Reduction Method for IBIS Curves

Lance Wang
lwang@iometh.com
Asian (China) IBIS Summit
Taipei, Nov. 12, 2010

(Presented previously at the IBIS Summit on November 9, 2010)

Outline

- Point Reduction Introduction
- “Greatest Change” method
- Issue with “Greatest Change” method for IBIS curve representation
- The “Weighted Best Point” (WBP) method
- Conclusions

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Point Reduction Introduction

- What is Point Reduction method for?
  - In some situations, a set of data (e.g. waveform) can not satisfy a specification (e.g. IBIS) data limit without sacrifice of its accuracy. For an example, 10,000 extracted I-V curve data points for only 100 point limit in IBIS specification.
  - Point Reduction method intends to use algorithms for proper point number reduction with minimum sacrifices on its accuracy. It is about accurate representation of whole data set with limited data points
- IBIS Cookbook introduces two methods:
  - Points selected using a regular interval
  - Points selected using “greatest change” algorithm

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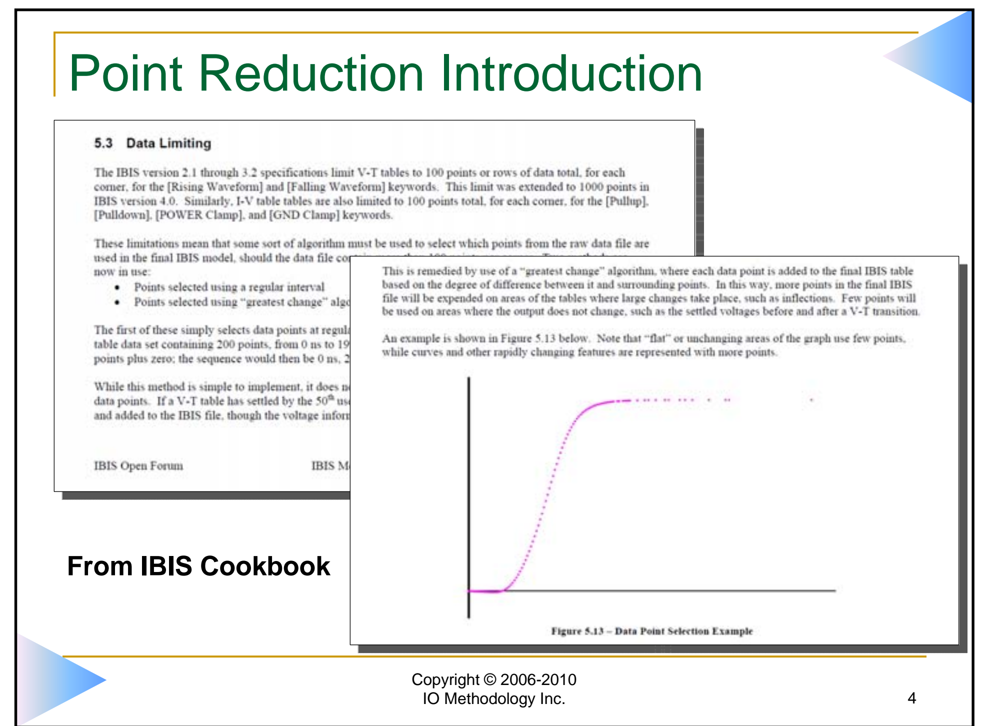

5.3 Data Limiting

The IBIS version 2.1 through 3.2 specifications limit V-T tables to 100 points or rows of data total, for each corner, for the [Rising Waveform] and [Falling Waveform] keywords. This limit was extended to 1000 points in IBIS version 4.0. Similarly, I-V table tables are also limited to 100 points total, for each corner, for the [Pullup], [Pulldown], [POWER Clamp], and [GND Clamp] keywords.

These limitations mean that some sort of algorithm must be used to select which points from the raw data file are used in the final IBIS model, should the data file co… now in use:

- Points selected using a regular interval
- Points selected using “greatest change” alg…

The first of these simply selects data points at regul… table data set containing 200 points, from 0 ns to 19… points plus zero; the sequence would then be 0 ns, 2…

While this method is simple to implement, it does n… data points. If a V-T table has settled by the 50th us… and added to the IBIS file, though the voltage infor…

IBIS Open Forum IBIS M…

This is remedied by use of a “greatest change” algorithm, where each data point is added to the final IBIS table based on the degree of difference between it and surrounding points. In this way, more points in the final IBIS file will be expended on areas of the tables where large changes take place, such as inflections. Few points will be used on areas where the output does not change, such as the settled voltages before and after a V-T transition.

An example is shown in Figure 5.13 below. Note that “flat” or unchanging areas of the graph use few points, while curves and other rapidly changing features are represented with more points.

Figure 5.13 – Data Point Selection Example

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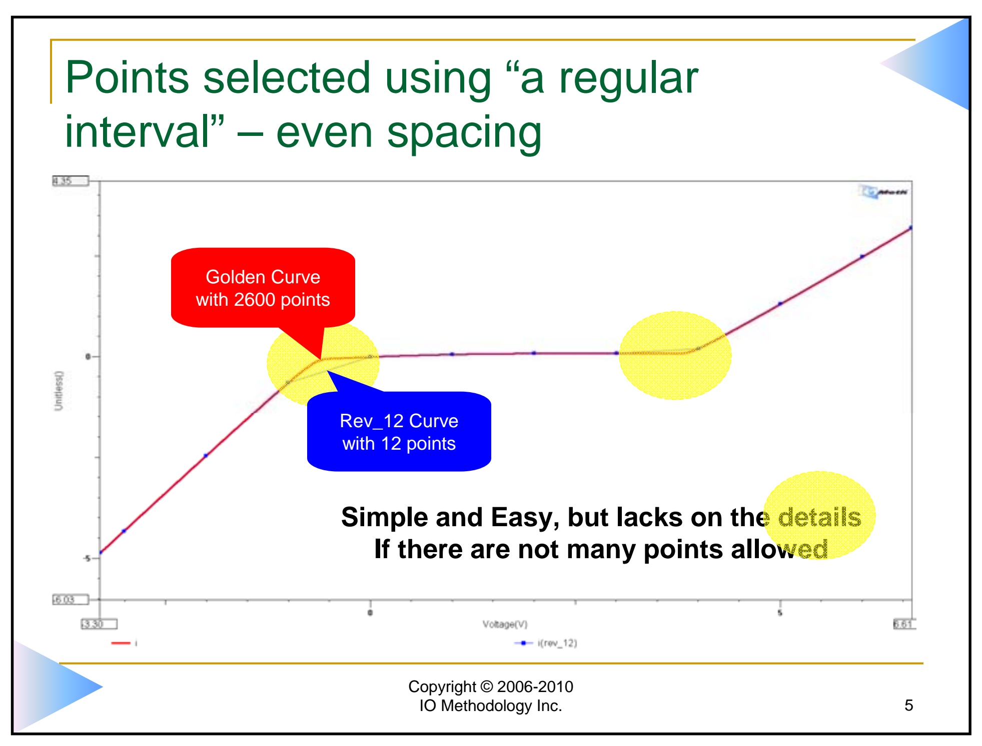
Points selected using "a regular interval" – even spacing
Golden Curve with 2600 points
Rev_12 Curve with 12 points
Simple and Easy, but lacks on the details
If there are not many points allowed
Voltage(V)
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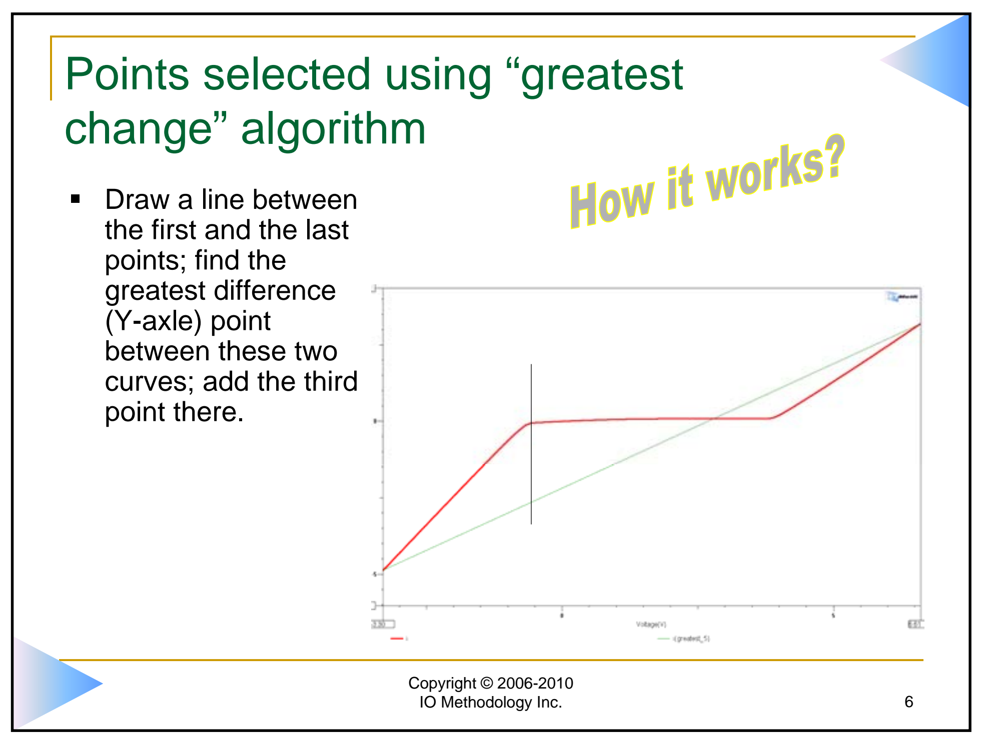
5


Points selected using "greatest change" algorithm
Draw a line between the first and the last points; find the greatest difference (Y-axle) point between these two curves; add the third point there.
How it works?
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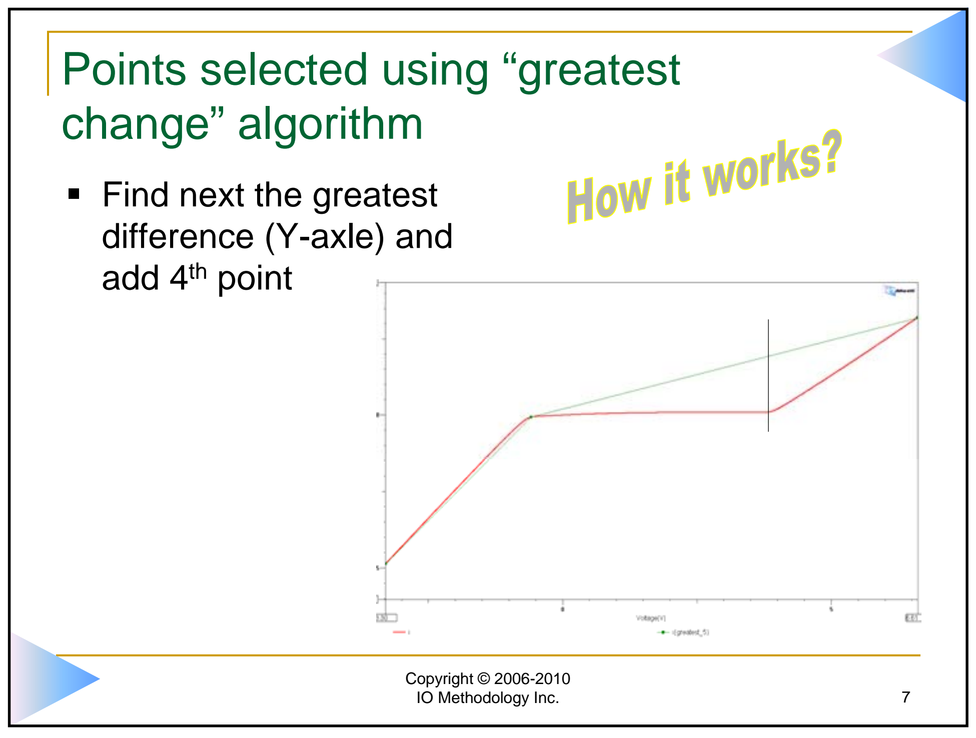
Points selected using "greatest change" algorithm
Find next the greatest difference (Y-axle) and add 4th point
How it works?
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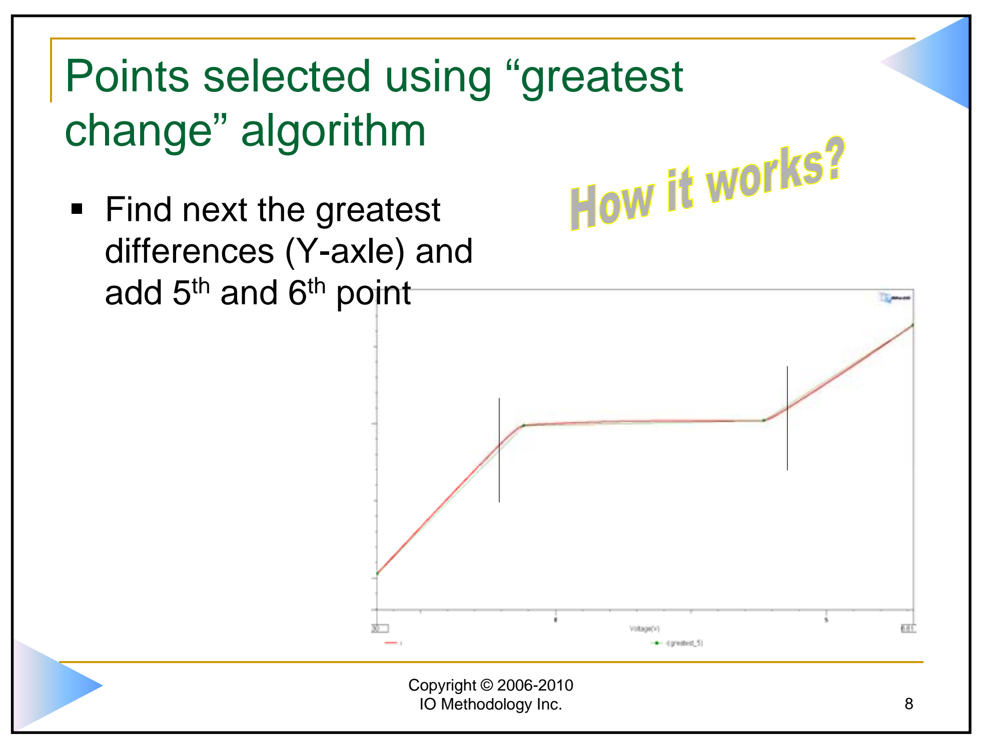
7


Points selected using "greatest change" algorithm
Find next the greatest differences (Y-axle) and add 5th and 6th point
How it works?
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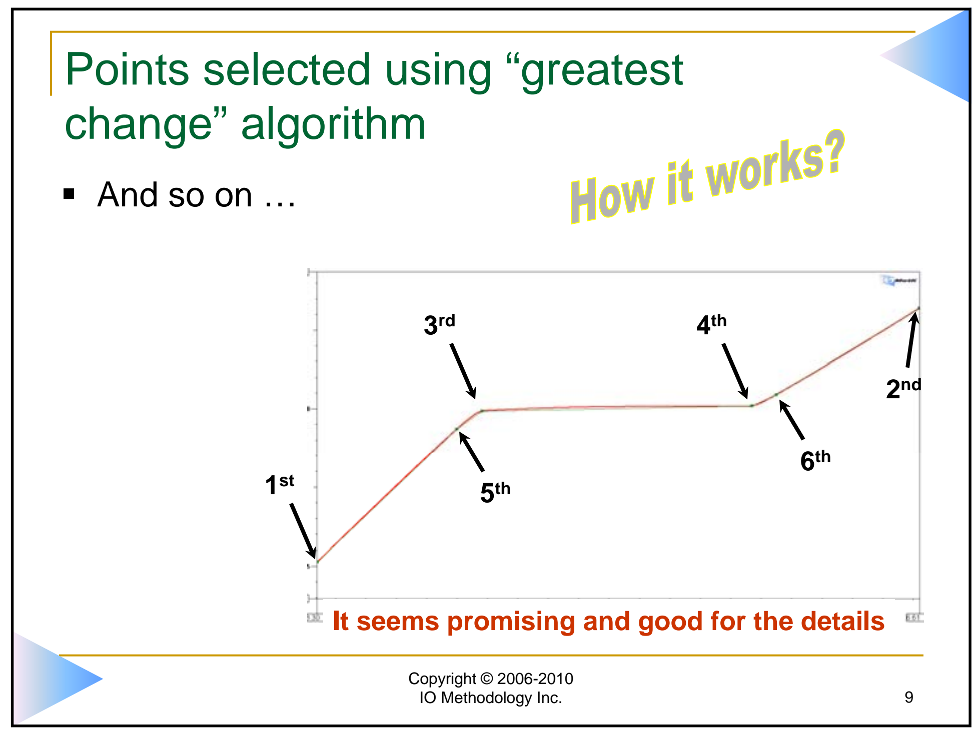
8


Points selected using "greatest change" algorithm
And so on …
How it works?
1st
2nd
3rd
4th
5th
6th
It seems promising and good for the details
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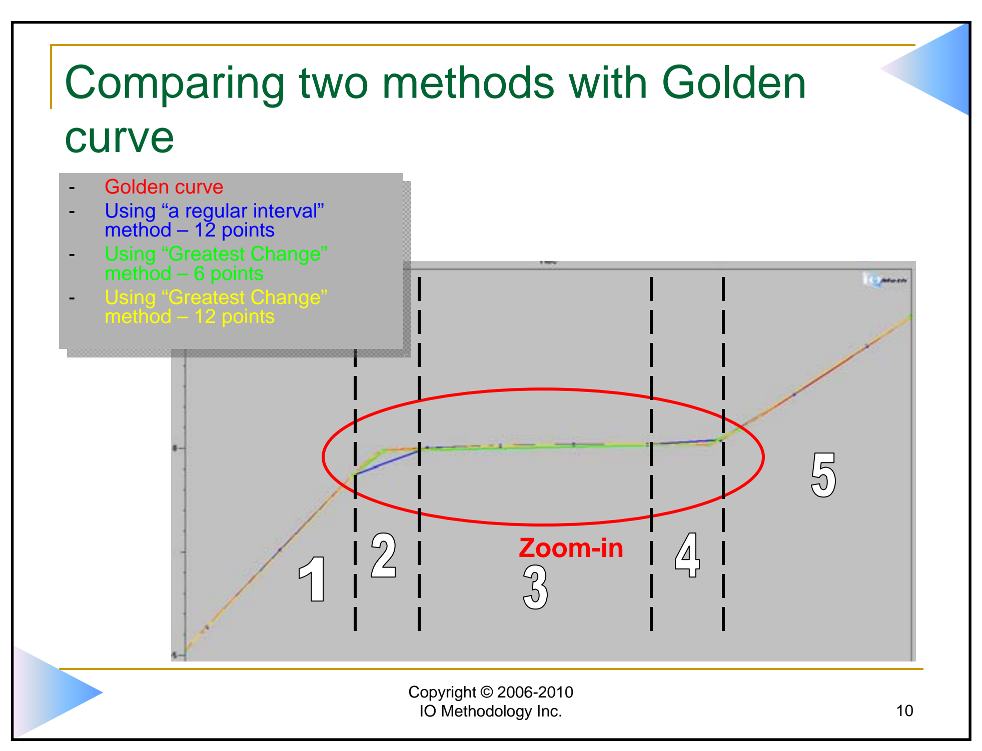
9


Comparing two methods with Golden curve
- Golden curve
- Using "a regular interval" method – 12 points
- Using "Greatest Change" method – 6 points
- Using "Greatest Change" method – 12 points
1
2
Zoom-in
3
4
5
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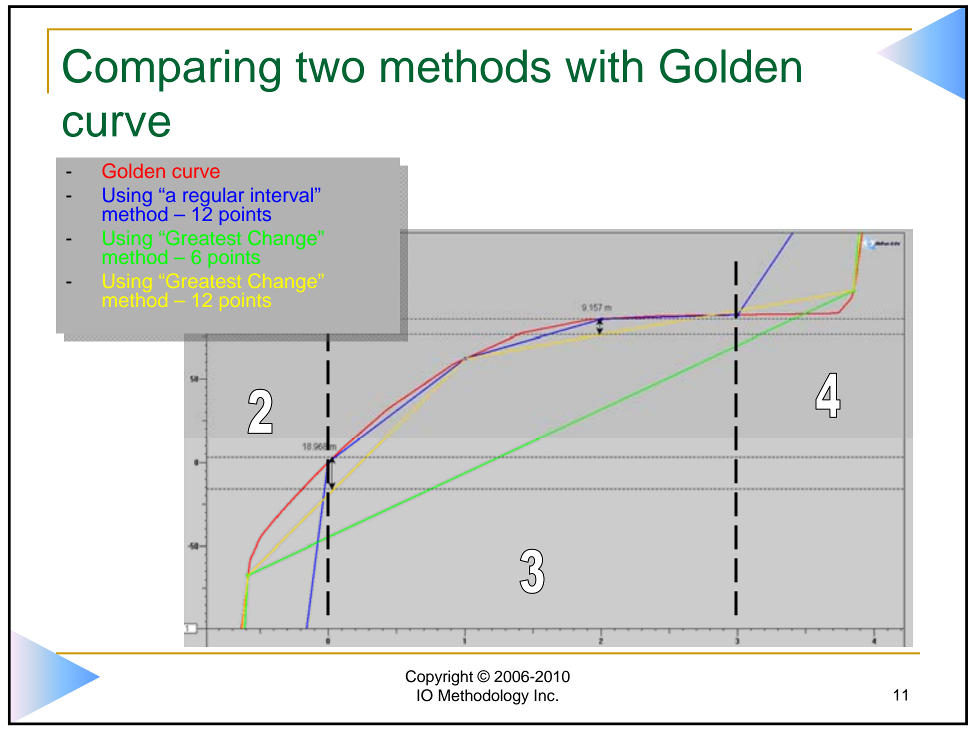
10



Comparing two methods with Golden curve

- We got:
  - "a regular interval" method – even spacing
    - ➢ Simple and easy
    - ➢ Lack on the details
    - ➢ Accuracy is highly depended on space/point numbers
  - "greatest change algorithm" method
    - ➢ Higher accuracy on average
    - ➢ Good on the details
    - ➢ May have "too few" points in the certain areas and it could compacts the results of simulations

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Issue with “Greatest Change” method for IBIS curve representation

- The most of IBIS generation tools are using “Greatest Change” algorithm (so called “Best Point” too) now.
- It works fine with IBIS VT curve point reduction
  - The big part of reason is that VT curves are co-factor in simulation calculations. More details are better.
- Sometimes it causes inaccurate simulation result due to too few points in the working range in the IV curves

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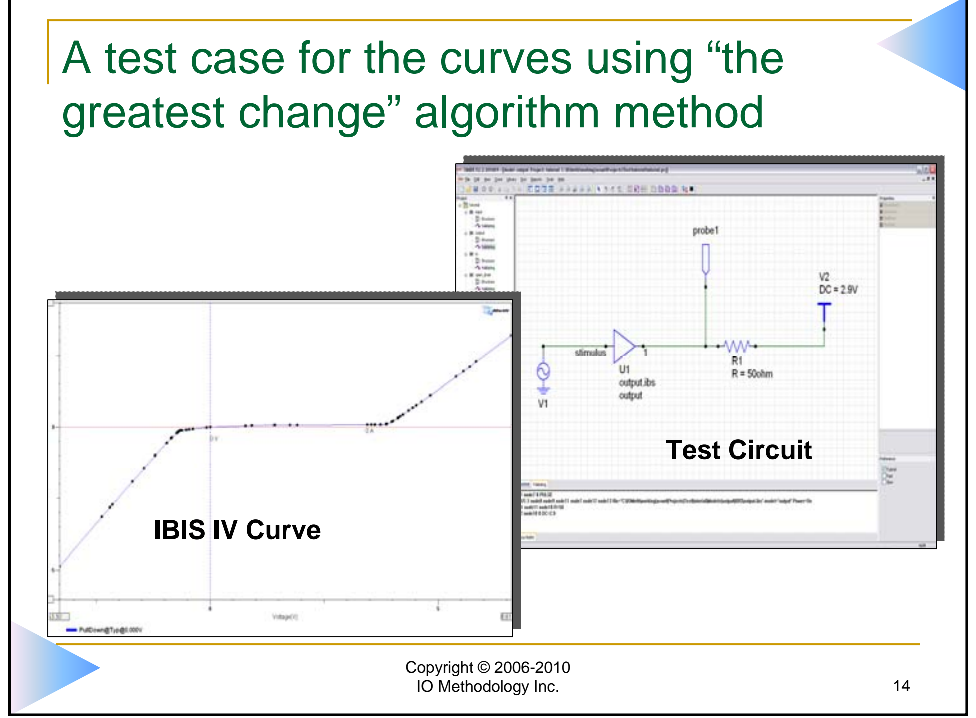
A test case for the curves using “the greatest change” algorithm method



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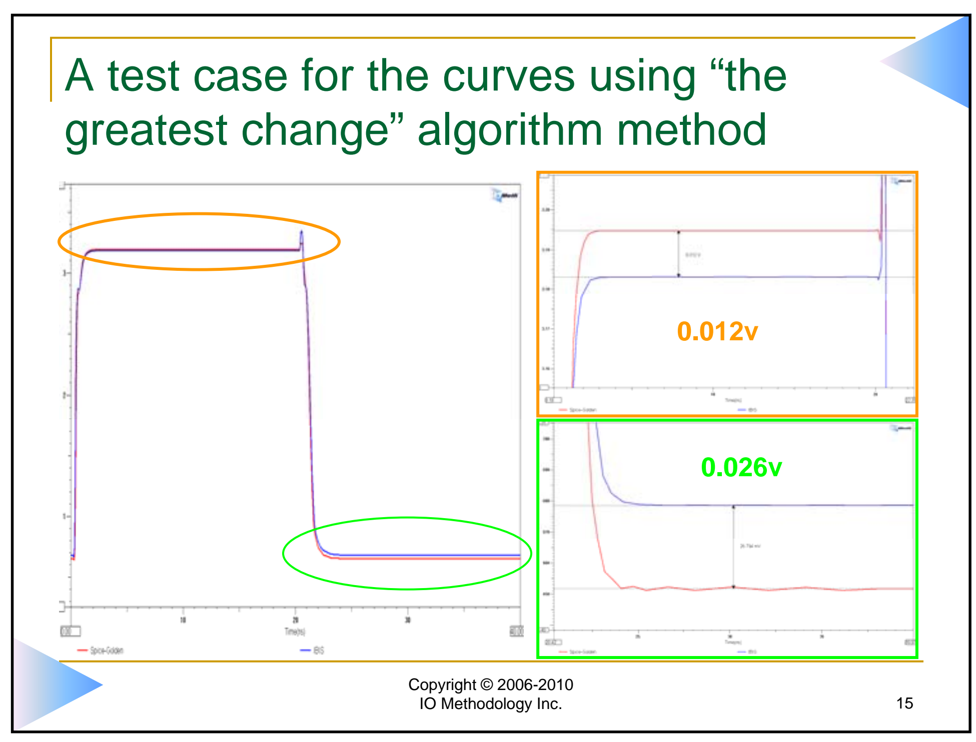
A test case for the curves using "the greatest change" algorithm method
0.012v
0.026v
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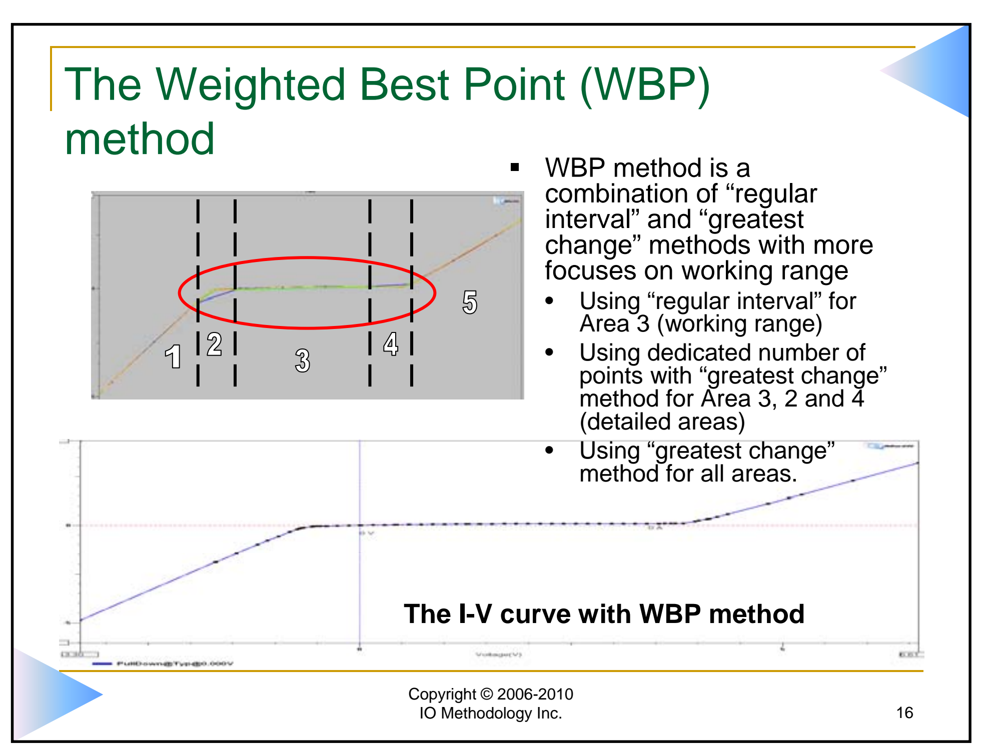
15


The Weighted Best Point (WBP) method
1
2
3
4
5
WBP method is a combination of "regular interval" and "greatest change" methods with more focuses on working range
Using "regular interval" for Area 3 (working range)
Using dedicated number of points with "greatest change" method for Area 3, 2 and 4 (detailed areas)
Using "greatest change" method for all areas.
The I-V curve with WBP method
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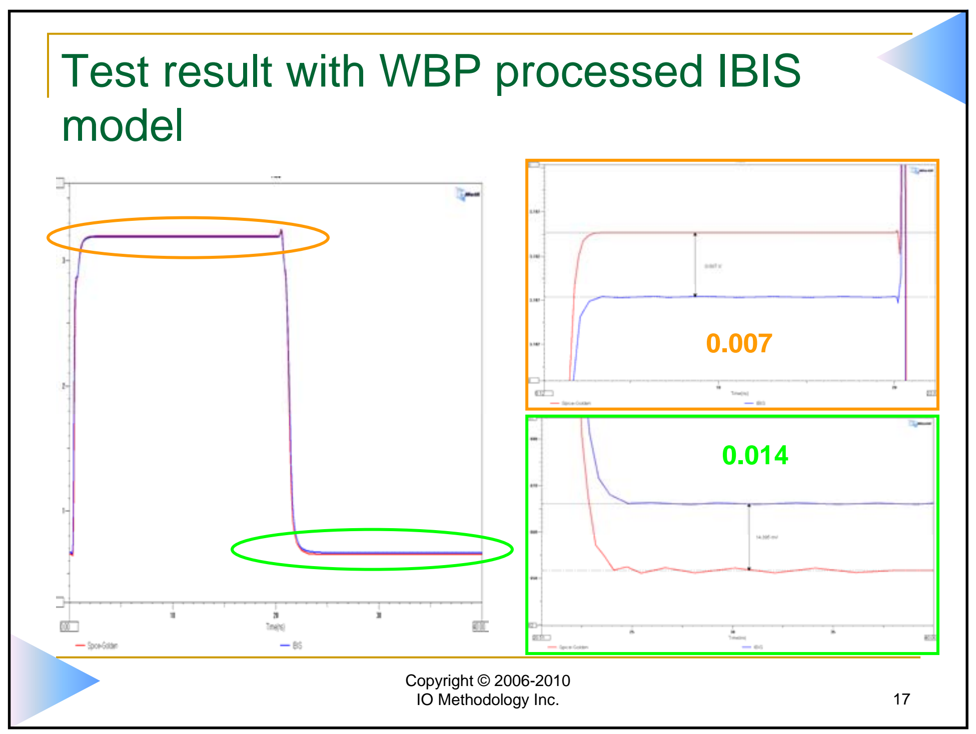

Conclusion

- Point Reduction method is needed for buffer I-V and V-T curve representations in IBIS format
- Both "Regular Interval" and "Greatest Change" algorithm methods have strong and weak areas
- WBP method combined both methods with focused areas. It improves the accuracy in IBIS simulations.
  - It is more effective for low-level signal buffer models

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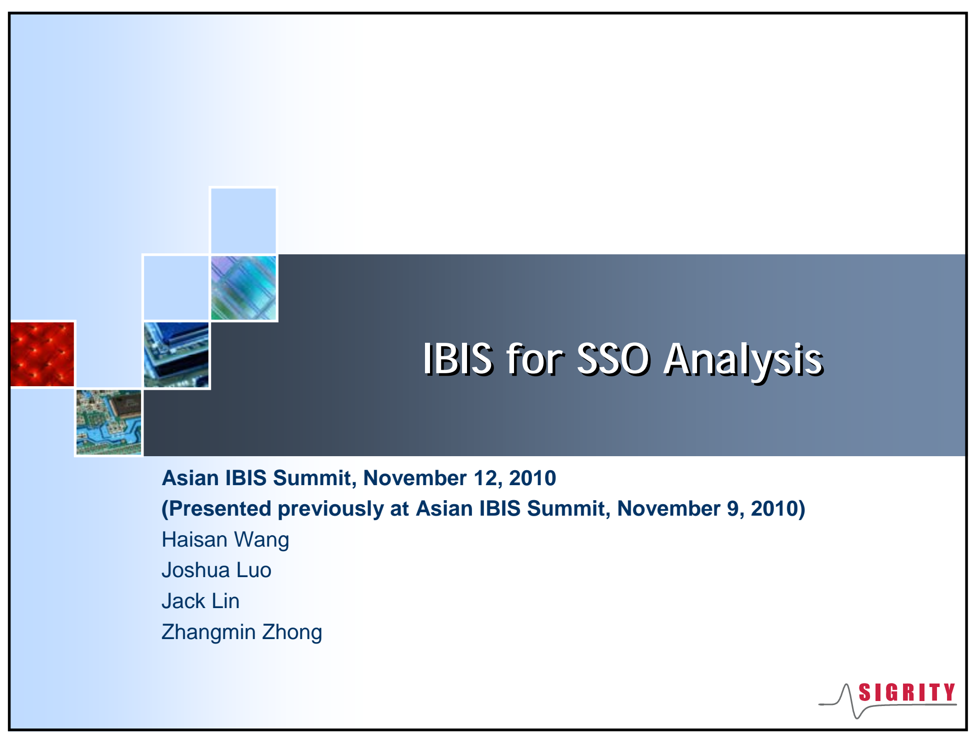
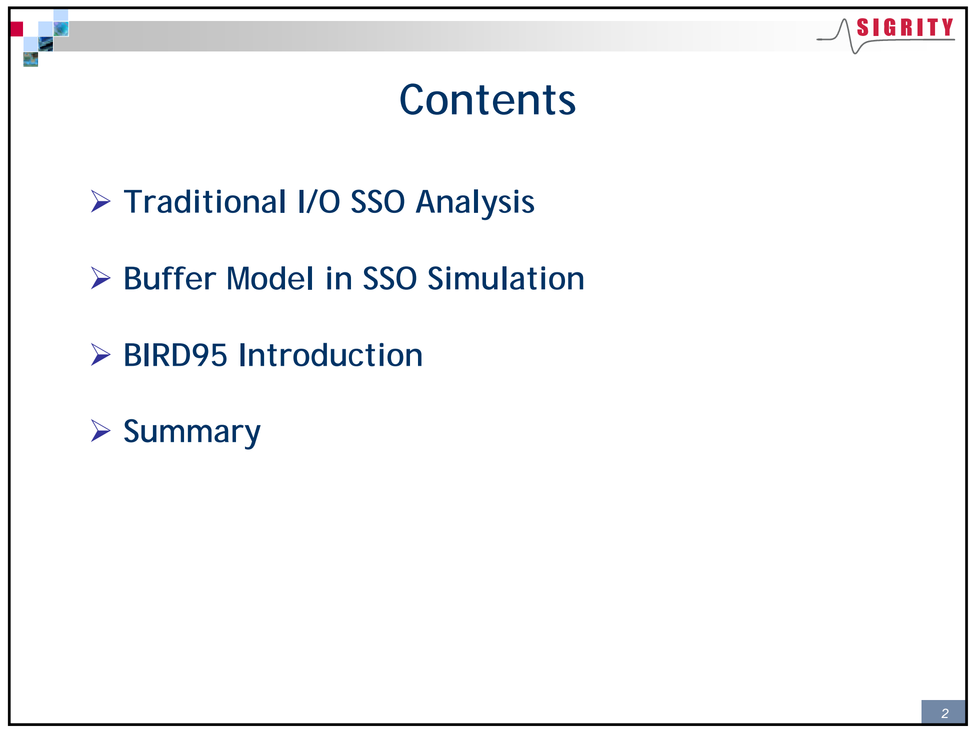
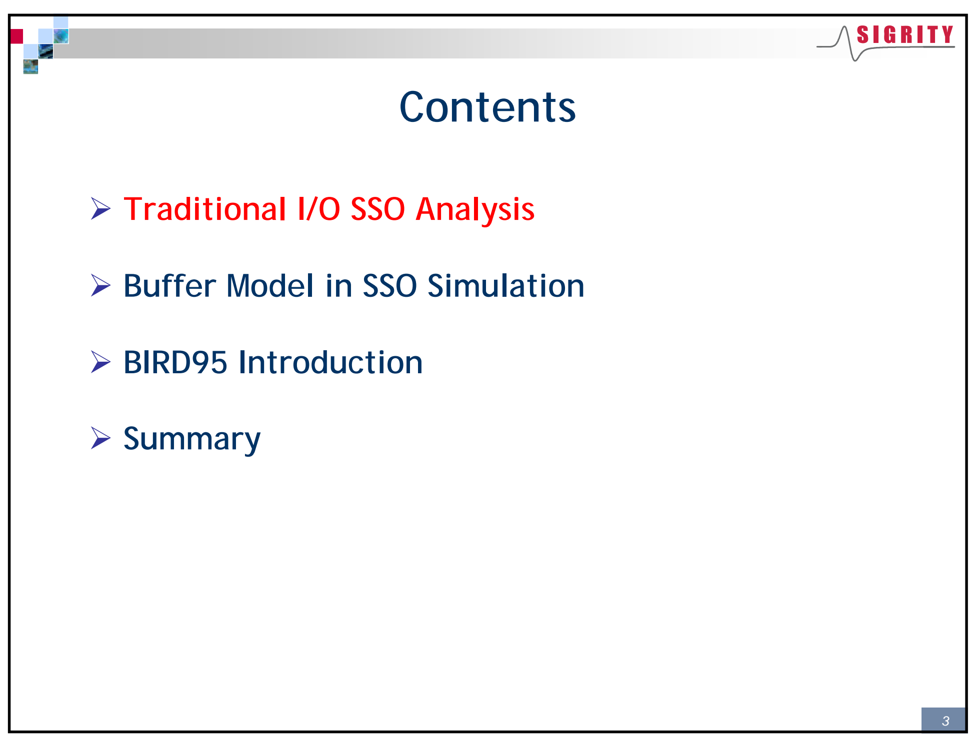

IBIS for SSO Analysis
Asian IBIS Summit, November 12, 2010
(Presented previously at Asian IBIS Summit, November 9, 2010)
Haisan Wang
Joshua Luo
Jack Lin
Zhangmin Zhong
SIGRITY


SIGRITY
Contents
Traditional I/O SSO Analysis
Buffer Model in SSO Simulation
BIRD95 Introduction
Summary
2


SIGRITY
Contents
Traditional I/O SSO Analysis
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BIRD95 Introduction
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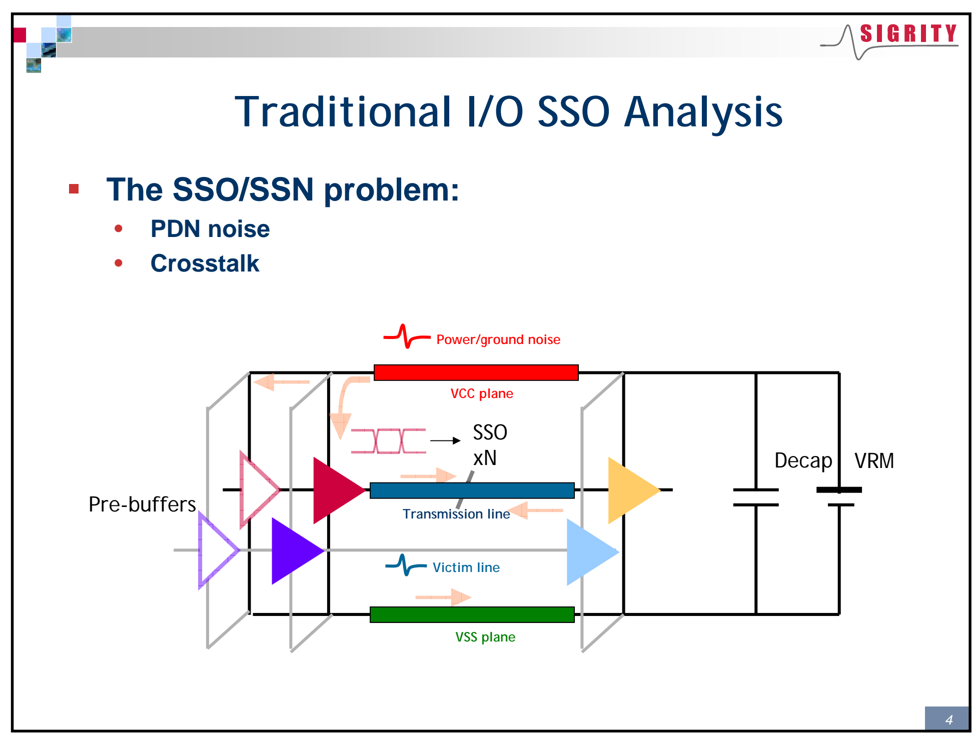
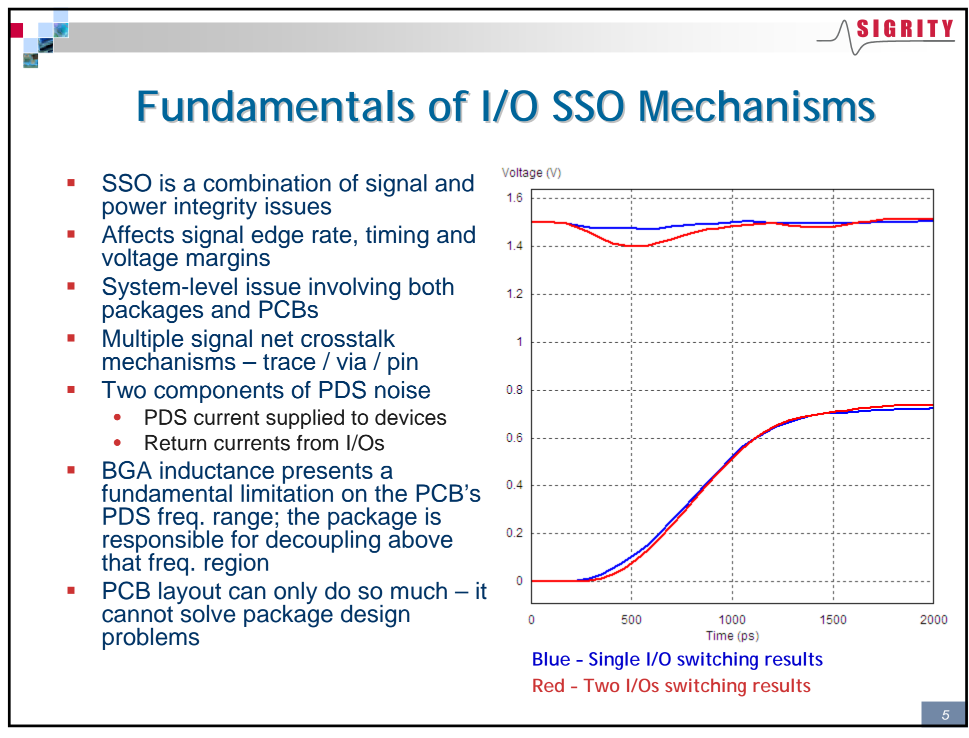
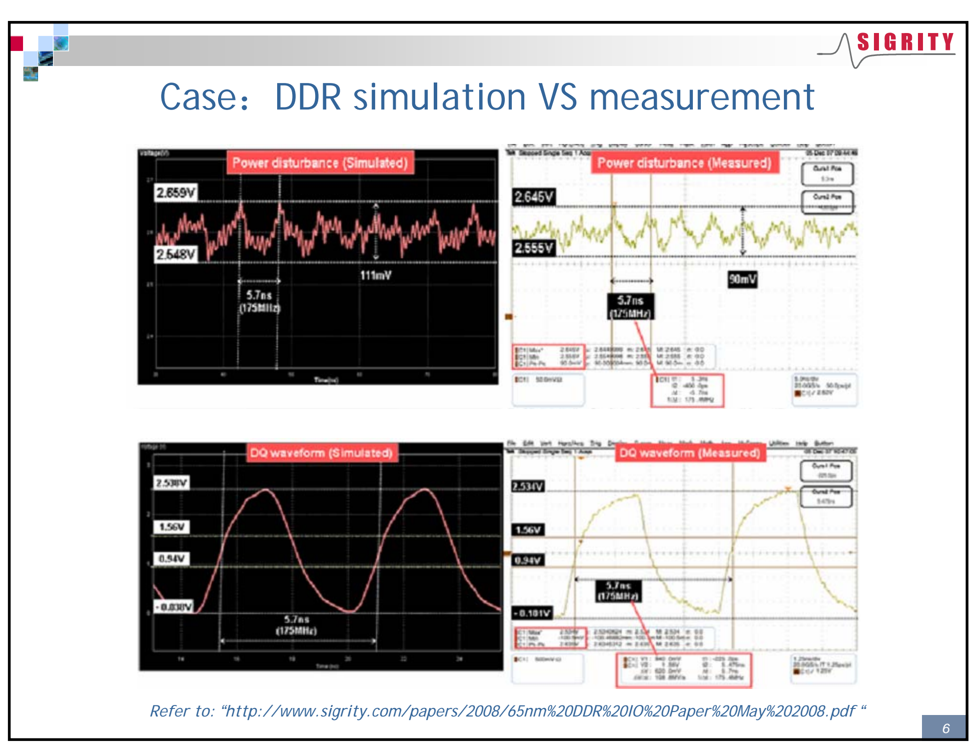
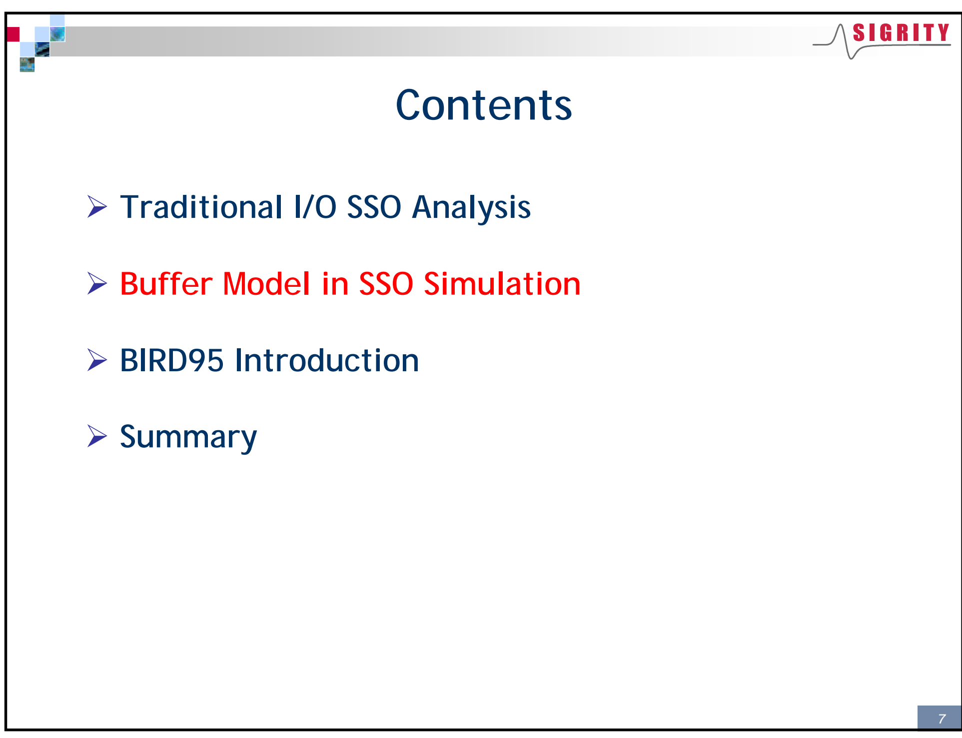
3


SIGRITY
Traditional I/O SSO Analysis
The SSO/SSN problem:
PDN noise
Crosstalk
Power/ground noise
VCC plane
SSO
xN
Decap
VRM
Pre-buffers
Transmission line
Victim line
VSS plane
4


SIGRITY
Fundamentals of I/O SSO Mechanisms
SSO is a combination of signal and power integrity issues
Affects signal edge rate, timing and voltage margins
System-level issue involving both packages and PCBs
Multiple signal net crosstalk mechanisms – trace / via / pin
Two components of PDS noise
PDS current supplied to devices
Return currents from I/Os
BGA inductance presents a fundamental limitation on the PCB's PDS freq. range; the package is responsible for decoupling above that freq. region
PCB layout can only do so much – it cannot solve package design problems
Voltage (V)
Time (ps)
Blue - Single I/O switching results
Red - Two I/Os switching results
5


SIGRITY
Case：DDR simulation VS measurement
Power disturbance (Simulated)
Power disturbance (Measured)
2.659V
2.548V
111mV
5.7ns (175MHz)
2.645V
2.555V
90mV
DQ waveform (Simulated)
DQ waveform (Measured)
2.530V
1.56V
0.94V
-0.830V
2.534V
-0.181V
Refer to: "http://www.sigrity.com/papers/2008/65nm%20DDR%20IO%20Paper%20May%202008.pdf "
6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Summary
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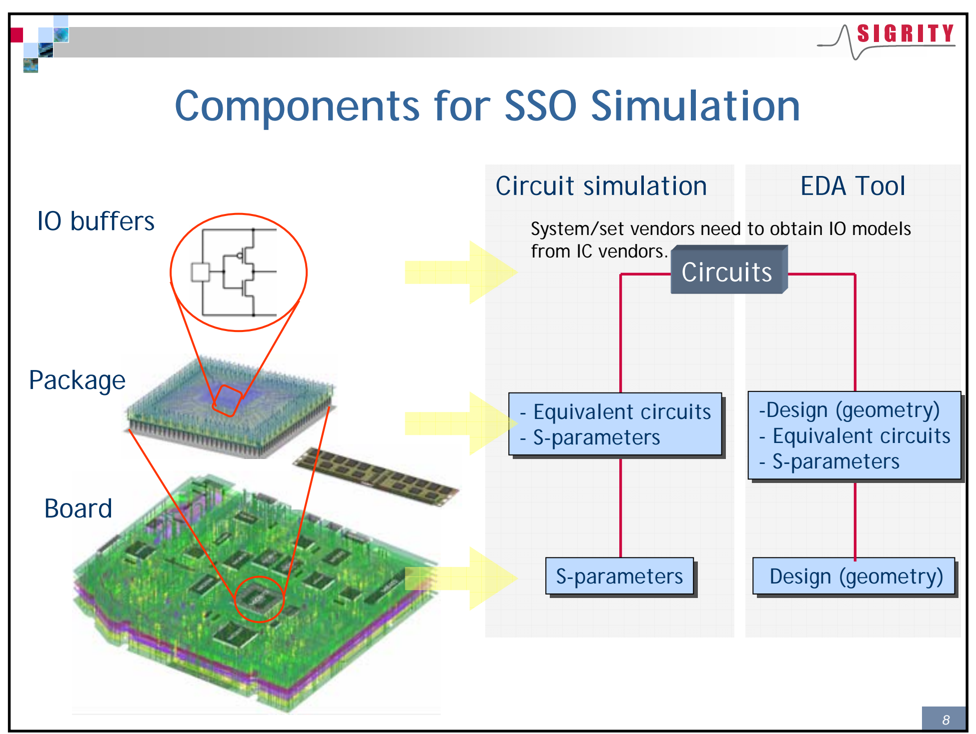
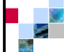

SIGRITY
Components for SSO Simulation
IO buffers
Package
Board
Circuit simulation
EDA Tool
System/set vendors need to obtain IO models from IC vendors.
Circuits
- Equivalent circuits
- S-parameters
-Design (geometry)
- Equivalent circuits
- S-parameters
S-parameters
Design (geometry)
8

Trade-off in IO buffer model

	SPICE transistor level model	IBIS model
Contents	▪ Detailed circuits and netlists ▪ Device library, parameters ▪ Related deign information	▪ I-V/V-T for the final stage ▪ Pin information
Accuracy	Very good	▪ Good for SI ▪ ? for PI
Format	▪ Usually, encrypted for outside IC vendors. ▪ Usually, NDA is necessary.	▪ Text file ▪ Open format
Simulation time	Typically, several to 10 times slower than IBIS	Much faster than SPICE model
EDA tools Utilization	Specific simulator is necessary for encrypted models	Many SI/PI tools support.

There may be some other choices, such as the current mirror circuit or VCR

9



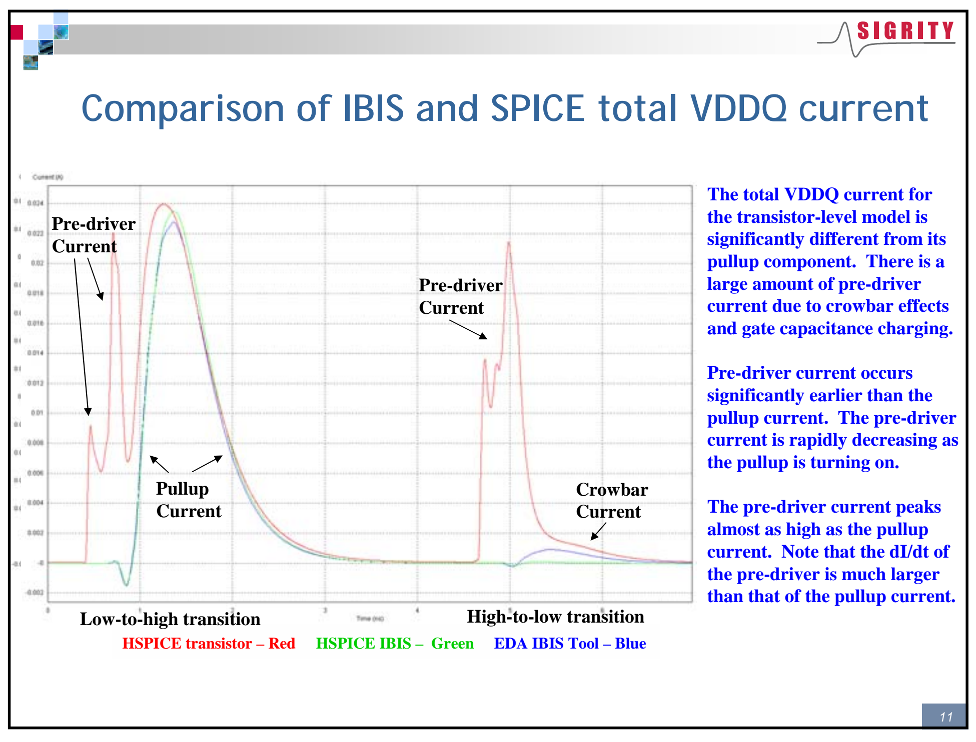
Requirements in SSO Simulation

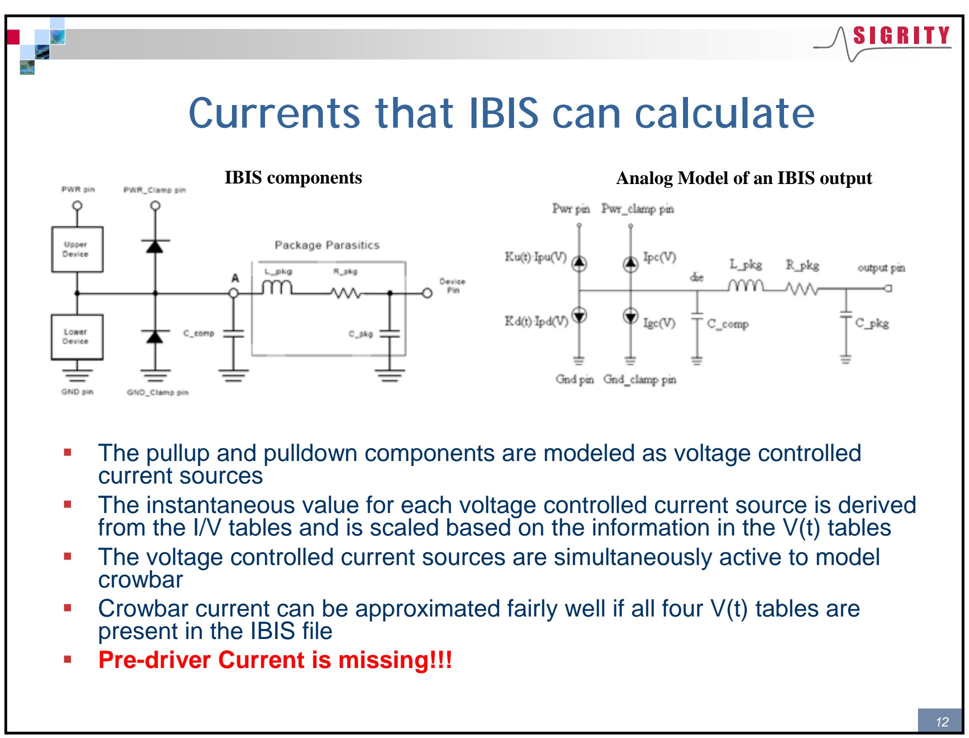
- Easy setup
  - Hope to eliminate painful manual work
- Fast runtime
  - Want to test various conditions (corners, stimulus, …)
  - Want to promptly reflect package/board design change

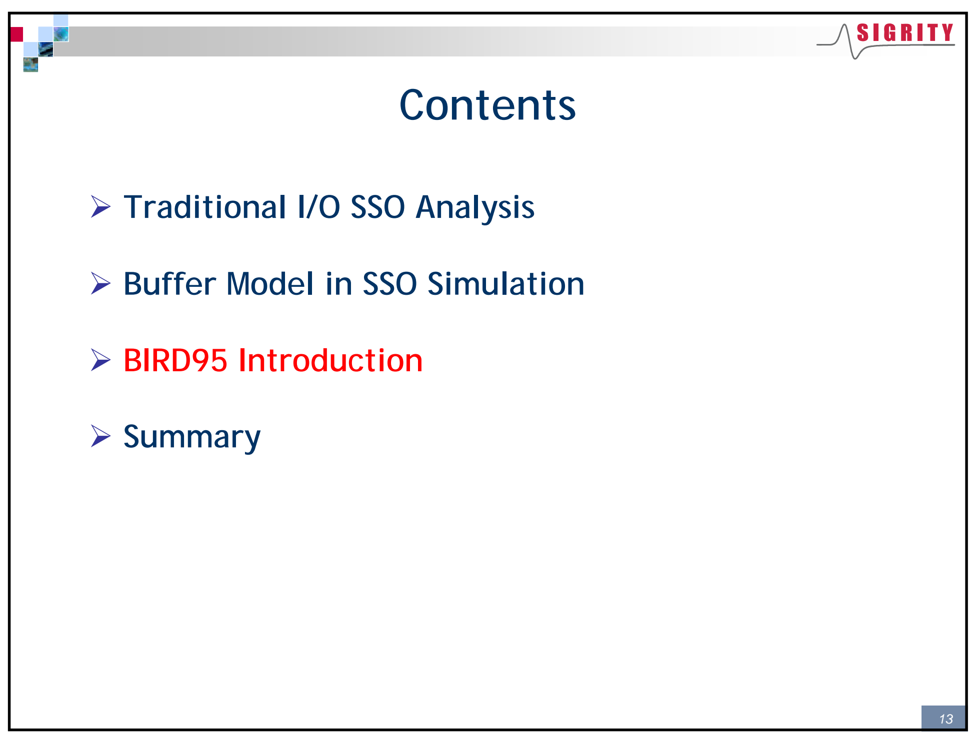
→ SPICE transistor model may not fit.

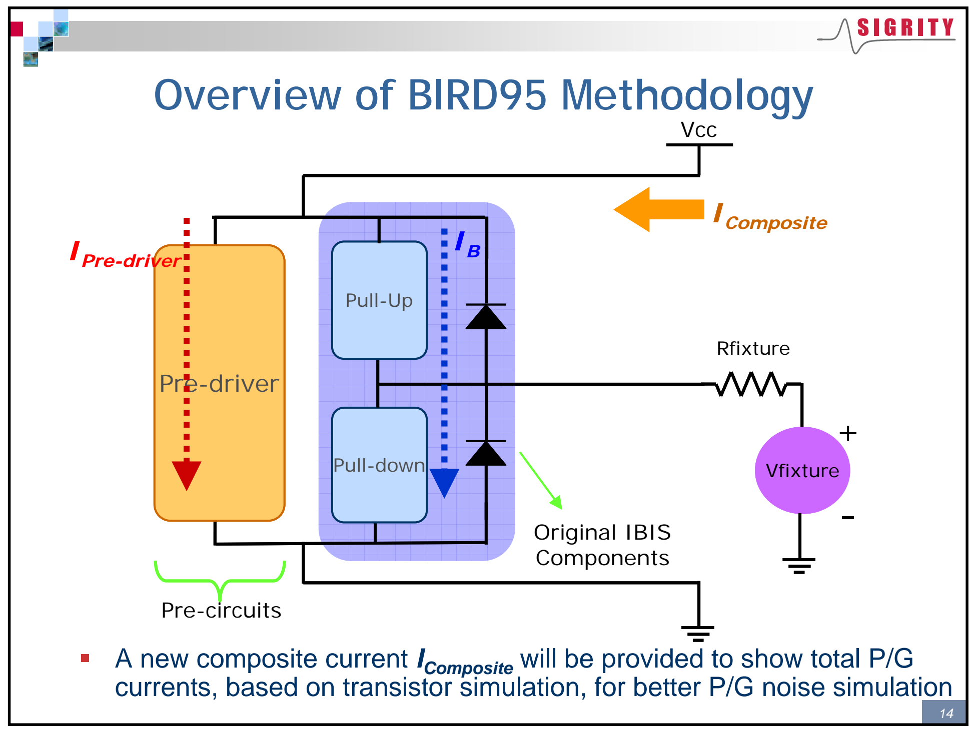
→ What about IBIS model ?

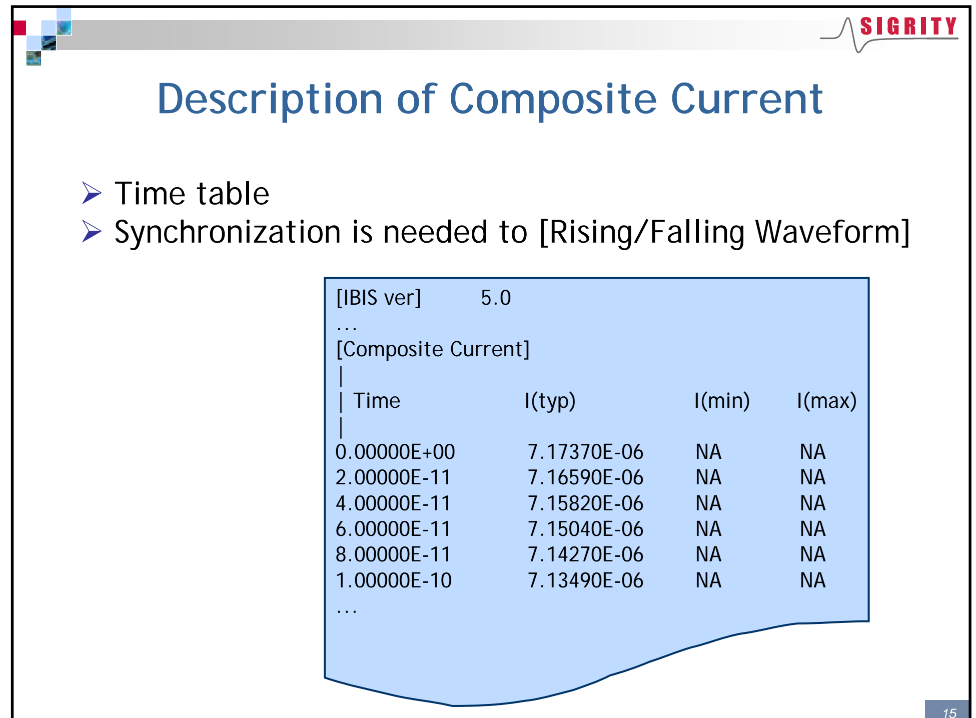
10


SIGRITY
Comparison of IBIS and SPICE total VDDQ current
Pre-driver Current
Pre-driver Current
Pullup Current
Crowbar Current
Low-to-high transition
High-to-low transition
HSPICE transistor – Red
HSPICE IBIS – Green
EDA IBIS Tool – Blue
The total VDDQ current for the transistor-level model is significantly different from its pullup component. There is a large amount of pre-driver current due to crowbar effects and gate capacitance charging.
Pre-driver current occurs significantly earlier than the pullup current. The pre-driver current is rapidly decreasing as the pullup is turning on.
The pre-driver current peaks almost as high as the pullup current. Note that the dI/dt of the pre-driver is much larger than that of the pullup current.
11


SIGRITY
Currents that IBIS can calculate
IBIS components
Analog Model of an IBIS output
Package Parasitics
Pwr pin
Pwr_clamp pin
Gnd pin
Gnd_clamp pin
L_pkg
R_pkg
C_comp
C_pkg
output pin
die
Ku(t) Ipu(V)
Kd(t) Ipd(V)
Ipc(V)
Igc(V)
The pullup and pulldown components are modeled as voltage controlled current sources
The instantaneous value for each voltage controlled current source is derived from the I/V tables and is scaled based on the information in the V(t) tables
The voltage controlled current sources are simultaneously active to model crowbar
Crowbar current can be approximated fairly well if all four V(t) tables are present in the IBIS file
Pre-driver Current is missing!!!
12


SIGRITY
Contents
Traditional I/O SSO Analysis
Buffer Model in SSO Simulation
BIRD95 Introduction
Summary
13

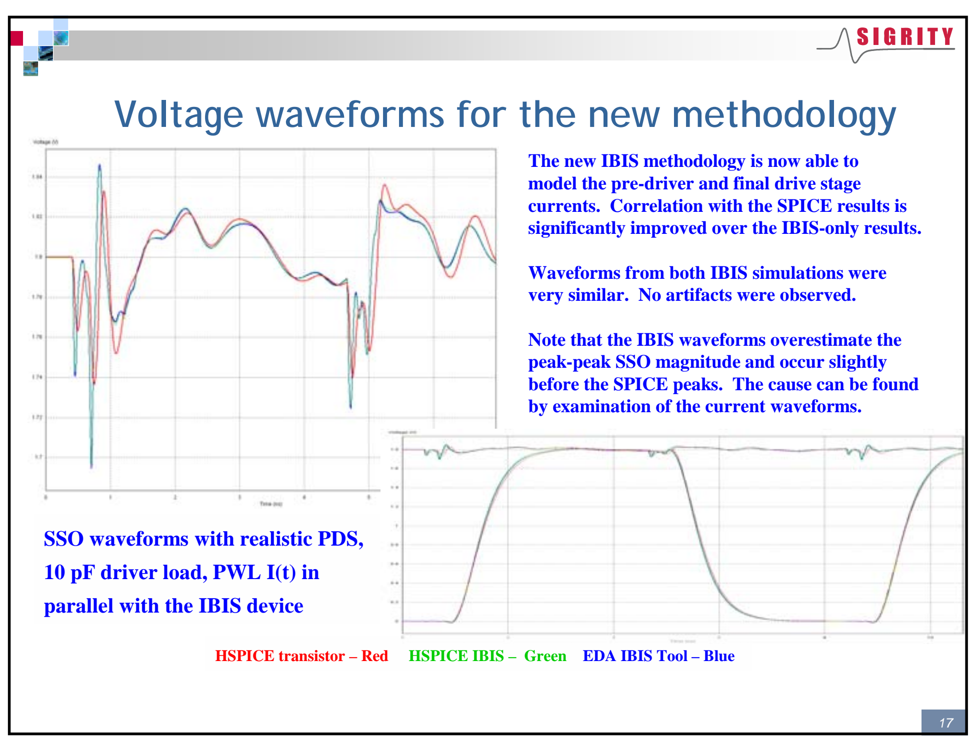

SIGRITY
Overview of BIRD95 Methodology
Vcc
I Composite
I Pre-driver
I B
Pull-Up
Pre-driver
Pull-down
Rfixture
+
Vfixture
-
Original IBIS
Components
Pre-circuits
A new composite current I Composite will be provided to show total P/G currents, based on transistor simulation, for better P/G noise simulation
14

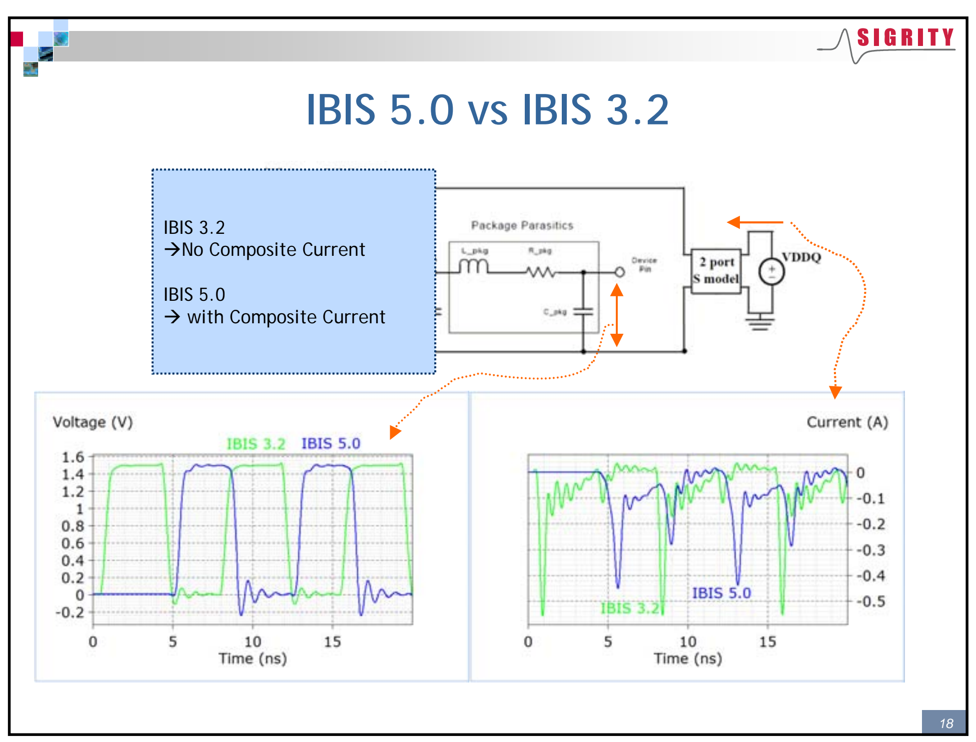


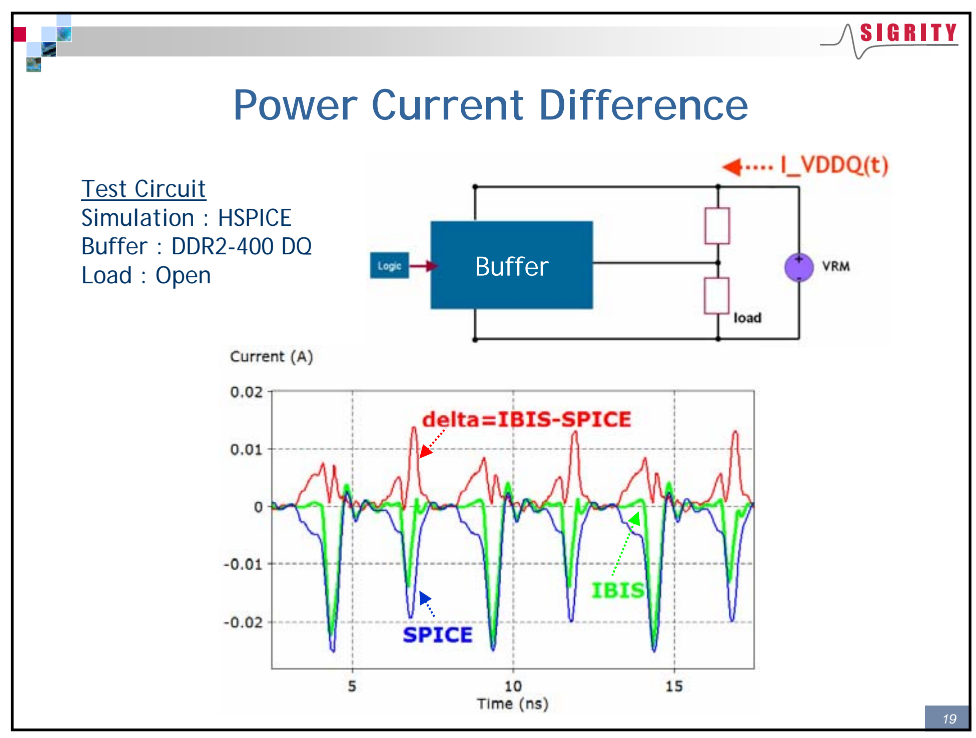
How Simulator handle IBIS with $I_{Composite}$?

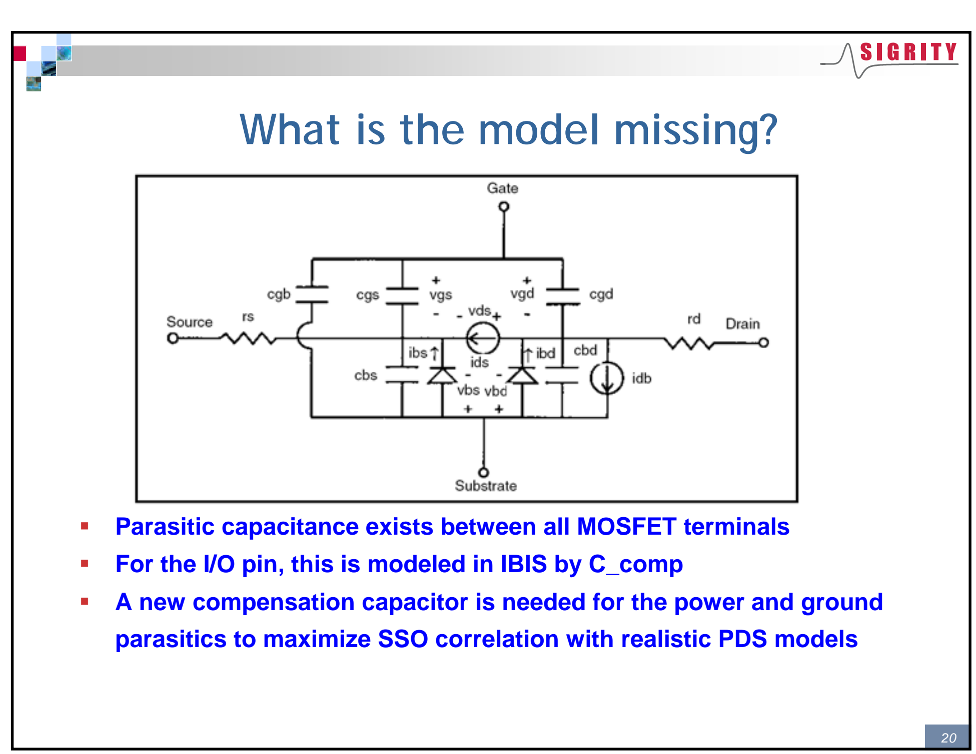
- Obtain composite currents $I_{Composite}$ from IBIS file (version 5.0)
- Obtain I_B from regular IBIS simulation during pre-simulation
- Obtain $I_{Pre\text{-}driver}$, Using
  - $I_{Pre\text{-}driver}(t) = I_{Composite}(t) - I_B(t)$
- Add $I_{Pre\text{-}driver}(t)$ as PWL current source in parallel with IBIS B element model

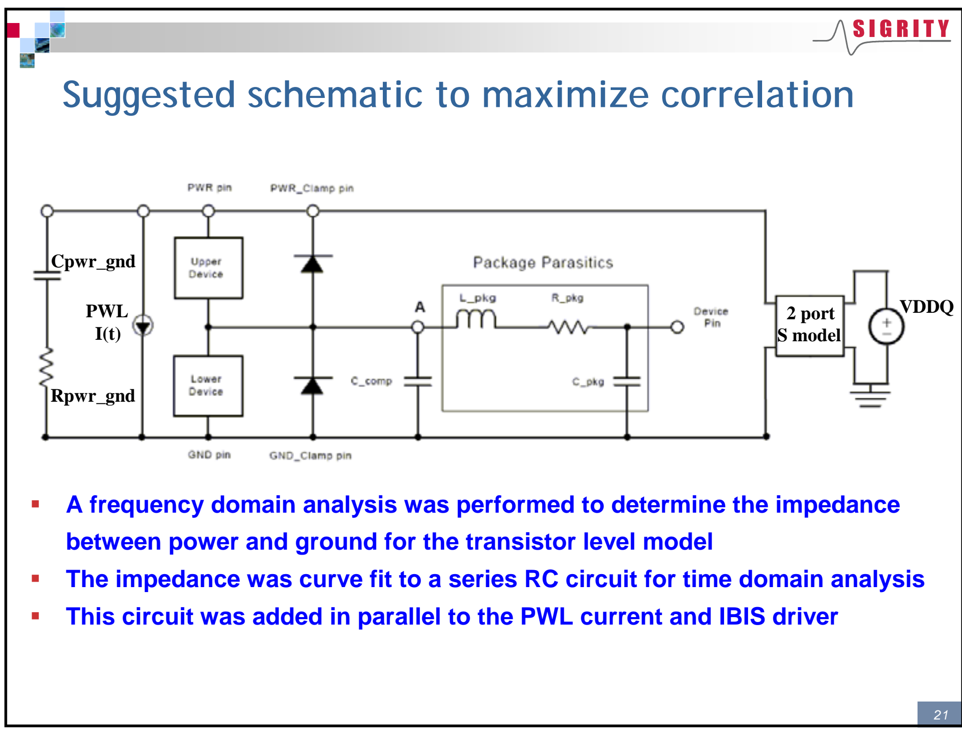
16

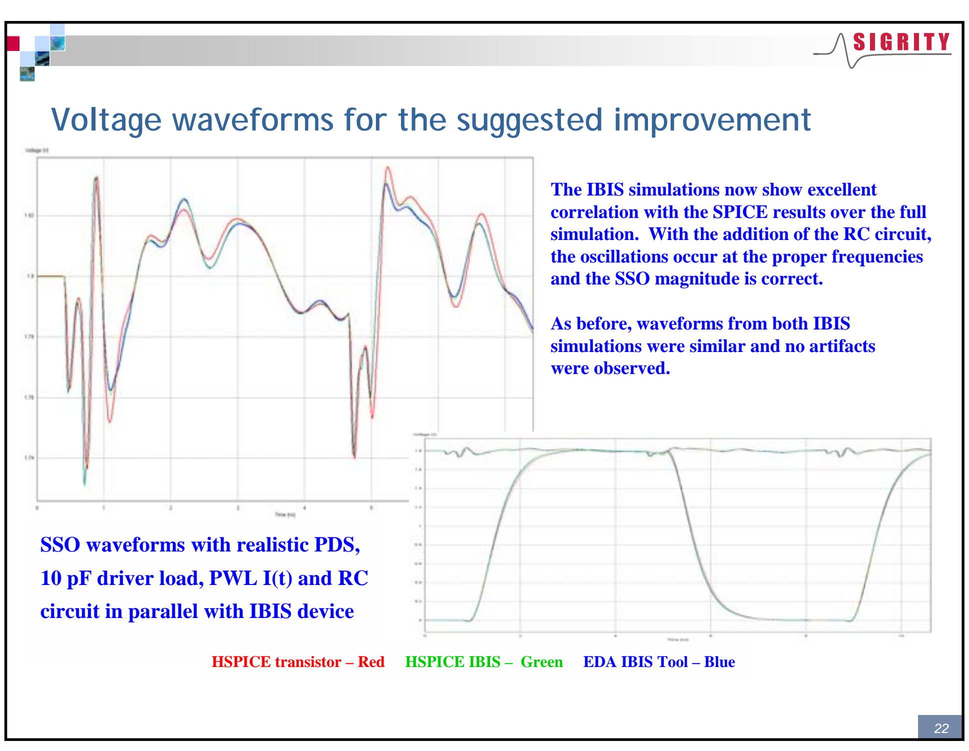

SIGRITY
Voltage waveforms for the new methodology
The new IBIS methodology is now able to model the pre-driver and final drive stage currents. Correlation with the SPICE results is significantly improved over the IBIS-only results.
Waveforms from both IBIS simulations were very similar. No artifacts were observed.
Note that the IBIS waveforms overestimate the peak-peak SSO magnitude and occur slightly before the SPICE peaks. The cause can be found by examination of the current waveforms.
SSO waveforms with realistic PDS, 10 pF driver load, PWL I(t) in parallel with the IBIS device
HSPICE transistor – Red
HSPICE IBIS – Green
EDA IBIS Tool – Blue
17

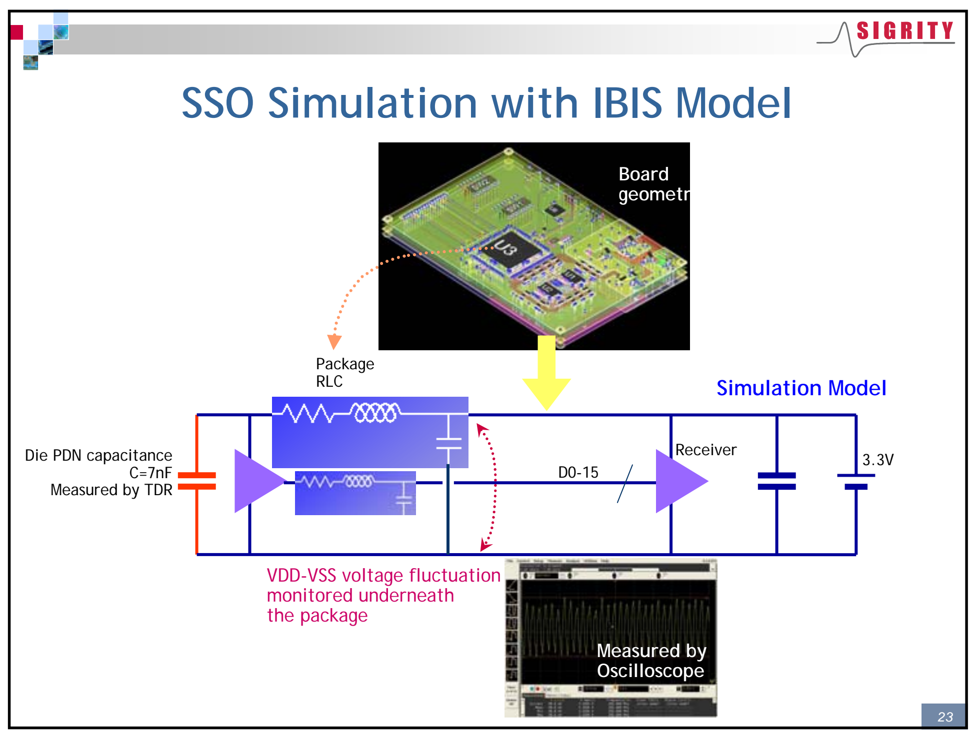

SIGRITY
IBIS 5.0 vs IBIS 3.2
IBIS 3.2
→No Composite Current
IBIS 5.0
→ with Composite Current
Package Parasitics
2 port
S model
VDDQ
Voltage (V)
IBIS 3.2
IBIS 5.0
Time (ns)
Current (A)
IBIS 3.2
IBIS 5.0
Time (ns)
18

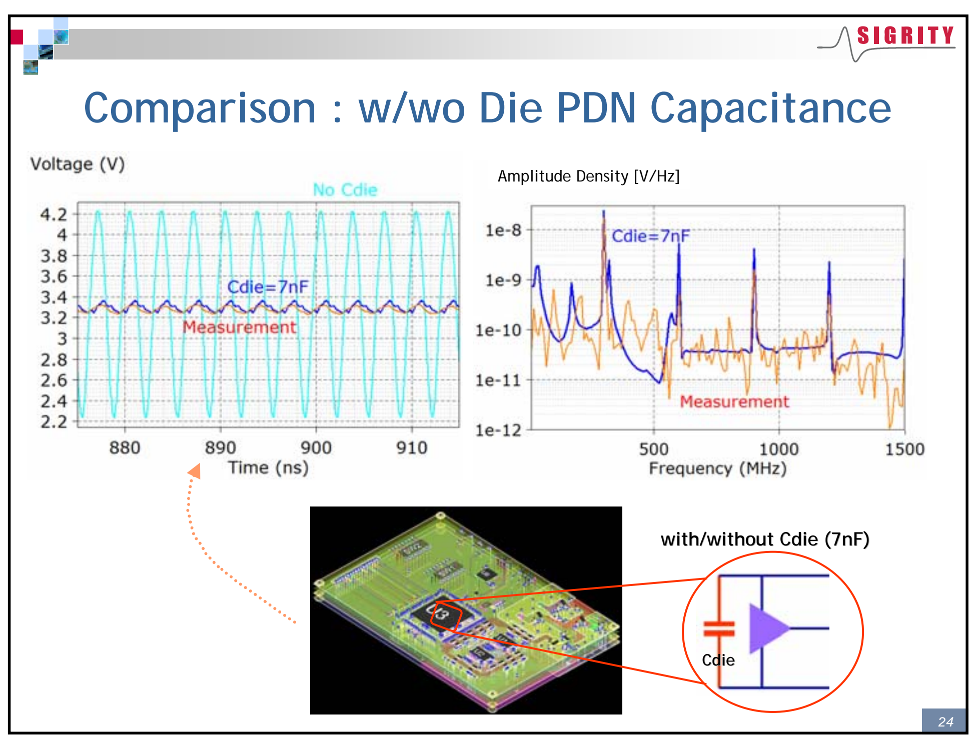

SIGRITY
Power Current Difference
Test Circuit
Simulation : HSPICE
Buffer : DDR2-400 DQ
Load : Open
I_VDDQ(t)
Logic
Buffer
VRM
load
Current (A)
0.02
0.01
0
-0.01
-0.02
delta=IBIS-SPICE
IBIS
SPICE
5
10
15
Time (ns)
19

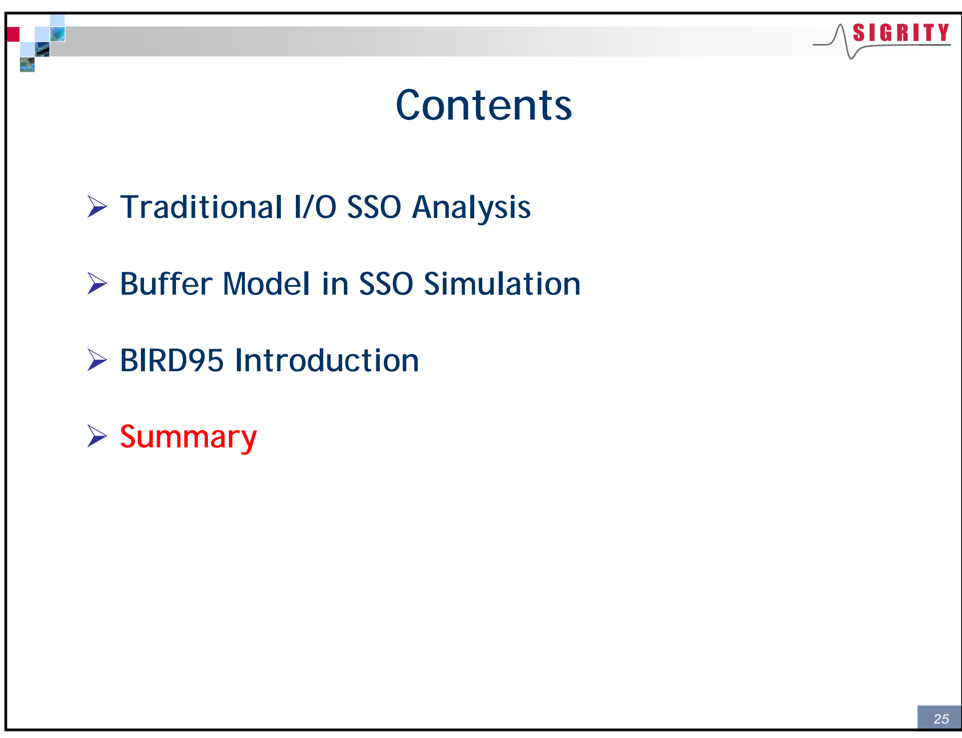

SIGRITY
What is the model missing?
Gate
Source
Drain
Substrate
cgb
cgs
vgs
vgd
cgd
rs
vds
rd
ibs
ids
ibd
cbd
cbs
vbs
vbd
idb
Parasitic capacitance exists between all MOSFET terminals
For the I/O pin, this is modeled in IBIS by C_comp
A new compensation capacitor is needed for the power and ground parasitics to maximize SSO correlation with realistic PDS models
20


SIGRITY
Suggested schematic to maximize correlation
PWR pin
PWR_Clamp pin
Cpwr_gnd
Upper Device
Package Parasitics
PWL I(t)
A
L_pkg
R_pkg
Device Pin
2 port S model
VDDQ
Lower Device
C_comp
C_pkg
Rpwr_gnd
GND pin
GND_Clamp pin
A frequency domain analysis was performed to determine the impedance between power and ground for the transistor level model
The impedance was curve fit to a series RC circuit for time domain analysis
This circuit was added in parallel to the PWL current and IBIS driver
21


SIGRITY
Voltage waveforms for the suggested improvement
The IBIS simulations now show excellent correlation with the SPICE results over the full simulation. With the addition of the RC circuit, the oscillations occur at the proper frequencies and the SSO magnitude is correct.
As before, waveforms from both IBIS simulations were similar and no artifacts were observed.
SSO waveforms with realistic PDS, 10 pF driver load, PWL I(t) and RC circuit in parallel with IBIS device
HSPICE transistor – Red
HSPICE IBIS – Green
EDA IBIS Tool – Blue
22


SIGRITY
SSO Simulation with IBIS Model
Board
geometr
Package
RLC
Simulation Model
Die PDN capacitance
C=7nF
Measured by TDR
D0-15
Receiver
3.3V
VDD-VSS voltage fluctuation
monitored underneath
the package
Measured by
Oscilloscope
23


SIGRITY
Comparison : w/wo Die PDN Capacitance
Voltage (V)
No Cdie
Cdie=7nF
Measurement
Time (ns)
Amplitude Density [V/Hz]
Cdie=7nF
Measurement
Frequency (MHz)
with/without Cdie (7nF)
Cdie
24


SIGRITY
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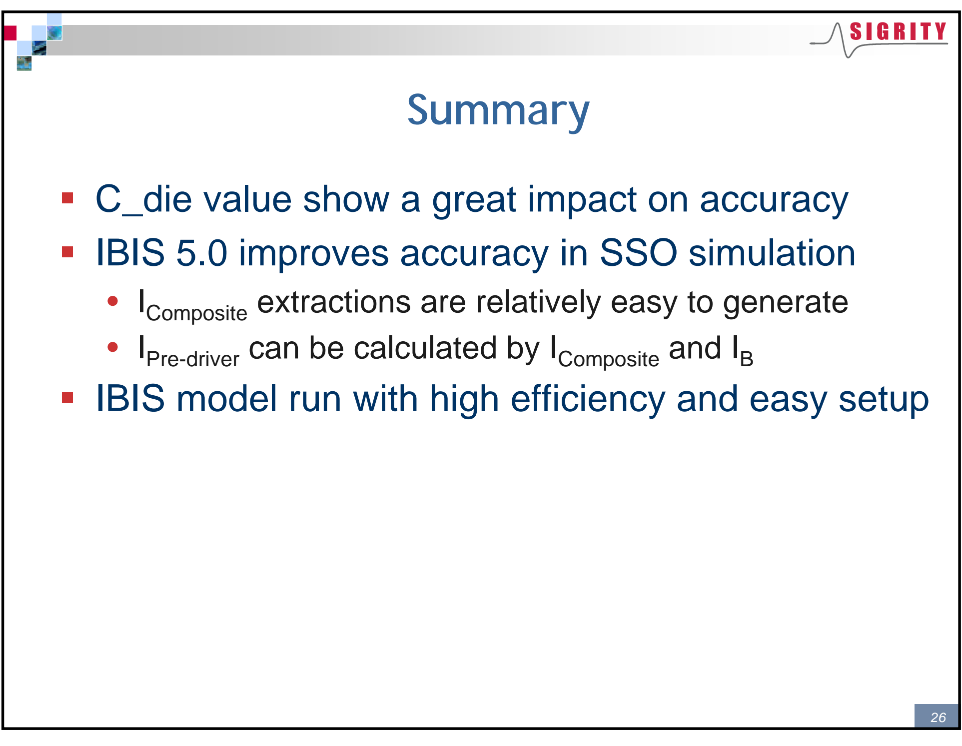
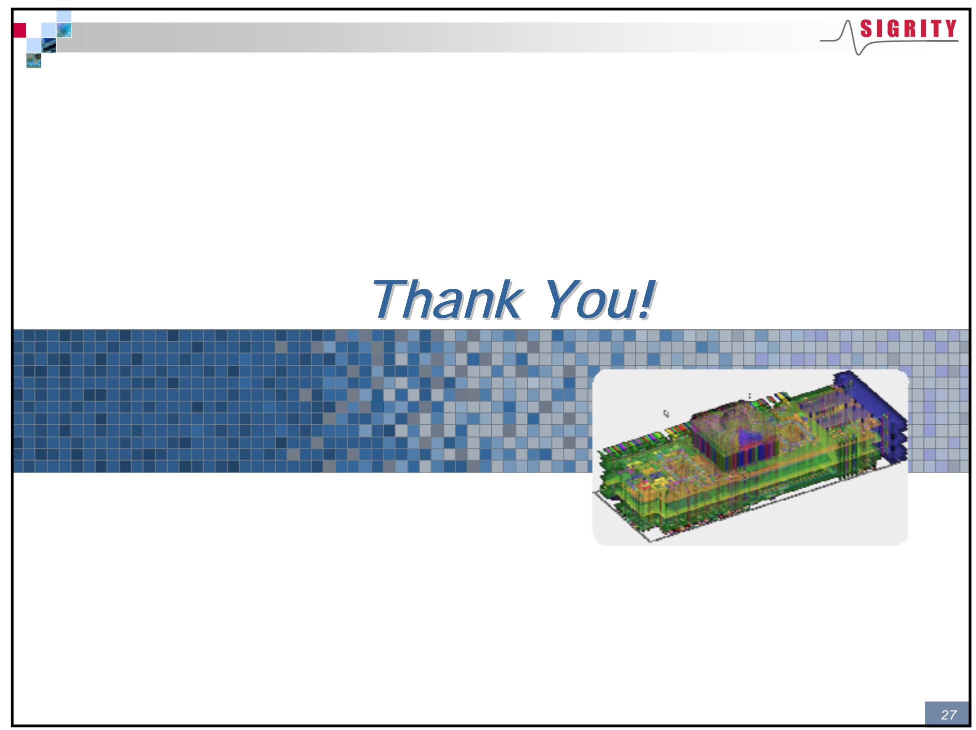

SIGRITY
Summary
C_die value show a great impact on accuracy
IBIS 5.0 improves accuracy in SSO simulation
$I_{Composite}$ extractions are relatively easy to generate
$I_{Pre\text{-}driver}$ can be calculated by $I_{Composite}$ and I_B
IBIS model run with high efficiency and easy setup
26


SIGRITY
Thank You!
27

Correlating C_pin Capacitance with Measurements

Asian IBIS Summit
Taipei, Taiwan
November 12, 2010
(Presented previously at IBIS Summit on November 9, 2010)

Randy Wolff
Micron Technology
rrwolff@micron.com

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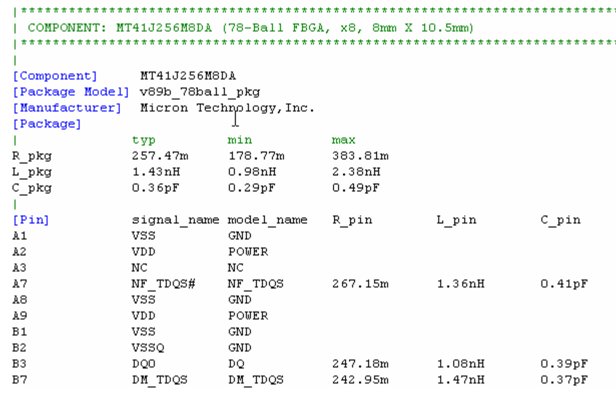
C_pin

- Package capacitance for a specific signal [Pin]
- Typically from diagonal elements of the capacitance matrix – extracted from 3D field solvers



```
|***************************************************************************
| COMPONENT: MT41J256M8DA (78-Ball FBGA, x8, 8mm X 10.5mm)
|***************************************************************************
|
[Component]      MT41J256M8DA
[Package Model]  v89b_78ball_pkg
[Manufacturer]   Micron Technology,Inc.
[Package]
|               typ         min         max
R_pkg           257.47m     178.77m     383.81m
L_pkg           1.43nH      0.98nH      2.38nH
C_pkg           0.36pF      0.29pF      0.49pF
|
[Pin]           signal_name model_name  R_pin       L_pin       C_pin
A1              VSS         GND
A2              VDD         POWER
A3              NC          NC
A7              NF_TDQS#    NF_TDQS     267.15m     1.36nH      0.41pF
A8              VSS         GND
A9              VDD         POWER
B1              VSS         GND
B2              VSSQ        GND
B3              DQ0         DQ          247.18m     1.08nH      0.39pF
B7              DM_TDQS     DM_TDQS     242.95m     1.47nH      0.37pF
```

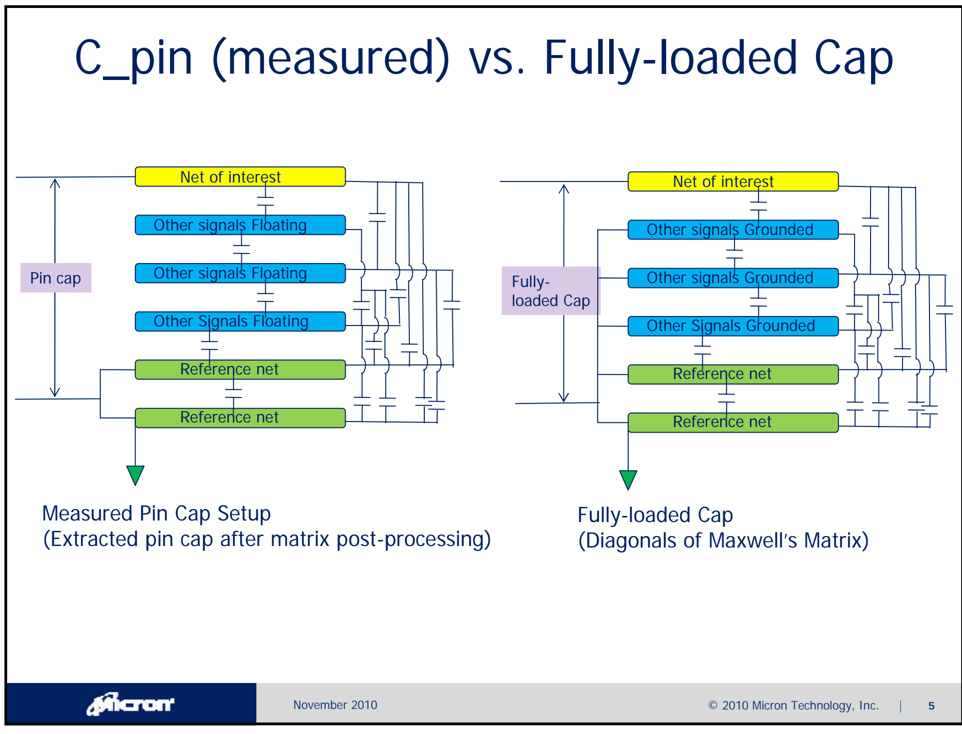
Measured Capacitance

- Diagonal of matrix is total capacitance seen by each line with all other lines grounded
  - Fully-loaded capacitance is useful for single line simulations
- Measured capacitance is less than fully-loaded capacitance
  - Signal is referenced to power and ground (pwr/gnd decoupled)
  - All other signal lines are floating

Why is this important?

- C_comp calculation and Model correlation
  - C_comp = C_signal(measured) – C_pin(measured)
  - C_pin ≠ C_pin(measured)
- Datasheet comparisons
  - $C_{specification}$ is based on measured values, not total capacitance
  - Estimating measured values from package simulation data aids in optimizing package designs to meet capacitance specifications

Capacitance Parameters	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
CK and CK#	C_{CK}	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	0.8	1.3	pF
ΔC: CK to CK#	C_{DCK}	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	pF
Single-end I/O: DQ, DM	C_{IO}	1.5	3.0	1.5	3.0	1.5	2.5	1.5	2.3	1.4	2.2	pF
Differential I/O: DQS, DQS#, TDQS, TDQS#	C_{IO}	1.5	3.0	1.5	3.0	1.5	2.5	1.5	2.3	1.4	2.2	pF
ΔC: DQS to DQS#, TDQS, TDQS#	C_{DDQS}	0	0.2	0	0.2	0	0.15	0	0.15	0	0.15	pF
ΔC: DQ to DQS	C_{DIO}	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF


C_pin (measured) vs. Fully-loaded Cap
Net of interest
Other signals Floating
Other signals Floating
Other Signals Floating
Reference net
Reference net
Pin cap
Net of interest
Other signals Grounded
Other signals Grounded
Other Signals Grounded
Reference net
Reference net
Fully-loaded Cap
Measured Pin Cap Setup
(Extracted pin cap after matrix post-processing)
Fully-loaded Cap
(Diagonals of Maxwell's Matrix)
November 2010
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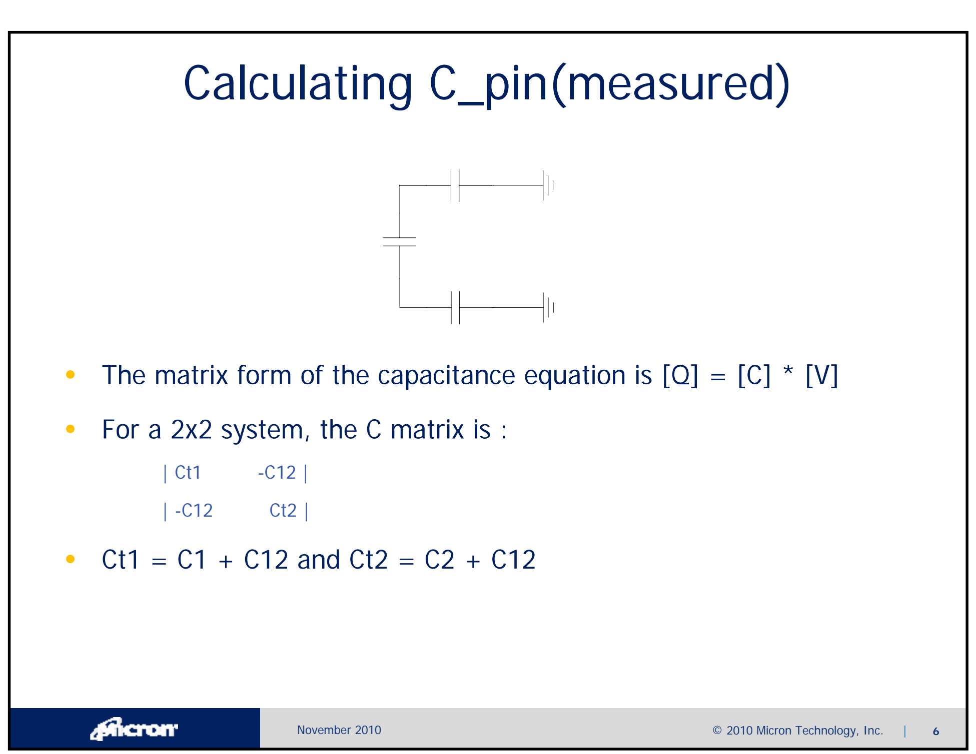
Calculating C_pin(measured)
The matrix form of the capacitance equation is [Q] = [C] * [V]
For a 2x2 system, the C matrix is :
| Ct1 -C12 |
| -C12 Ct2 |
Ct1 = C1 + C12 and Ct2 = C2 + C12
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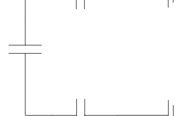
Calculating C_pin(measured)



- Deposit a charge of Q on Node 1

  | Ct1 -C12 | * | V1 | = | Q |

  | -C12 Ct2 | * | V2 | = | 0 |

- Ct1 * V1 – C12 * V2 = Q
- -C12 * V1 + Ct2 * V2 = 0, V2 = C12/Ct2 * V1
- (Ct1 - C12^2/Ct2) * V1 = Q
- Cnode1 = Q/V1 = (Ct1 - C12^2/Ct2)
- In matrix form, let Q = 1 coulomb

  | V1 | = Inv (| Ct1 -C12 |) * | 1 |

  | V2 | = Inv (| -C12 Ct2 |) * | 0 |

- This yields V1 and V2 and Cnode1 = 1/V1, since Q = 1

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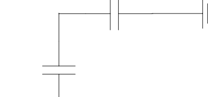
Calculating C_pin(measured)

- Let Node 2 be grounded - this forces V2 = 0 and allows a net negative charge on Node 2

  | Ct1 -C12 | * | V1 | = | 1 |

  | -C12 Ct2 | * | 0 | = | Q |



- 1: Ct1 * V1 – C12 * 0 = 1 , V1 = 1/Ct1
- 2: -C12 * V1 + Ct2 * 0 = Q, Q = - C12/Ct1
- The only value of interest is V1, only equation 1 is needed. This is the same as eliminating the 2nd row of the [C] matrix.
- V2 = 0, so all of the terms in the 2nd column will multiply to 0. This eliminates the 2nd column of [C].
- The matrix equation reduces to | Ct1 | * | V1 | = | 1 |

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Calculating C_pin(measured)

- Generalized: Let [C] be an n+m x n+m matrix representing n floating nodes and m nodes clamped to power or ground.
- Step 1 – eliminate the rows and columns associated with clamped nodes.
  - [C] -> [C′], where [C′] is an n x n matrix.
  - |C′| = |Reduction Matrix2| * |C| * |Reduction Matrix1|
  - If net i is clamped then row i of Reduction Matrix1 is all 0s
  - If net i is floating then row i of Reduction Matrix1 is all 0s with a 1 in column x
    - x = i - # of clamped nets between net 1 and net i
  - If net i is clamped then column i of Reduction Matrix2 is all 0s
  - If net i is floating then column i of Reduction Matrix2 is all 0s with a 1 in row x
    - x = i - # of clamped nets between net 1 and net i

Calculating C_pin(measured)

- Step 2 – Generate Q matrix – n x n identity matrix
  - Represents a 1 coulomb charge deposited on each floating node, one at a time.
- Step 3 – solve for [V] matrix
  - [V] = inv([C′]) * [Q], where [Q] is identity matrix
- Step 4 – Calculate floating node capacitances
  - Cnode(x) = 1/Vxx, where Vxx are the diagonal elements of [V]
- Overall effect is mutual capacitances are reduced due to shorting of the mutual terms to power and ground nets

Micron's Capacitance Analyzer Tool

- Excel spreadsheet macro
- Reads in matrix data from several Field Solver tools
- Solves for 'measured' capacitance
- Nets are defined as either 'floating' or 'grounded'

Line number	Line Name	Signal_State
1	A0	Floating
2	A1	Floating
3	A2	Floating
59	VDD	Grounded
60	VDDQ	Grounded
61	VSS	Grounded
62	VSSQ	Grounded
63	WE#	Floating

Signal Names	Pin Capacitance	Maxwell Diagonal Capacitance
A0	9.48269E-13	1.22479E-12
A1	1.05993E-12	1.29176E-12
A2	1.06298E-12	1.20089E-12
A3	9.97877E-13	1.0904E-12
A4	7.88691E-13	8.36509E-13
A5	8.79004E-13	1.09757E-12

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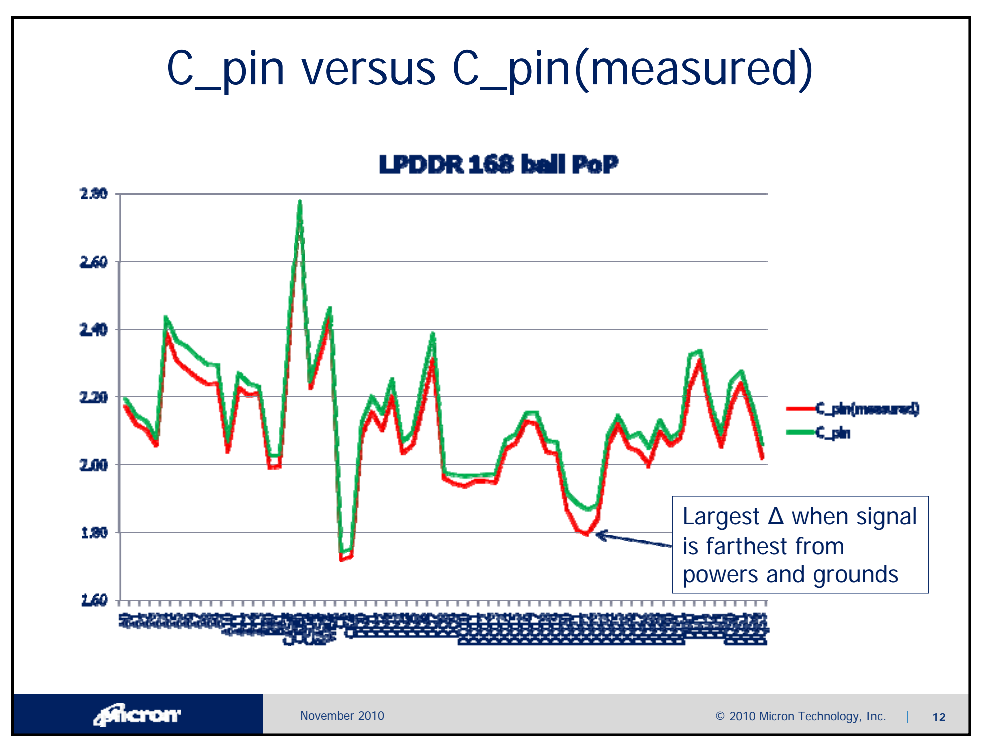

Conclusions

- Capacitance matrix data must be manipulated when comparing it to measured capacitance
  - Maxwell capacitance is not what is typically measured
  - Important for datasheet comparisons and model to simulation correlation

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Acknowledgements

- Thanks to Bruce Schober at Micron for development of the analyzer tool and figuring out the matrix math.

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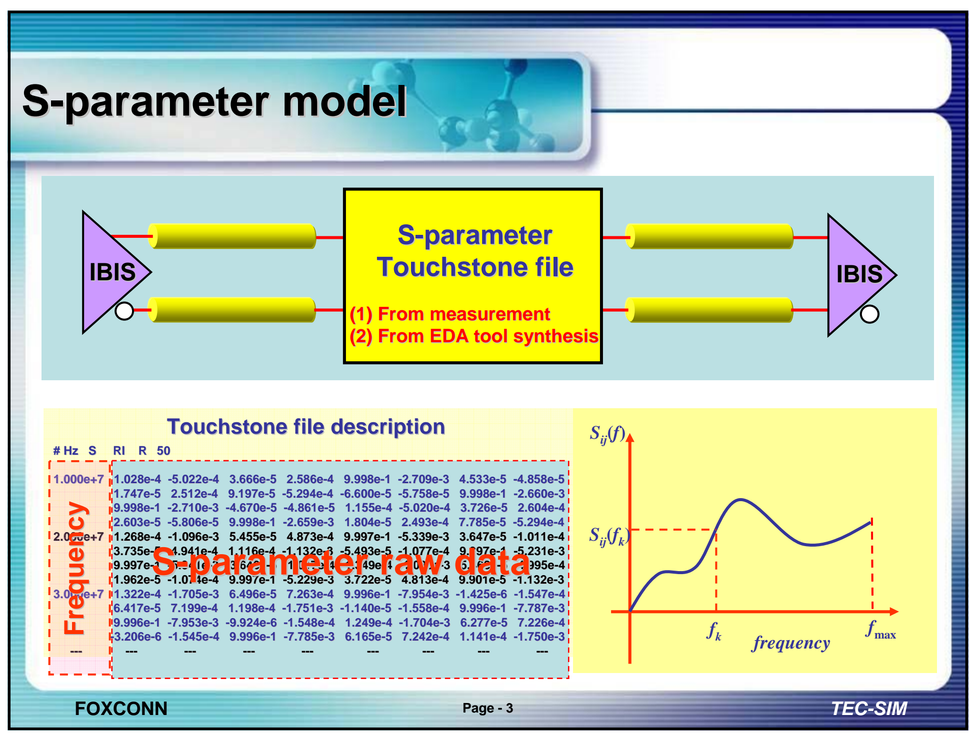
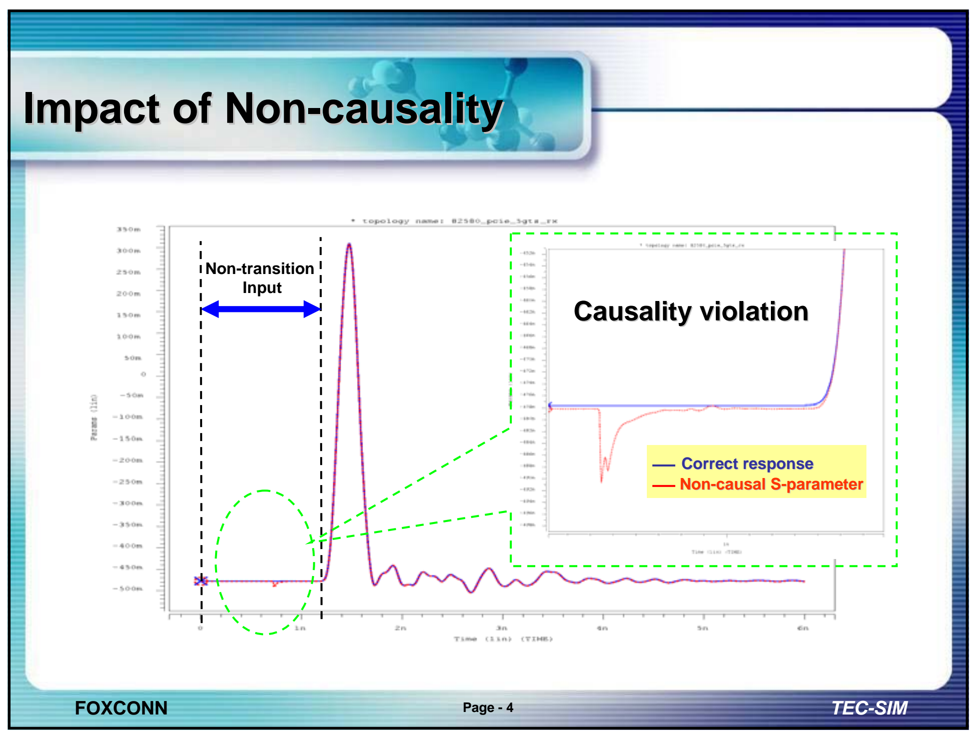
Agenda

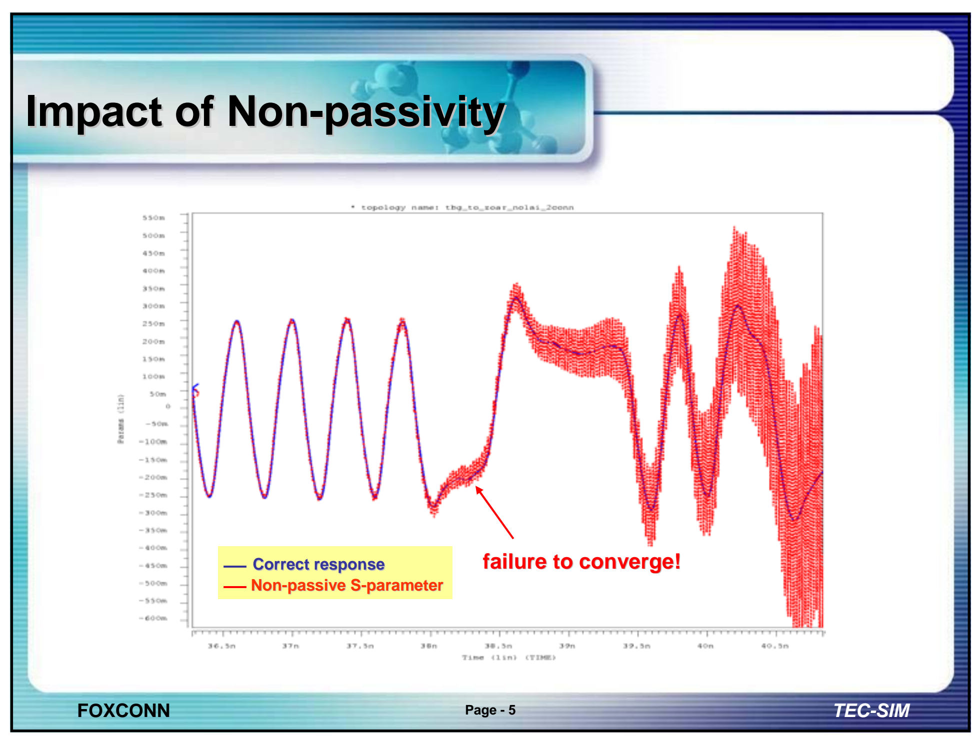
- Causality and passivity fundamentals
- Enforcing passivity for sampled frequency data
- S-parameter rational function approximation
- A new format of S-parameter rational function
- Summary

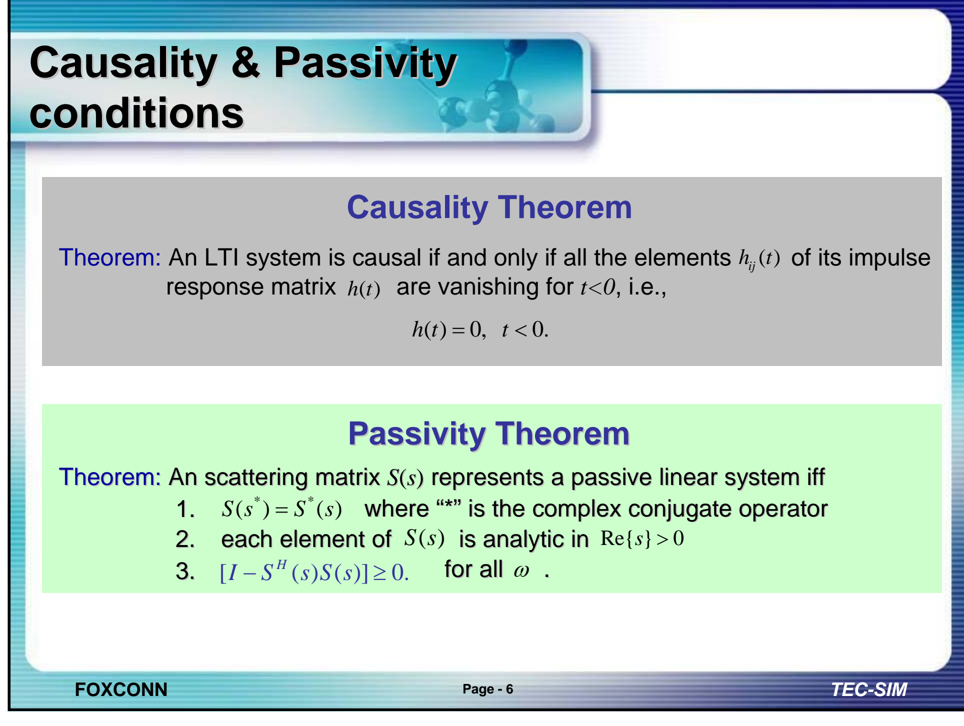


S-parameter model
IBIS
S-parameter
Touchstone file
(1) From measurement
(2) From EDA tool synthesis
IBIS
Touchstone file description
Hz S RI R 50
1.000e+7 1.028e-4 -5.022e-4 3.666e-5 2.586e-4 9.998e-1 -2.709e-3 4.533e-5 -4.858e-5
1.747e-5 2.512e-4 9.197e-5 -5.294e-4 -6.600e-5 -5.758e-5 9.998e-1 -2.660e-3
9.998e-1 -2.710e-3 -4.670e-5 -4.861e-5 1.155e-4 -5.020e-4 3.726e-5 2.604e-4
2.603e-5 -5.806e-5 9.998e-1 -2.659e-3 1.804e-5 2.493e-4 7.785e-5 -5.294e-4
1.268e-4 -1.096e-3 5.455e-5 4.873e-4 9.997e-1 -5.339e-3 3.647e-5 -1.011e-4
1.322e-4 -1.705e-3 6.496e-5 7.263e-4 9.996e-1 -7.954e-3 -1.425e-6 -1.547e-4
6.417e-5 7.199e-4 1.198e-4 -1.751e-3 -1.140e-5 -1.558e-4 9.996e-1 -7.787e-3
9.996e-1 -7.953e-3 -9.924e-6 -1.548e-4 1.249e-4 -1.704e-3 6.277e-5 7.226e-4
3.206e-6 -1.545e-4 9.996e-1 -7.785e-3 6.165e-5 7.242e-4 1.141e-4 -1.750e-3
Frequency
S-parameter raw data
$S_{ij}(f)$
$S_{ij}(f_k)$
f_k
frequency
f_{max}
FOXCONN
Page - 3
TEC-SIM



Impact of Non-causality
Non-transition
Input
Causality violation
Correct response
Non-causal S-parameter
FOXCONN
Page - 4
TEC-SIM


Impact of Non-passivity
Correct response
Non-passive S-parameter
failure to converge!
FOXCONN
Page - 5
TEC-SIM


Causality & Passivity conditions
Causality Theorem
Theorem: An LTI system is causal if and only if all the elements $h_{ij}(t)$ of its impulse response matrix $h(t)$ are vanishing for $t<0$, i.e.,
$h(t)=0, \quad t<0.$
Passivity Theorem
Theorem: An scattering matrix $S(s)$ represents a passive linear system iff
1. $S(s^*)=S^*(s)$ where "*" is the complex conjugate operator
2. each element of $S(s)$ is analytic in $\mathrm{Re}\{s\}>0$
3. $[I-S^H(s)S(s)]\geq 0.$ for all ω .
FOXCONN
Page - 6
TEC-SIM

Causality & Passivity conditions

- **Passivity Condition 2 satisfies Kramers-Kronig relations, since the following theorem.**

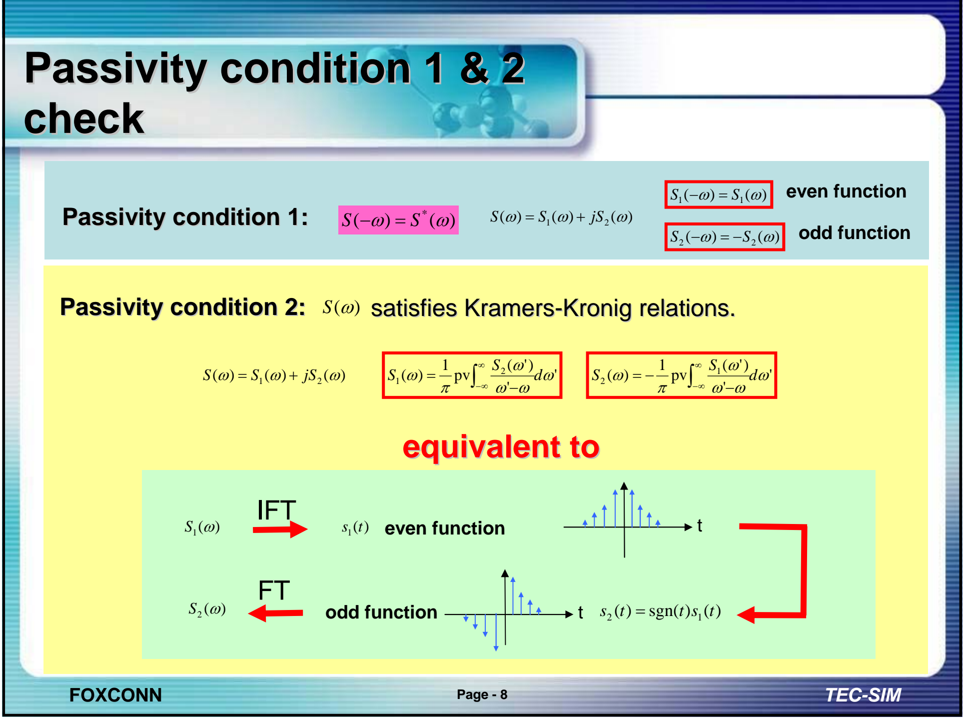
Theorem: If $h(t)$ admits a Fourier transform, the following facts are equivalent.

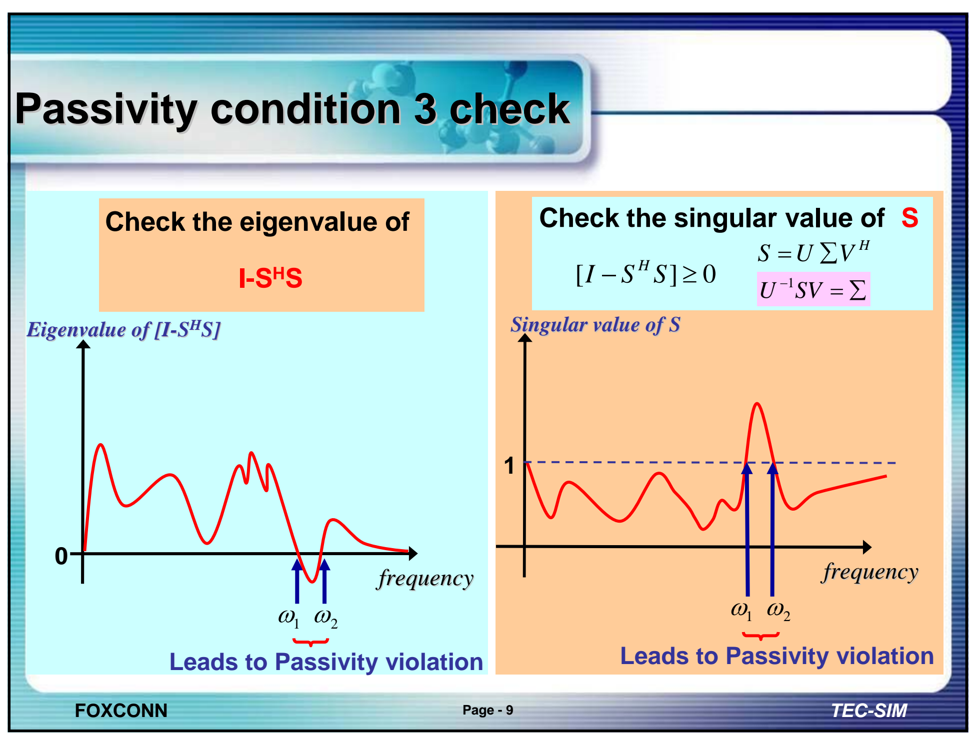
1. $h(t) = 0, \quad t < 0.$
2. $H(j\omega)$ is the limit, as $\sigma \to 0$, of a function $H(s)$ defined in $\mathrm{Re}\{s\} > 0$ and here analytic and of polynomial growth.
3. $H(j\omega) = \mathrm{F}\{h(t)\}$ satisfies Kramers-Kronig relations.

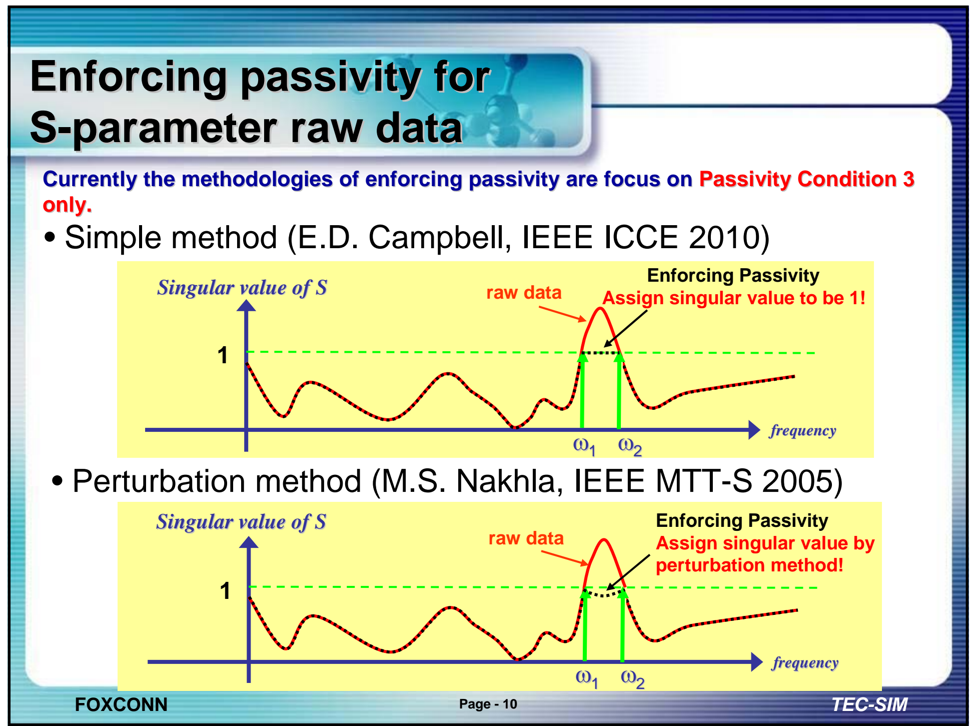
Theorem: If an LTI system is passive, then it is also causal.

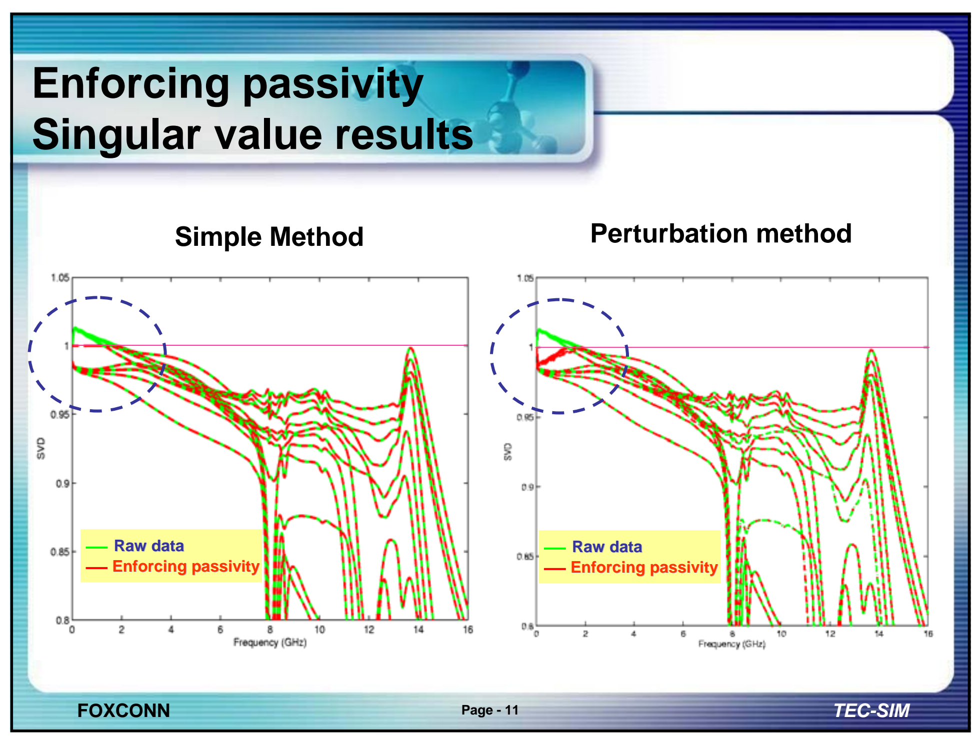
Reference: Piero Triverio, S. Grivet-Talocia, M.S. Nakhla, F.G. Canavero and R. Achar, "Stability, Causality, and Passivity in Electrical Interconnect Models," IEEE TRANS. on ADVANCED PACKAGING, VOL. 30, NO. 4, NOVEMBER 2007.

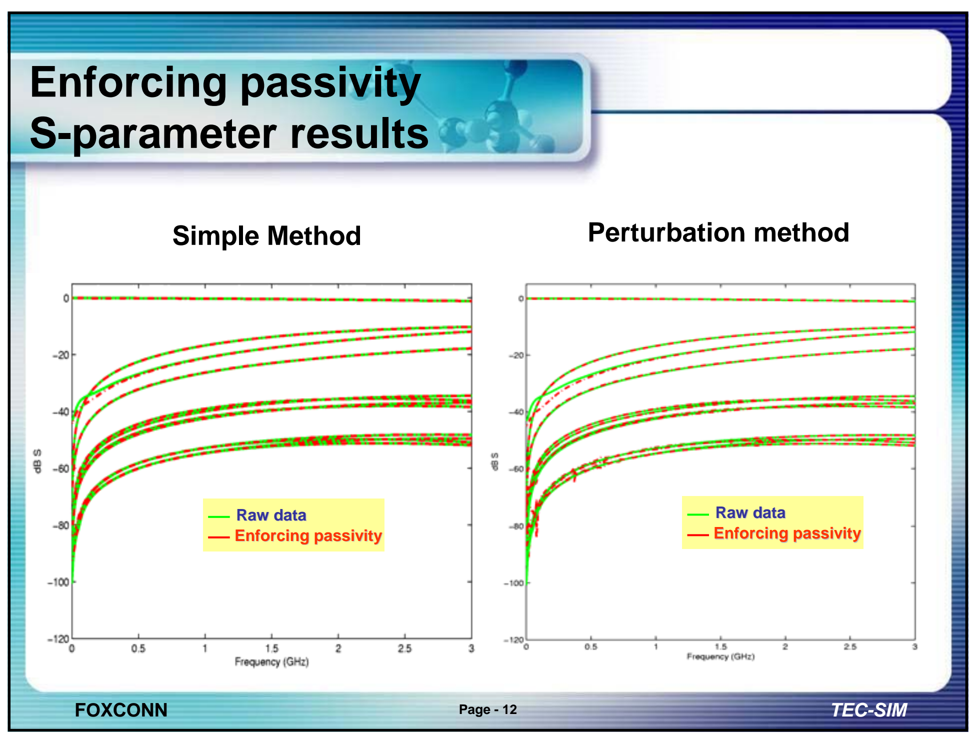
FOXCONN Page - 7 TEC-SIM

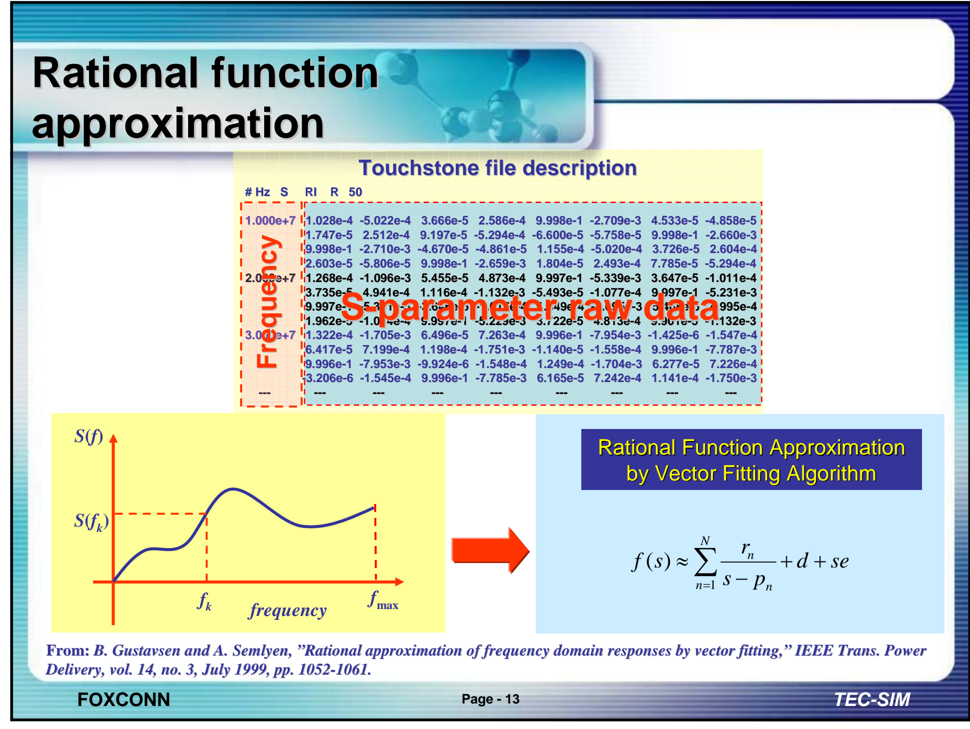



Passivity condition 3 check
Check the eigenvalue of
I-S^H S
Eigenvalue of [I-S^H S]
0
frequency
ω1 ω2
Leads to Passivity violation
Check the singular value of S
$[I - S^H S] \geq 0$
$S = U \Sigma V^H$
$U^{-1} S V = \Sigma$
Singular value of S
1
frequency
ω1 ω2
Leads to Passivity violation
FOXCONN
Page - 9
TEC-SIM


Enforcing passivity for S-parameter raw data
Currently the methodologies of enforcing passivity are focus on Passivity Condition 3 only.
• Simple method (E.D. Campbell, IEEE ICCE 2010)
Singular value of S
raw data
Enforcing Passivity
Assign singular value to be 1!
1
frequency
ω1 ω2
• Perturbation method (M.S. Nakhla, IEEE MTT-S 2005)
Singular value of S
raw data
Enforcing Passivity
Assign singular value by perturbation method!
1
frequency
ω1 ω2
FOXCONN
Page - 10
TEC-SIM


Enforcing passivity
Singular value results
Simple Method
Perturbation method
Raw data
Enforcing passivity
Raw data
Enforcing passivity
SVD
Frequency (GHz)
FOXCONN
Page - 11
TEC-SIM


Enforcing passivity
S-parameter results
Simple Method
Perturbation method
Raw data
Enforcing passivity
Raw data
Enforcing passivity
dB S
Frequency (GHz)
FOXCONN
Page - 12
TEC-SIM



Rational function passivity conditions

- If $S(s)$ is a rational function, the passivity condition 1 is satisfied.
- If $S(s)$ is a rational function of s, the passivity condition 3 implies the analyticity of $S(s)$ for $\mathrm{Re}\{s\} > 0$.

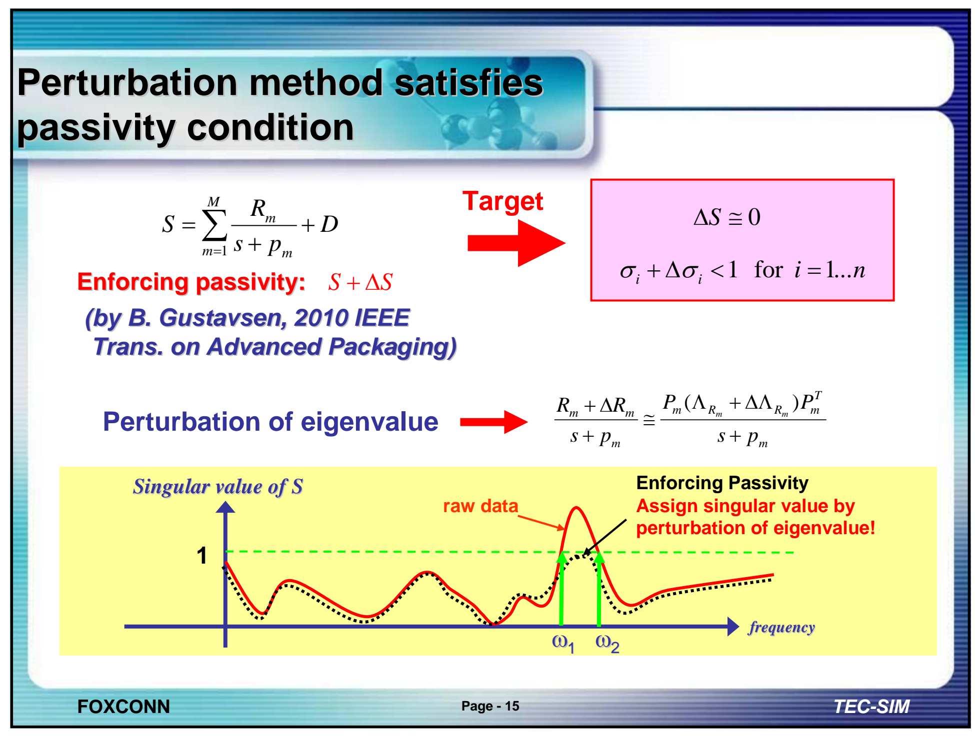
Passivity Theorem for rational function

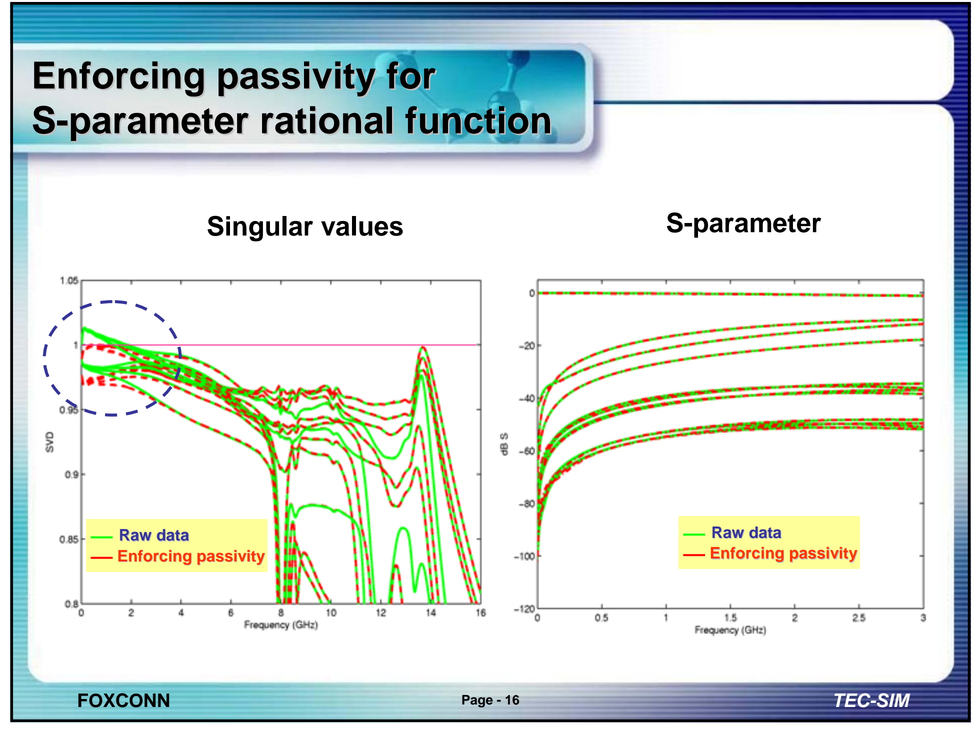
Theorem: A rational function of scattering matrix $S(s)$ represents a passive linear system iff

$$[I - S^H(s)S(s)] \geq 0. \text{ for all } \omega .$$

Reference:
[1] Piero Triverio, S. Grivet-Talocia, M.S. Nakhla, F.G. Canavero and R. Achar, "Stability, Causality, and Passivity in Electrical Interconnect Models," IEEE TRANS. on ADVANCED PACKAGING, VOL. 30, NO. 4, NOVEMBER 2007.
[2] Altan Odabasioglu, Mustafa Celik and Lawrence T. Pileggi,"PRIMA: Passive Reduced-Order Interconnect Macromodeling Algorithm," IEEE TRANS. on COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS,, VOL. 17, NO. 8, Aug. 1998.

FOXCONN Page - 14 TEC-SIM


Perturbation method satisfies passivity condition
$S = \sum_{m=1}^{M} \frac{R_m}{s+p_m} + D$
Target
$\Delta S \cong 0$
$\sigma_i + \Delta\sigma_i < 1$ for $i = 1 \ldots n$
Enforcing passivity: $S + \Delta S$
(by B. Gustavsen, 2010 IEEE Trans. on Advanced Packaging)
Perturbation of eigenvalue
$\frac{R_m + \Delta R_m}{s+p_m} \cong \frac{P_m(\Lambda_{R_m} + \Delta\Lambda_{R_m})P_m^T}{s+p_m}$
Singular value of S
raw data
Enforcing Passivity
Assign singular value by perturbation of eigenvalue!
1
frequency
ω_1 ω_2
FOXCONN
Page - 15
TEC-SIM


Enforcing passivity for S-parameter rational function
Singular values
S-parameter
Raw data
Enforcing passivity
SVD
Frequency (GHz)
dB S
Raw data
Enforcing passivity
Frequency (GHz)
FOXCONN
Page - 16
TEC-SIM

Propose Common-pole Rational Function Standard File

$$S_{i,j} = D_{i,j} + j\omega E_{i,j} + \sum_{n=1}^{N} \frac{Rr_{i,j}^{n}}{s+pr_n} + \sum_{m=1}^{M} \left(\frac{Rc_m}{s+pc_m} + \frac{Rc_m^*}{s+pc_m^*} \right)$$

R Zo1 Zo2 Zo3 Zo4	! reference resistor of ports
Common pole	! Common pole definition
Real *N*	! Real pole definition
$pr_1 \ pr_2 \ \cdots \ pr_N$	! Real pole data
Complex *M*	! Complex pole definition
$\mathrm{Re}(pc_1) \ \mathrm{Re}(pc_2) \ \cdots \ \mathrm{Re}(pc_M)$	! Complex pole real part data
$\mathrm{Im}(pc_1) \ \mathrm{Im}(pc_2) \ \cdots \ \mathrm{Im}(pc_M)$	! Complex pole imagery part data
i j	! Element definition, i is row and j is column
DC D_{ij}	! DC element definition
E E_{ij}	! E element definition
Real residue *N*	! Real residue definition
$Rr_{ij}^1 \ Rr_{ij}^2 \ \cdots \ Rr_{ij}^N$	! Real residue data
Complex residue *M*	! Complex residue definition
$\mathrm{Re}(Rc_{ij}^1) \ \mathrm{Re}(Rc_{ij}^2) \ \cdots \ \mathrm{Re}(Rc_{ij}^M)$	! Complex residue real part data
$\mathrm{Im}(Rc_{ij}^1) \ \mathrm{Im}(Rc_{ij}^2) \ \cdots \ \mathrm{Im}(Rc_{ij}^M)$	! Complex residue imagery part data

Advantage of rational function standard file

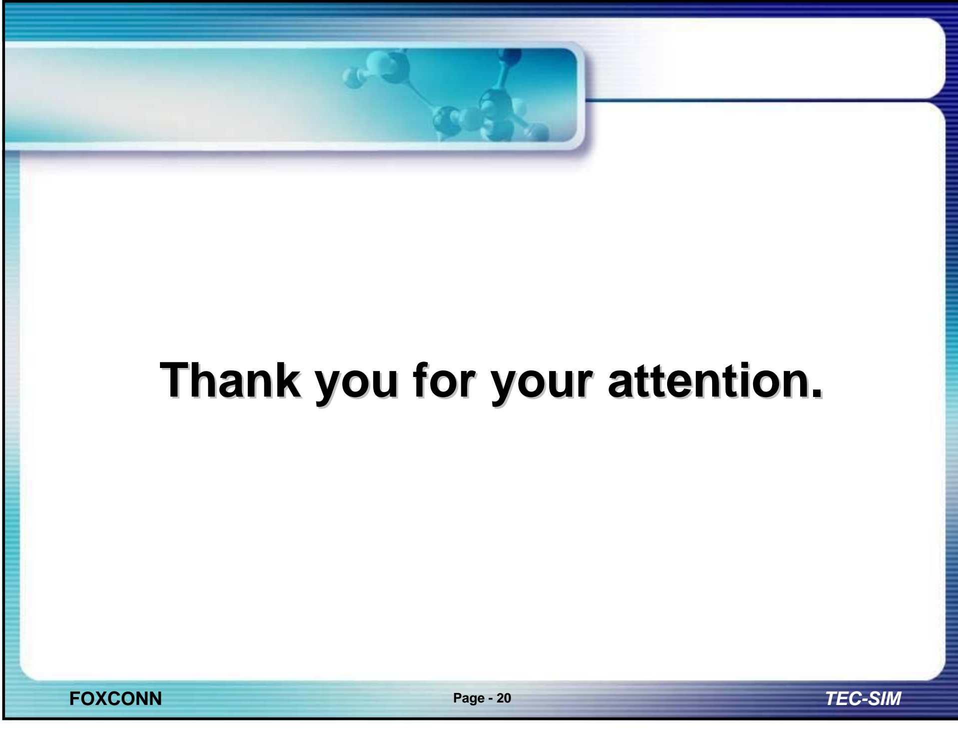
- Present S-parameter on full spectrum.
- It could be causality and passivity guarantee on full spectrum after enforcing passivity.
- Rapidly reduce the size of S-parameter sampled frequency data.

Type	No. of Sampled data	No. of port	No. of pole-residue	Size of Touchstone file	Size of proposed file	Size reduced to
Via	2000	4	12	1.66M	6.88K	0.41%
Connector	2000	12	78	9.21M	334.38K	3.63%
Trace	2000	42	240	105.16M	1.35M	1.28%

Summary

- The traditional enforcing passivity for S-parameter raw date are not sufficient to satisfy the passivity conditions.
- Using enforcing passivity rational function to fit S-parameter raw data could be causality and passivity guarantee on full spectrum.
- The proposed rational function standard file has the advantage in size reduction of S-parameter sampled frequency data.

FOXCONN Page - 19 TEC-SIM



Automated AMI Model Generation & Validation

José Luis Pino
Amolak Badesha

Manuel Luschas
Antonis Orphanou
Halil Civit

Asian IBIS Summit, Taipei, Taiwan November 12, 2010
(Presented previously at the IBIS Summits on June 15, 2010 and November 9, 2010)

Agenda

- AMI Model Generation Barriers
- Automated AMI Model-generation flow
  - Example-1: 6.25 Gb/s
  - Example-2: 10.3125 Gb/s
- TX Model Correlation Study
  - -with Transistor Simulations
  - -with Measurements
- Benefits of Automated AMI flow

#1 AMI modeling barrier

Model Generation Time

AMI Modeling suppose to Speed-up System Design Cycle,
BUT, Model-generation takes Significant Time & Resources

....System Vendors have to wait a LONG time before accurate AMI models become available

Note: Vendors with NO experience in AMI modeling are spending 6-12+ months to come up with first-generation models

Models come very late in Design Cycle → used only for Validation, NOT Design

Page 3

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Why AMI-model generation takes so long?

Typical Signal Integrity Engineers are NOT programmers

....they are having "Nightmares" in trying to develop AMI models

- Cryptic Matlab/C++ code passed from System-Architectures → AMI Modeler (if lucky)
- Challenge to Convert Algorithm design Code → AMI format

0 months — Nightmare Begins
AMI 101, Decipher Code
4 months
8 months — Early Model prototypes
First-model to Customer
12 months

Page 4

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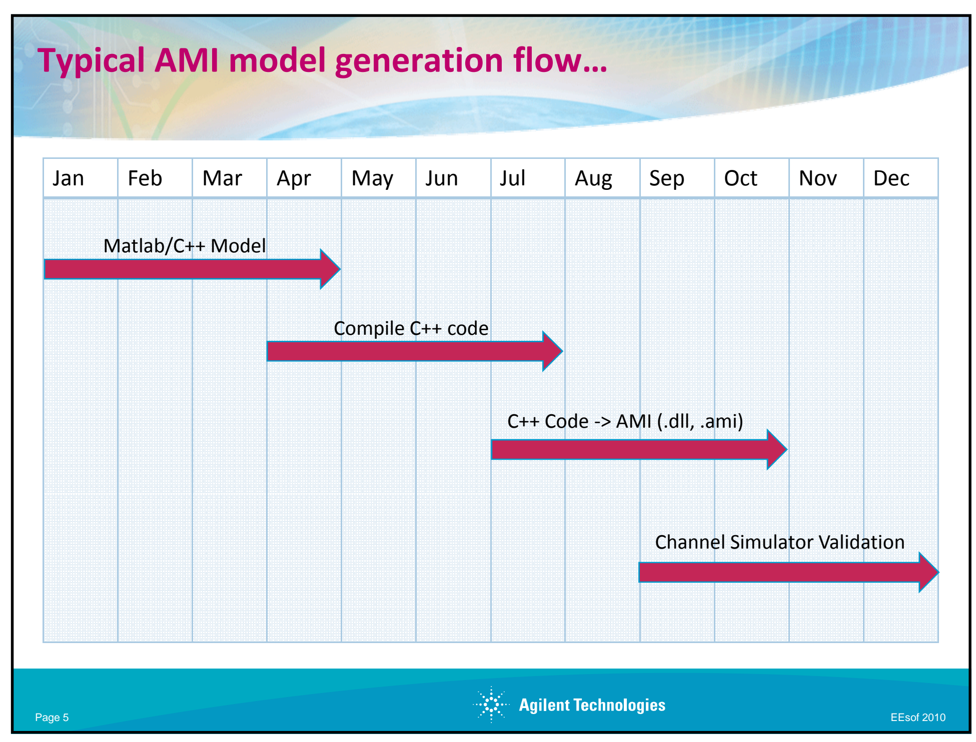
Typical AMI model generation flow…
Jan
Feb
Mar
Apr
May
Jun
Jul
Aug
Sep
Oct
Nov
Dec
Matlab/C++ Model
Compile C++ code
C++ Code -> AMI (.dll, .ami)
Channel Simulator Validation
Page 5
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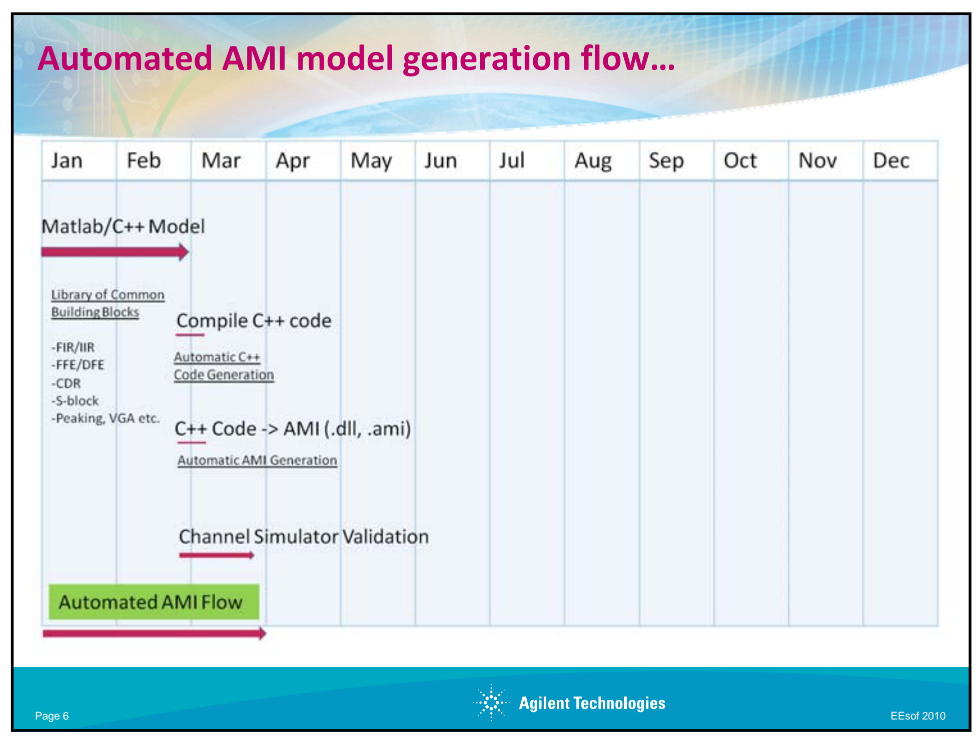
Automated AMI model generation flow…
Jan
Feb
Mar
Apr
May
Jun
Jul
Aug
Sep
Oct
Nov
Dec
Matlab/C++ Model
Library of Common
Building Blocks
-FIR/IIR
-FFE/DFE
-CDR
-S-block
-Peaking, VGA etc.
Compile C++ code
Automatic C++
Code Generation
C++ Code -> AMI (.dll, .ami)
Automatic AMI Generation
Channel Simulator Validation
Automated AMI Flow
Page 6
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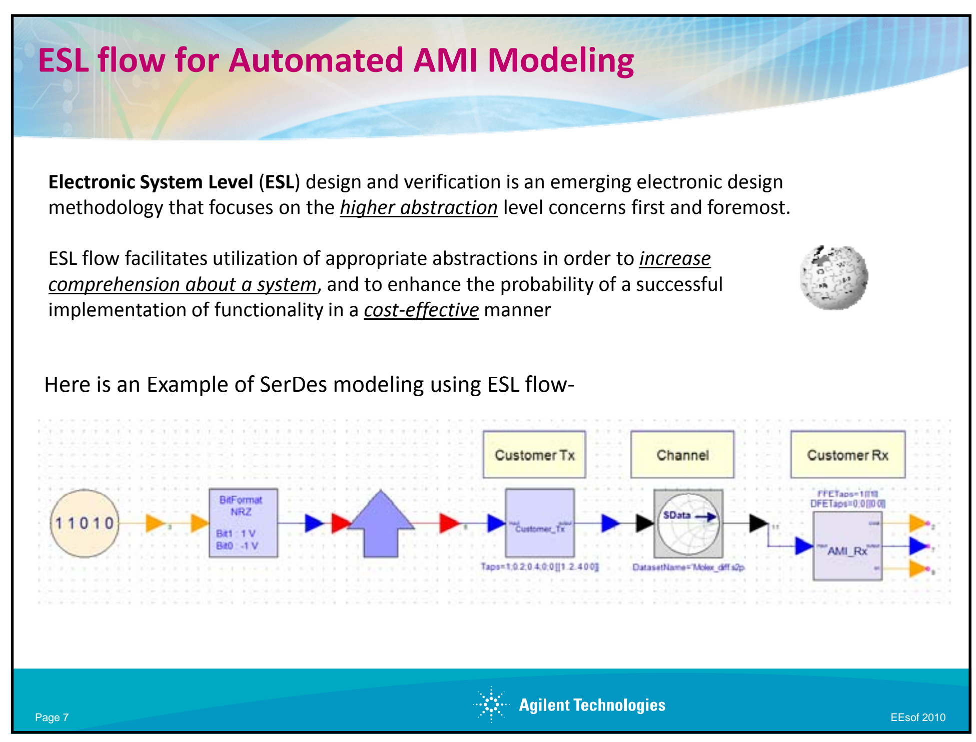
ESL flow for Automated AMI Modeling
Electronic System Level (**ESL**) design and verification is an emerging electronic design methodology that focuses on the *higher abstraction* level concerns first and foremost.
ESL flow facilitates utilization of appropriate abstractions in order to *increase comprehension about a system*, and to enhance the probability of a successful implementation of functionality in a *cost-effective* manner
Here is an Example of SerDes modeling using ESL flow-
Customer Tx
Channel
Customer Rx
11010
BitFormat
NRZ
Bit1 : 1 V
Bit0 : -1 V
SData
AMI_Rx
Page 7
Agilent Technologies
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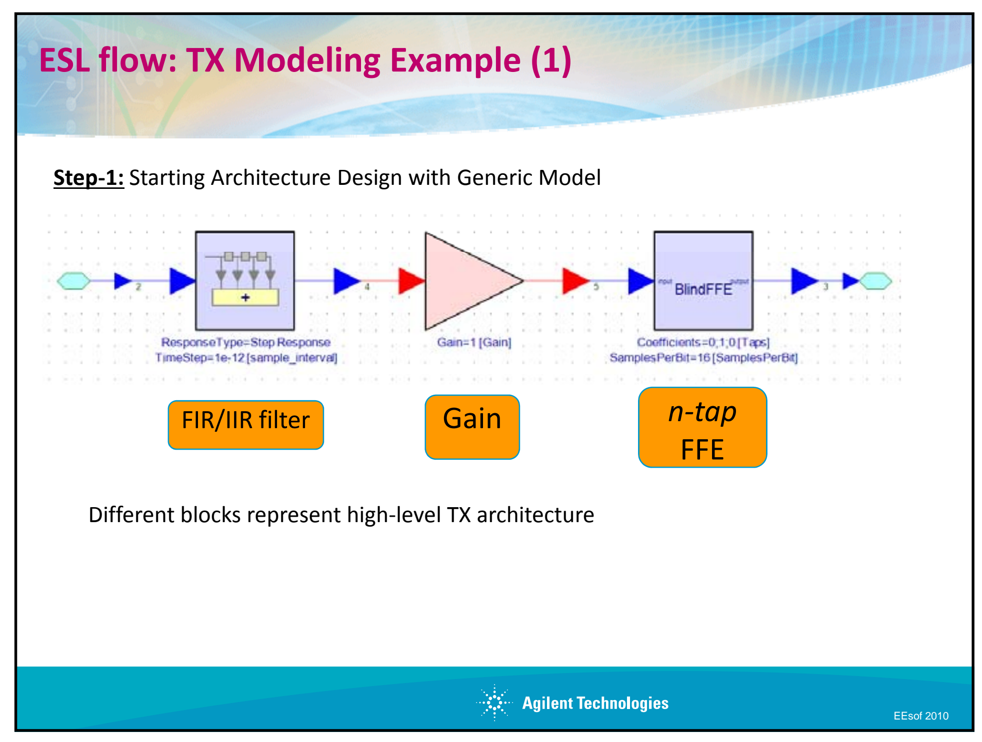
ESL flow: TX Modeling Example (1)
Step-1: Starting Architecture Design with Generic Model
ResponseType=Step Response
TimeStep=1e-12 [sample_interval]
Gain=1 [Gain]
BlindFFE
Coefficients=0;1;0 [Taps]
SamplesPerBit=16 [SamplesPerBit]
FIR/IIR filter
Gain
n-tap
FFE
Different blocks represent high-level TX architecture
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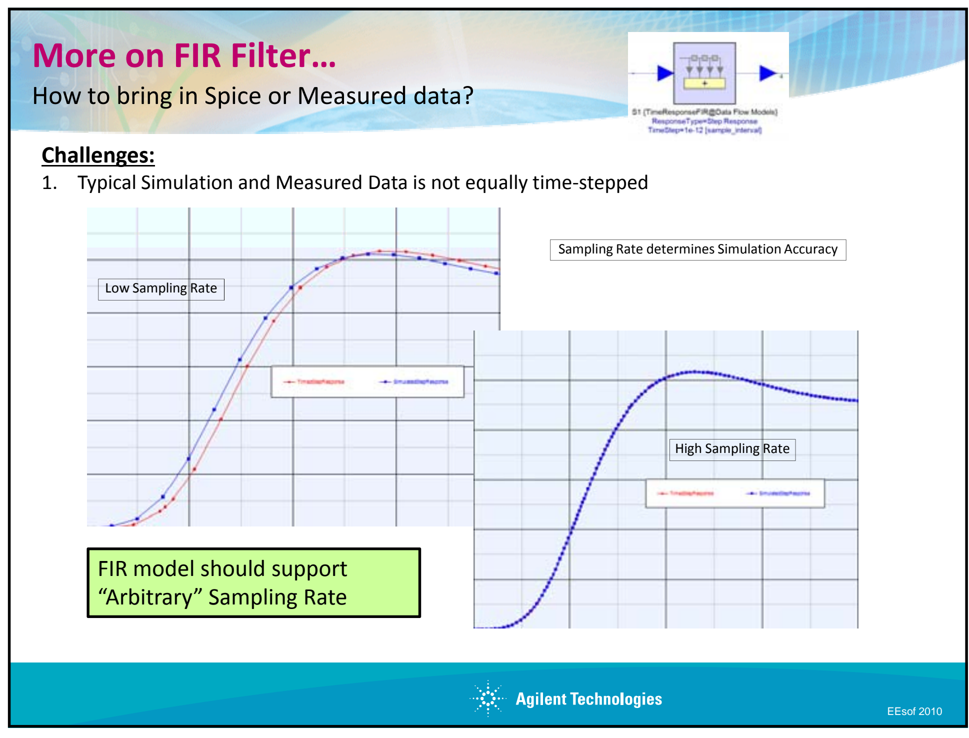
More on FIR Filter…
How to bring in Spice or Measured data?
Challenges:
1. Typical Simulation and Measured Data is not equally time-stepped
Sampling Rate determines Simulation Accuracy
Low Sampling Rate
High Sampling Rate
FIR model should support "Arbitrary" Sampling Rate
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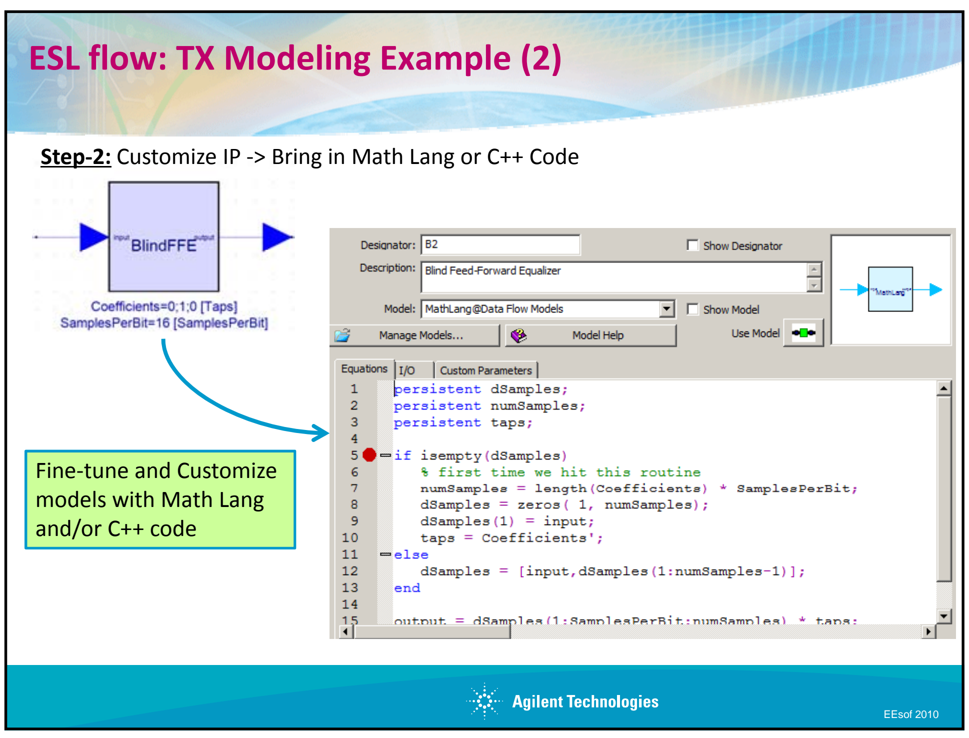
ESL flow: TX Modeling Example (2)
Step-2: Customize IP -> Bring in Math Lang or C++ Code
BlindFFE
Coefficients=0;1;0 [Taps]
SamplesPerBit=16 [SamplesPerBit]
Fine-tune and Customize models with Math Lang and/or C++ code
Designator: B2
Show Designator
Description: Blind Feed-Forward Equalizer
Model: MathLang@Data Flow Models
Show Model
Manage Models...
Model Help
Use Model
Equations
I/O
Custom Parameters
persistent dSamples;
persistent numSamples;
persistent taps;
if isempty(dSamples)
% first time we hit this routine
numSamples = length(Coefficients) * SamplesPerBit;
dSamples = zeros(1, numSamples);
dSamples(1) = input;
taps = Coefficients';
else
dSamples = [input,dSamples(1:numSamples-1)];
end
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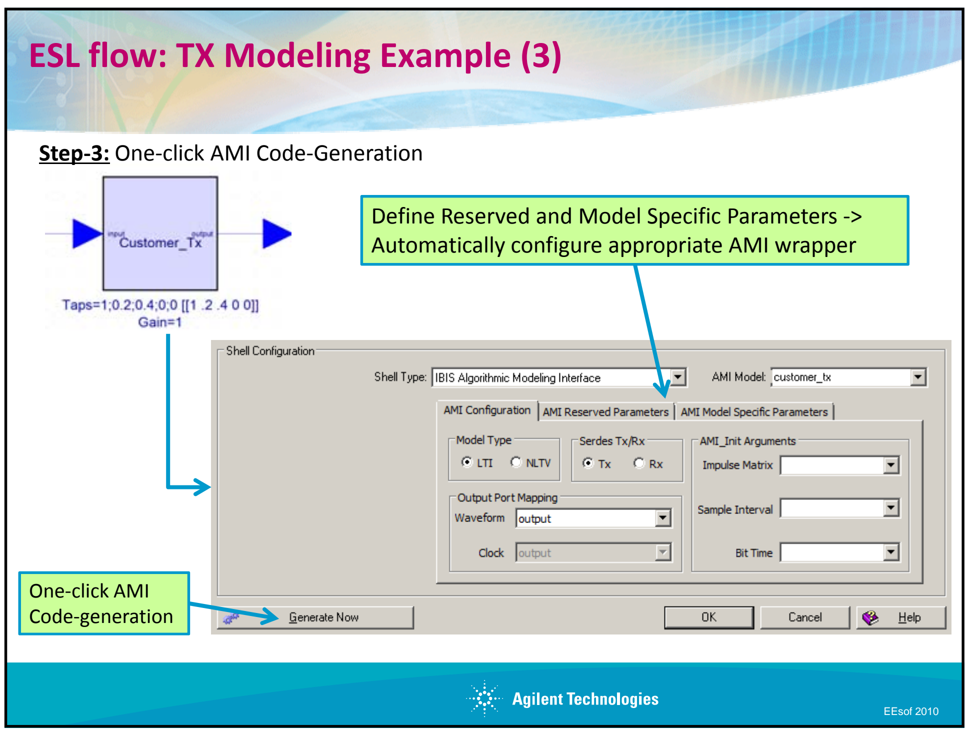
ESL flow: TX Modeling Example (3)
Step-3: One-click AMI Code-Generation
Customer_Tx
Taps=1;0.2;0.4;0;0 [[1 .2 .4 0 0]]
Gain=1
Define Reserved and Model Specific Parameters ->
Automatically configure appropriate AMI wrapper
Shell Configuration
Shell Type: IBIS Algorithmic Modeling Interface
AMI Model: customer_tx
AMI Configuration
AMI Reserved Parameters
AMI Model Specific Parameters
Model Type
LTI
NLTV
Serdes Tx/Rx
Tx
Rx
AMI_Init Arguments
Impulse Matrix
Output Port Mapping
Waveform
output
Sample Interval
Clock
Bit Time
One-click AMI
Code-generation
Generate Now
OK
Cancel
Help
Agilent Technologies
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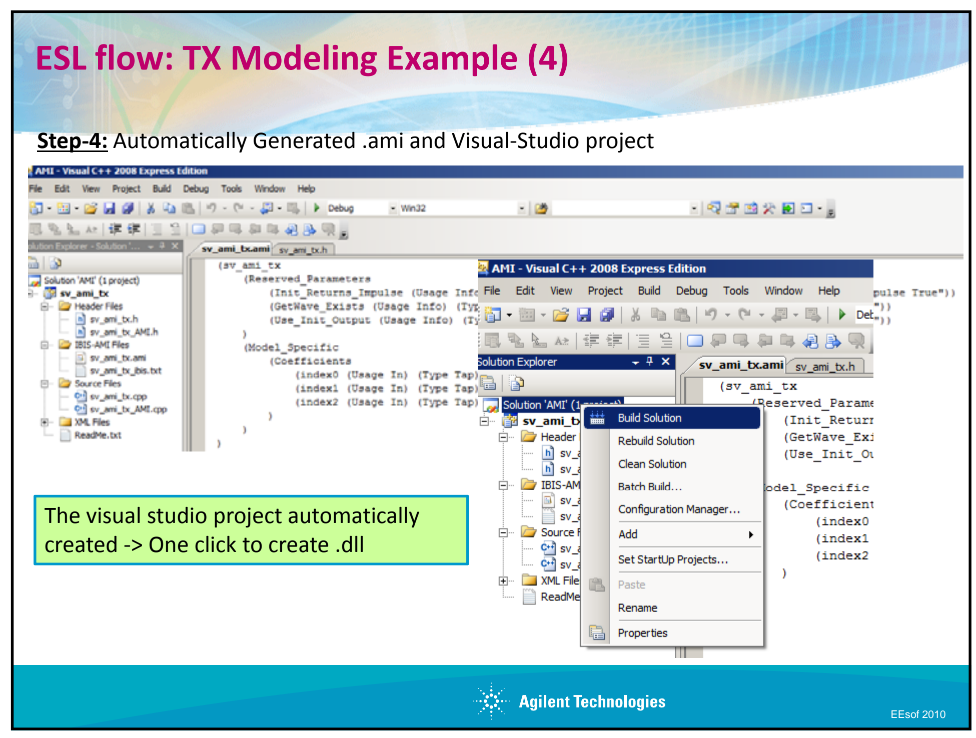
ESL flow: TX Modeling Example (4)
Step-4: Automatically Generated .ami and Visual-Studio project
AMI - Visual C++ 2008 Express Edition
File Edit View Project Build Debug Tools Window Help
Solution Explorer
Solution 'AMI' (1 project)
sv_ami_tx
Header Files
sv_ami_tx.h
sv_ami_tx_AMI.h
IBIS-AMI Files
sv_ami_tx.ami
sv_ami_tx_ibis.txt
Source Files
sv_ami_tx.cpp
sv_ami_tx_AMI.cpp
XML Files
ReadMe.txt
sv_ami_tx.ami
sv_ami_tx.h
(sv_ami_tx
(Reserved_Parameters
(Init_Returns_Impulse (Usage Info)
(GetWave_Exists (Usage Info)
(Use_Init_Output (Usage Info)
(Model_Specific
(Coefficients
(index0 (Usage In) (Type Tap)
(index1 (Usage In) (Type Tap)
(index2 (Usage In) (Type Tap)
Build Solution
Rebuild Solution
Clean Solution
Batch Build...
Configuration Manager...
Add
Set StartUp Projects...
Paste
Rename
Properties
The visual studio project automatically
created -> One click to create .dll
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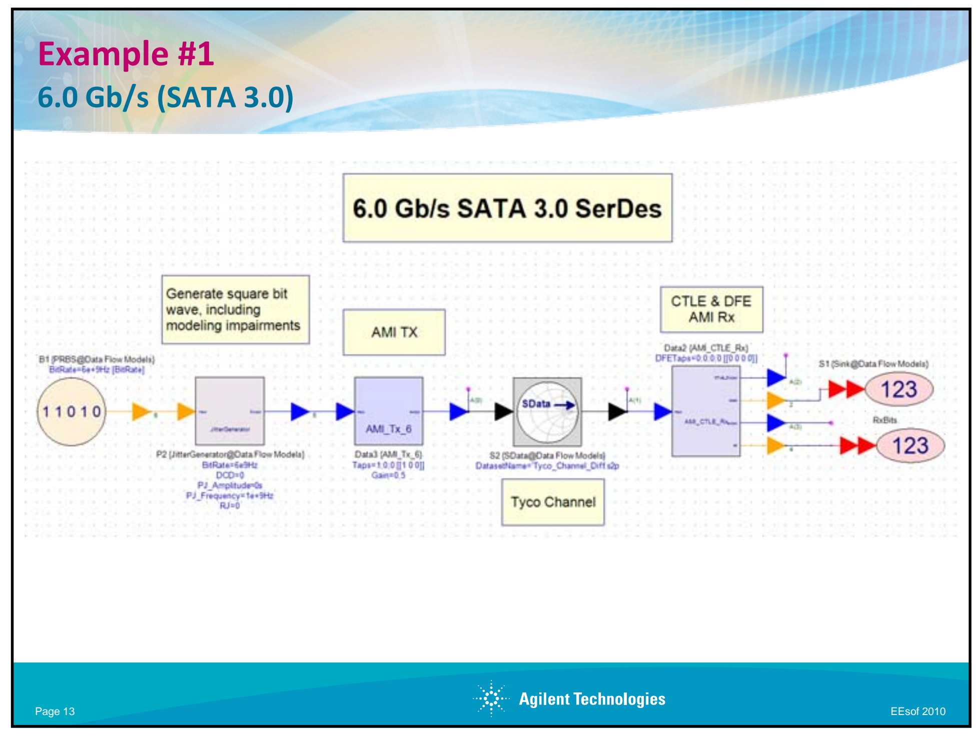
Example #1
6.0 Gb/s (SATA 3.0)
6.0 Gb/s SATA 3.0 SerDes
Generate square bit wave, including modeling impairments
AMI TX
CTLE & DFE AMI Rx
11010
AMI_Tx_6
SData
123
123
Tyco Channel
Page 13
Agilent Technologies
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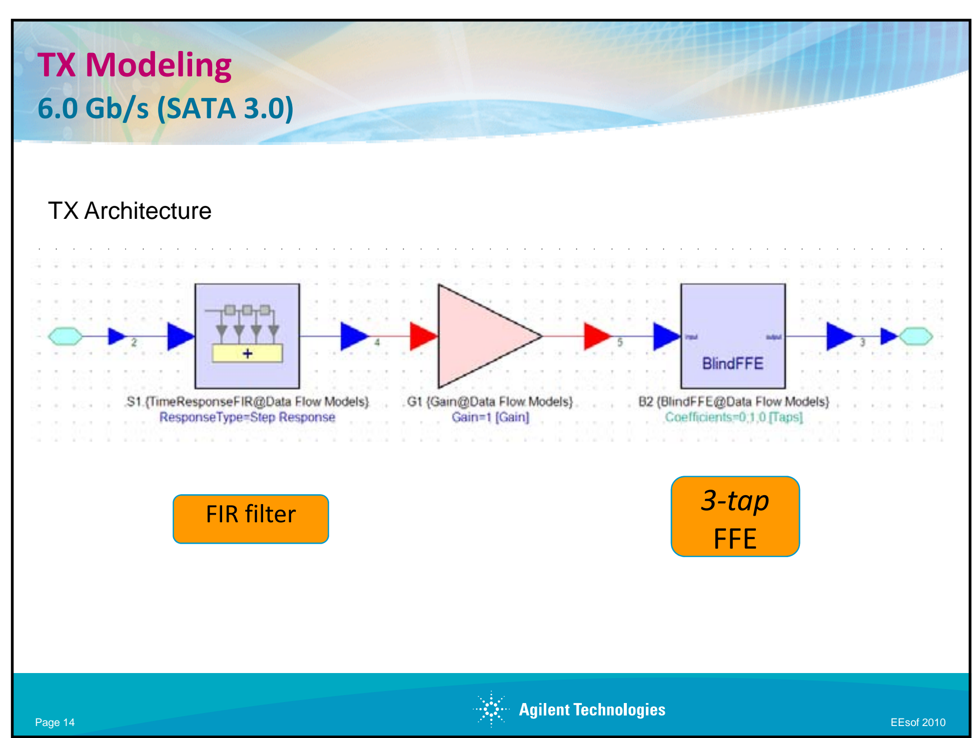
TX Modeling
6.0 Gb/s (SATA 3.0)
TX Architecture
BlindFFE
S1 {TimeResponseFIR@Data Flow Models}
ResponseType=Step Response
G1 {Gain@Data Flow Models}
Gain=1 [Gain]
B2 {BlindFFE@Data Flow Models}
Coefficients=0,1,0 [Taps]
FIR filter
3-tap
FFE
Page 14
Agilent Technologies
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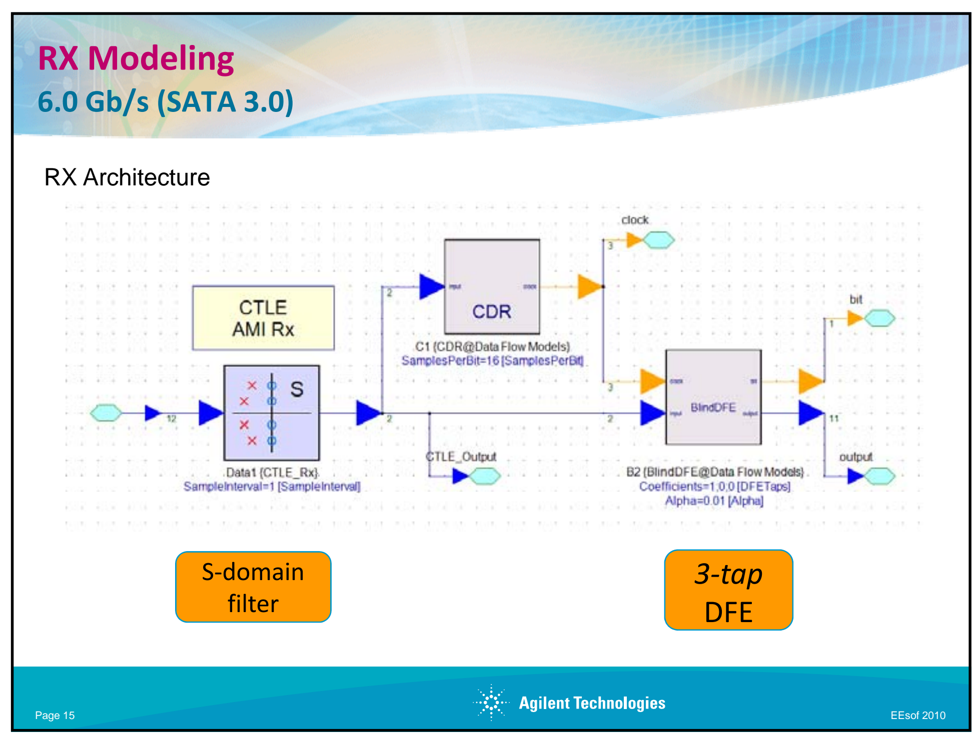
RX Modeling
6.0 Gb/s (SATA 3.0)
RX Architecture
CTLE
AMI Rx
CDR
C1 {CDR@Data Flow Models}
SamplesPerBit=16 [SamplesPerBit]
clock
bit
BlindDFE
CTLE_Output
output
Data1 {CTLE_Rx}
SampleInterval=1 [SampleInterval]
B2 {BlindDFE@Data Flow Models}
Coefficients=1,0,0 [DFETaps]
Alpha=0.01 [Alpha]
S-domain filter
3-tap DFE
Page 15
Agilent Technologies
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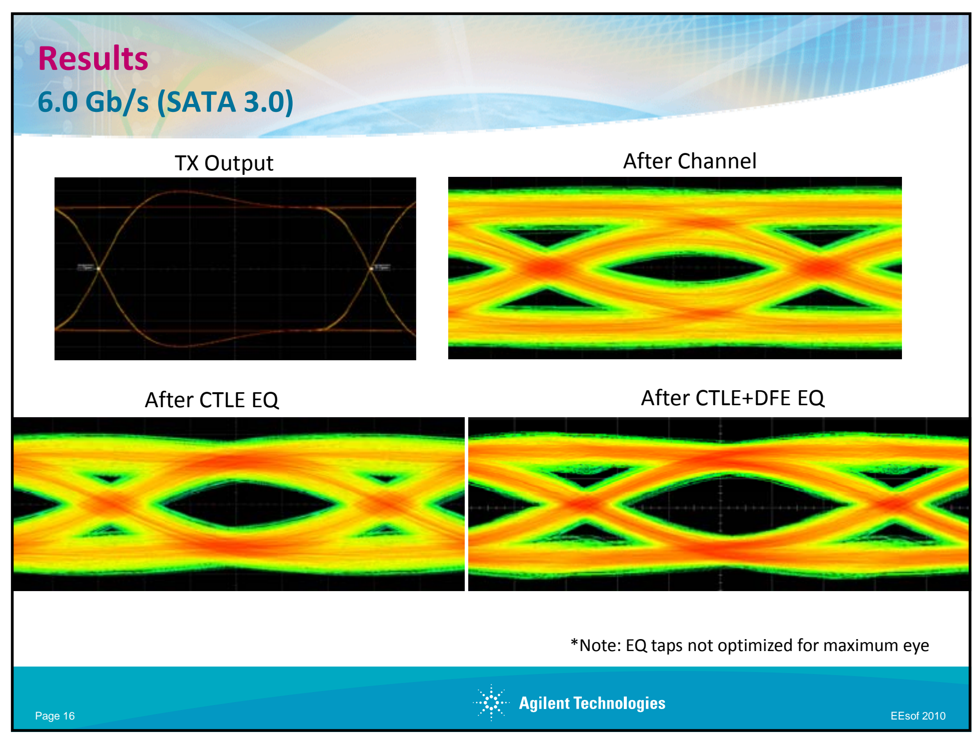
Results
6.0 Gb/s (SATA 3.0)
TX Output
After Channel
After CTLE EQ
After CTLE+DFE EQ
*Note: EQ taps not optimized for maximum eye
Page 16
Agilent Technologies
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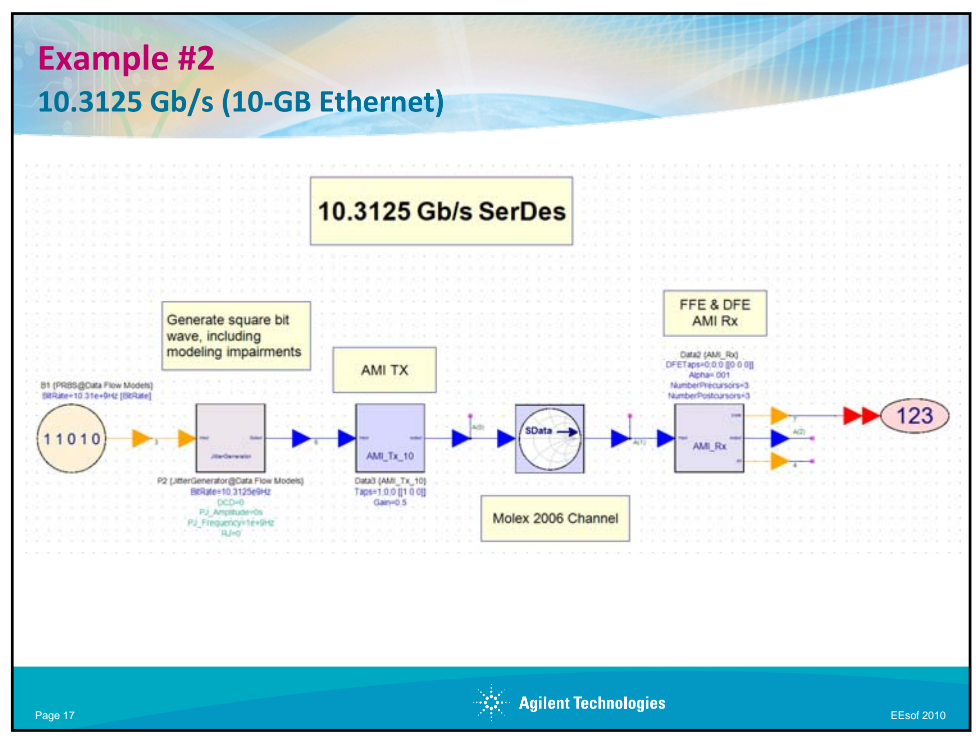
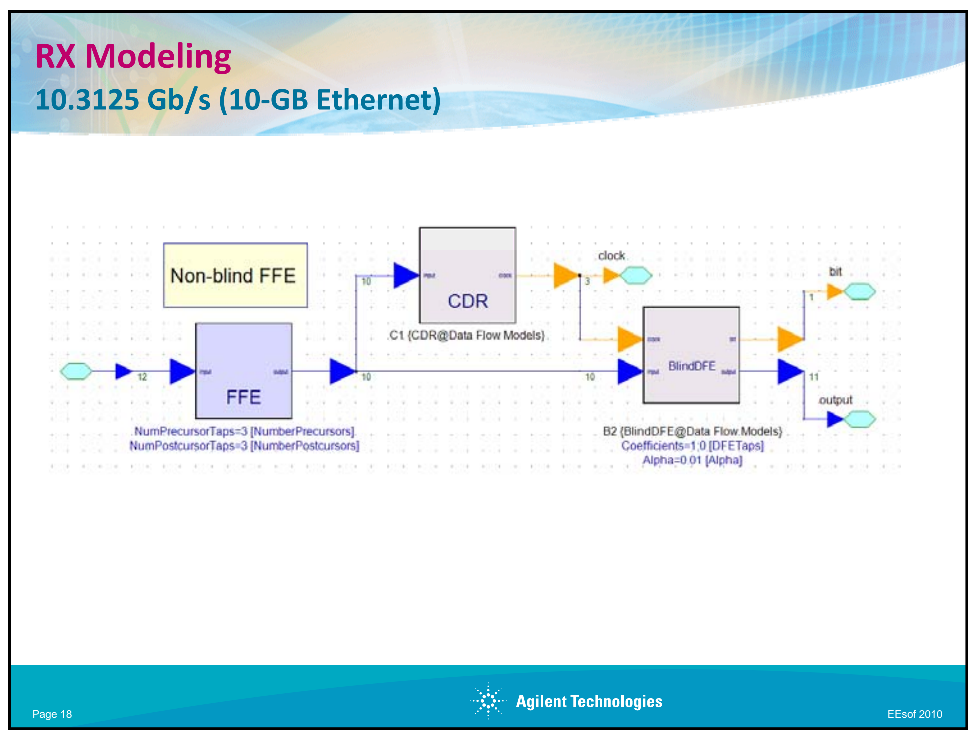
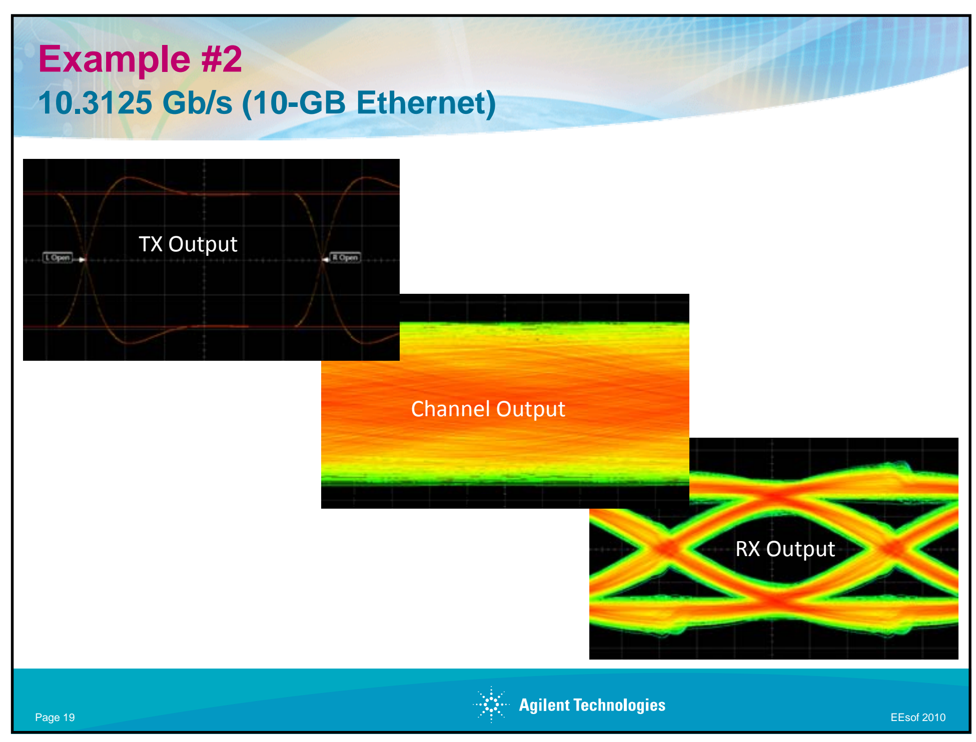

Example #2
10.3125 Gb/s (10-GB Ethernet)
10.3125 Gb/s SerDes
Generate square bit wave, including modeling impairments
AMI TX
FFE & DFE AMI Rx
Molex 2006 Channel
11010
123
Page 17
Agilent Technologies
EEsof 2010


RX Modeling
10.3125 Gb/s (10-GB Ethernet)
Non-blind FFE
CDR
C1 {CDR@Data Flow Models}
clock
bit
FFE
BlindDFE
output
NumPrecursorTaps=3 [NumberPrecursors]
NumPostcursorTaps=3 [NumberPostcursors]
B2 {BlindDFE@Data Flow Models}
Coefficients=1.0 [DFETaps]
Alpha=0.01 [Alpha]
Page 18
Agilent Technologies
EEsof 2010


Example #2
10.3125 Gb/s (10-GB Ethernet)
TX Output
Channel Output
RX Output
Page 19
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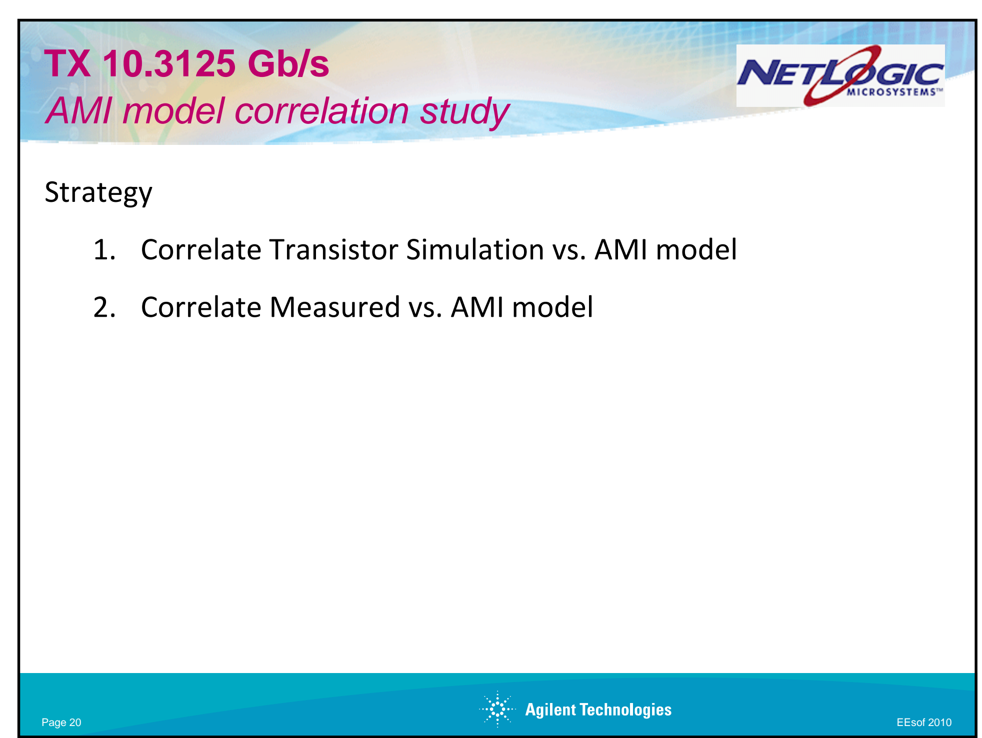
TX 10.3125 Gb/s
AMI model correlation study
NETLOGIC MICROSYSTEMS
Strategy
1. Correlate Transistor Simulation vs. AMI model
2. Correlate Measured vs. AMI model
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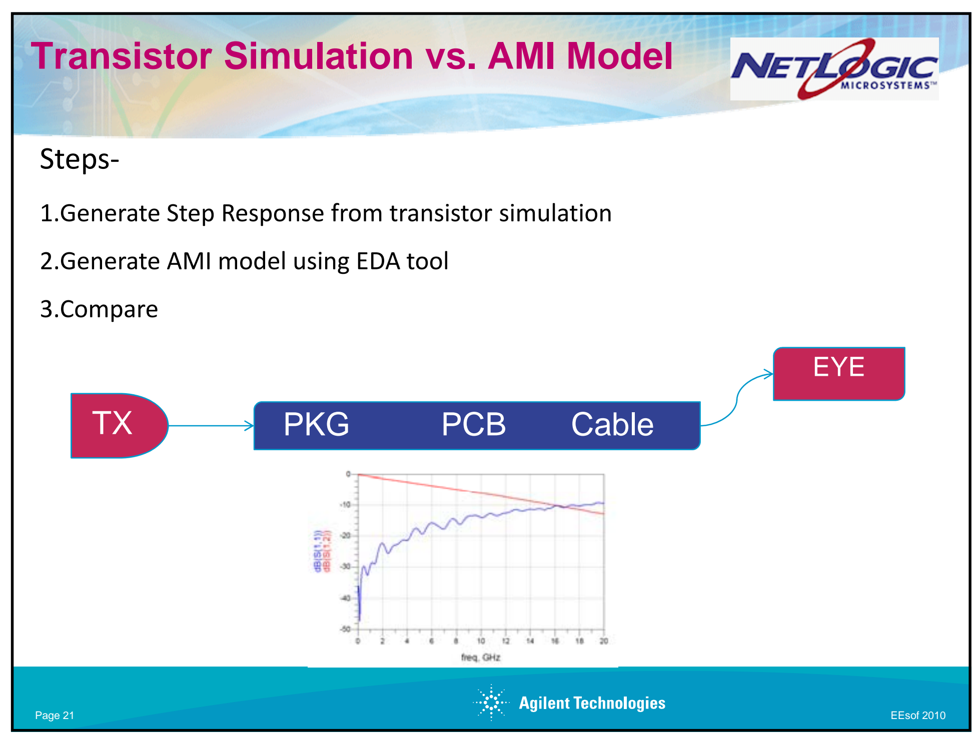
Transistor Simulation vs. AMI Model
NETLOGIC MICROSYSTEMS
Steps-
1.Generate Step Response from transistor simulation
2.Generate AMI model using EDA tool
3.Compare
EYE
TX
PKG
PCB
Cable
freq, GHz
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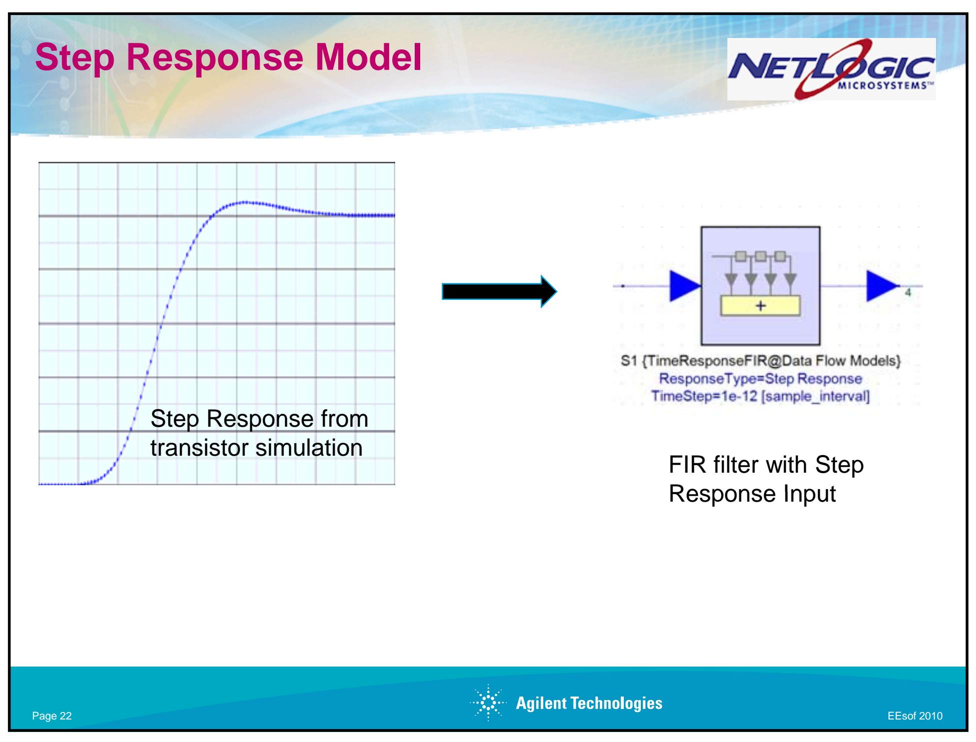
Step Response Model
NETLOGIC MICROSYSTEMS
Step Response from transistor simulation
S1 {TimeResponseFIR@Data Flow Models}
ResponseType=Step Response
TimeStep=1e-12 [sample_interval]
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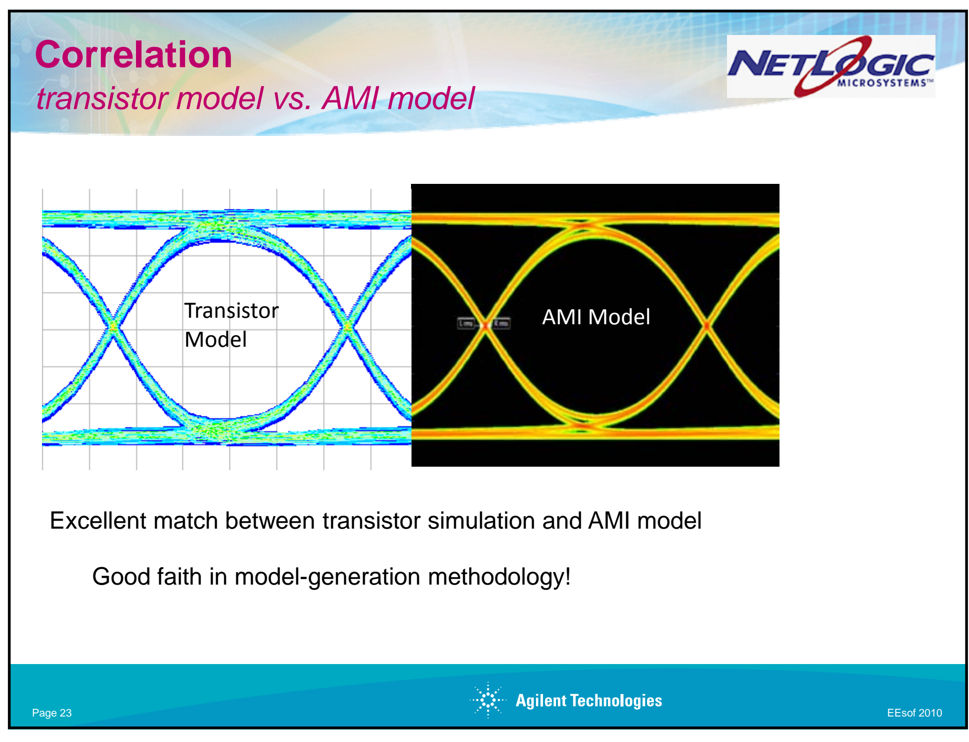
Correlation
transistor model vs. AMI model
NETLOGIC MICROSYSTEMS
Transistor Model
AMI Model
Excellent match between transistor simulation and AMI model
Good faith in model-generation methodology!
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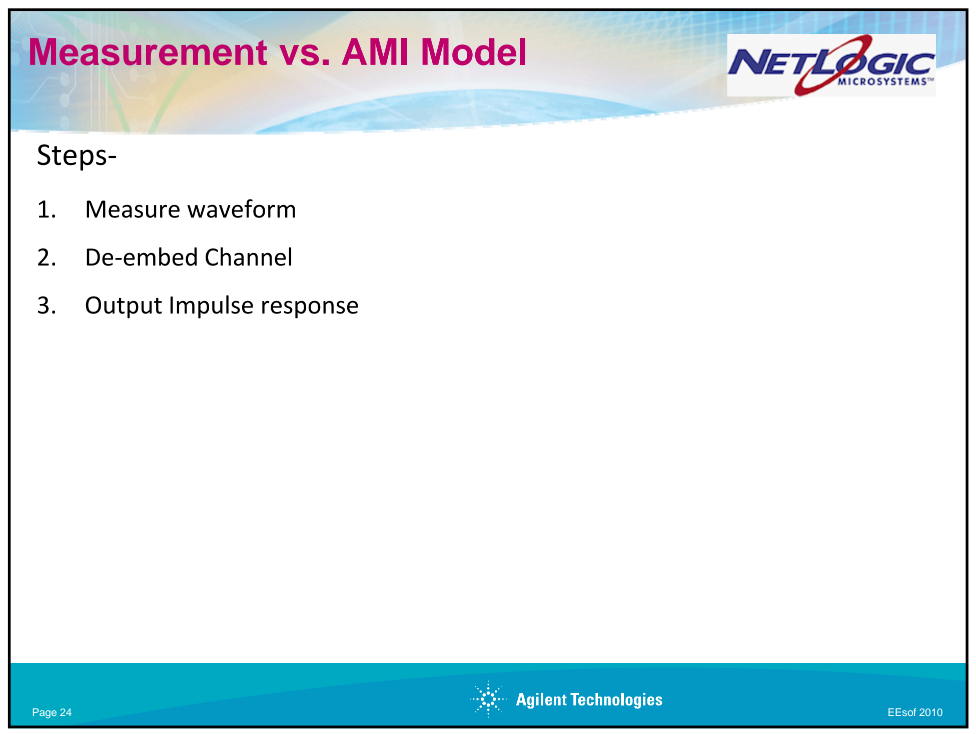
Measurement vs. AMI Model
NETLOGIC MICROSYSTEMS
Steps-
1. Measure waveform
2. De-embed Channel
3. Output Impulse response
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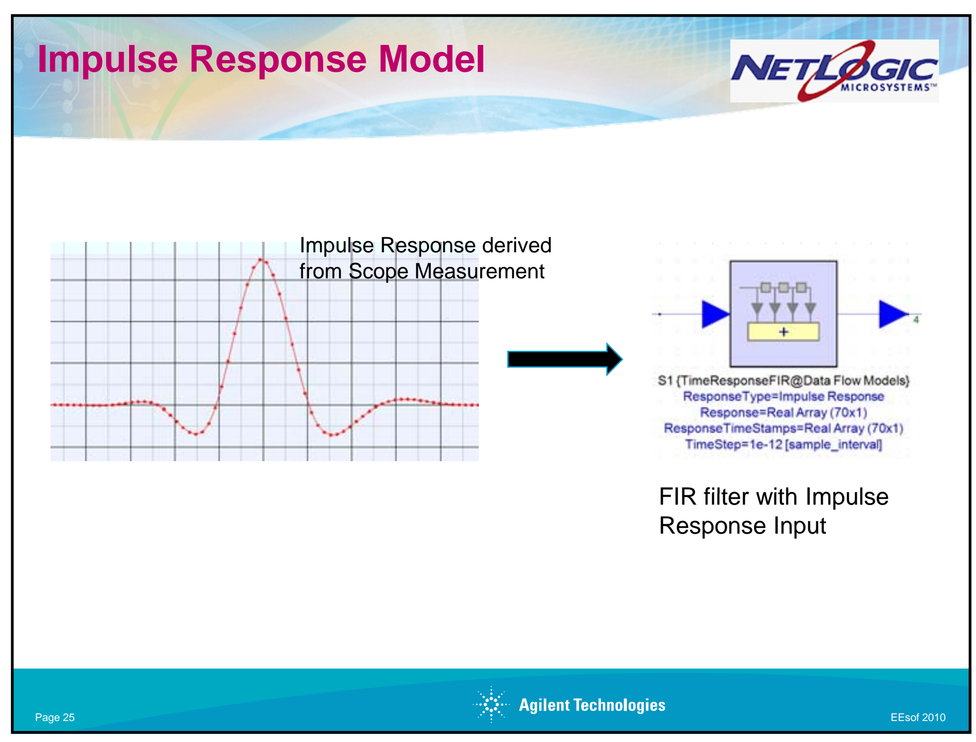
Impulse Response Model
NETLOGIC MICROSYSTEMS
Impulse Response derived from Scope Measurement
S1 {TimeResponseFIR@Data Flow Models}
ResponseType=Impulse Response
Response=Real Array (70x1)
ResponseTimeStamps=Real Array (70x1)
TimeStep=1e-12 [sample_interval]
FIR filter with Impulse Response Input
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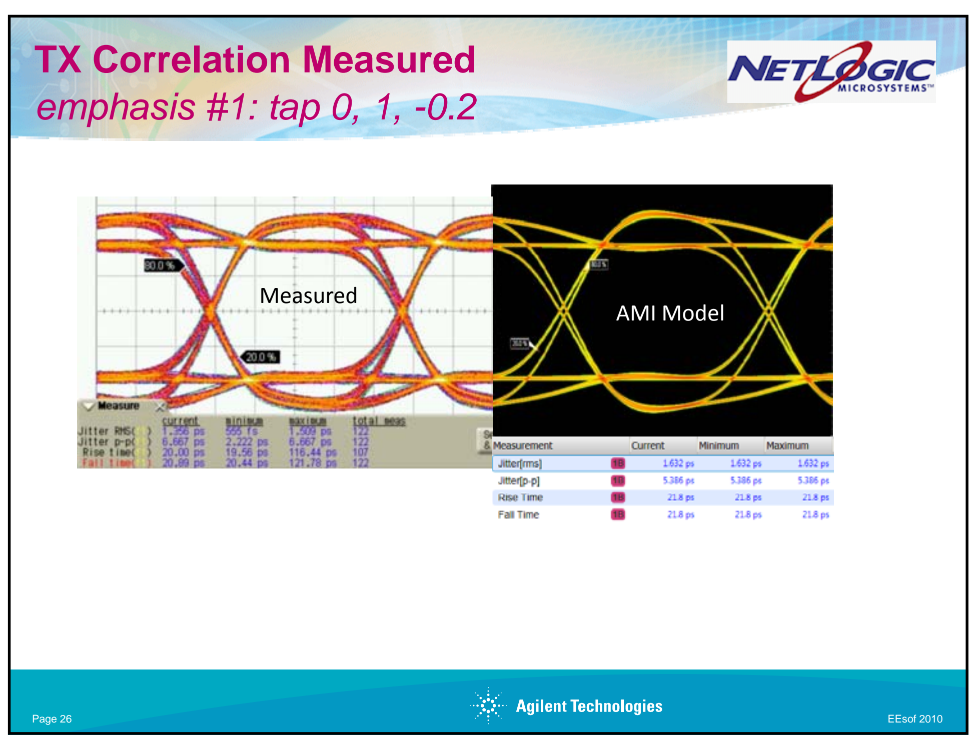
TX Correlation Measured
emphasis #1: tap 0, 1, -0.2
NETLOGIC MICROSYSTEMS
Measured
AMI Model
Measurement
Current
Minimum
Maximum
Jitter(rms)
Jitter(p-p)
Rise Time
Fall Time
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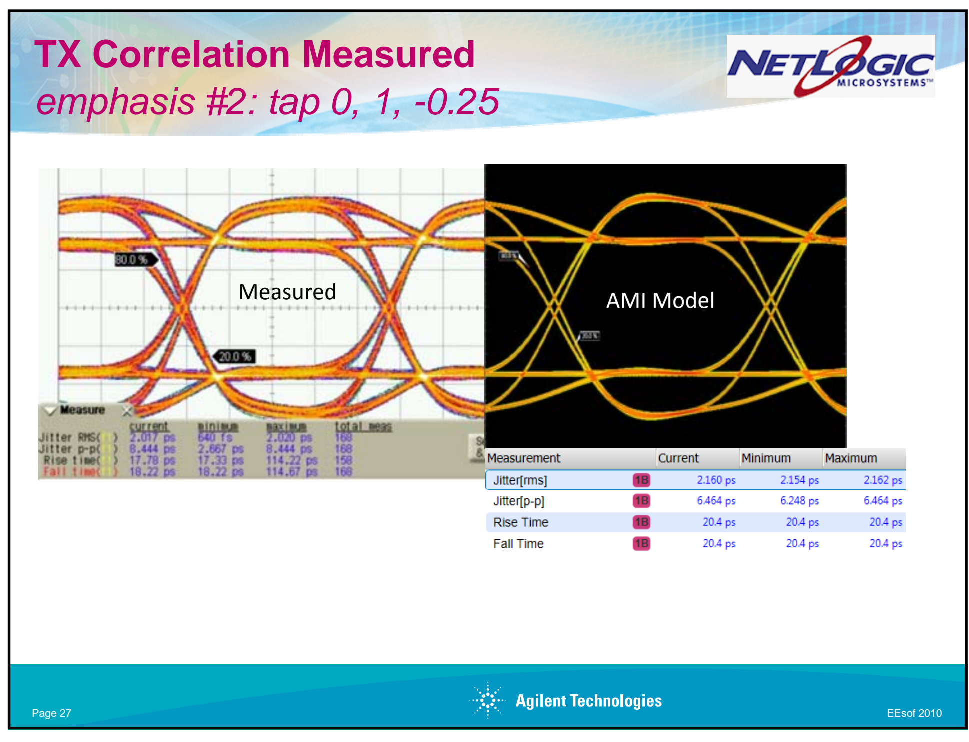
TX Correlation Measured
emphasis #2: tap 0, 1, -0.25
NETLOGIC MICROSYSTEMS
80.0 %
Measured
20.0 %
AMI Model
Measure
current minimum maximum total meas
Jitter RMS( ) 2.017 ps 640 fs 2.020 ps 168
Jitter p-p( ) 8.444 ps 2.667 ps 8.444 ps 168
Rise time( ) 17.78 ps 17.33 ps 114.22 ps 158
Fall time( ) 18.22 ps 18.22 ps 114.67 ps 168
Measurement Current Minimum Maximum
Jitter[rms] 1B 2.160 ps 2.154 ps 2.162 ps
Jitter[p-p] 1B 6.464 ps 6.248 ps 6.464 ps
Rise Time 1B 20.4 ps 20.4 ps 20.4 ps
Fall Time 1B 20.4 ps 20.4 ps 20.4 ps
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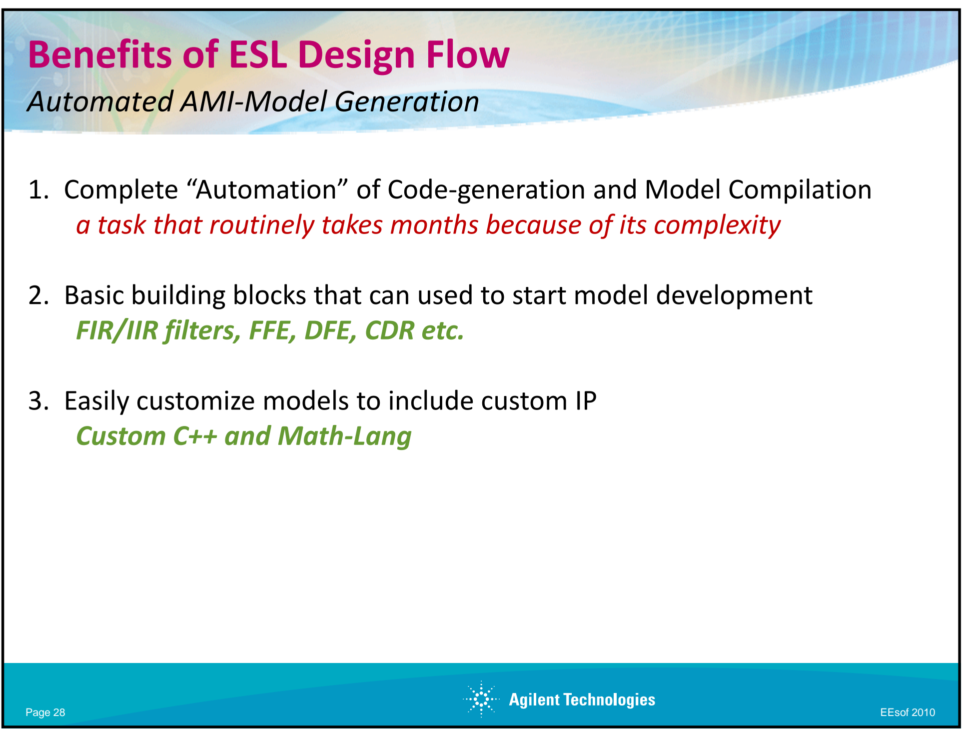
Benefits of ESL Design Flow
Automated AMI-Model Generation
1. Complete "Automation" of Code-generation and Model Compilation
a task that routinely takes months because of its complexity
2. Basic building blocks that can used to start model development
FIR/IIR filters, FFE, DFE, CDR etc.
3. Easily customize models to include custom IP
Custom C++ and Math-Lang
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Extending/Leveraging IBIS Constructs to Model High-Speed I/Os and Packages using AMI, Spice, and S-Parameters

John Lin
Flextronics, Inc

Taranjit Kukal, Feras Al-Hawari, Ambrish Varma
Cadence Design Systems, Inc.

Presented by: Kevin Liu – Cadence

Note: Previously presented at IBIS Summit in China Nov. 9

Asian IBIS Summit
Taipei, Taiwan
November 12, 2010

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Agenda

- **IBIS Overview**
- **Why extend IBIS to SPICE models**
  - **Current Limitations**
- **Leveraging [External Model] to allow including Package S-Parameters for High Speed simulation**
  - **Example**
- **Extending [External Model] to:**
  - Simulate VI-VT model in conjunction with Spice sub-circuits that represent RDL elements, DSP Spice code, etc.
  - Dynamically switch sub-circuits to take care of corners and parametric variations.
  - Simulate AMI with [External Model] that represents analog IO modeled in Spice or S-parameters.
- **Summary**

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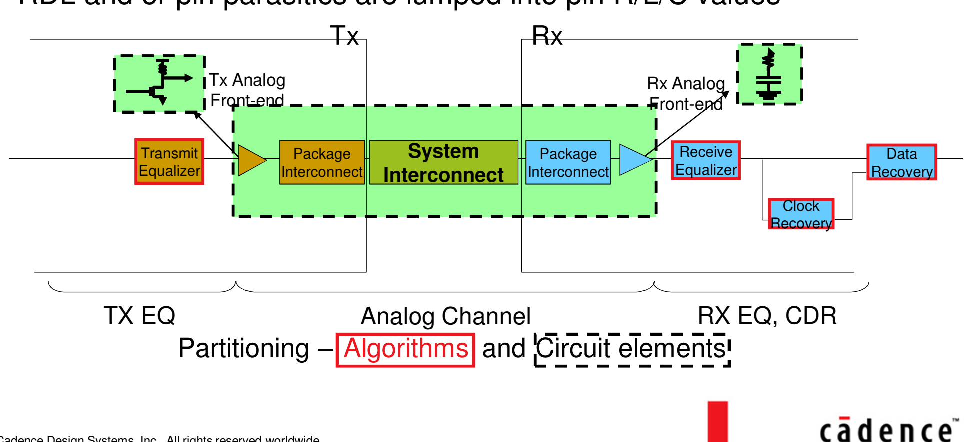
IBIS overview

- Analog IO model is modelled by IBIS VI and VT curves
- Equalization (DSP algorithmic) portion of IO model is modelled by AMI C-code (Algorithmic Model Interface) that is pointed by IBIS model
- RDL and or pin parasitics are lumped into pin R/L/C values



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Why extend IBIS to SPICE models

- **At high frequencies, IO buffers could have portions that need to be modeled using Spice files**:
  - On DIE Terminations (ODT) that vary with frequencies need to be expressed as s-parameters or RLGC Spice files
  - On DIE RDL parasitics become significant and vary with frequencies and hence have to be expressed as s-parameters or SPEF
  - Analog portion of IO-buffer is expressed as Spice as against VI-VT curve; s-parameters can also be used to describe transfer characteristics of IO-buffer amplifiers.
  - Some algorithmic portion may be modeled in Spice as against AMI code

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Why extend IBIS to SPICE models

- **Multiple Sub-circuits / Spice files**
  - Different Spice sub-circuits could be applicable for different process corners. On-DIE RDL could be expressed as different s-parameter files for typ/min/max conditions.
  - Different Spice sub-circuits could be applicable for different buffer configurations. For example, Pre-emphasis portion could have been modeled as Spice using different sub-circuits for different settings.
  - ODT could be a function of current being drawn out of IO-buffer (Dynamic ODT) and could have been expressed as behavioral Spice, Verilog-A

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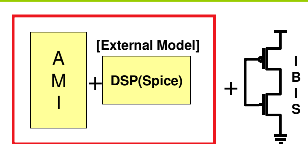
Current Approach and Limitations

- Package parasitics can be used as S-parameters by including them as part of interconnect network in a way similar to external interconnect parasitics.
  - Limitation
    - RDL parasitics that need to be part of IO-buffer characterization are treated as interconnects and assumed bi-directional.
- Spice IO-buffers can be included as part of IBIS using [External Model] Keyword.
  - Limitations
    - Cannot model DSP (in SPICE) in conjunction with AMI model
      - Use of [External Model] in conjunction with VI-VT (IBIS) is not recommended today
    - Does not directly support s-parameters (Touchstone)
      - For example, it is not easy to model RDL and other elements in conjunction with VI-VT curves cannot take care of process corners and parametric selection of subcircuits



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Leveraging [External Model] to Support Package S-Parameters

- Long-term: IBIS model should have Keywords to support Touchstone S-parameters under Package section, with fields to
  - point to touchstone file from the Package section
  - provide port-mapping of IO-buffer pins to s-parameter ports
  - R/L/C values should be ignored by SI tools if s-parameter file is used
- Short-term: This can be achieved through use of [External Model] keyword
  - Set R/L/C values in package keyword as ZERO (to avoid double counting)
  - Point to the touchstone file of the package inside the Spice subcircuits

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Example : Support for S-parameters for package parasitics using [External Model]

- Use IBIS Device with 4 pins (1, 2, 3, and 4)
- Pins 1 and 2 are +ve and -ve diff pins respectively, with a “tx” diff model assigned to both of them
- Pins 3 and 4 are +ve and -ve diff pins respectively, with a “rx” tdiff model assigned to both of them
- Tx and Rx contain corresponding
  - [External Model] section

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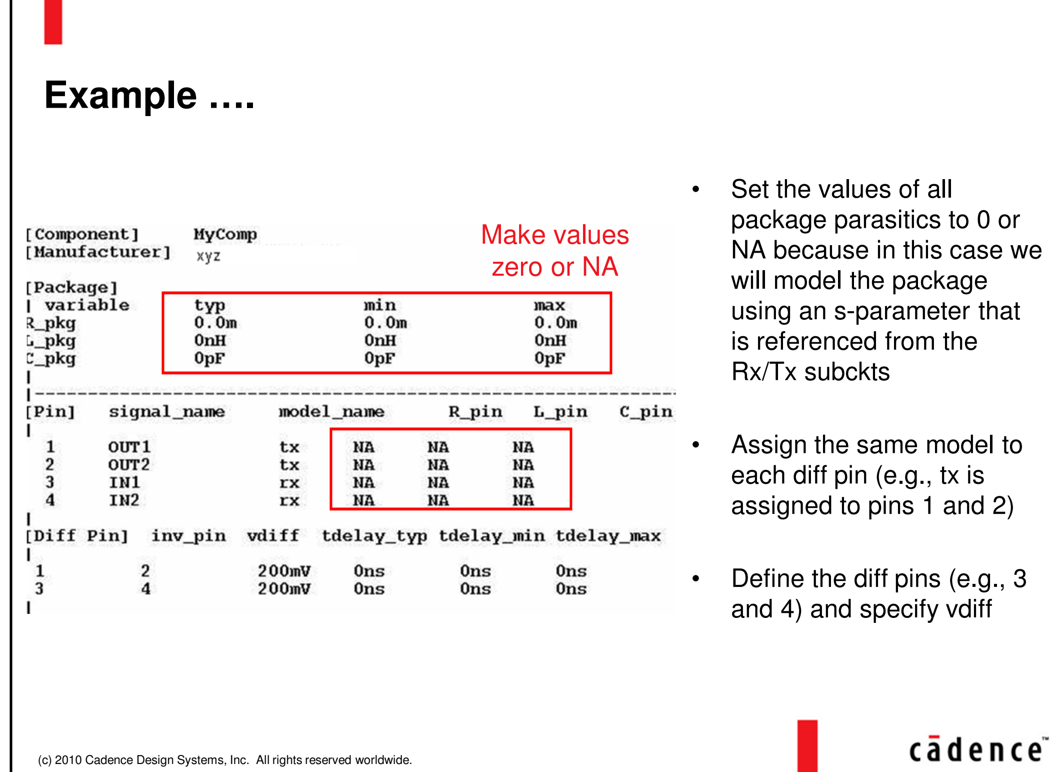
Example ….
[Component] MyComp
[Manufacturer] xyz
[Package]
| variable typ min max
R_pkg 0.0m 0.0m 0.0m
L_pkg 0nH 0nH 0nH
C_pkg 0pF 0pF 0pF
|
|---
[Pin] signal_name model_name R_pin L_pin C_pin
|
1 OUT1 tx NA NA NA
2 OUT2 tx NA NA NA
3 IN1 rx NA NA NA
4 IN2 rx NA NA NA
|
[Diff Pin] inv_pin vdiff tdelay_typ tdelay_min tdelay_max
|
1 2 200mV 0ns 0ns 0ns
3 4 200mV 0ns 0ns 0ns
|
Make values zero or NA
• Set the values of all package parasitics to 0 or NA because in this case we will model the package using an s-parameter that is referenced from the Rx/Tx subckts
• Assign the same model to each diff pin (e.g., tx is assigned to pins 1 and 2)
• Define the diff pins (e.g., 3 and 4) and specify vdiff
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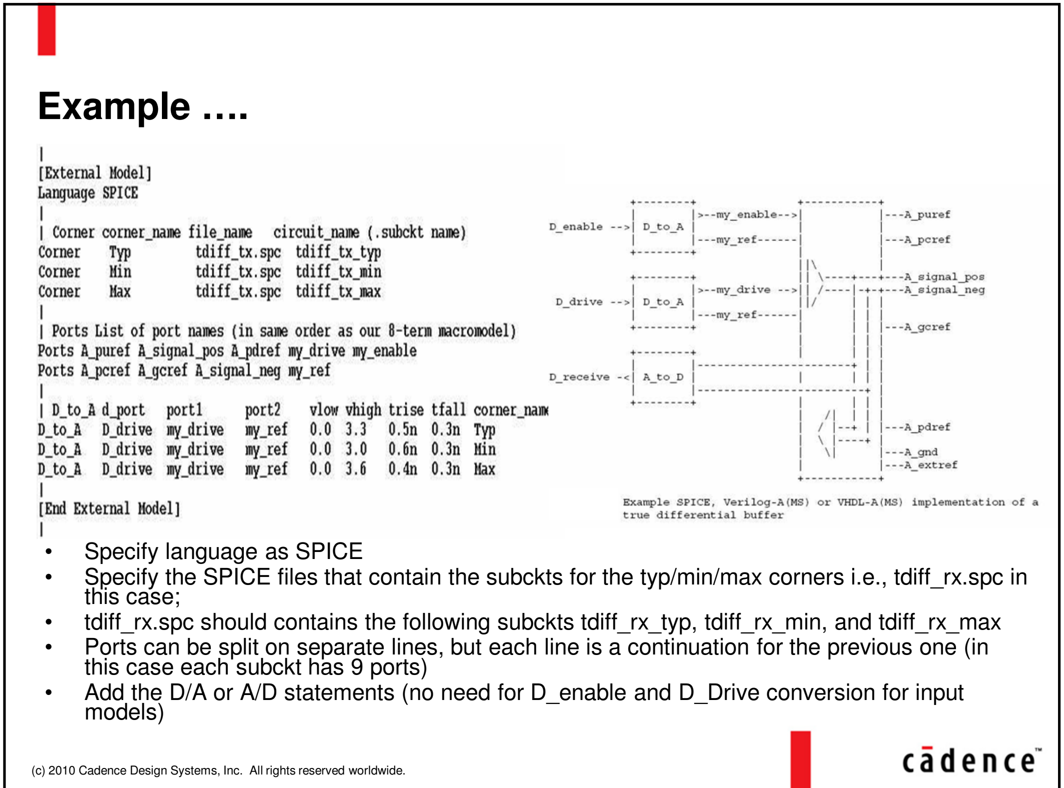
Example ….
|
[External Model]
Language SPICE
|
| Corner corner_name file_name circuit_name (.subckt name)
Corner Typ tdiff_tx.spc tdiff_tx_typ
Corner Min tdiff_tx.spc tdiff_tx_min
Corner Max tdiff_tx.spc tdiff_tx_max
|
| Ports List of port names (in same order as our 8-term macromodel)
Ports A_puref A_signal_pos A_pdref my_drive my_enable
Ports A_pcref A_gcref A_signal_neg my_ref
|
| D_to_A d_port port1 port2 vlow vhigh trise tfall corner_name
D_to_A D_drive my_drive my_ref 0.0 3.3 0.5n 0.3n Typ
D_to_A D_drive my_drive my_ref 0.0 3.0 0.6n 0.3n Min
D_to_A D_drive my_drive my_ref 0.0 3.6 0.4n 0.3n Max
|
[End External Model]
|
D_enable
D_to_A
my_enable
my_ref
A_puref
A_pcref
A_signal_pos
A_signal_neg
D_drive
my_drive
A_gcref
D_receive
A_to_D
A_pdref
A_gnd
A_extref
Example SPICE, Verilog-A(MS) or VHDL-A(MS) implementation of a true differential buffer
• Specify language as SPICE
• Specify the SPICE files that contain the subckts for the typ/min/max corners i.e., tdiff_rx.spc in this case;
• tdiff_rx.spc should contains the following subckts tdiff_rx_typ, tdiff_rx_min, and tdiff_rx_max
• Ports can be split on separate lines, but each line is a continuation for the previous one (in this case each subckt has 9 ports)
• Add the D/A or A/D statements (no need for D_enable and D_Drive conversion for input models)
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Example ….

```
.subckt tdiff_tx_typ 1 2 3 my_drive my_enable 6 7 8 my_ref
* The terminals in an 8-terminal differential MacroModel are as follows:
*     power = 1
*     outp = 2
*     ground = 3
*     input = 4
*     enable = 5
*     power_clamp_reference = 6
*     ground_clamp_reference = 7
*     outn = 8

v1 my_ref 0 0
r1 my_enable 0 1e6
r2 my_drive my_ref 1e6

erx in 0 v='v(my_drive,my_ref)'
einv inv 0 v='v(1) - v(in)'

S1 in 2 inv 8 algorithm=default file= diff_pkg.s4p

.ends
```

- The SPICE subckt tdiff_tx_typ for the typical corner in tdiff_tx.spc is as shown on the left. Min and Max similar.
- We need to connect the extra IBIS nodes inside the subckt to make sure there are no disconnected nodes in the circuit
- This is a simple pass-through driver that applies the "in" stimulus and its inverted pattern to the package input nodes
- The s-parameter file (diff_pkg.dat) for the package is referenced internally in the subckt and connects the in and inv stimulus to the I/O output nodes i.e. 2 and 8

Similar for Rx

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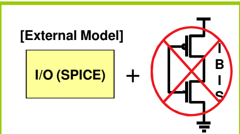
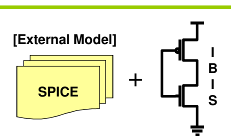
Simulate VI-VT model in conjunction with Spice

- Traditionally [External Model] keyword has been used for IO-buffer that needs to characterized as Spice IO in which case IBIS VI-VT data is not required.



- Extend use of [External Model] keyword to point to Spice sub-circuits that augment VI-VT data for complete characterization of IO-buffer.
  - Model On-DIE RDL parasitics using Spice or S-parameters that connect to Analog IO-buffer characterized as VI-VT data
  - Model DSP algorithm in Spice that works in conjunction with VI-VT data



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Simulate VI-VT model in conjunction with Spice

```
[External Model]
Language SPICE | SPARAM
Type Other

|corner        file_name                     circuit_name
 Typ           dsp.spc | dsp_typ.s4p         dsp_typ
 Min           dsp.spc | dsp_min.s4p         dsp_min
 Max           dsp.spc | dsp_max.s4p         dsp_max

| Ports List of port names (in same order as in SPICE | SPARAM)
Ports A_signal_pos A_signal_neg my_receive my_drive my_enable
Ports A_puref A_pdref A_pcref A_gcref A_extref my_ref A_gnd
```

(VI-VT tables are required when Type is not I/O, Allowed Types are 'I/O' and 'Other', where 'Other' can be RDL, ODT, DSP, etc or any combination)

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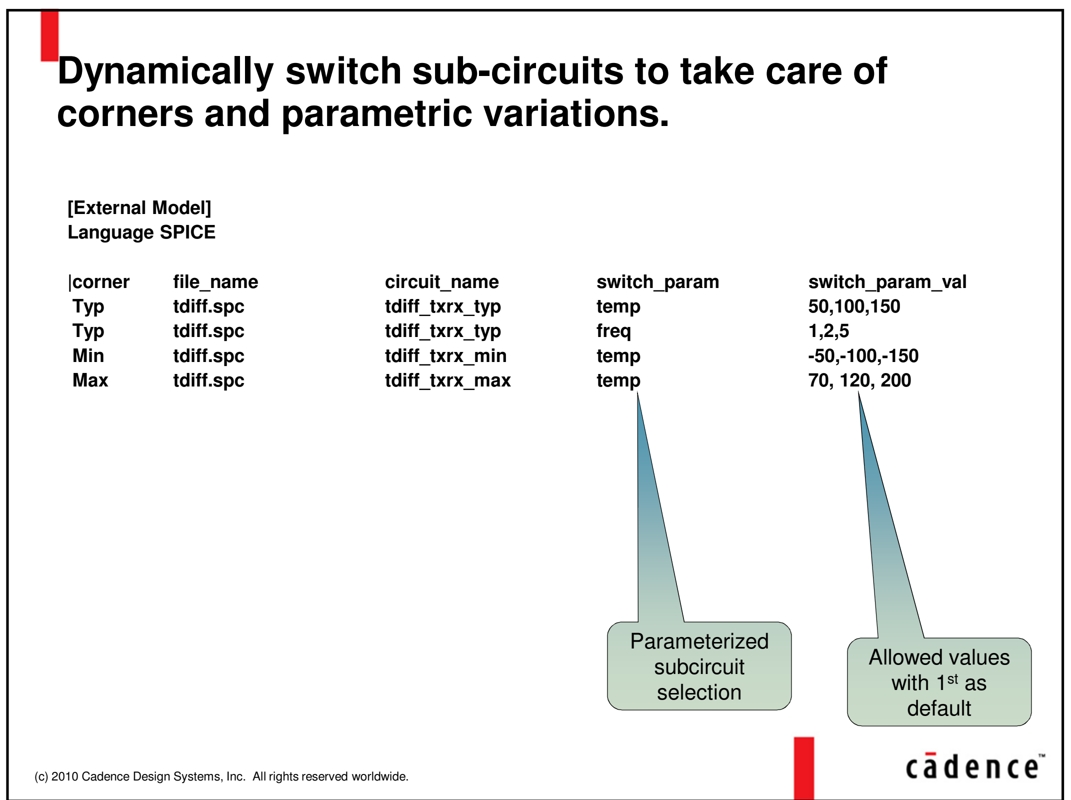

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Using AMI in conjunction with [External Model]

- Analog IO buffers in some cases could be modeled as s-parameters or as Spice sub-circuits. These models then work in conjunction with AMI code that represents DSP portion of IO-buffers. There could be even situations where IO-core itself becomes part of this AMI code.
- Hence we need to support AMI model simulation in absence of VI-VT data.
  - AMI model + Analog buffer represented as Spice-IO
  - AMI model + VI-VT Analog buffer + RDL (etc) in [External Model] (Case 1)
  - AMI model + Analog buffer represented as S-parameter-IO (Case 2)
  - AMI model (contains Analog-IO buffer coded as in AMI itself) + S-parameter/Spice RDL (Case 3)

```
[External Model]
Language SPARAM
Type I/O

|corner              file_name
 Typ                 io_typ.s4p
 Min                 io_min.s4p
 Max                 io_max.s4p

| Ports List of port names (in same order as in SPICE | SPARAM)
Ports A_signal_pos A_signal_neg my_receive my_drive my_enable
Ports A_puref A_pdref A_pcref A_gcref A_extref my_ref A_gnd
```

(VI-VT tables are not required as S-Params represent the analog I/O buffer or RDL etc + I/O buffer)

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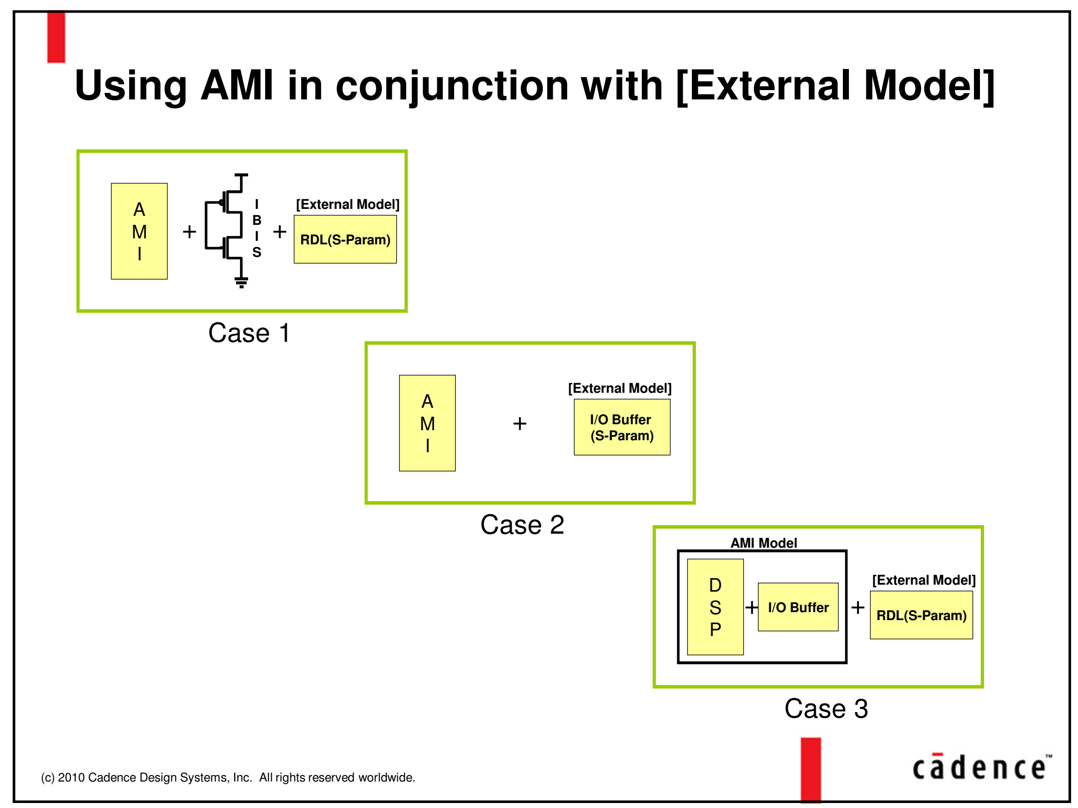
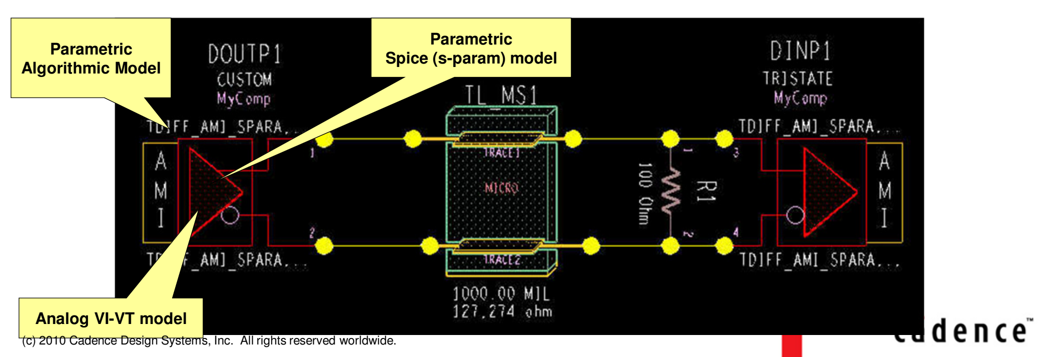


Summary

- Package parasitics can be modeled as SPICE using [External Model]; but we need to support S-parameters and it should be under proper keyword in Package-Section
- [External Model] has been traditionally used as alternate to VI-VT data; but we need to leverage it to use this model in conjunction with VI-VT
- [External Model] should support parameter switching to pick subcircuits dynamically
- AMI model today assumes analog-IO available as VI-VT; AMI model should work in conjunction with [External Model]



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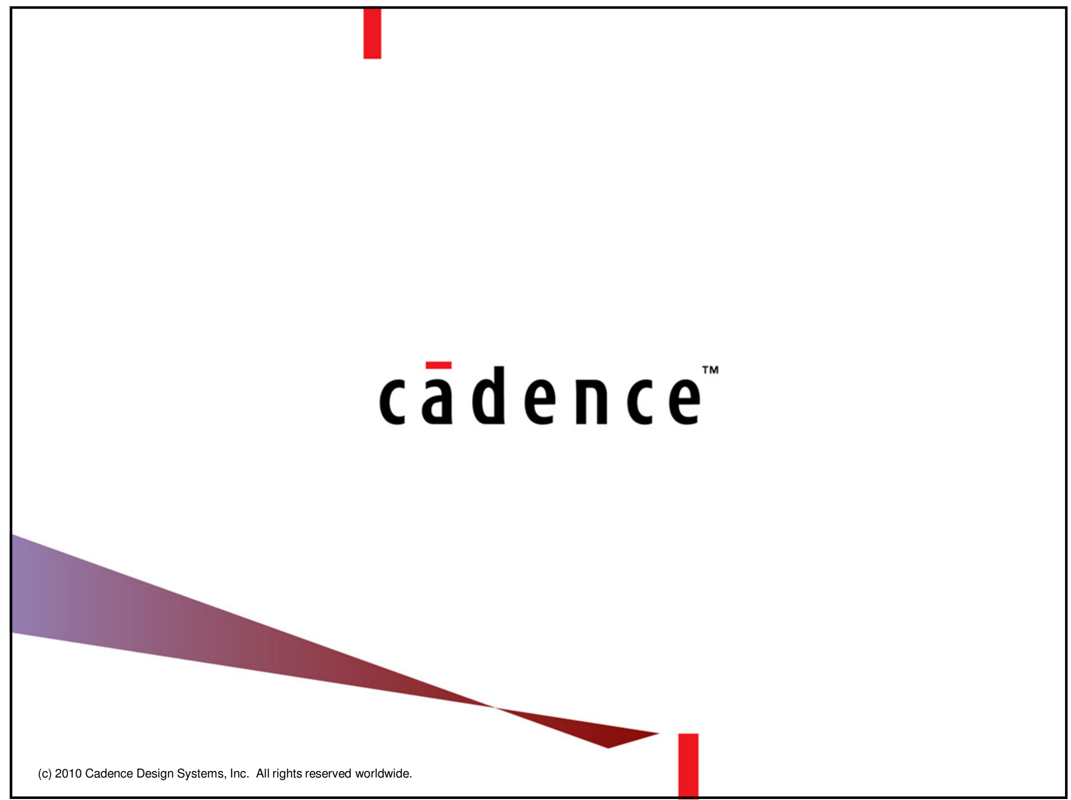
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IBIS-ISS: What It Is and What It Means to You

Michael Mirmak 馬夢寬
Intel Corporation 英特爾公司
Chair, IBIS Open Forum IBIS 委員會主席

IBIS Summit Taipei 台北 IBIS 技術研討會
November 12, 2010 2010 年 11 月 12 日

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Agenda

- The Problem of SPICE* Model Portability
- The Concept of IBIS-ISS
- What Is and Isn't Supported
- IBIS-ISS and Good SPICE Usage
- Status and Future Work
- Summary and Call for Action!

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A Standard SPICE* Does Not Exist

- What does the following SPICE* statement do?

```
Bexample 1 2 I=sin(V(3,0))
```

- Results depend on the SPICE tool you use
  - IBIS or non-linear dependent source?
- Some elements are not supported or do not share a common meaning in all SPICE variants
  - Other non-universal elements include P, W, Y, Z

How do you ensure a model works in your tool or your customers' tools?

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A Solution for SI/PI Interconnects

- SPICE* netlists include interconnects, devices and engine commands
  - e.g., .tran analysis for a driver and receiver on a PCB trace
- IBIS supports portable device models directly
- Engine commands are specific to EDA tools
- How to ensure interconnect models are portable?
  - Package, via, connector, PCB trace, on-die PDN…

IBIS-ISS: an industry baseline for interconnect modeling in SPICE

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IBIS-ISS in Simple Terms

- IBIS-ISS: IBIS Interconnect SPICE* Subcircuits
- Defines a limited set of common, basic elements useful for SI interconnect modeling
- Based on documents and concepts donated by Synopsys as seen in Synopsys HSPICE*
- Developed with SI community through IBIS Interconnect Task Group
  - EDA vendors, IC vendors and system vendors

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What Is (and Is Not) Supported

- Fundamental circuit elements
  - Resistors, Inductors, Capacitors: R, L, K, C
  - Dependent Sources: E, F, G, H
  - Transmission Lines: T, W (including tabular, Foster, etc.)
  - S-parameters: S
- Subcircuit definitions and instantiation
  - .subckt, .ends, X element
- Other basic commands
  - .include, .end, .param

… but no engine commands, no active device support, and no field solver

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Usage Model

- IBIS-ISS consists entirely of subcircuits and subcircuit definitions
  - IBIS-ISS does not define netlists
  - Subcircuits may be nested or independent
- All parameters are local, and passed explicitly
- Multiple files are supported (.include)
- Compliant tools simply accept IBIS-ISS files
  - Meaning, properly apply IBIS-ISS assumptions within the scope of the top-level subcircuit

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How Does It Work?

```
.subckt my_trace_group 1 2 3 4 5 6 7 8 ref length=5e-3
* Units are meters
* This is a top-level subcircuit
* The user/system designer will instantiate this circuit in a netlist

Xtrace_a 1 ref 2 ref single_trace local_length=length
Xtrace_b 3 ref 4 ref single_trace local_length=length
Xtrace_c 5 ref 6 ref single_trace local_length=length
Xtrace_d 7 ref 8 ref single_trace local_length=length

* This circuit assumes no crosstalk

    .subckt single_trace in local_ref out local_ref local_length=1

    Wsingle in local_ref out local_ref N=1 L='local_length'
    + TABLEMODEL='single_line_table'

    .include 'single_line_table.inc'
    * This file defines the tabular data using .MODEL
    * This file should also be written using ISS rules
    .ends

.ends
```


Using SPICE* Correctly

- Good SPICE* habits will make IBIS-ISS adoption and use easier
  - Pass parameters explicitly and sparingly
  - Do not rely on global parameter definitions
  - Avoid using global nodes
  - Use modular circuit design
  - Make node, parameter and element names clear and unique
  - Avoid setting engine options in subcircuits
  - Avoid ambiguous units and multipliers (e.g., amps vs. atto-)

Practice using IBIS-ISS rules in your circuits today

Status and Future Work

- Draft v0.7 now in review
- Once drafts are complete, the document will be provided to the IBIS Open Forum for approval
- A parser is under consideration
- Documents and background materials on-line:
  – http://www.eda.org/ibis/interconnect_wip/
- Mailing list available for updates and discussion:
  – http://www.freelists.org/list/ibis-interconn/

Questions and comments are welcome!

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Summary

- If you model interconnects, IBIS-ISS can help ensure usability across SPICE* tools
- If you use SPICE of any kind, IBIS-ISS will be familiar to you
- Following principles of good SPICE circuit construction makes IBIS-ISS easy to use

Please study, learn, discuss and comment on the IBIS-ISS draft.

Your contributions are important!

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Model Connection Protocol extensions for Mixed Signal SiP

Taranjit Kukal (kukal@cadence.com)
Dr. Wenliang Dai (wldai@cadence.com)
Brad Brim (bradb@sigrity.com)
assisted by Eiji Fujine Fujitsu VLSI Limited

Presented by: Kevin Liu – Cadence

Note: Previously presented at IBIS Summit in China Nov. 9

Asian IBIS Summit
Taipei, Taiwan
November 12, 2010

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Agenda

- Why Model Connection Protocol
- Model Connection Protocol overview
- Extensions required for Mixed Signal SiP
- MCP Applications
- Summary

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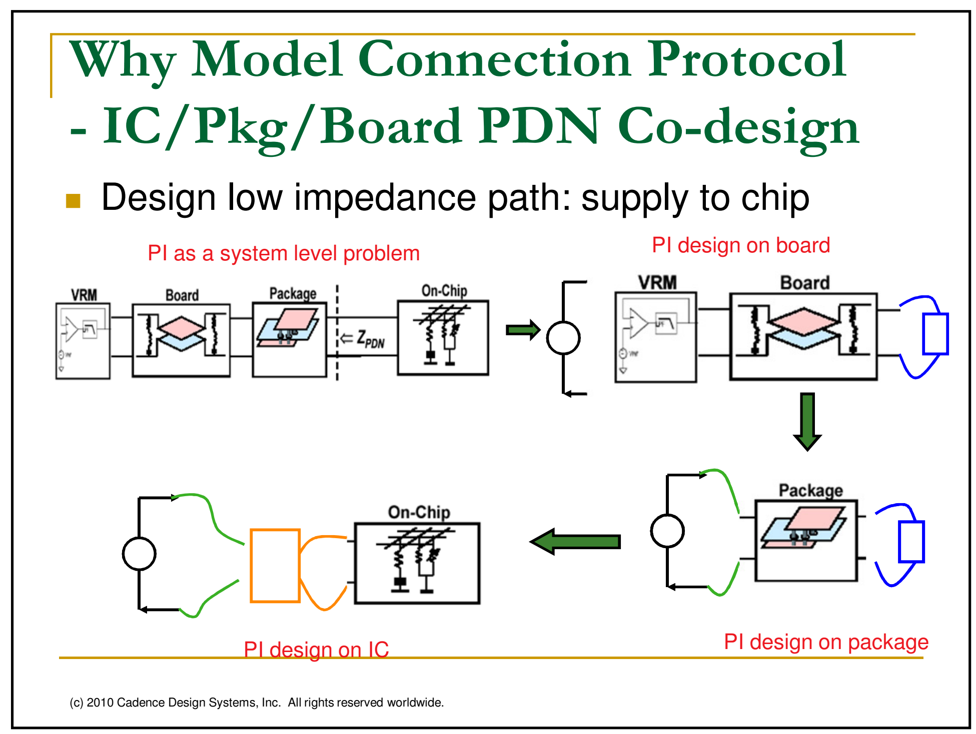
Why Model Connection Protocol
- IC/Pkg/Board PDN Co-design
Design low impedance path: supply to chip
PI as a system level problem
PI design on board
VRM
Board
Package
On-Chip
PI design on IC
PI design on package
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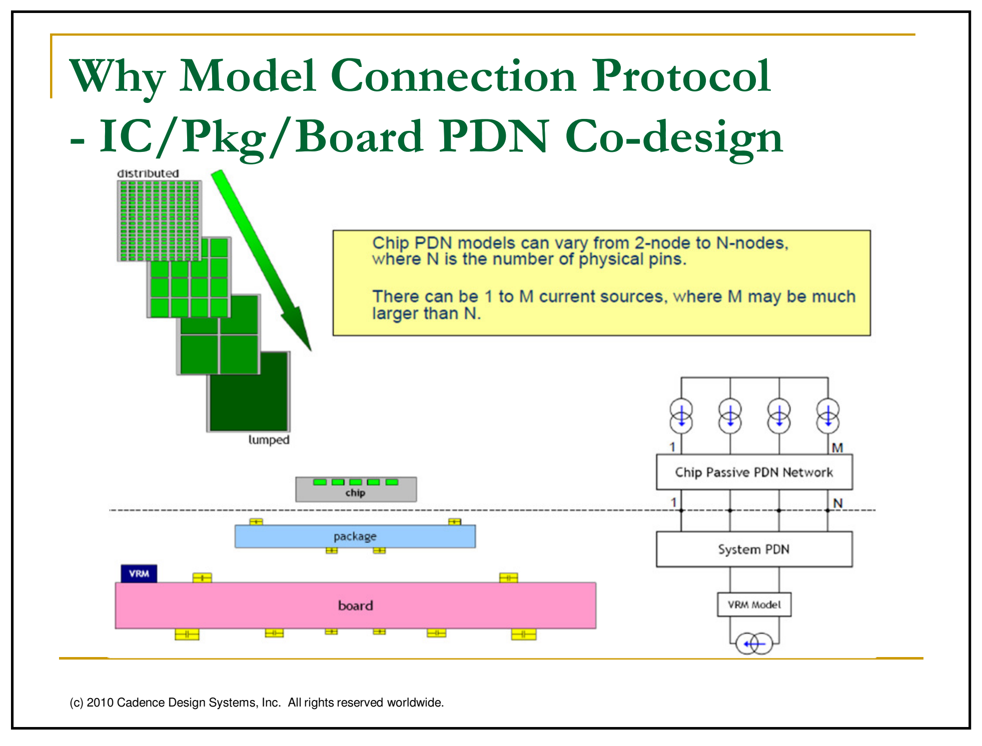
Why Model Connection Protocol
- IC/Pkg/Board PDN Co-design
distributed
lumped
Chip PDN models can vary from 2-node to N-nodes, where N is the number of physical pins.
There can be 1 to M current sources, where M may be much larger than N.
chip
package
VRM
board
Chip Passive PDN Network
System PDN
VRM Model
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Why Model Connection Protocol - IC/Pkg/Board PDN Co-design

- Chip/Package/Board have many physical connections
  - Chip-Package Boundary:100-6000
  - Package-Board Boundary: 100-3000
- Not all electrical nodes can have per-pin resolution
  - Models may become too large for computation, simulation
- Need way to group pins and auto-connect models across IC/Pkg/Board

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MCP Overview - Establish mapping

- Pin grouping and mapping
  - **physical pin (of layout) to electrical node (of model) per Net**
  - **Mapping to connecting structure using physical location**

Example of VDD net across chip-pkg-board

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MCP Overview
- Establish mapping

Pins of net
Electrical node
Netname
X-Y loc of pin

```
.subckt chip  d1 d2 d3 d4 d5 d6 d7
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] DIE
* [MCP Source] chip extraction tool
* [Coordinate Unit] um
* [Connection] pkg1  pkg_bumps  7
*   [Connection Type] PKG
*     [Power Nets]
*       pin1  d1  VDD    0    0
*       pin2  d2  VDD    0  100
*       pin3  d3  VDD  100    0
*       pin4  d4  VDD  100  100
*       pin5  d5  VDD   50    0
*       pin6  d6  VDD   50   50
*       pin7  d7  VDD   50  100
* [MCP End]
 --- SPICE elements ---
.ends
```

```
.subckt package  p1 p2 p3 p4
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] PKG
* [MCP Source] package extraction tool
* [Coordinate Unit] um
* [Connection] die1  myCPU  7
*   [Connection Type] DIE
*     [Power Nets]
*       01  p1  VDD    0    0
*       02  p1  VDD    0  100
*       03  p1  VDD  100    0
*       04  p1  VDD  100  100
*       05  p2  VDD   50    0
*       06  p2  VDD   50   50
*       07  p2  VDD   50  100
* [Connection] board1  my_board  4
*   [Connection Type] PCB
*     [Power Nets]
*       08  p3  VDD    0    0
*       09  p3  VDD    0  200
*       10  p4  VDD  200    0
*       11  p4  VDD  200  200
* [MCP End]
 --- SPICE elements ---
.ends
```

```
.subckt board  b1
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] PCB
* [MCP Source] board extraction tool
* [Coordinate Unit] mm
* [Connection] pkg1  pkg_balls  4
*   [Connection Type] PKG
*     [Power Nets]
*       pin_1  b1  VDD  0.0  0.0
*       pin_2  b1  VDD  0.0  0.2
*       pin_3  b1  VDD  0.2  0.0
*       pin_4  b1  VDD  0.2  0.2
* [MCP End]
 --- SPICE elements ---
.ends
```

Example of VDD net across chip-pkg-board

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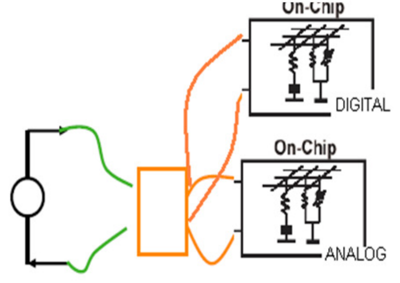
MCP Extensions for Mixed Signal SiP

- Analyze power-delivery to ICs when Package rails supply power to
  - different ICs that could be digital and/or analog
  - RF-modules and Passive/Active SMDs
- Need Schematic driven Mixed Signal Simulations to process IR-drop at power-rails



PDN supplying Analog and Digital multi-DIE system

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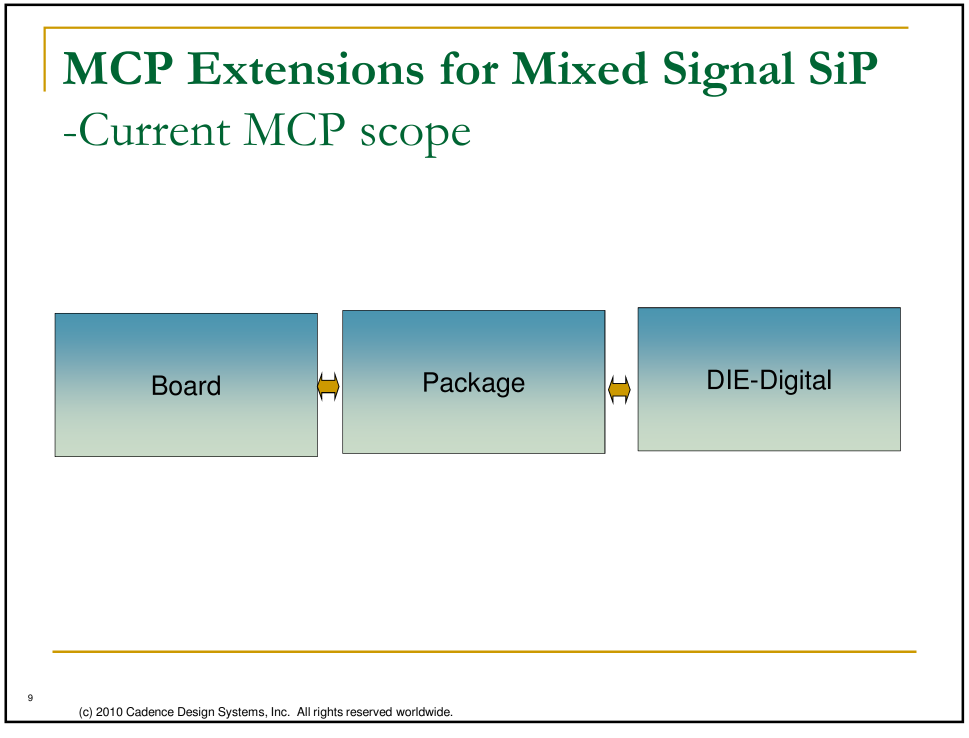
MCP Extensions for Mixed Signal SiP
-Current MCP scope
Board
Package
DIE-Digital
9
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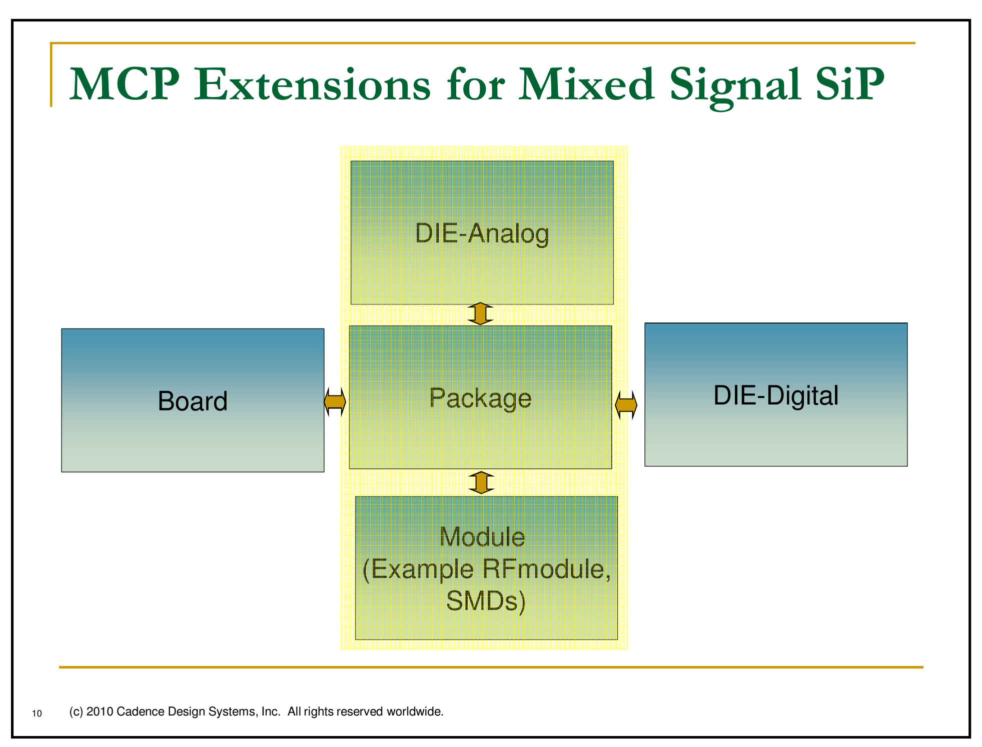
MCP Extensions for Mixed Signal SiP
DIE-Analog
Board
Package
DIE-Digital
Module
(Example RFmodule,
SMDs)
10
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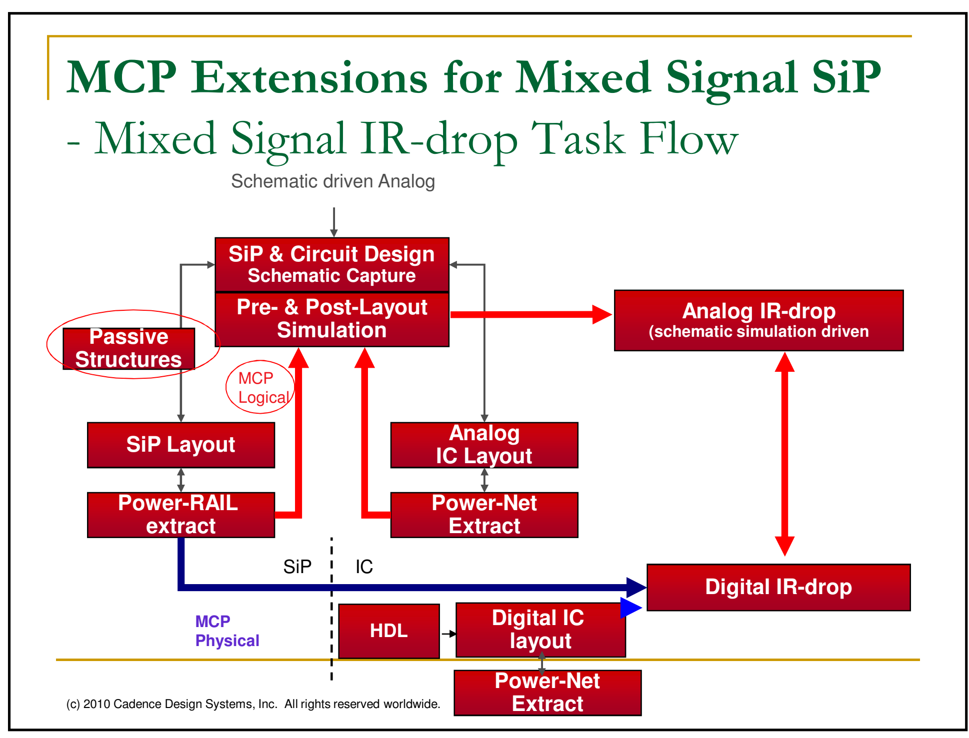

MCP Extensions for Mixed Signal SiP
- Mixed Signal IR-drop Task Flow
Schematic driven Analog
SiP & Circuit Design
Schematic Capture
Pre- & Post-Layout
Simulation
Analog IR-drop
(schematic simulation driven
Passive
Structures
MCP
Logical
SiP Layout
Analog
IC Layout
Power-RAIL
extract
Power-Net
Extract
SiP
IC
Digital IR-drop
MCP
Physical
HDL
Digital IC
layout
Power-Net
Extract
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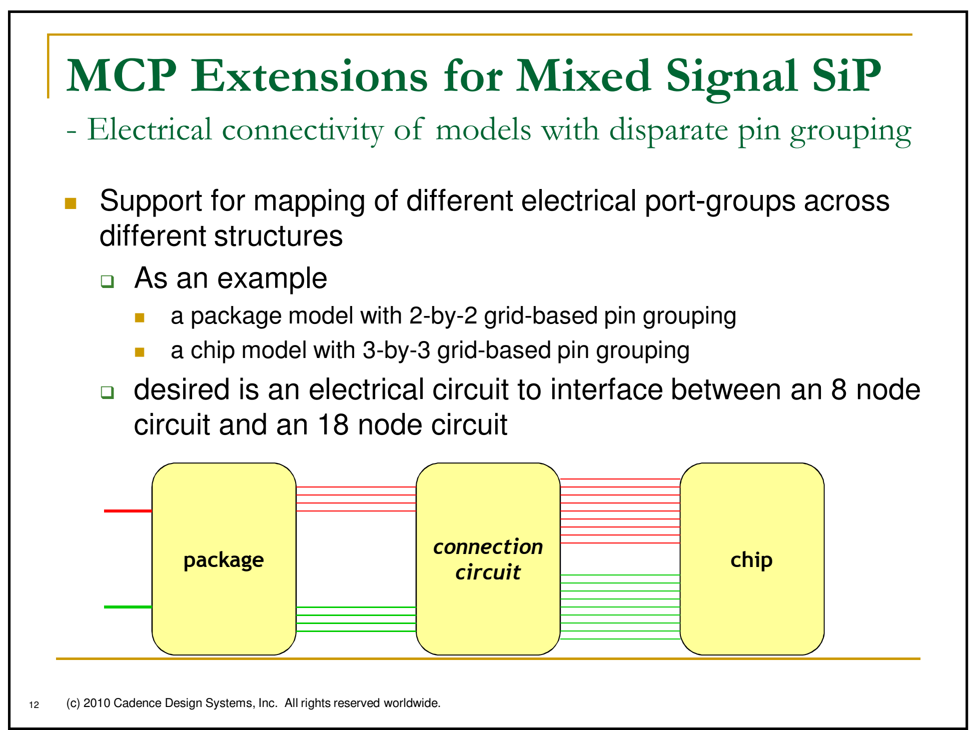

MCP Extensions for Mixed Signal SiP
- Electrical connectivity of models with disparate pin grouping
Support for mapping of different electrical port-groups across different structures
As an example
a package model with 2-by-2 grid-based pin grouping
a chip model with 3-by-3 grid-based pin grouping
desired is an electrical circuit to interface between an 8 node circuit and an 18 node circuit
package
connection circuit
chip
12
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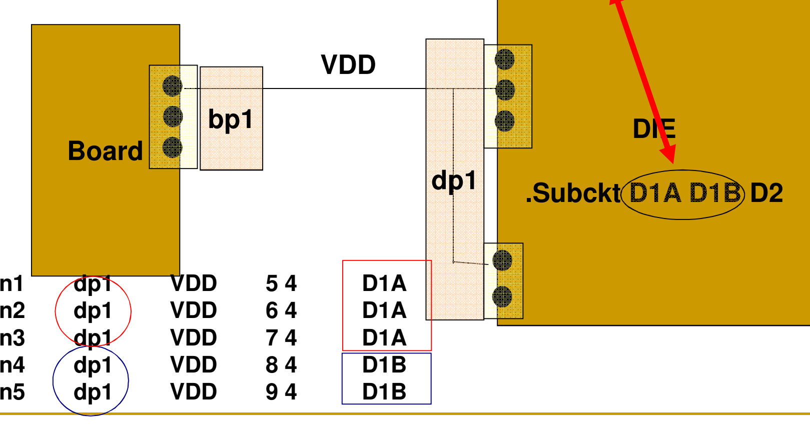
MCP Extensions for Mixed Signal SiP

- Optional Column for mapping of electrical nodes across structures



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MCP Extensions for Mixed Signal SiP

- Caution: Electrical connectivity with disparate pin grouping

- Examine the nodes of the each net
  - for overlapping pin group domains, the corresponding nodes are shorted together
    - (1,1) node shorts together {(1,1), (1,2), (2,1), (2,2)} nodes
    - (1,2) node shorts together {(1,2), (1,3), (2,2), (2,3)} nodes
    - (2,1) node shorts together {(2,1), (2,2), (3,1), (3,2)} nodes
    - (2,2) node shorts together {(2,2), (2,3), (3,2), (3,3)} nodes

    alternately
    - (2,2) node shorts together {(1,1), (1,2), (2,1), (2,2)} nodes
  - all nodes are shorted together, reducing to per-net connectivity
    - instead of 8 or 18 node electrical connectivity it is actually 2 node connectivity
- Recommendation
  - Connecting two disparately pin-grouped models is possible by choosing to short together electrical nodes that have overlapping pin domains
    - but it can reduce the effective resolution of the model at the chip/package interface
    - Useful in case of early debugging and quick connectivity

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Extensions over existing MCP

- Support for Modules as connect type structures

- Mixed Signal SiPs would have elements other that ICs like
  - RFmodules
  - Metal Passive structures
  - SMD components
  - Silicon Interposers
- These structure draw power impacting PDN loading and hence we need to support [Module] category besides IC, Package and Board

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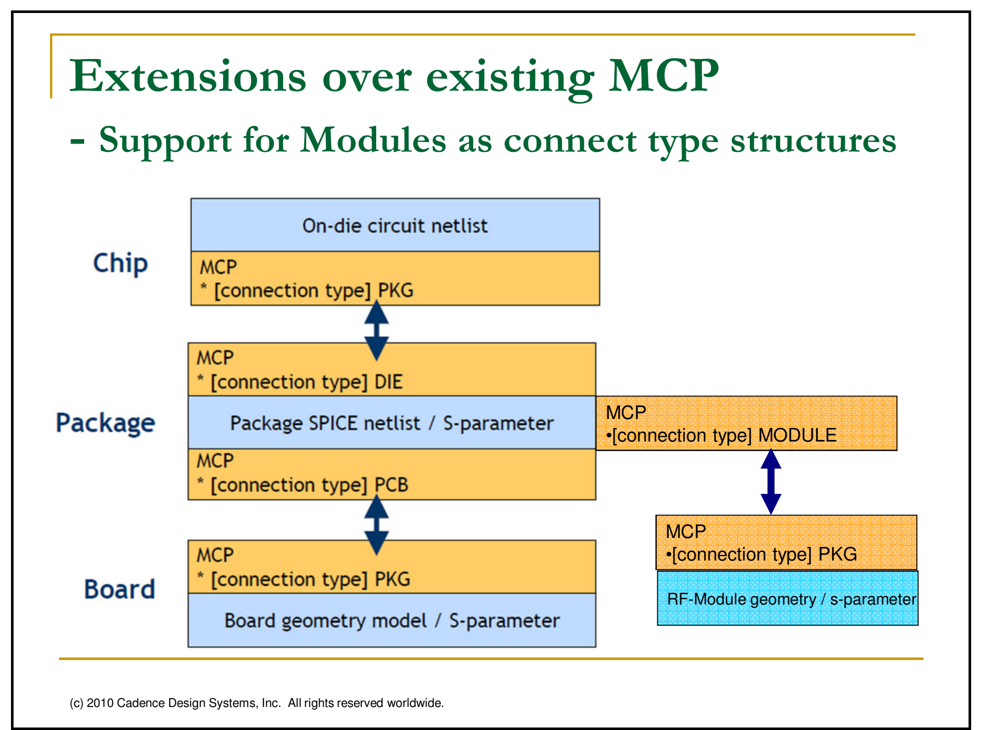
Extensions over existing MCP

- Support for Modules as connect type structures



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Extensions over existing MCP

- Connection by Refdes besides X-Y location

- In order to connect to structures that are SMD or metal-passive structures on SiP – usually a case for Mixed Signal SiP, it becomes difficult to connect by X-Y locations.
- Early analysis may require quick way of stitching the models across structures and minor placement or resolution changes can cause X-Y mapping to fail.
- Optional column showing connection by REFDES makes easy mapping for Mixed-Signal modules and early trials
  - Examples of connecting interfaces could be
    - IO-cellname (DIE IO)
    - R1:1 (pin 1 of R1)
    - CONN:1 (pin1 of PCB connector)
    - my_model_opamp:3 (port-3 of opamp subcircuit)

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Extensions over existing MCP

- Connection by Refdes besides X-Y location

- Simulating Analog DIE in package schematics with loading from passive structures connected to DIE
- The simulation data is post-processed to obtain IR-drop at power-rails

VDD

[connection type MODULE]

Pin1	**dp1**	**VDD**	**~~5 4~~**	**varistor1:2** //Reference_design:pin//
Pin2	**dp1**	**VDD**	**~~6 4~~**	**varistor2:2**
Pin3	**dp1**	**VDD**	**~~7 4~~**	

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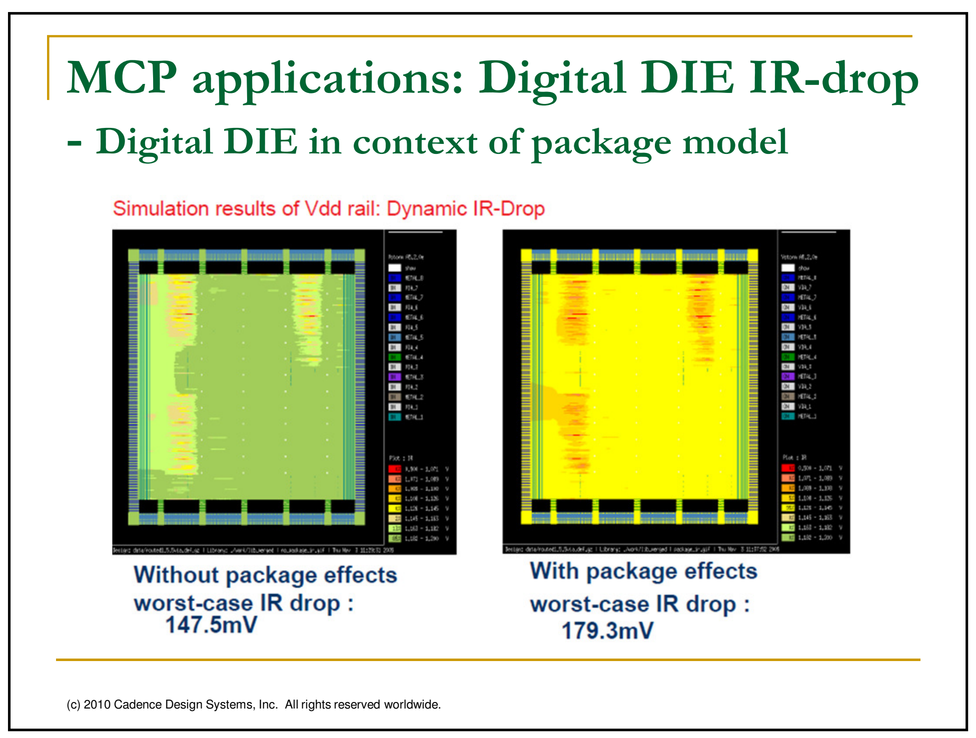
MCP applications: Digital DIE IR-drop
- Digital DIE in context of package model
Simulation results of Vdd rail: Dynamic IR-Drop
Without package effects
worst-case IR drop :
147.5mV
With package effects
worst-case IR drop :
179.3mV
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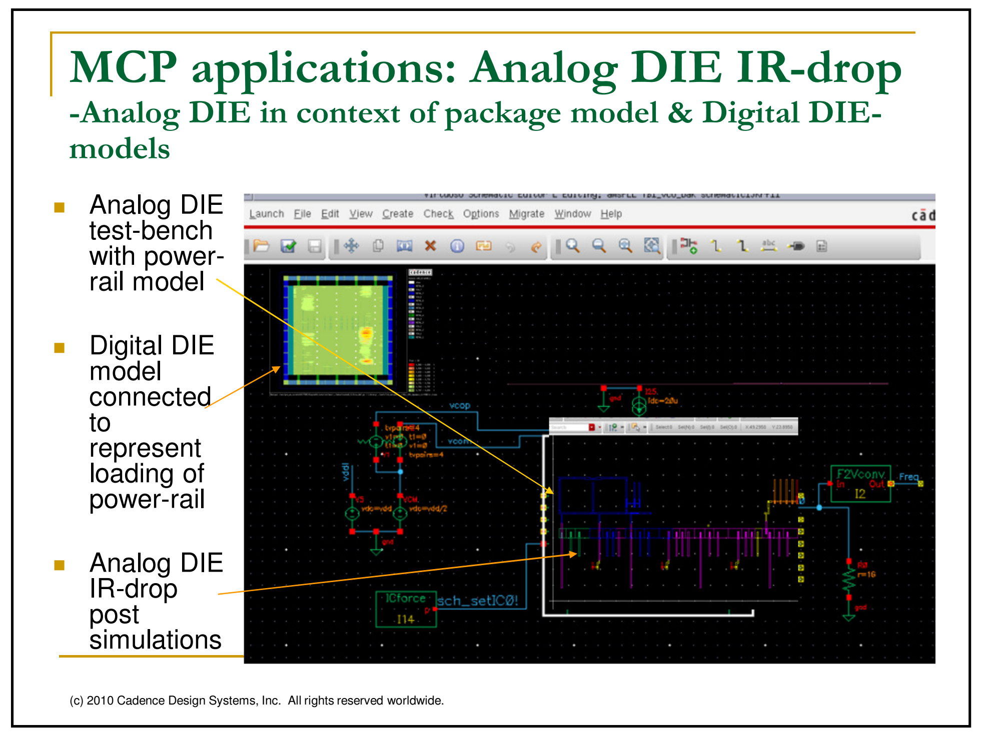
MCP applications: Analog DIE IR-drop
-Analog DIE in context of package model & Digital DIE-models
Analog DIE test-bench with power-rail model
Digital DIE model connected to represent loading of power-rail
Analog DIE IR-drop post simulations
Launch File Edit View Create Check Options Migrate Window Help
vcop
F2Vconv
Freq
ICforce
sch_setIC0!
I14
I2
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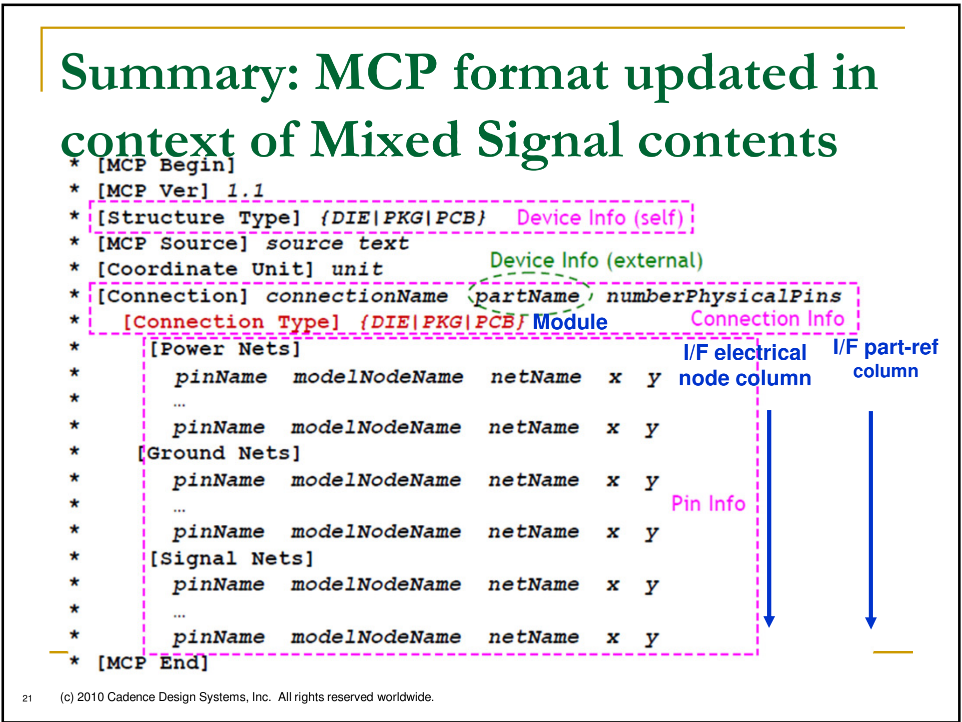
Summary: MCP format updated in context of Mixed Signal contents
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] {DIE|PKG|PCB}
Device Info (self)
* [MCP Source] source text
* [Coordinate Unit] unit
Device Info (external)
* [Connection] connectionName partName numberPhysicalPins
* [Connection Type] {DIE|PKG|PCB}
Module
Connection Info
* [Power Nets]
* pinName modelNodeName netName x y
* pinName modelNodeName netName x y
* [Ground Nets]
* pinName modelNodeName netName x y
* pinName modelNodeName netName x y
* [Signal Nets]
* pinName modelNodeName netName x y
* pinName modelNodeName netName x y
* [MCP End]
I/F electrical node column
I/F part-ref column
Pin Info
21
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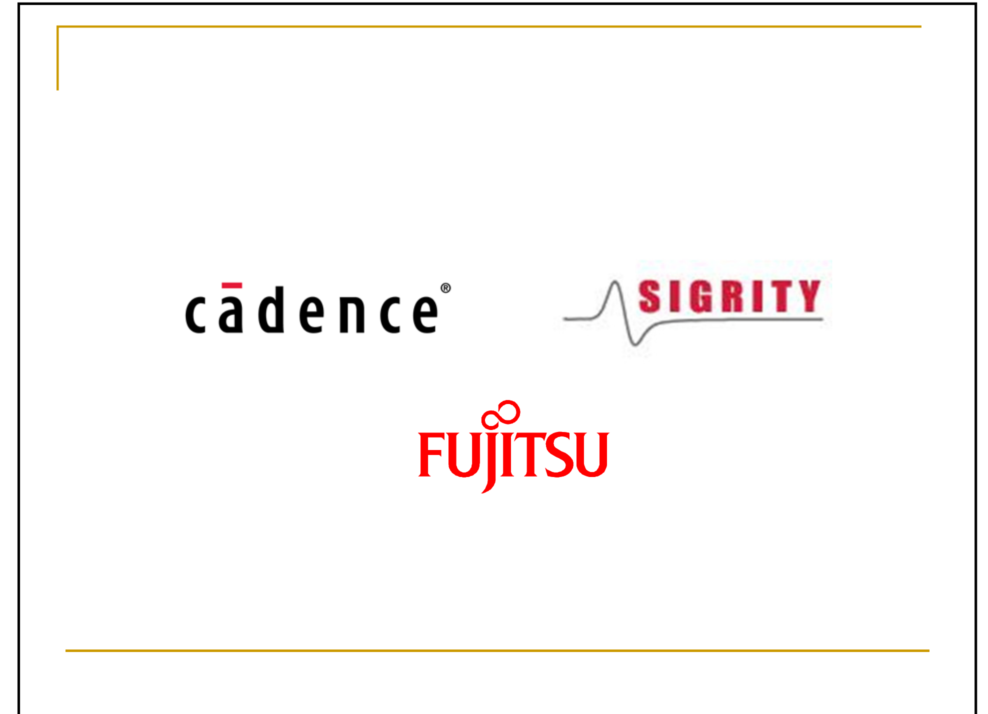
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