Correlating C_pin Capacitance with Measurements

Asian IBIS Summit
Shenzhen, China
November 9, 2010

Randy Wolff

Micron Technology

rrwolff@micron.com

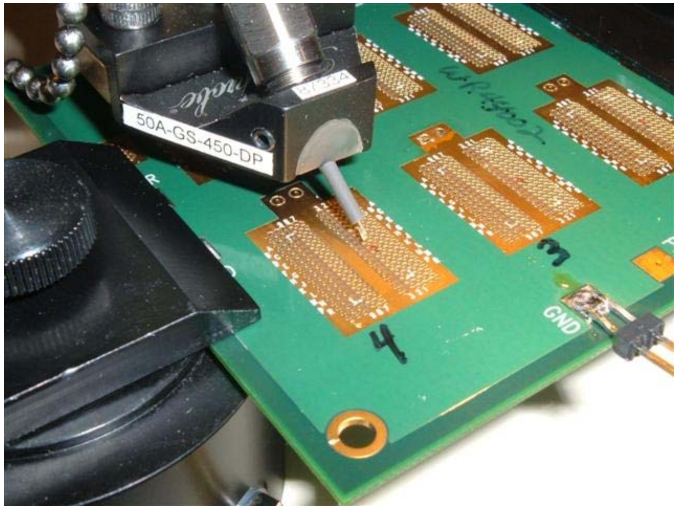
C_pin

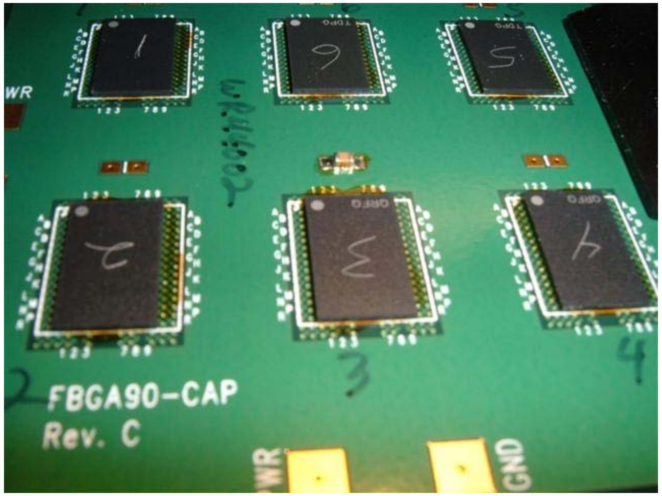
- Package capacitance for a specific signal [Pin]
- Typically from diagonal elements of the capacitance matrix – extracted from 3D field solvers

```
|**************************************************************************
| COMPONENT: MT41J256M8DA (78-Ball FBGA, x8, 8mm X 10.5mm)
|**************************************************************************
|
[Component]      MT41J256M8DA
[Package Model] v89b_78ball_pkg
[Manufacturer]  Micron Technology,Inc.
[Package]
|              typ          min          max
R_pkg          257.47m      178.77m      383.81m
L_pkg          1.43nH       0.98nH       2.38nH
C_pkg          0.36pF       0.29pF       0.49pF
|
[Pin]          signal_name model_name   R_pin        L_pin        C_pin
A1             VSS         GND
A2             VDD         POWER
A3             NC          NC
A7             NF_TDQS#    NF_TDQS      267.15m      1.36nH       0.41pF
A8             VSS         GND
A9             VDD         POWER
B1             VSS         GND
B2             VSSQ        GND
B3             DQ0         DQ           247.18m      1.08nH       0.39pF
B7             DM_TDQS     DM_TDQS      242.95m      1.47nH       0.37pF
```

Measured Capacitance

- Diagonal of matrix is total capacitance seen by each line with all other lines grounded
  - Fully-loaded capacitance is useful for single line simulations
- Measured capacitance is less than fully-loaded capacitance
  - Signal is referenced to power and ground (pwr/gnd decoupled)
  - All other signal lines are floating



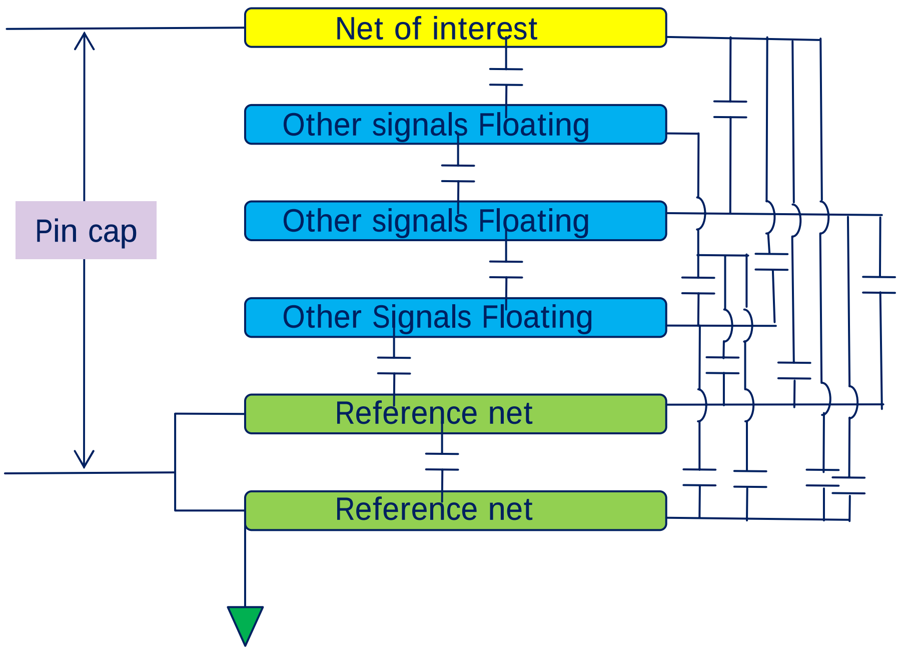


Why is this important?

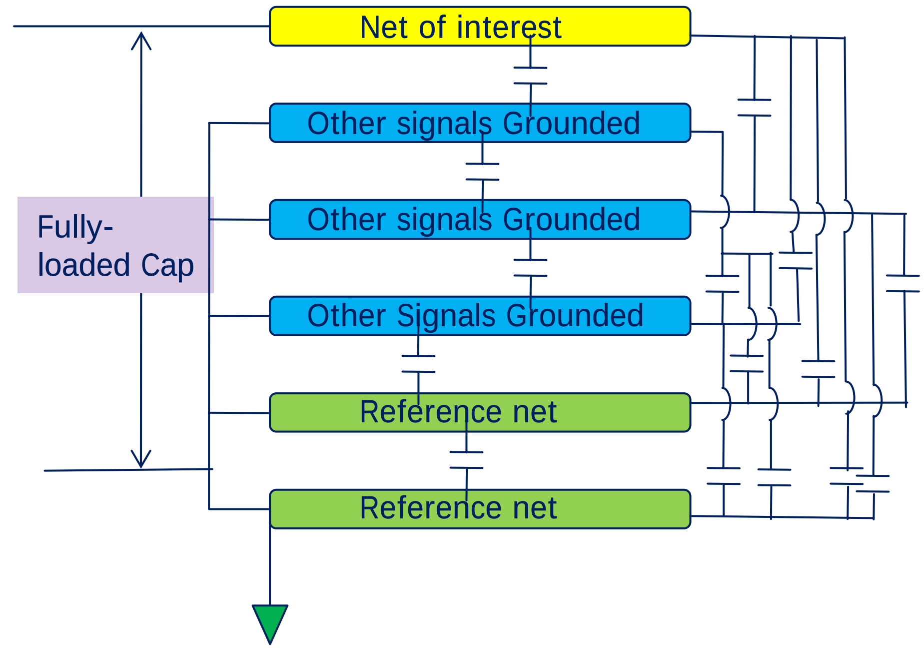
- C_comp calculation and Model correlation
  - C_comp = C_signal(measured) – C_pin(measured)
  - C_pin ≠ C_pin(measured)
- Datasheet comparisons
  - $C_{specification}$ is based on measured values, not total capacitance
  - Estimating measured values from package simulation data aids in optimizing package designs to meet capacitance specifications

Capacitance Parameters	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
CK and CK#	C_{CK}	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	0.8	1.3	pF
ΔC: CK to CK#	C_{DCK}	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	pF
Single-end I/O: DQ, DM	C_{IO}	1.5	3.0	1.5	3.0	1.5	2.5	1.5	2.3	1.4	2.2	pF
Differential I/O: DQS, DQS#, TDQS, TDQS#	C_{IO}	1.5	3.0	1.5	3.0	1.5	2.5	1.5	2.3	1.4	2.2	pF
ΔC: DQS to DQS#, TDQS, TDQS#	C_{DDQS}	0	0.2	0	0.2	0	0.15	0	0.15	0	0.15	pF
ΔC: DQ to DQS	C_{DIO}	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF

C_pin (measured) vs. Fully-loaded Cap

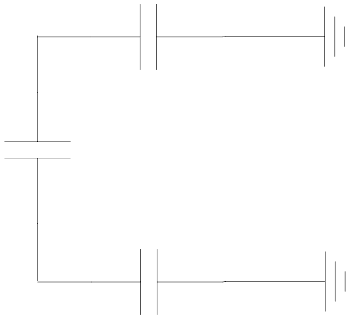


Measured Pin Cap Setup
(Extracted pin cap after matrix post-processing)



Fully-loaded Cap
(Diagonals of Maxwell's Matrix)

Calculating C_pin(measured)

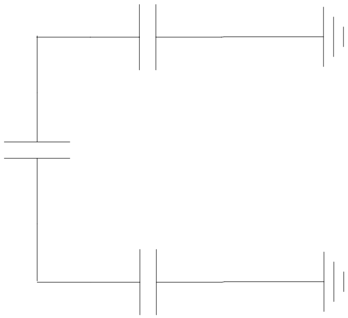


- The matrix form of the capacitance equation is [Q] = [C] * [V]
- For a 2x2 system, the C matrix is :

$$\begin{vmatrix} Ct1 & -C12 \\ -C12 & Ct2 \end{vmatrix}$$

- Ct1 = C1 + C12 and Ct2 = C2 + C12

Calculating C_pin(measured)



- Deposit a charge of Q on Node 1

$$\begin{vmatrix} Ct1 & -C12 \\ -C12 & Ct2 \end{vmatrix} * \begin{vmatrix} V1 \\ V2 \end{vmatrix} = \begin{vmatrix} Q \\ 0 \end{vmatrix}$$

- $Ct1 * V1 – C12 * V2 = Q$
- $-C12 * V1 + Ct2 * V2 = 0$, $V2 = C12/Ct2 * V1$
- $(Ct1 - C12^2/Ct2) * V1 = Q$
- $Cnode1 = Q/V1 = (Ct1 - C12^2/Ct2)$
- In matrix form, let Q = 1 coulomb

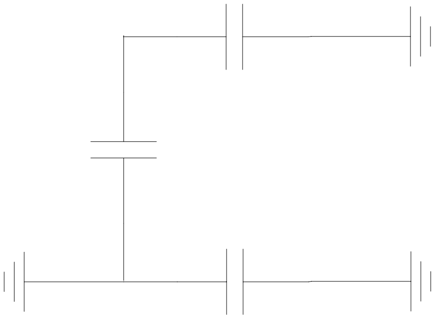
$$\begin{vmatrix} V1 \\ V2 \end{vmatrix} = Inv\left(\begin{vmatrix} Ct1 & -C12 \\ -C12 & Ct2 \end{vmatrix}\right) * \begin{vmatrix} 1 \\ 0 \end{vmatrix}$$

- This yields V1 and V2 and Cnode1 = 1/V1, since Q = 1

Calculating C_pin(measured)

- Let Node 2 be grounded - this forces V2 = 0 and allows a net negative charge on Node 2

$$\begin{vmatrix} Ct1 & -C12 \\ -C12 & Ct2 \end{vmatrix} * \begin{vmatrix} V1 \\ 0 \end{vmatrix} = \begin{vmatrix} 1 \\ Q \end{vmatrix}$$



- 1: Ct1 * V1 – C12 * 0 = 1 , V1 = 1/Ct1
- 2: -C12 * V1 + Ct2 * 0 = Q, Q = - C12/Ct1
- The only value of interest is V1, only equation 1 is needed. This is the same as eliminating the 2nd row of the [C] matrix.
- V2 = 0, so all of the terms in the 2nd column will multiply to 0. This eliminates the 2nd column of [C].
- The matrix equation reduces to | Ct1 | * | V1 | = | 1 |

Calculating C_pin(measured)

- Generalized: Let [C] be an n+m x n+m matrix representing n floating nodes and m nodes clamped to power or ground.
- Step 1 – eliminate the rows and columns associated with clamped nodes.
  - [C] -> [C'], where [C'] is an n x n matrix.
  - |C'| = |Reduction Matrix2| * |C| * |Reduction Matrix1|
  - If net i is clamped then row i of Reduction Matrix1 is all 0s
  - If net i is floating then row i of Reduction Matrix1 is all 0s with a 1 in column x
    - x = i - # of clamped nets between net 1 and net i
  - If net i is clamped then column i of Reduction Matrix2 is all 0s
  - If net i is floating then column i of Reduction Matrix2 is all 0s with a 1 in row x
    - x = i - # of clamped nets between net 1 and net i

Calculating C_pin(measured)

- Step 2 – Generate Q matrix – n x n identity matrix
  - Represents a 1 coulomb charge deposited on each floating node, one at a time.
- Step 3 – solve for [V] matrix
  - [V] = inv([C']) * [Q], where [Q] is identity matrix
- Step 4 – Calculate floating node capacitances
  - Cnode(x) = 1/Vxx, where Vxx are the diagonal elements of [V]
- Overall effect is mutual capacitances are reduced due to shorting of the mutual terms to power and ground nets

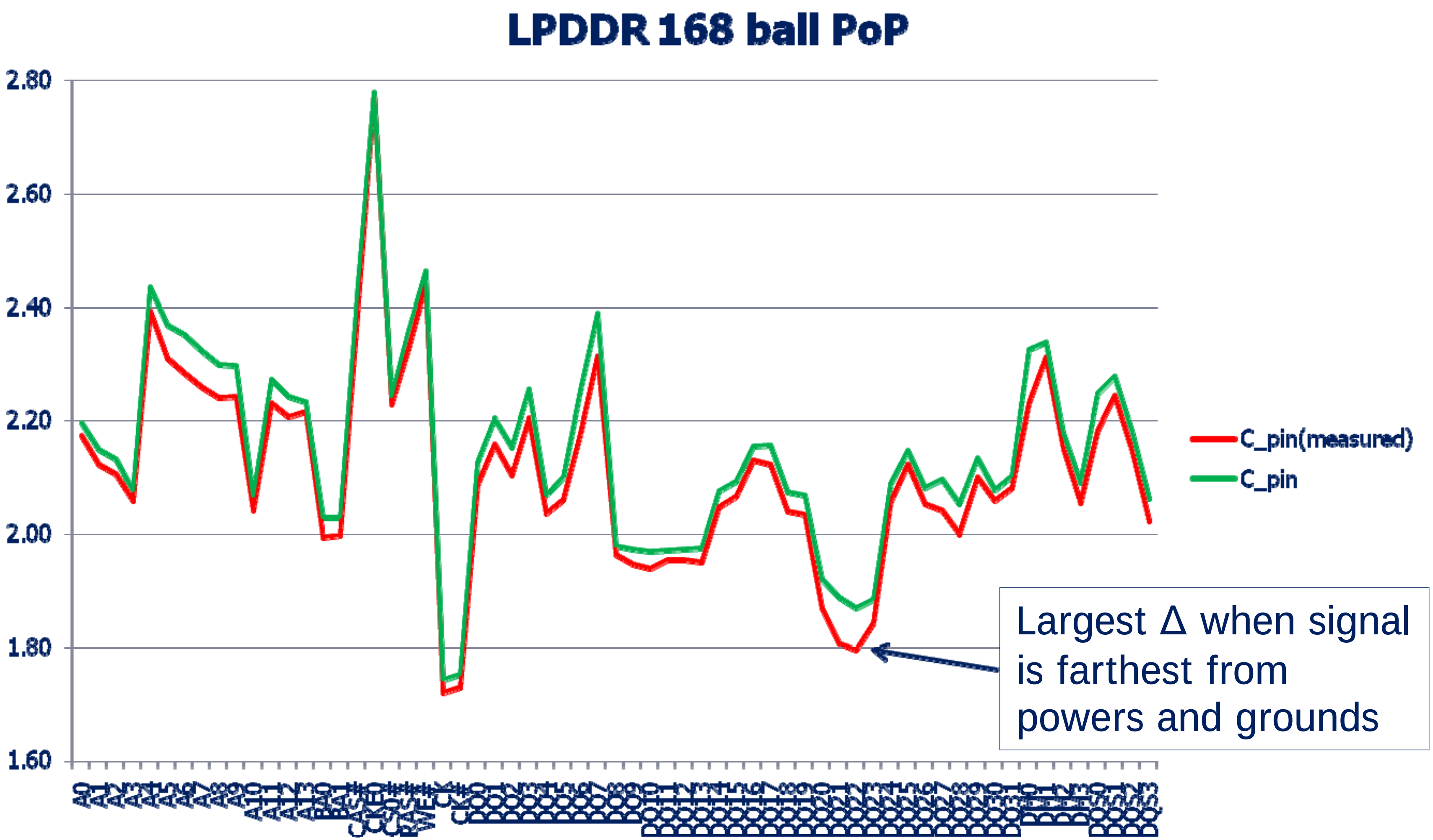
Micron's Capacitance Analyzer Tool

- Excel spreadsheet macro
- Reads in matrix data from several Field Solver tools
- Solves for 'measured' capacitance
- Nets are defined as either 'floating' or 'grounded'

Line number	Line Name	Signal_State
1	A0	Floating
2	A1	Floating
3	A2	Floating
59	VDD	Grounded
60	VDDQ	Grounded
61	VSS	Grounded
62	VSSQ	Grounded
63	WE#	Floating

Signal Names	Pin Capacitance	Maxwell Diagonal Capacitance
A0	9.48269E-13	1.22479E-12
A1	1.05993E-12	1.29176E-12
A2	1.06298E-12	1.20089E-12
A3	9.97877E-13	1.0904E-12
A4	7.88691E-13	8.36509E-13
A5	8.79004E-13	1.09757E-12

C_pin versus C_pin(measured)



Largest Δ when signal is farthest from powers and grounds

Conclusions

- Capacitance matrix data must be manipulated when comparing it to measured capacitance
  - Maxwell capacitance is not what is typically measured
  - Important for datasheet comparisons and model to simulation correlation

Acknowledgements

- Thanks to Bruce Schober at Micron for development of the analyzer tool and figuring out the matrix math.

Micron®