

PDN design and analysis methodology in SI&PI co-design

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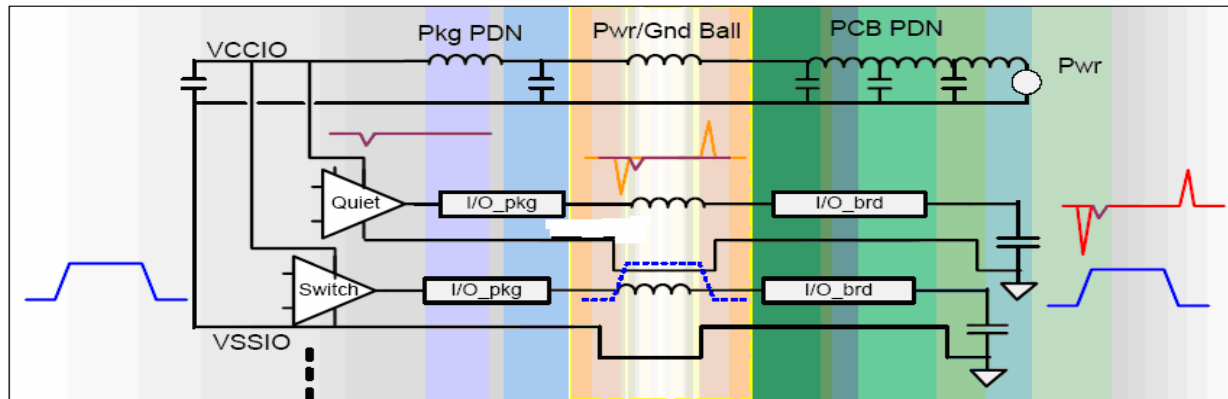
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Agenda

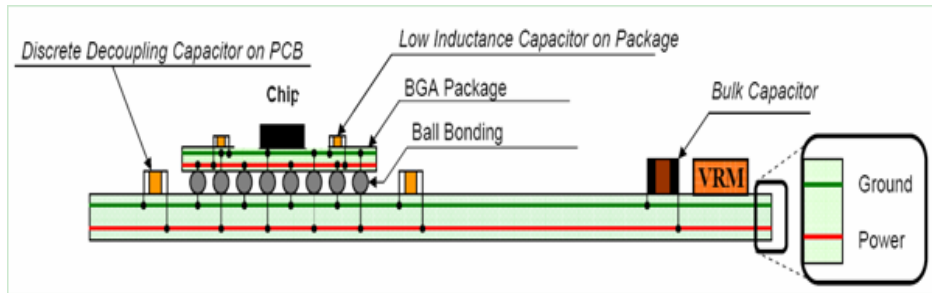
- ❖ **SI&PI co-design challenge**
- ❖ **Key parameters in PDN design**
- ❖ **Modeling the loop inductance of high frequency capacitor**
- ❖ **High frequency capacitor' global decouple effect**
- ❖ **Tight coupling Power-Gnd pair in board' PDN**
- ❖ **SSN analysis of PDN' SI&PI co-design via PDN' IBIS model**

SI&PI co-design challenge



- ◆ As signal IO voltage level decreasing and signal speed constantly increasing, the effect of SSN become serious,.
- ◆ SSN noise directly affect noise margin of low voltage level and time margin of high speed signal.
- ◆ Traditional independent SI and PI analysis bring the limitation.

Key parameters in PDN design

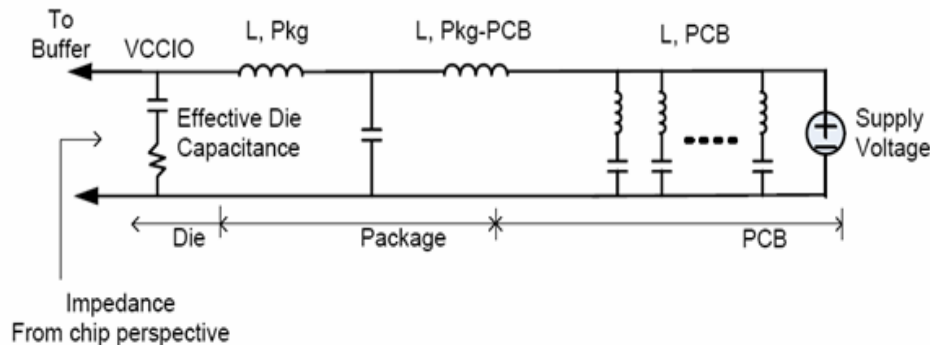


Board' PDN sketch map

PDN of Board:

- ◆VRM
- ◆Bulk capacitor
- ◆High frequency capacitor
- ◆Power-Gnd plane capacitor
- ◆Chip' PDN

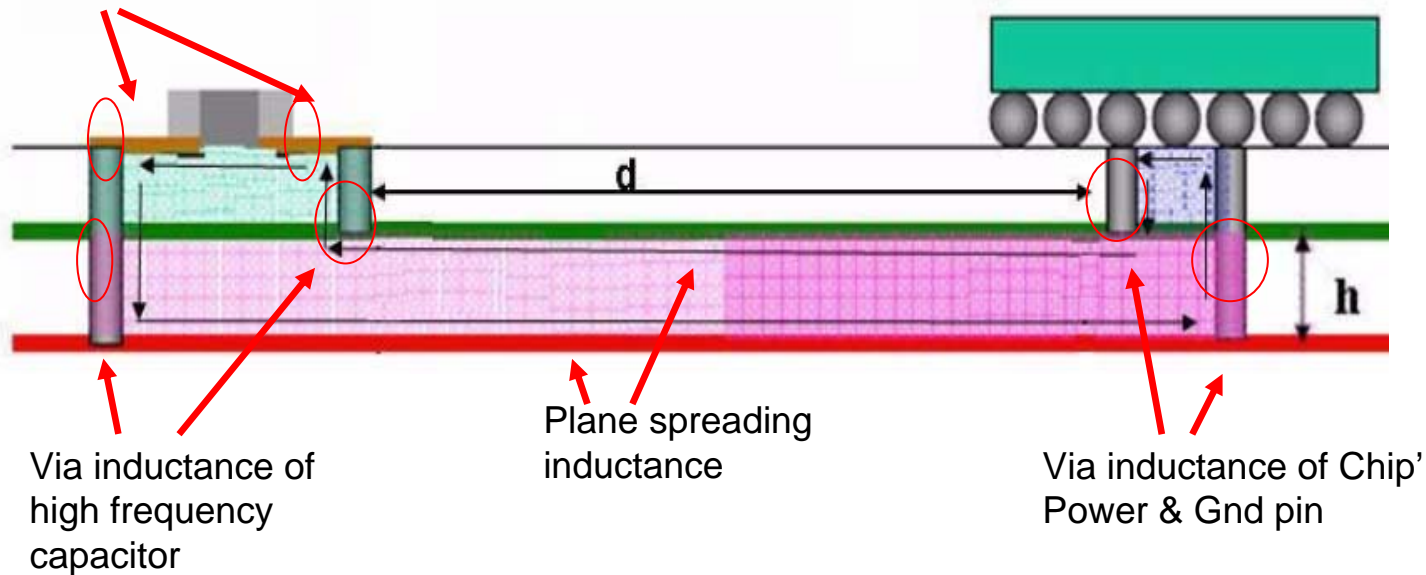
High frequency capacitor and Power-Gnd plane play an important role in PDN design;



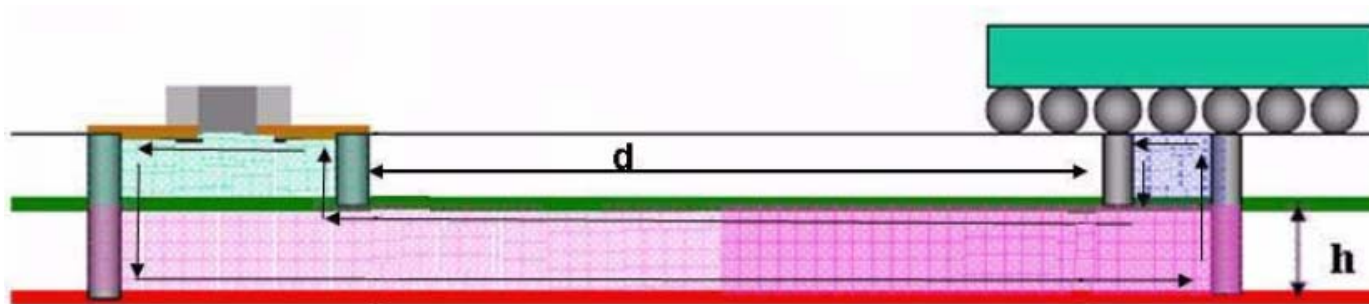
Equivalent circuit of board' PDN

Loop inductance of high frequency capacitor

Fanout inductance

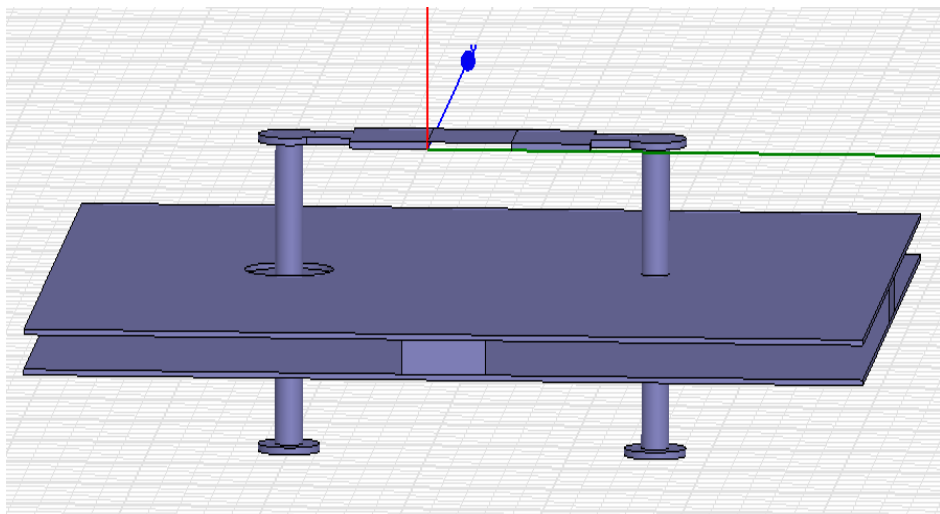


Via inductance effect in Loop inductance



- ◆Capacitor' ESL: 0.4~0.65nH;
- ◆Special fanout inductance: 0.25~0.3nH;
- ◆Plane spreading inductance: hundreds of pH;
- ◆Via inductance of Capacitor: 1nH~2.5nH,when in different stackup, The Value will be varied

Modeling the via inductance

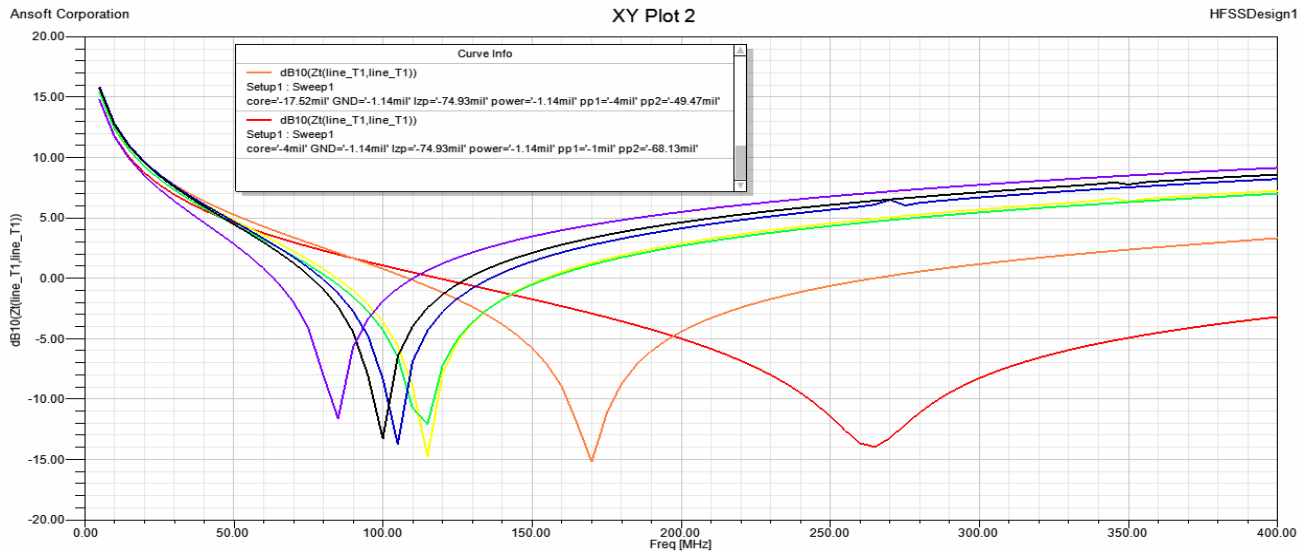


measurement	Simulation	precision
2.29nH	2.25nH	98%

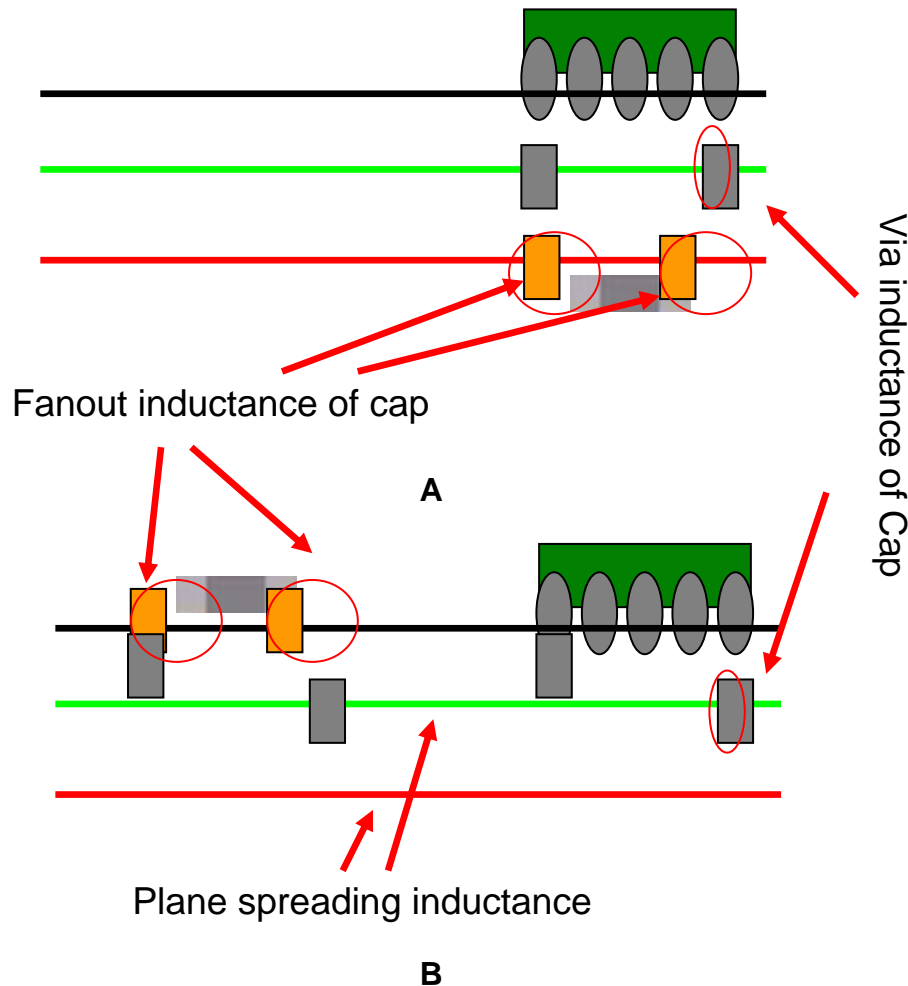
- ◆ Via inductance is about 75%~80% of the total loop inductance;
- ◆ As the the Power-Gnd pair space and location changed, the via inductance of capacitor may varies;
- ◆ Optimizing the design of Power-Gnd pair will decrease the via inductance, increase the decouple effect of high frequency capacitor;
- ◆ Evaluate the value of via inductance by simulation, comparison between simulation and measurement validate the precision of via inductance model.

Comparison of capacitor decouple effect with different via inductance

Power-Gnd plane space	Power-Gnd plane location	Via inductance of Caps	Corresponding line
$S \leq 10\text{mil}$	Above of the Stackup	$0.3\text{nH} < L < 0.55\text{nH}$	Red line
$10\text{mil} < S < 30\text{mil}$	Above of the Stackup	$0.55\text{nH} < L < 1.5\text{nH}$	Orange line
$S \leq 10\text{mil}$	Center of the Stackup	$L \approx 2.5\text{nH}$	Green line
$10\text{mil} < S < 30\text{mil}$	Center of the Stackup	$2\text{nH} < L < 2.5\text{nH}$	Yellow line
$30\text{mil} < S < 65\text{mil}$	Center of the Stackup	$2.3\text{nH} < L < 3\text{nH}$	Blue line
$10\text{mil} < S < 30\text{mil}$	Underside of the stackup	$3\text{nH} \leq L$	Black line
$S \leq 10\text{mil}$	Underside of the stackup	$3.2\text{nH} < L$	Purple line

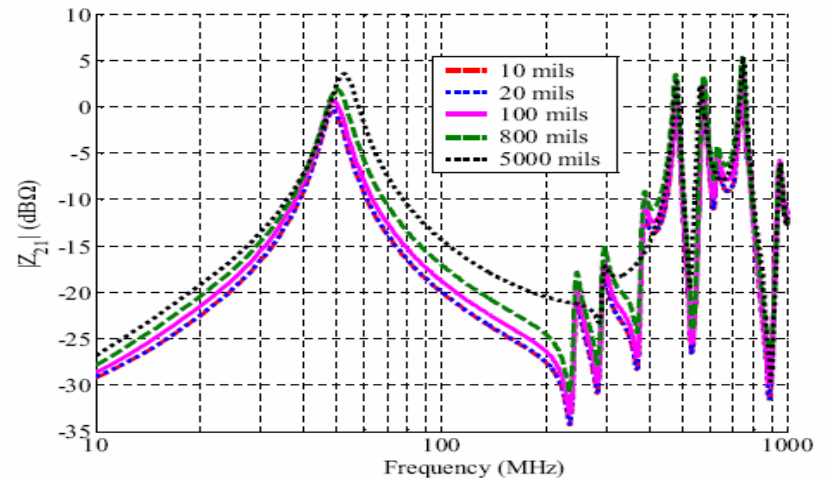
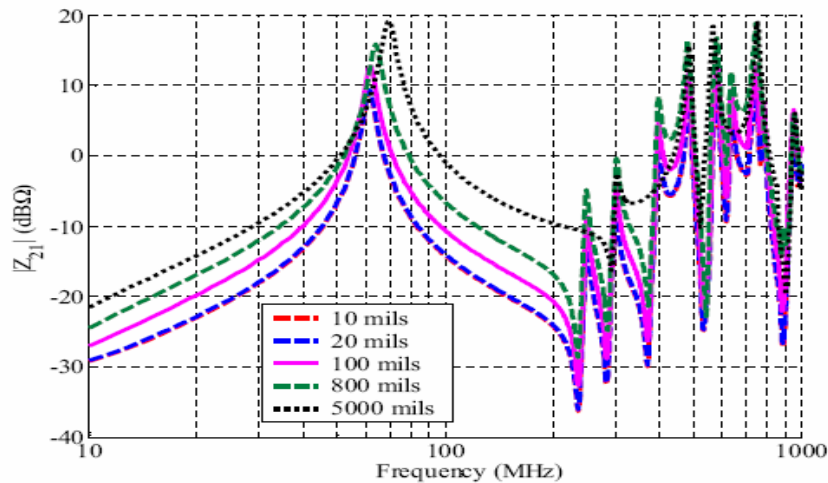


Plane spreading inductance affect high frequency cap decouple



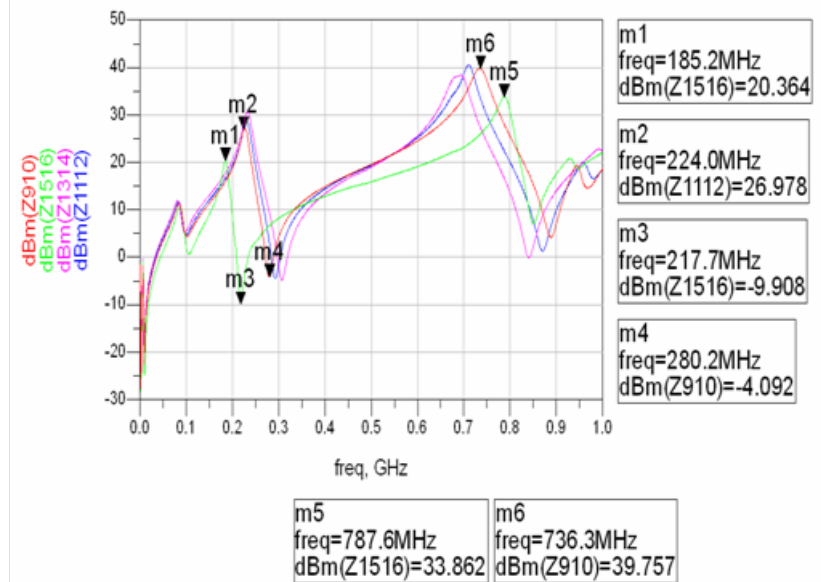
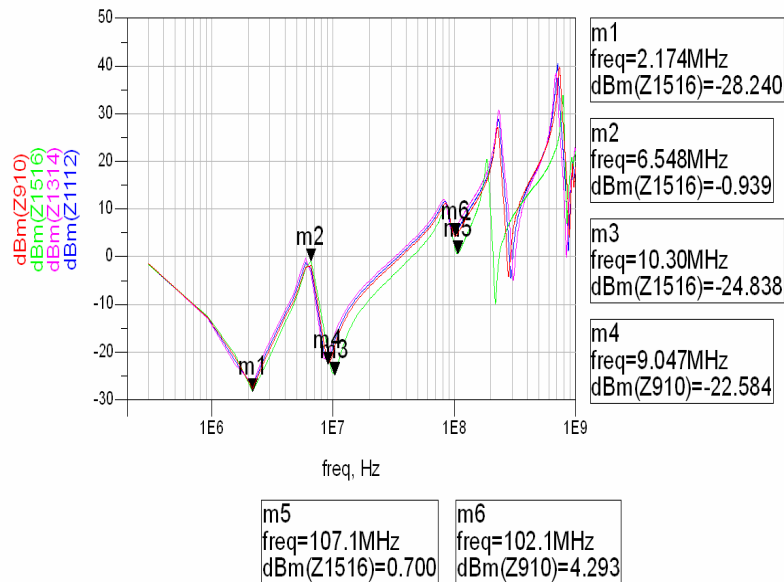
- ◆ Designing the PDN of PCB, in order to decrease loop inductance of capacitor, high frequency decoupling capacitor will be located as close as possible to chips' power pin;
- ◆ High frequency decaps usually locate under the chip, close to the power pin;
- ◆ In actual design, Both chips and decaps need to be located on top side of PCB, for the limitation of chip's dimension, decaps only can be near to the chips, not close to power pin,
- ◆ as seen as left fig B, plane spreading inductance increase while both chip and decap be located on top side of PCB;
- ◆ Compared with fig A, the total loop inductance in fig B will increase, and High frequency capacitor' decouple effect obviously decrease;

Global decouple effect of high frequency cap



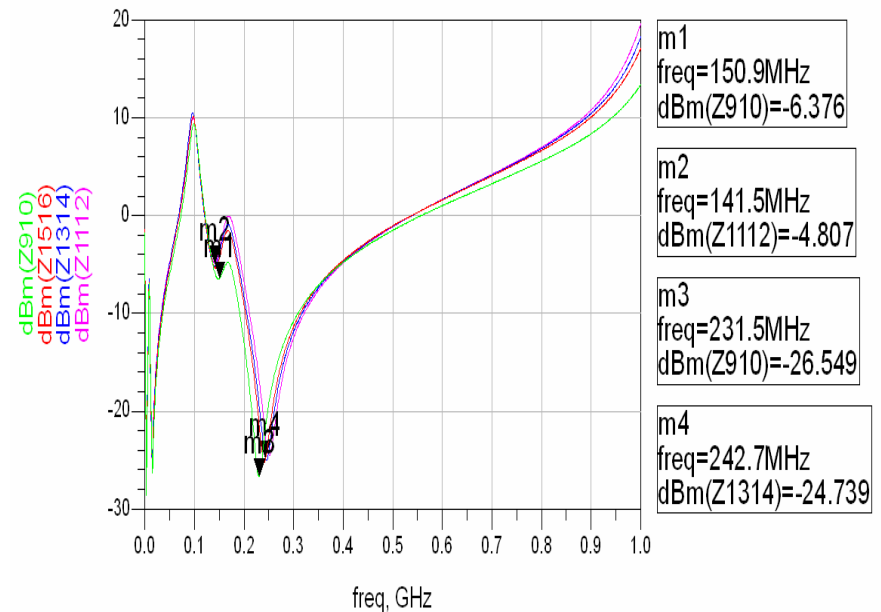
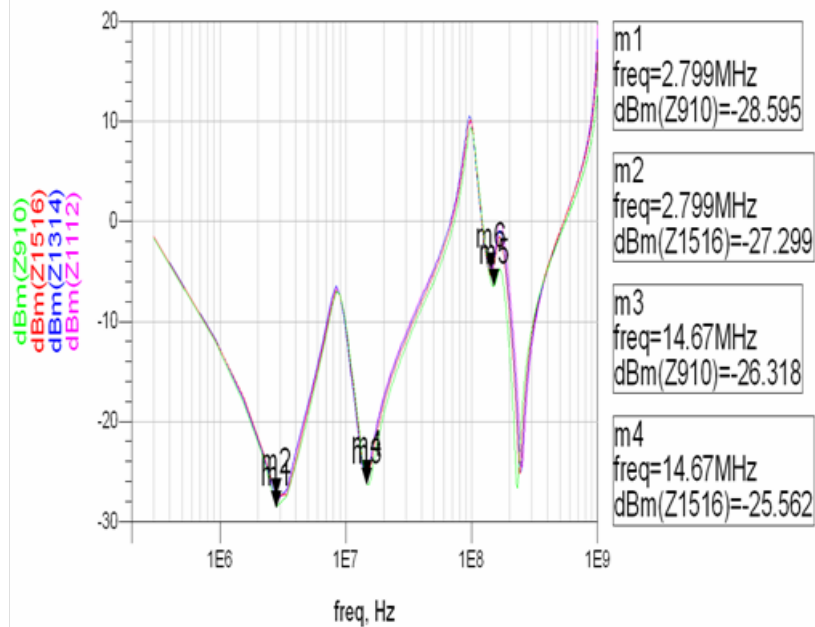
◆ As decreasing the space between the Power Ground plane, the total loop inductance also decrease, and high frequency caps will show an global decouple effect.

Power-Gnd pair space more than 30mils,high frequency capacitor show an local effect



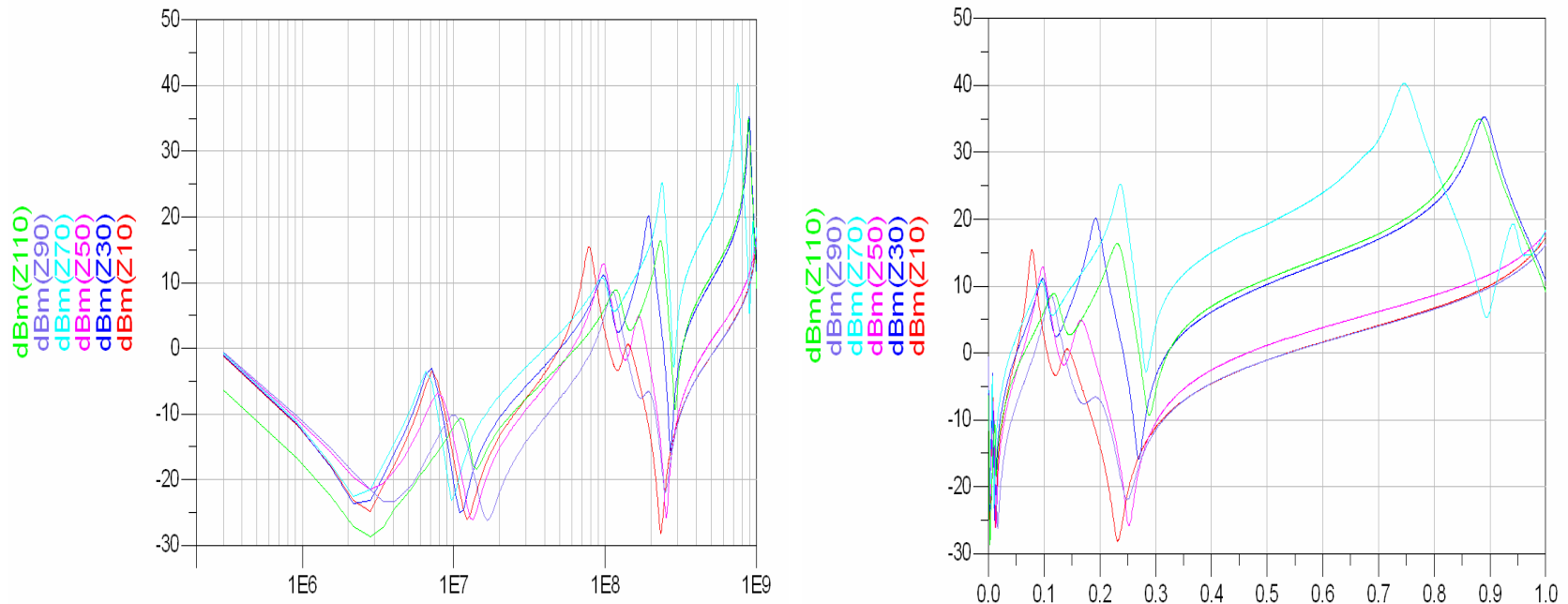
◆Power-Gnd pair space more than 30mils, distance between chip and capacitor varying from 500mils to 1000mils, the resonance frequency and anti-resonance frequency of high frequency capacitor will change.

Power-Gnd pair space less than 10mils, high frequency capacitor show an global effect



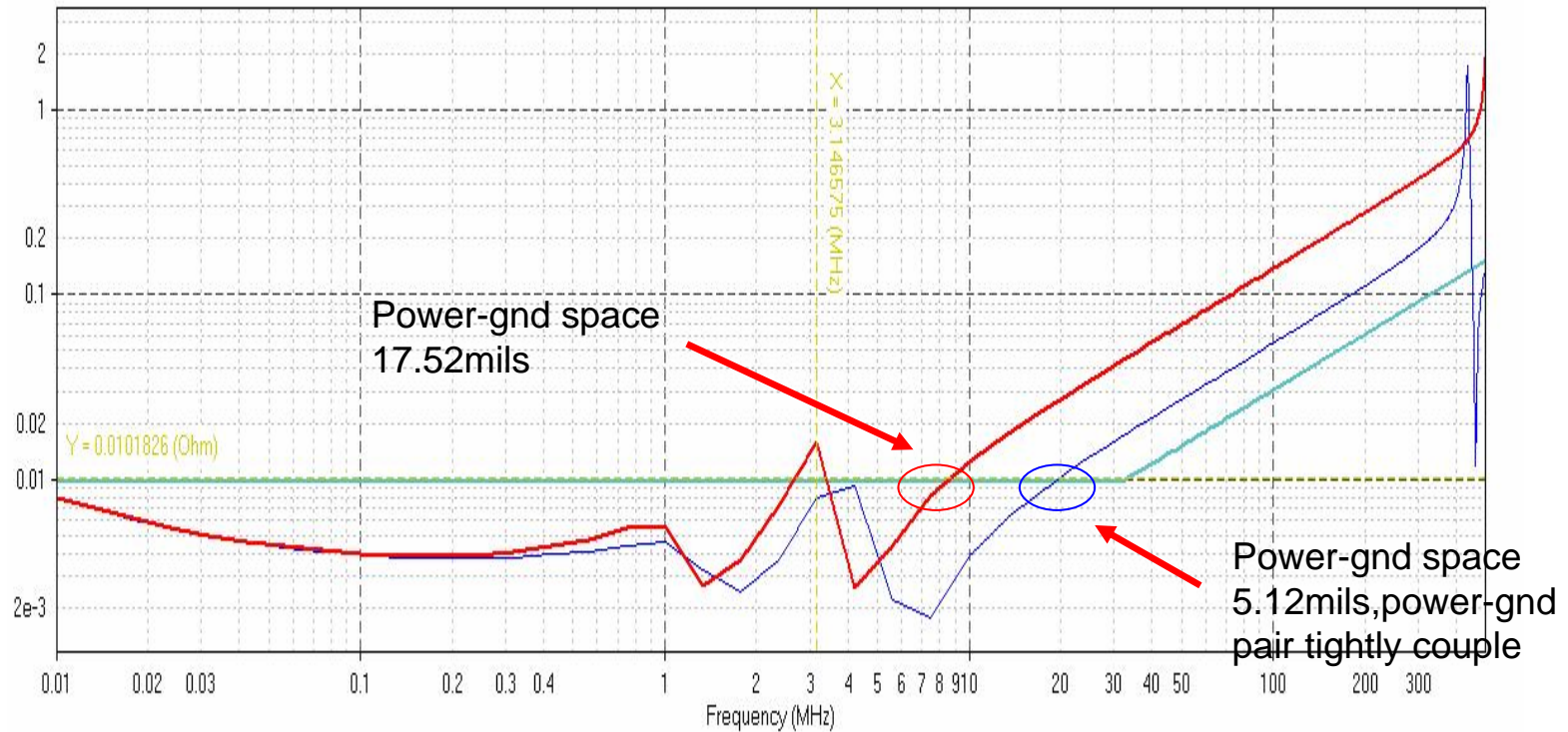
◆ Power-Gnd pair space less than 10mils, distance between chip and capacitor varying from 500mils to 1000mils, the resonance frequency and anti-resonance frequency of high frequency capacitor almost keep same.

Power-Gnd pair space effect analysis of PDN design

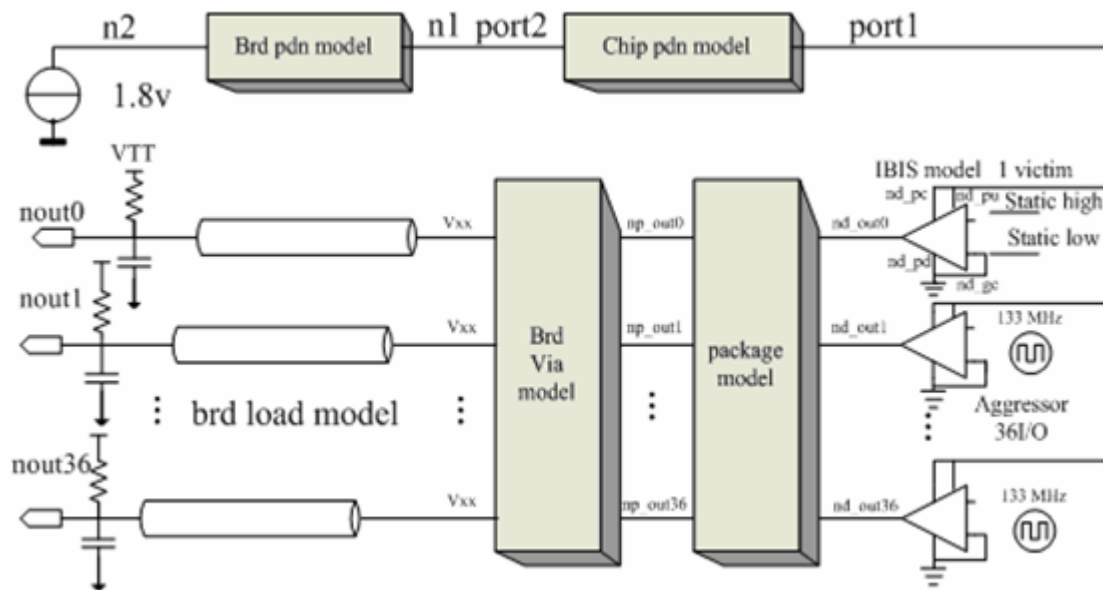


◆ Distance between chip and capacitor keep constant, power-gnd pair space varying from 5.12mils to 56.2mils, the resonance frequency and anti-resonance frequency of high frequency capacitor change.

Tight coupling Power-Gnd pair in PDN



SSN Mechanism and SI/PI Co-Design Challenges



SSN Mechanisms:

◆ Delta-I Noise and IR Drop from the System PDN (Including Die, Pkg and PCB)

$$V = L \frac{dI}{dT} + IR$$

◆ Inductive Coupling from the Whole signal link

$$\Delta v' = \sum M_{iq} di/dt$$

SSN Influence :

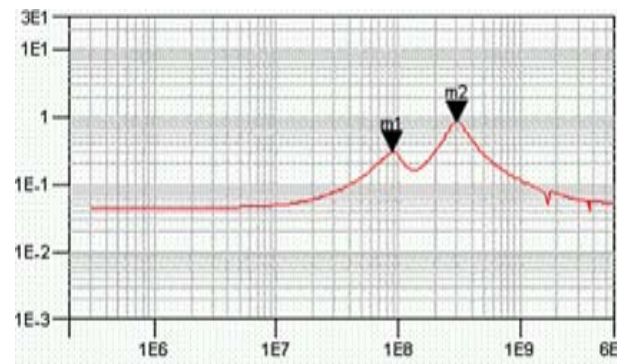
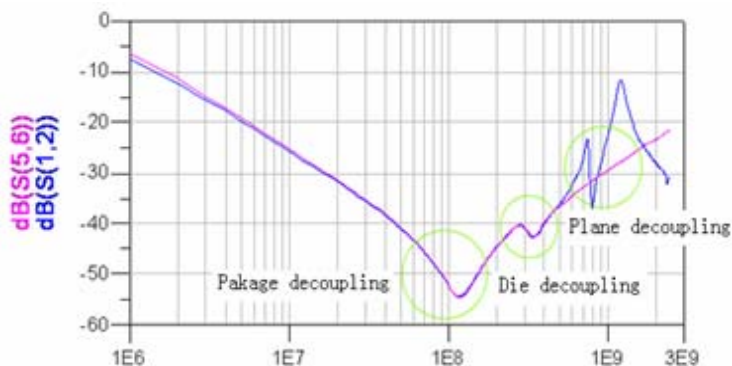
- ◆ Decrease the noise margin and timing margin
- ◆ Increase Power noise and EMI problem

SSN Simulation challenges :

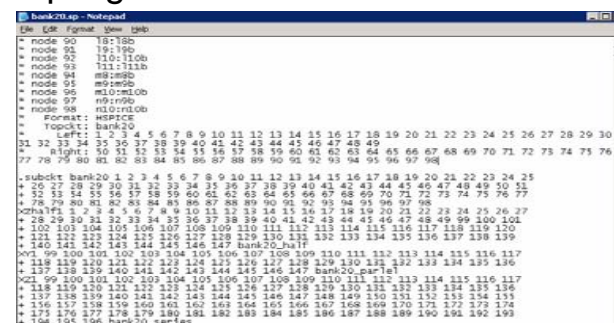
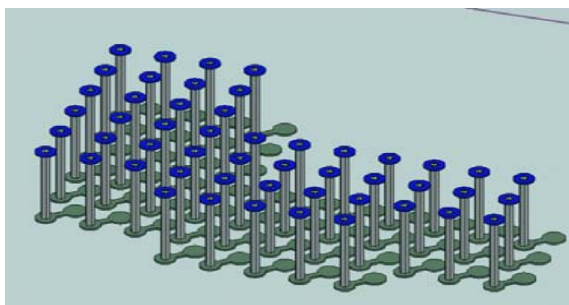
- ◆ Multi signal and PDN co-design
- ◆ Whole PDN and Coupling models
- ◆ Source active models

PDN Modeling and ibis active

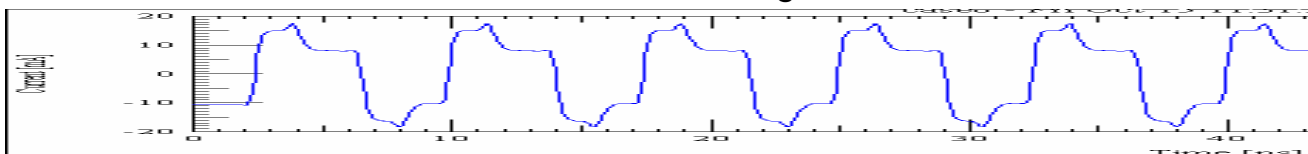
◆PDN Modeling : Die+Pkg PDN Model and System PDN Model



◆Coupling Modeling : Pkg Coupling Model and Via Coupling Model

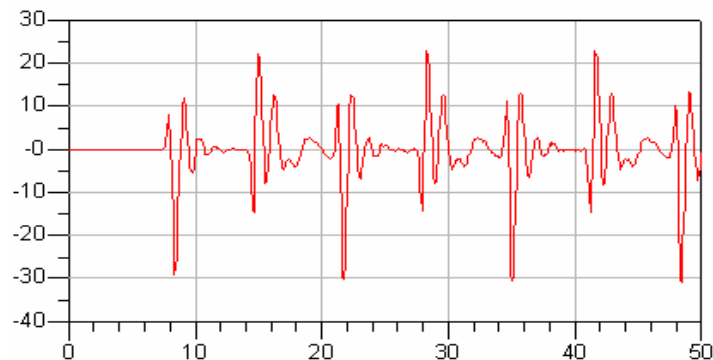
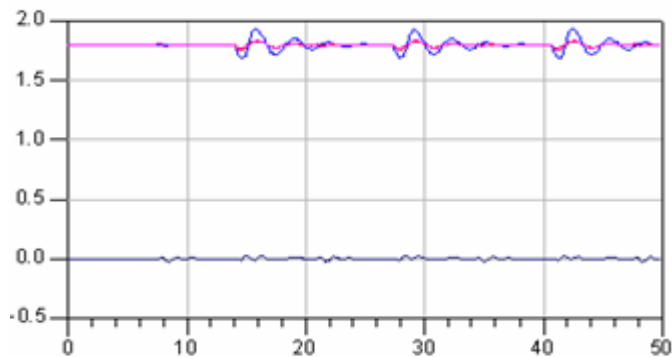


◆IBIS for the active model : IBIS buffer has some advantage and limitation for SSN simulation

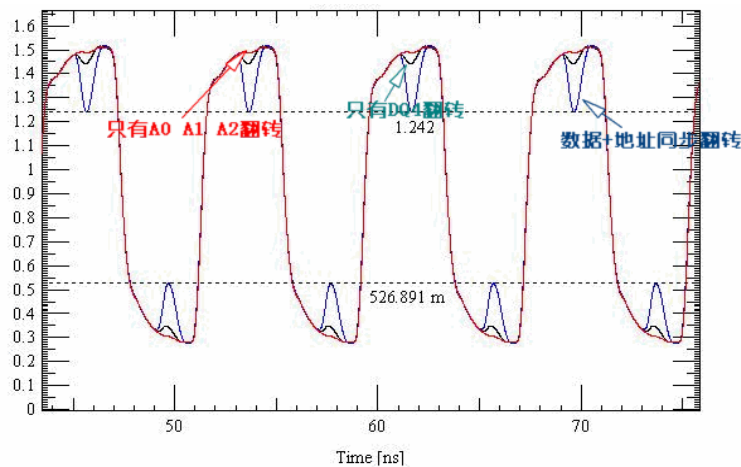
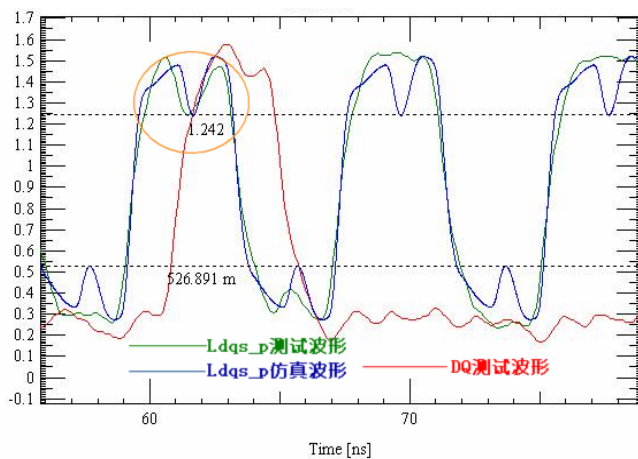


SSN Simulation using ibis models

◆Delta-I Noise and Multi Crosstalk



◆SI+PI Co-simulation using ibis models



Conclusion

PDN directly determine the board' power delivery system design quality, and in board' PDN high frequency capacitor and Power-Gnd plane play an important role;

- ◆The loop inductance of high frequency capacitor decrease as smaller as possible in a well designed PDN ,and capacitor show an global decouple effect;

- ◆The tight coupling PDN adequately consider power-gnd plane capacitor, expanding the efficiency frequency band;

SSN analysis via PDN' IBIS model enhance simulation efficiency and speed. Implementing SI&PI co-design.

Thank you

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