Spice Subcircuit Support for Serial Link Channel Design Using IBIS [External Model]

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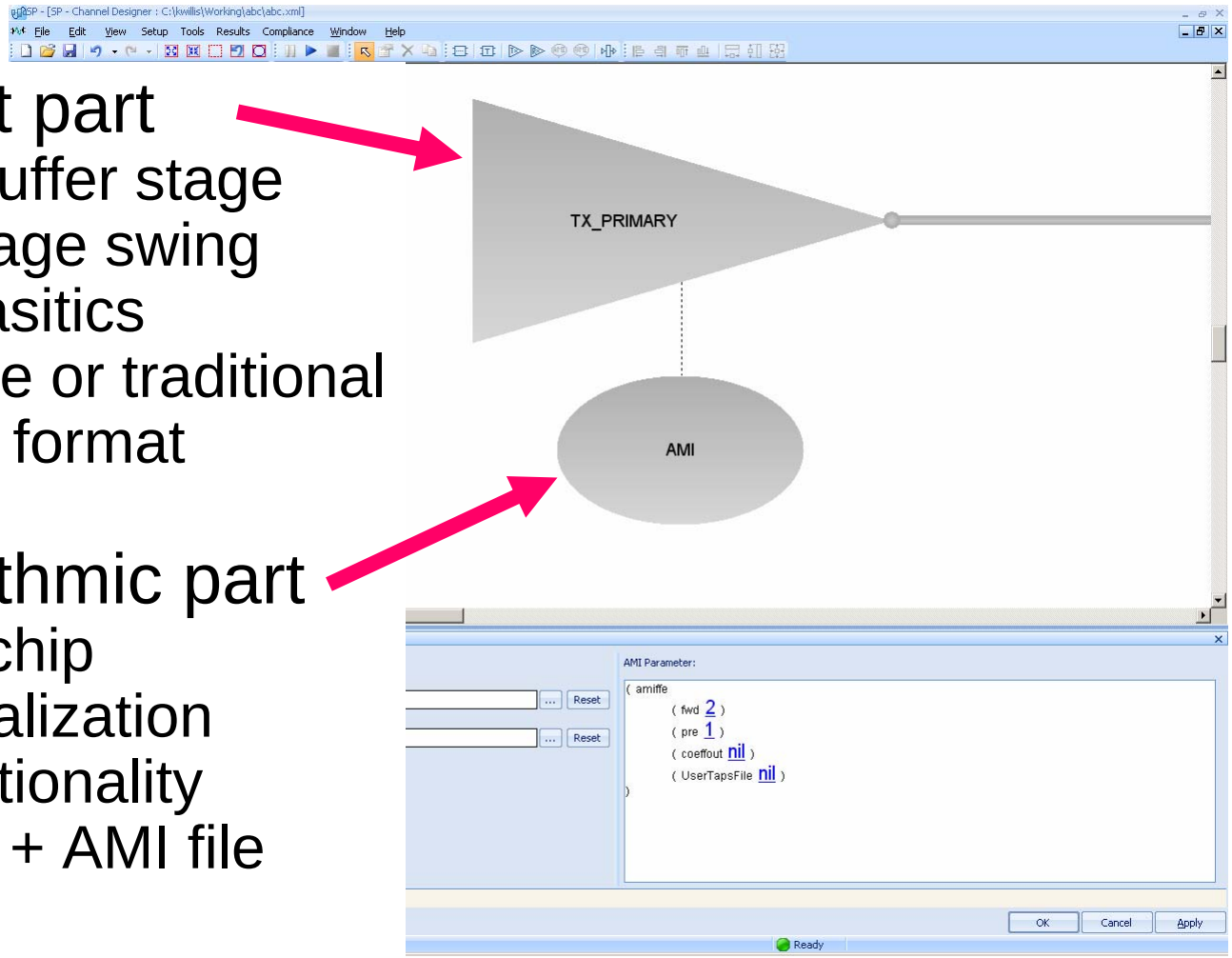
Agenda

- Review existing solutions for serial link IBIS models in channel design
- The advantages of using Spice-based IO models for serial links
- Support Spice-based models using IBIS [External Model] keyword

IBIS-AMI Model Sub-Components

- Circuit part
  - IO buffer stage
  - Voltage swing
  - Parasitics
  - Spice or traditional IBIS format
- Algorithmic part
  - On-chip
  - Equalization functionality
  - DLL + AMI file



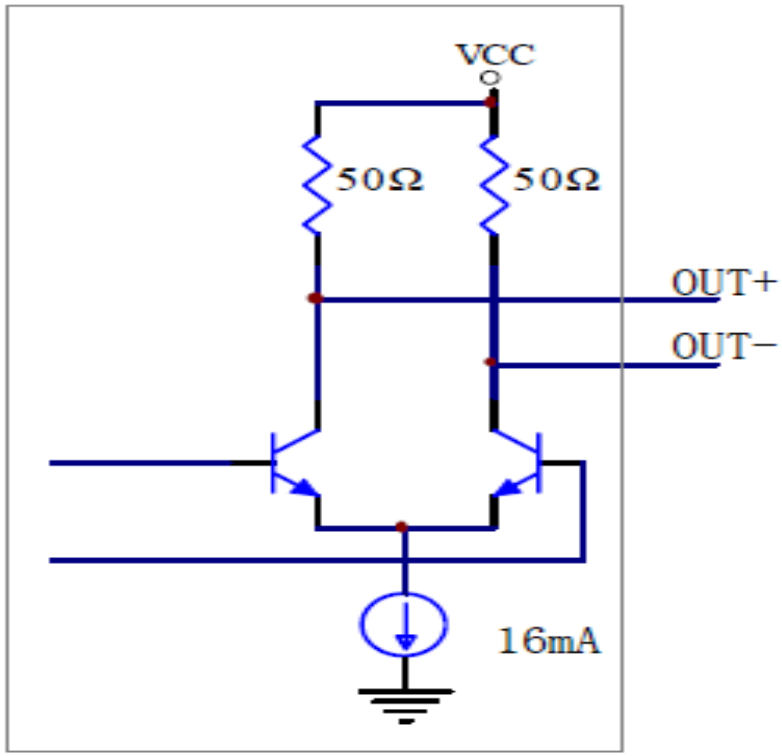
This presentation focuses on the "circuit" part

Existing Solutions for Serial Link IBIS Circuit Models

- Most of the models use Spice-based subcircuits
  - No standards for the description of the subcircuits
  - May need much manual work to edit the netlist for specific EDA tools
- Specified (not standard) keywords in IBIS models
  - Specifications are provided by specified EDA tool
  - Don’t need manual work to edit the netlist, but only appropriate for specified EDA tool

Spice-Based IO Circuit Model

- Can easily represent the actual IO structure (ex. pullup resistor with pulldown current source for CML)



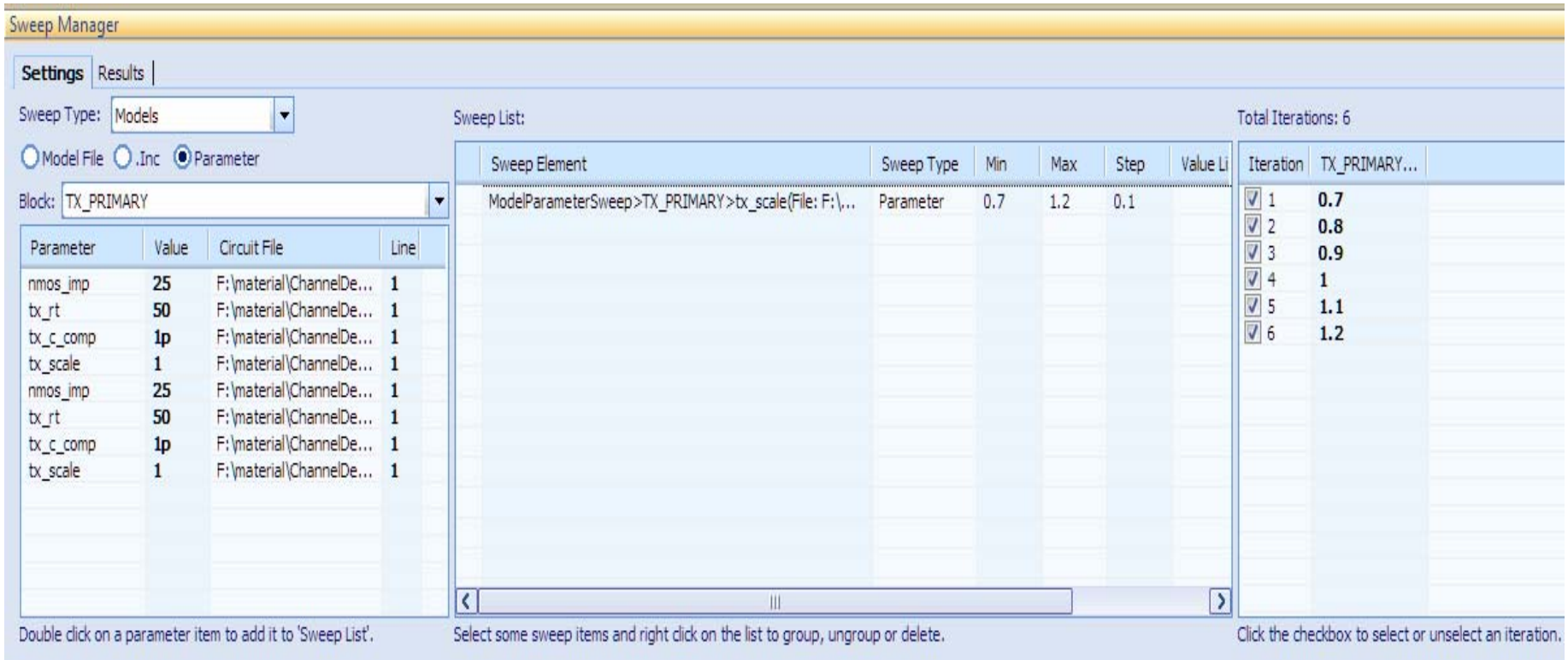
Spice-Based IO Circuit Model (Cont.)

- Incorporate hookups for non-ideal power connections
  - External power supply can be linked with the power node of the Spice subcircuit and used for non-ideal power analysis

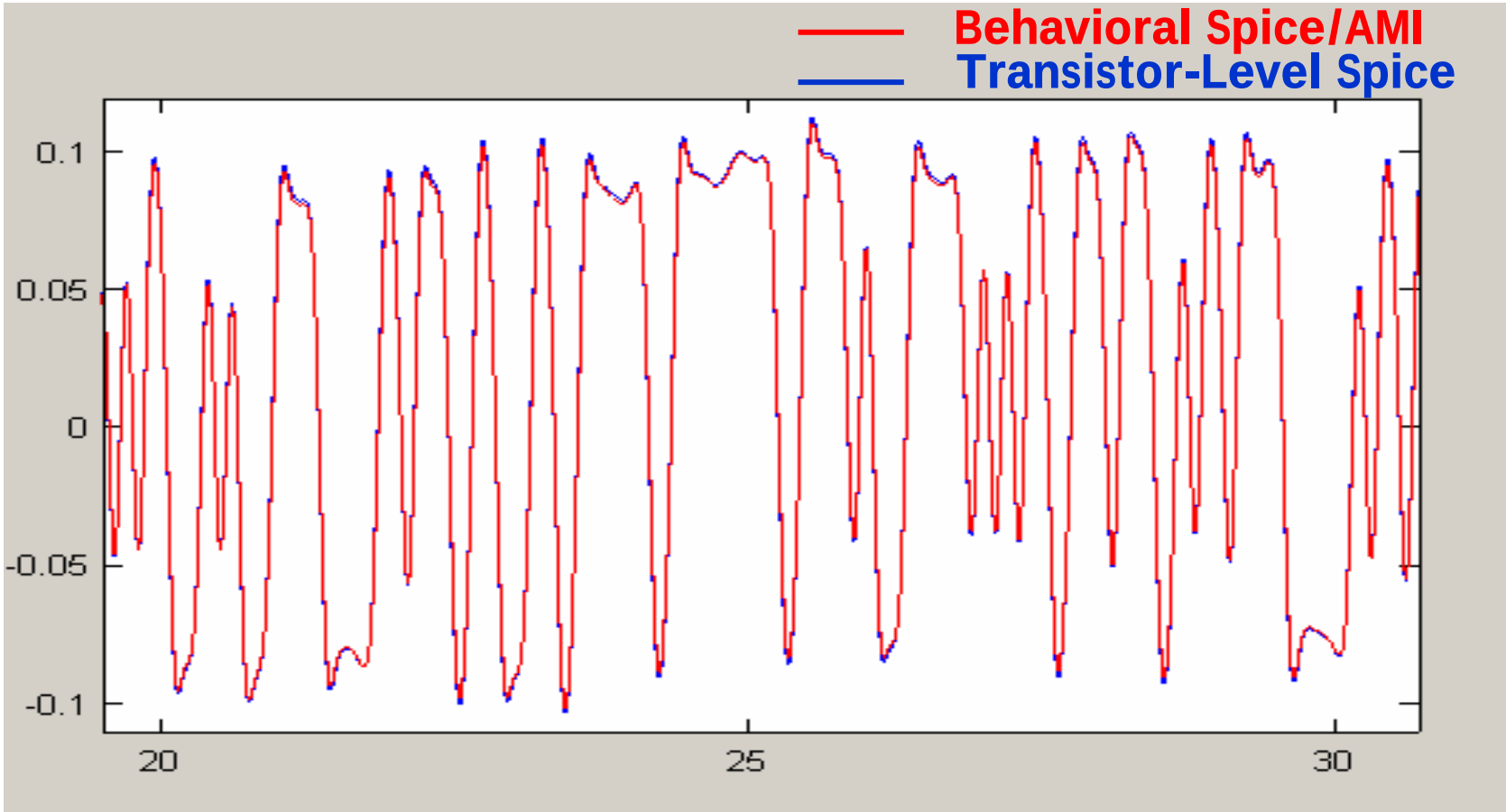
- Incorporate on-chip parasitics easily, including PDS, S-params for RDL routing, etc.

Spice-Based IO Circuit Model (Cont.)

- Usage of parameterized subcircuits, where these parameters can be swept in EDA tools



Behavioral Spice/AMI vs. Transistor-Level Spice at 10 Gbps, EQ on (from telecomm chip company)

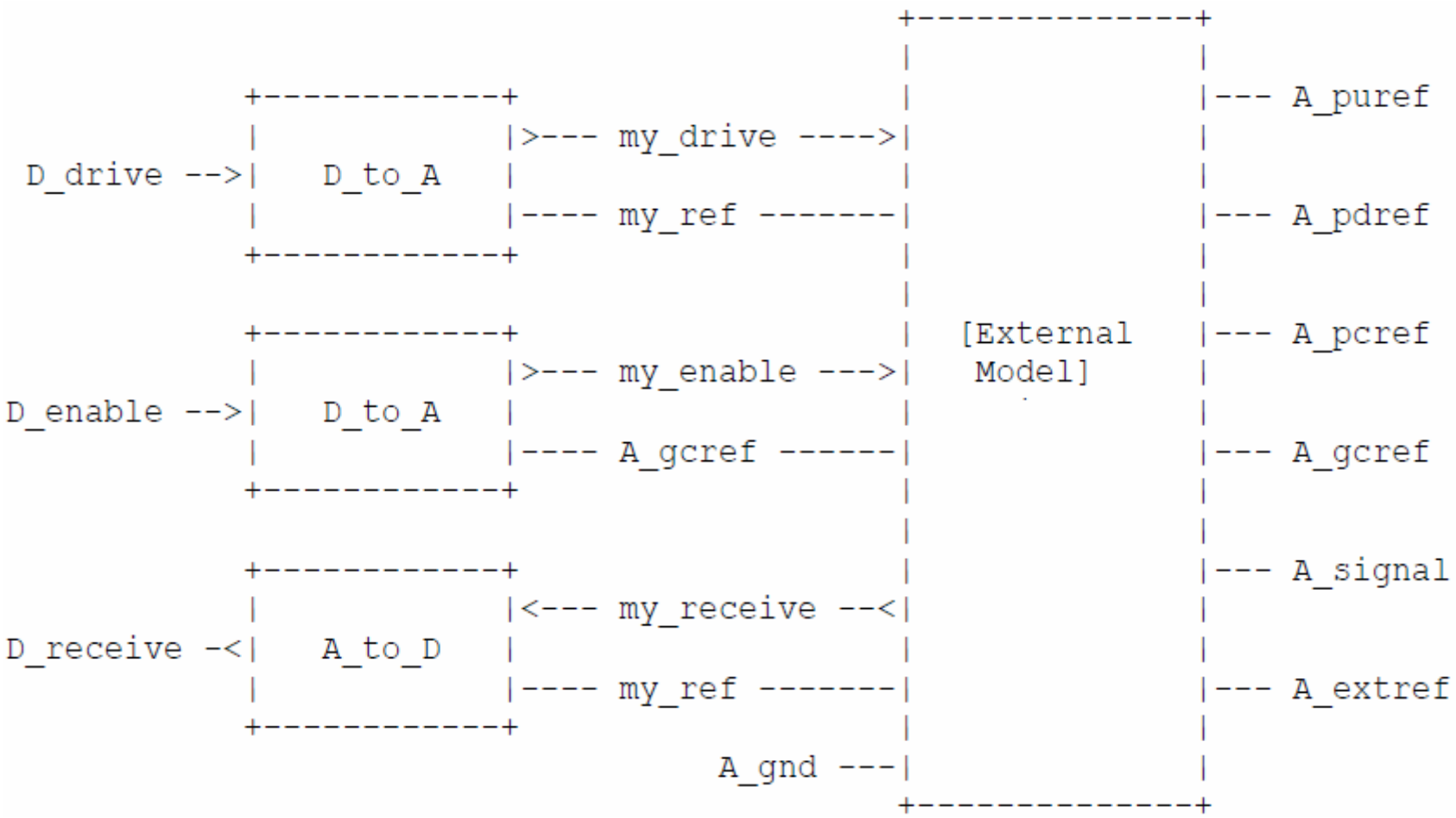


IBIS [External Model]

- Used to reference an external file written in one of the supported languages containing an arbitrary circuit definition

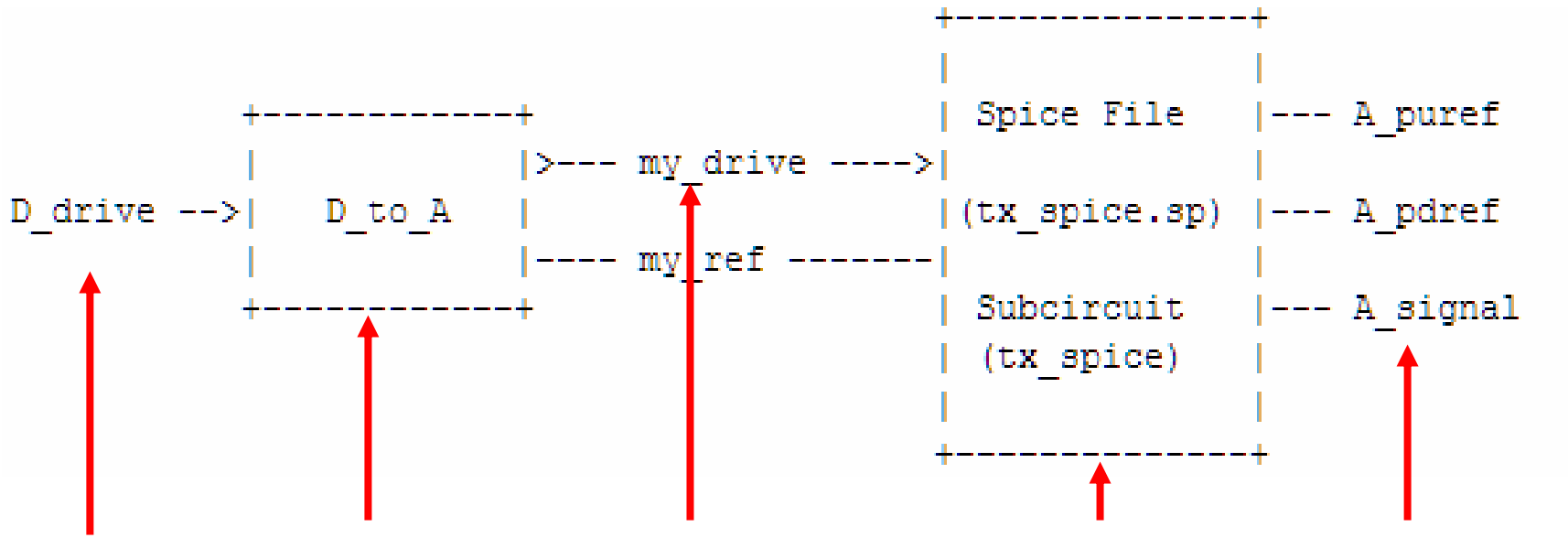
- Can be used to support the Spice-based IO models
  - Standard IBIS keyword
  - Don’t need manual work to edit the netlist
  - Suitable for all EDA tools if the tool can support standard IBIS [External Model] keyword

Ports Under [External Model]



Refer to IBIS Specification

Example of an [External Model] Output Buffer Using Spice



Digital stimulus

Defines voltage levels, input ramp rise and fall times

Voltage stimulus for Spice subcircuit

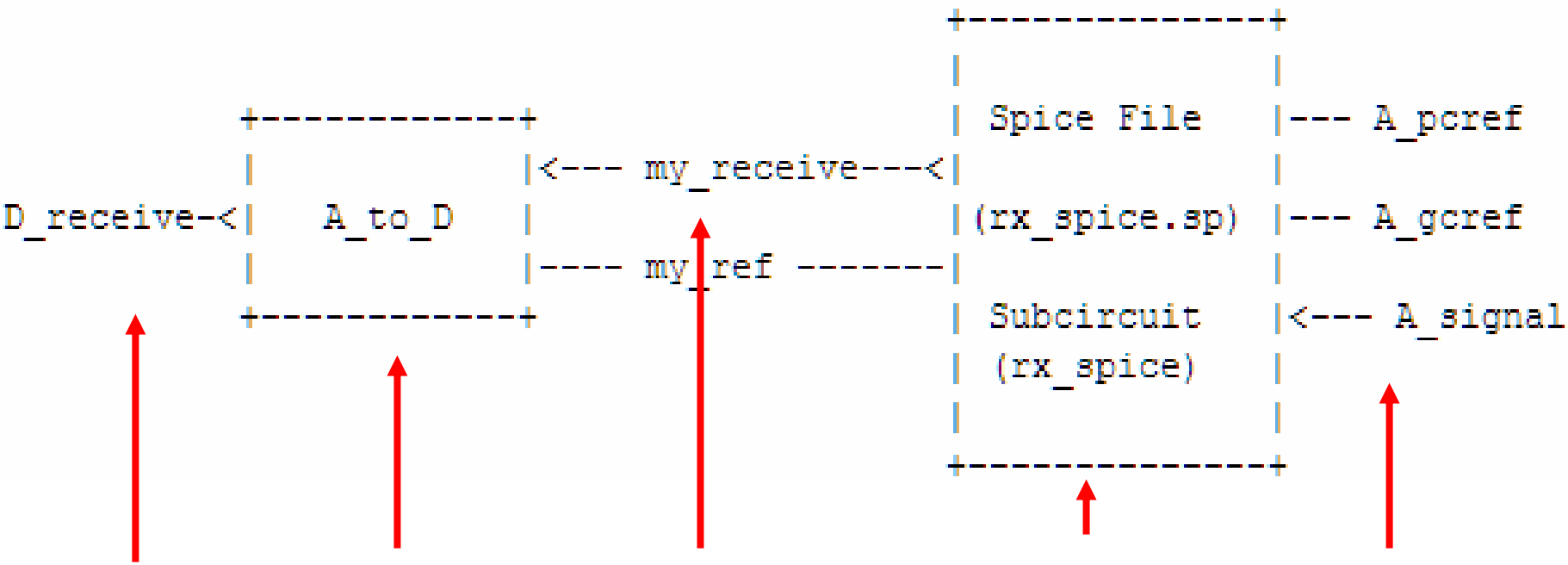
Spice-based model

Output port, pull up and pull down reference ports

[External Model] Description for Output

```
[External Model]
Language Spice
| Corner  corner_name  file_name     circuit_name (.subckt name)
Corner       Typ          tx_Spice.sp         tx_Spice
|
| Ports List of port names (in same order as in Spice)
Ports    A_puref    A_pdref   A_signal   my_drive
|
| D_to_A   d_port      port1         port2      vlow   vhigh   trise    tfall      corner_name
D_to_A    D_drive   my_drive   A_pdref     0.0     1.0    0.020n 0.020n     Typ
|
[End External Model]
```

Example of an [External Model] Input Buffer Using Spice



Digital state

Defines input threshold voltage values

Received voltage for Spice subcircuit

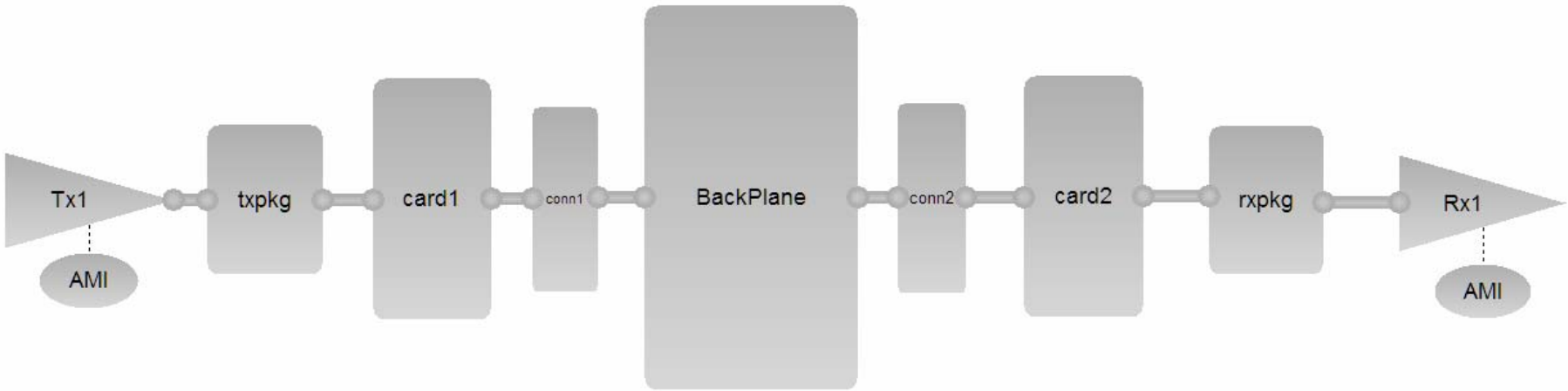
Spice-based model

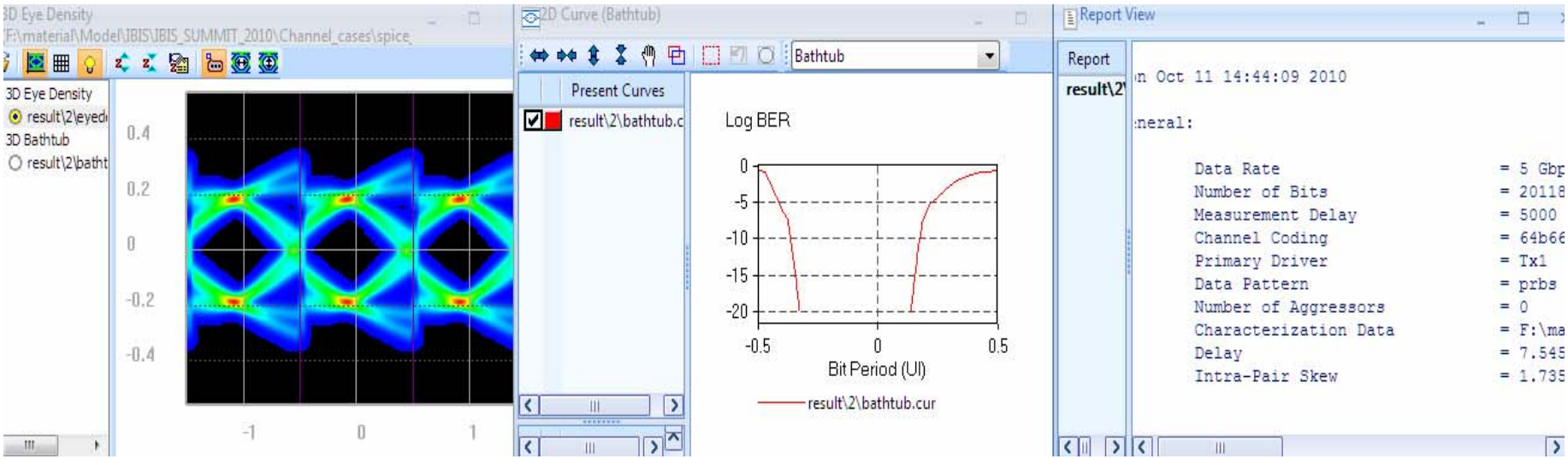
Input port, power clamp and ground clamp reference ports

[External Model] Description for Input

```
[External Model]
Language Spice
|
| Corner  corner_name    file_name      circuit_name (.subckt name)
Corner      Typ              rx_Spice.sp      rx_Spice
|
| Ports List of port names (in same order as in Spice)
Ports    A_pcref   A_gcref   A_signal   my_receive
|
| A_to_D   d_port        port1          port2          vlow   vhigh   corner_name
|A_to_D   D_receive  my_receive    A_gcref      -400m   400m     Typ
|
[End External Model]
```

System Analysis





Summary

- Spice-based subcircuits are convenient, fast, and accurate for serial link IO circuit modeling

- IBIS [External Model] keyword can be used to support Spice-based IO models, and don’t require the [Pulldown], [Pullup], [POWER Clamp], [GND Clamp] data

Thank You!