WELCOME FROM MICHAEL MIRMAK, INTEL CORPORATION

On behalf of the IBIS Open Forum, I would like to welcome you to the sixth annual Asian IBIS Summit (China). We have always been happy to visit with our friends in the People's Republic and exchange thoughts and ideas with them. I am happy to see that, regardless of conditions, the IBIS community here continues to grow in size and achievement.

We are grateful to our generous co-sponsors for their assistance in making these events possible and hope that you will encourage them to continue their support in the years to come.

These annual Summits are only part of the IBIS Open Forum's ongoing activities. We invite your participation throughout the year in on-line discussions over our e-mail reflectors and during our teleconference meetings. IBIS and the specifications it manages can only advance through the active involvement of signal and power integrity communities worldwide.

As always, we hope that you enjoy the Summit and find the presentations and discussions useful. We wish you success.

Michael Mirmak
Chair, IBIS Open Forum

欢迎词

我仅代表IBIS开放论坛欢迎各位参加第六次亚洲IBIS（中国）峰会。我们一直都很高兴地来到中华人民共和国和我们的朋友交流技术与心得。我很高兴地看到，在任何条件下，无论从使用的规模和研究的深度上，IBIS都在这里继续普及和增长。

我们感谢各赞助单位对这个会议的经济支持，并希望你们将来能继续支持这个峰会的顺利召开。

每年的IBIS峰会仅仅是IBIS开放论坛正在进行的活动的一部分。我们邀请各位能积极参与在我们的电子邮件论坛和电话会议上讨论。 IBIS开放论坛和其规范的发展依赖于全世界的工程师在信号和电源完整性的积极参与。

与往常一样，我们希望您能从此次峰会中发现有用的资料和讨论。祝大家成功。

马梦宽
IBIS峰会主席

WELCOME FROM LI JINJUN, HUAWEI TECHNOLOGIES

Dear Experts, Ladies and Gentlemen,

Since the year of 2005, the IBIS Asian Summit in China has been successful meeting on high-speed design topics. This year the attendance, paper quality and quantity have increased, and more companies are joining as sponsors.

Huawei continues to support the IBIS Committee. We greatly appreciate you, the attendees, whose enthusiasm help make these events successful.

Welcome everyone.

Best Regards,
Li Jinjun
Huawei Technologies

各位专家，各位来宾，

自从 2005 年以来，IBIS 已经成为了中国国内高速设计的一次盛会。现在，不仅内容一届比一届更深入，范围更广泛，赞助厂商和参加人数都在增加。
华为一如既往支持 IBIS 组织的活动，预祝 IBIS 技术研讨会取得成功。

谢谢大家
华为公司 厉进军

Shanghai 2009

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

8:15 REFRESHMENTS & SIGN IN
- Vendor Tables Open at 8:30

9:15 **Welcome**
- Li, JinJun
  (Huawei Technologies, China)
- Mirmak, Michael
  (Chair, IBIS Open Forum, Intel Corporation, USA)

9:35 **Point Reduction Method for IBIS Curves 5**
Wang, Lance (IO Methodology, USA)

10:05 BREAK (Refreshments and Vendor Tables)

10:25 **IBIS for SSO Analysis 15**
Wang, HaiSan; Luo, Joshua, Lin, Jack; and Zhong, ZhangMin
(Sigrity, China)

11:05 **PDN Design and Analysis Methodology in SI&PI Co-design 29**
Luo, ZiPeng and Liu, SuYao (Huawei Technologies, China)

11:35 **Correlating C_pin Capacitance with Measurements 39**
Wolff, Randy (Micron Technology, USA)

12:00 FREE BUFFET LUNCH (Hosted by Sponsors)
- Vendor Tables

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

Point Reduction Method for IBIS Curves

Lance Wang
lwang@iometh.com
Asian (China) IBIS Summit
Shenzhen, Nov. 9, 2010

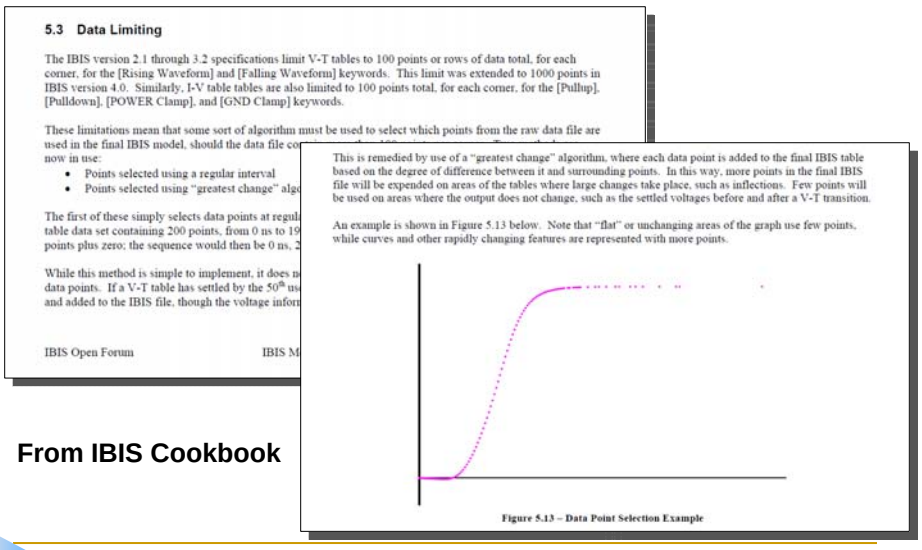
Outline

- Point Reduction Introduction
- “Greatest Change” method
- Issue with “Greatest Change” method for IBIS curve representation
- The “Weighted Best Point” (WBP) method
- Conclusions

Point Reduction Introduction

- What is Point Reduction method for?
  - In some situations, a set of data (e.g. waveform) can not satisfy a specification (e.g. IBIS) data limit without sacrifice of its accuracy. For an example, 10,000 extracted I-V curve data points for only 100 point limit in IBIS specification.
  - Point Reduction method intends to use algorithms for proper point number reduction with minimum sacrifices on its accuracy. It is about accurate representation of whole data set with limited data points
- IBIS Cookbook introduces two methods:
  - Points selected using a regular interval
  - Points selected using “greatest change” algorithm

Point Reduction Introduction



5.3 Data Limiting

The IBIS version 2.1 through 3.2 specifications limit V-T tables to 100 points or rows of data total, for each corner, for the [Rising Waveform] and [Falling Waveform] keywords. This limit was extended to 1000 points in IBIS version 4.0. Similarly, I-V table tables are also limited to 100 points total, for each corner, for the [Pullup], [Pulldown], [POWER Clamp], and [GND Clamp] keywords.

These limitations mean that some sort of algorithm must be used to select which points from the raw data file are used in the final IBIS model, should the data file co

now in use:

- Points selected using a regular interval
- Points selected using “greatest change” alg

The first of these simply selects data points at regul
table data set containing 200 points, from 0 ns to 19
points plus zero; the sequence would then be 0 ns, 2

While this method is simple to implement, it does n
data points. If a V-T table has settled by the 50th us
and added to the IBIS file, though the voltage infor

IBIS Open Forum IBIS M

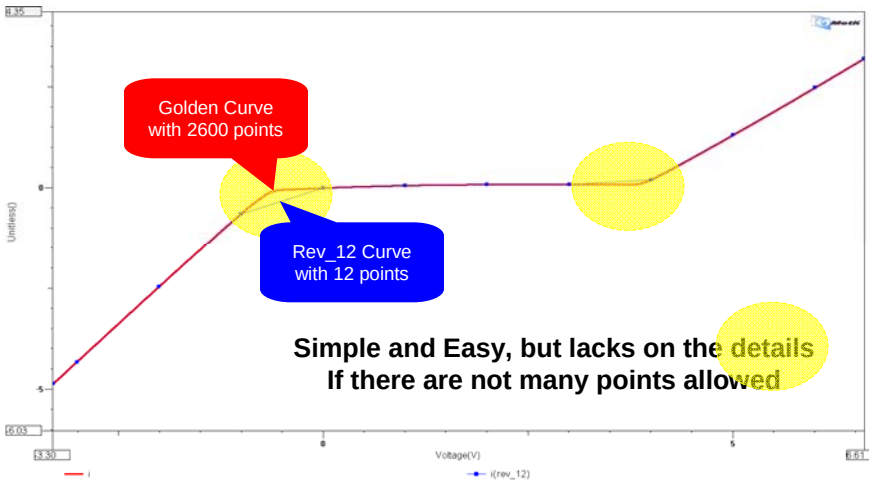
This is remedied by use of a “greatest change” algorithm, where each data point is added to the final IBIS table based on the degree of difference between it and surrounding points. In this way, more points in the final IBIS file will be expended on areas of the tables where large changes take place, such as inflections. Few points will be used on areas where the output does not change, such as the settled voltages before and after a V-T transition.

An example is shown in Figure 5.13 below. Note that “flat” or unchanging areas of the graph use few points, while curves and other rapidly changing features are represented with more points.

Figure 5.13 – Data Point Selection Example

From IBIS Cookbook

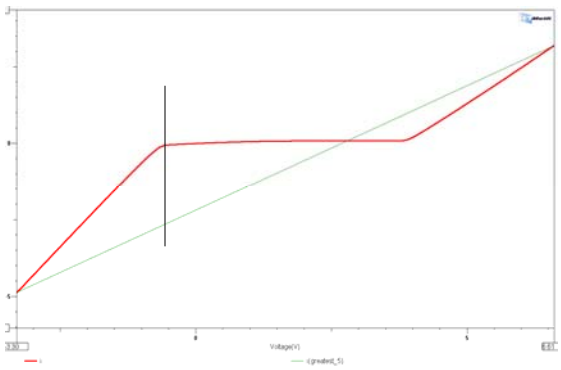
Points selected using “a regular interval” – even spacing



Points selected using “greatest change” algorithm

- Draw a line between the first and the last points; find the greatest difference (Y-axle) point between these two curves; add the third point there.

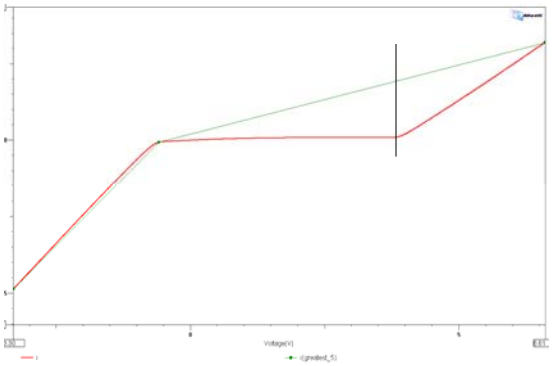
How it works?



Points selected using “greatest change” algorithm

- Find next the greatest difference (Y-axle) and add 4th point

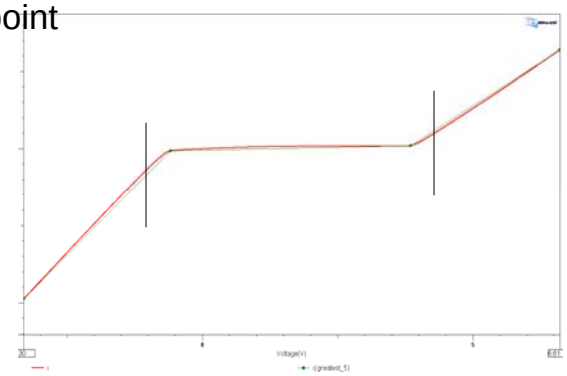
How it works?



Points selected using “greatest change” algorithm

- Find next the greatest differences (Y-axle) and add 5th and 6th point

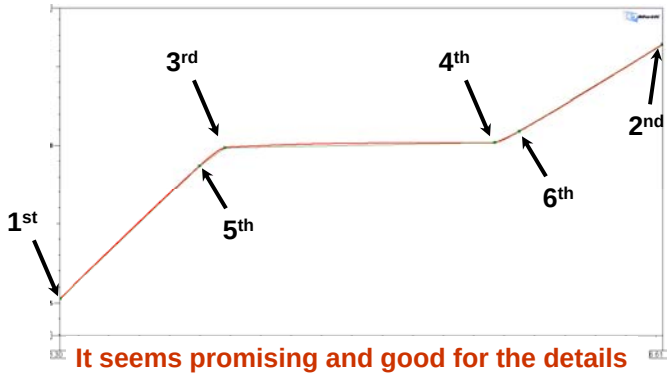
How it works?



Points selected using “greatest change” algorithm

- And so on …

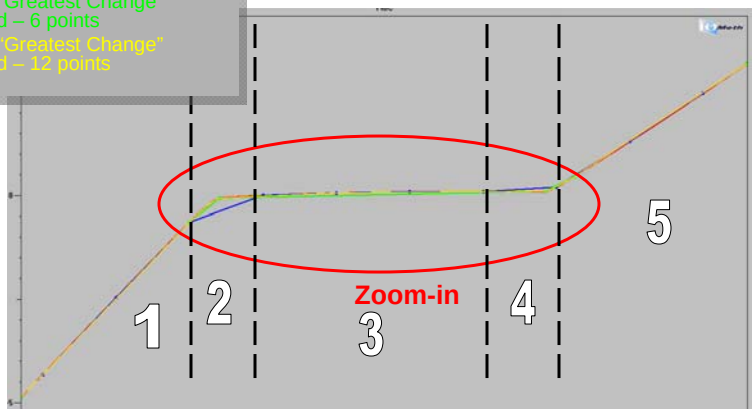
How it works?



It seems promising and good for the details

Comparing two methods with Golden curve

- Golden curve
- Using “a regular interval” method – 12 points
- Using “Greatest Change” method – 6 points
- Using “Greatest Change” method – 12 points



Comparing two methods with Golden curve

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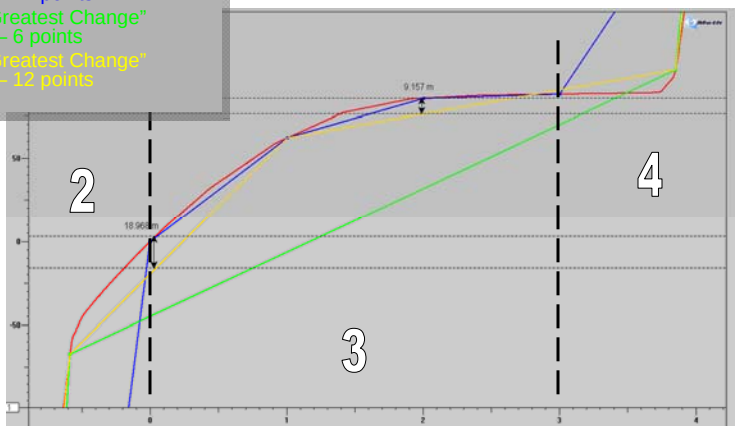

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Comparing two methods with Golden curve

- We got:
  - “a regular interval” method – even spacing
    - Simple and easy
    - Lack on the details
    - Accuracy is highly depended on space/point numbers
  - “greatest change algorithm” method
    - Higher accuracy on average
    - Good on the details
    - May have “too few” points in the certain areas and it could compacts the results of simulations

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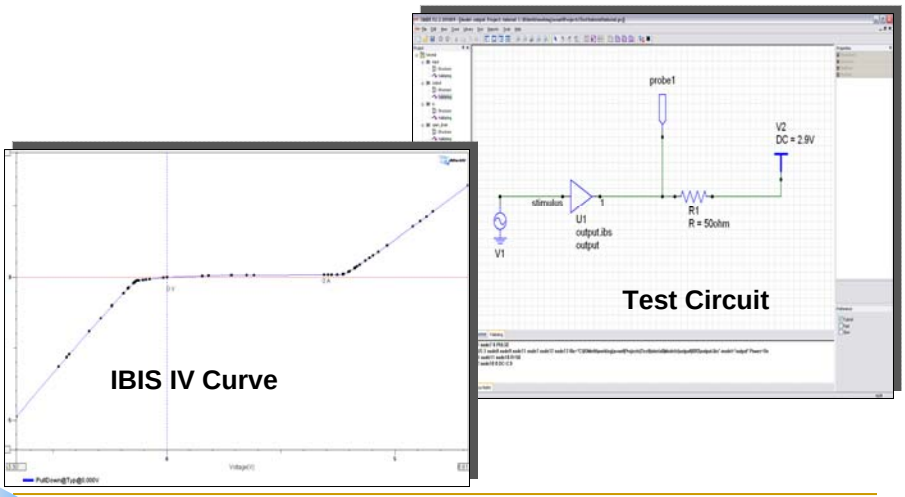
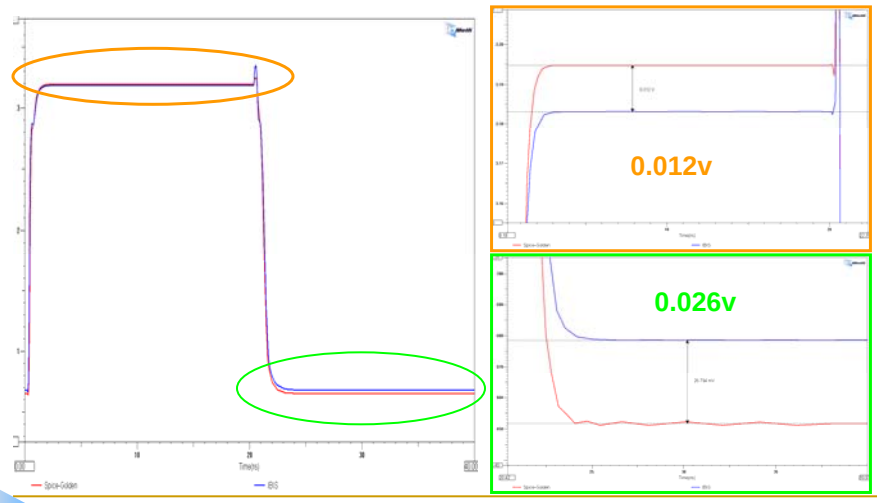
Issue with “Greatest Change” method for IBIS curve representation

- The most of IBIS generation tools are using “Greatest Change” algorithm (so called “Best Point” too) now.
- It works fine with IBIS VT curve point reduction
  - The big part of reason is that VT curves are co-factor in simulation calculations. More details are better.
- Sometimes it causes inaccurate simulation result due to too few points in the working range in the IV curves

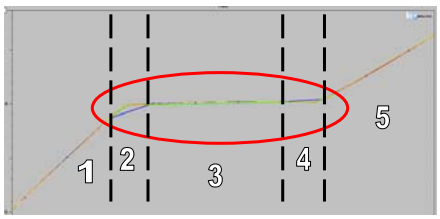
A test case for the curves using “the greatest change” algorithm method



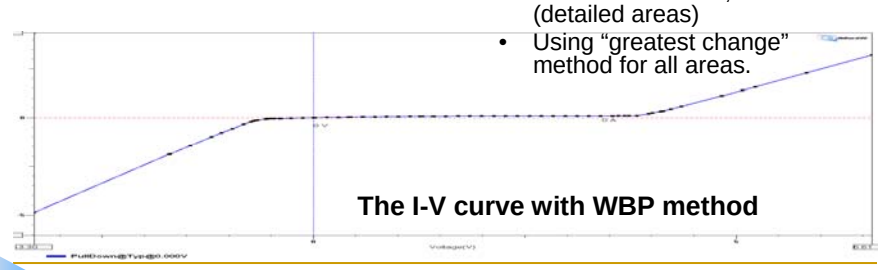
A test case for the curves using “the greatest change” algorithm method



The Weighted Best Point (WBP) method

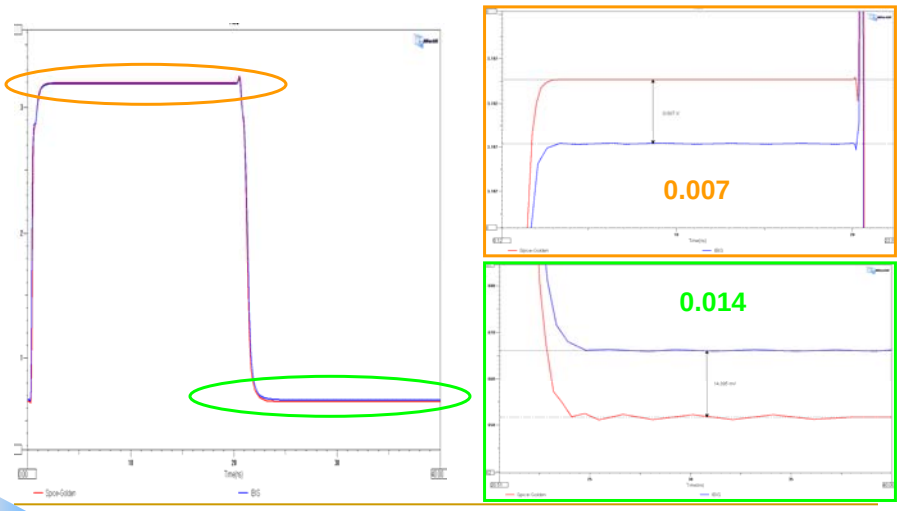


- WBP method is a combination of “regular interval” and “greatest change” methods with more focuses on working range
  - Using “regular interval” for Area 3 (working range)
  - Using dedicated number of points with “greatest change” method for Area 3, 2 and 4 (detailed areas)
  - Using “greatest change” method for all areas.



The I-V curve with WBP method

Test result with WBP processed IBIS model



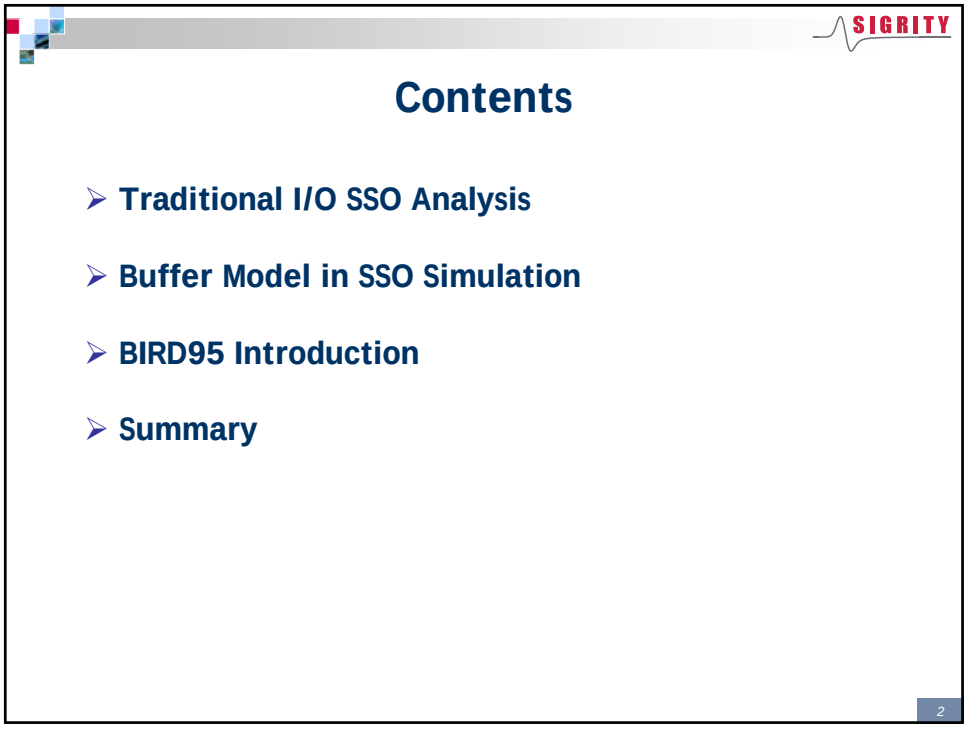
Conclusion

- Point Reduction method is needed for buffer I-V and V-T curve representations in IBIS format
- Both “Regular Interval” and “Greatest Change” algorithm methods have strong and weak areas
- WBP method combined both methods with focused areas. It improves the accuracy in IBIS simulations.
  - It is more effective for low-level signal buffer models

THE MODELING SPECIALIST

We care about accuracy!


IBIS for SSO Analysis
Asian IBIS Summit, November 9, 2010
Haisan Wang
Joshua Luo
Jack Lin
Zhangmin Zhong
SIGRITY


SIGRITY
Contents
Traditional I/O SSO Analysis
Buffer Model in SSO Simulation
BIRD95 Introduction
Summary
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SIGRITY

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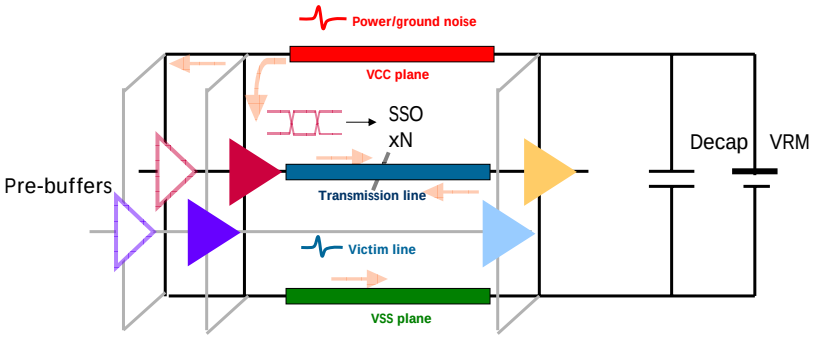
Traditional I/O SSO Analysis

- The SSO/SSN problem:
  - PDN noise
  - Crosstalk



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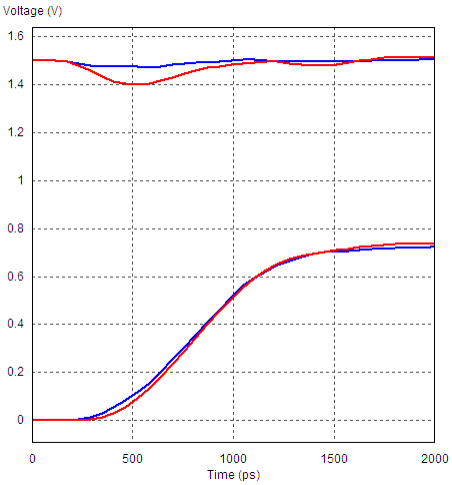
Fundamentals of I/O SSO Mechanisms

- SSO is a combination of signal and power integrity issues
- Affects signal edge rate, timing and voltage margins
- System-level issue involving both packages and PCBs
- Multiple signal net crosstalk mechanisms – trace / via / pin
- Two components of PDS noise
  - PDS current supplied to devices
  - Return currents from I/Os
- BGA inductance presents a fundamental limitation on the PCB's PDS freq. range; the package is responsible for decoupling above that freq. region
- PCB layout can only do so much – it cannot solve package design problems



Blue – Single I/O switching results

Red – Two I/Os switching results

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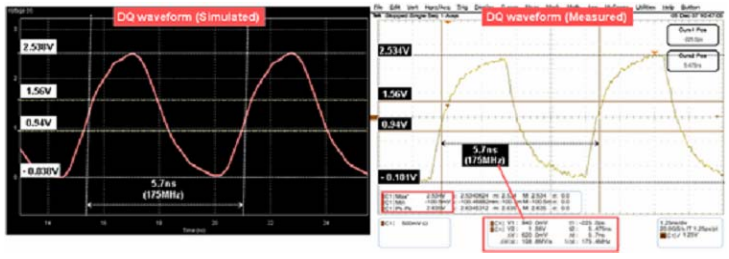
Case：DDR simulation VS measurement



Refer to: "http://www.sigrity.com/papers/2008/65nm%20DDR%20IO%20Paper%20May%202008.pdf "

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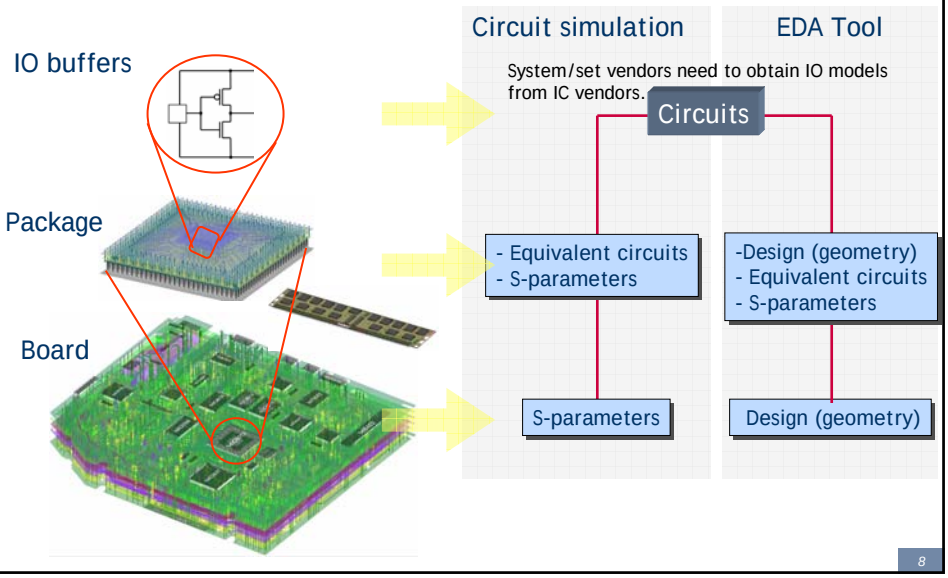
Components for SSO Simulation



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Trade-off in IO buffer model

	SPICE transistor level model	IBIS model
Contents	▪ Detailed circuits and netlists ▪ Device library, parameters ▪ Related deign information	▪ I-V/V-T for the final stage ▪ Pin information
Accuracy	Very good	▪ Good for SI ▪ ? for PI
Format	▪ Usually, encrypted for outside IC vendors. ▪ Usually, NDA is necessary.	▪ Text file ▪ Open format
Simulation time	Typically, several to 10 times slower than IBIS	Much faster than SPICE model
EDA tools Utilization	Specific simulator is necessary for encrypted models	Many SI/PI tools support.

There may be some other choices, such as the current mirror circuit or VCR

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Requirements in SSO Simulation

- Easy setup
  - Hope to eliminate painful manual work
- Fast runtime
  - Want to test various conditions (corners, stimulus, …)
  - Want to promptly reflect package/board design change

→ SPICE transistor model may not fit.
→ What about IBIS model ?

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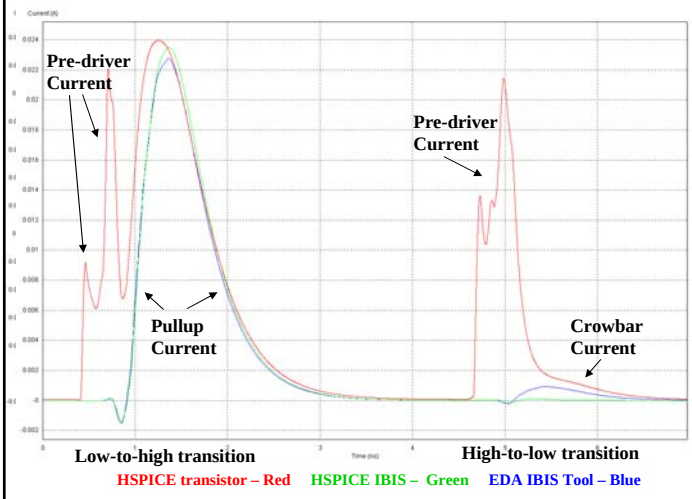
Comparison of IBIS and SPICE total VDDQ current



The total VDDQ current for the transistor-level model is significantly different from its pullup component. There is a large amount of pre-driver current due to crowbar effects and gate capacitance charging.

Pre-driver current occurs significantly earlier than the pullup current. The pre-driver current is rapidly decreasing as the pullup is turning on.

The pre-driver current peaks almost as high as the pullup current. Note that the dI/dt of the pre-driver is much larger than that of the pullup current.

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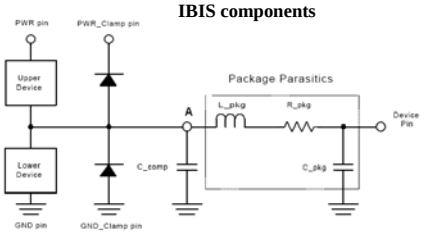
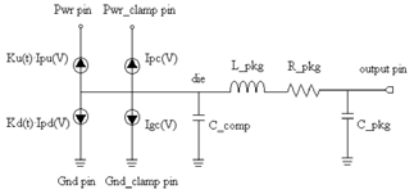
Currents that IBIS can calculate

IBIS components



Analog Model of an IBIS output



- The pullup and pulldown components are modeled as voltage controlled current sources
- The instantaneous value for each voltage controlled current source is derived from the I/V tables and is scaled based on the information in the V(t) tables
- The voltage controlled current sources are simultaneously active to model crowbar
- Crowbar current can be approximated fairly well if all four V(t) tables are present in the IBIS file
- **Pre-driver Current is missing!!!**

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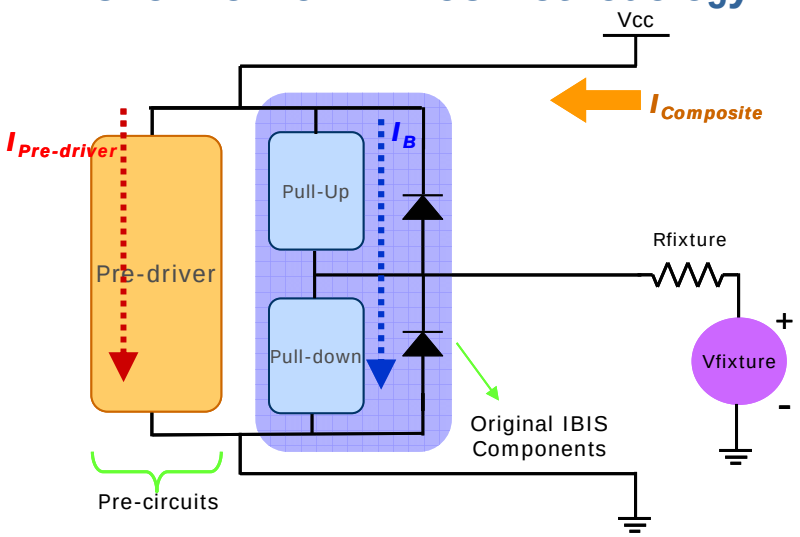
Overview of BIRD95 Methodology



- A new composite current $I_{Composite}$ will be provided to show total P/G currents, based on transistor simulation, for better P/G noise simulation

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Description of Composite Current

- Time table
- Synchronization is needed to [Rising/Falling Waveform]

```
[IBIS ver]        5.0
…
[Composite Current]
|
| Time              I(typ)              I(min)      I(max)
|
0.00000E+00         7.17370E-06         NA          NA
2.00000E-11         7.16590E-06         NA          NA
4.00000E-11         7.15820E-06         NA          NA
6.00000E-11         7.15040E-06         NA          NA
8.00000E-11         7.14270E-06         NA          NA
1.00000E-10         7.13490E-06         NA          NA
…
```

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How Simulator handle IBIS with $I_{Composite}$?

- Obtain composite currents $I_{Composite}$ from IBIS file (version 5.0)
- Obtain I_B from regular IBIS simulation during pre-simulation
- Obtain $I_{Pre\text{-}driver}$, Using
  - $I_{Pre\text{-}driver}(t) = I_{Composite}(t) – I_B(t)$
- Add $I_{Pre\text{-}driver}(t)$ as PWL current source in parallel with IBIS B element model

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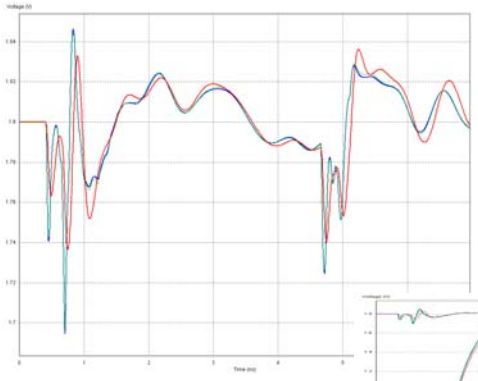
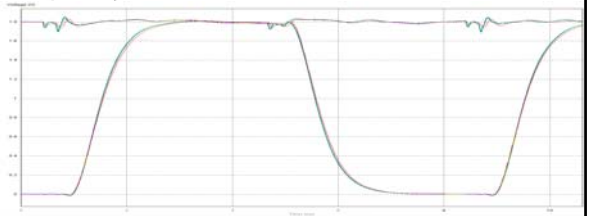
Voltage waveforms for the new methodology



The new IBIS methodology is now able to model the pre-driver and final drive stage currents. Correlation with the SPICE results is significantly improved over the IBIS-only results.

Waveforms from both IBIS simulations were very similar. No artifacts were observed.

Note that the IBIS waveforms overestimate the peak-peak SSO magnitude and occur slightly before the SPICE peaks. The cause can be found by examination of the current waveforms.



SSO waveforms with realistic PDS, 10 pF driver load, PWL I(t) in parallel with the IBIS device

HSPICE transistor – Red HSPICE IBIS – Green EDA IBIS Tool – Blue

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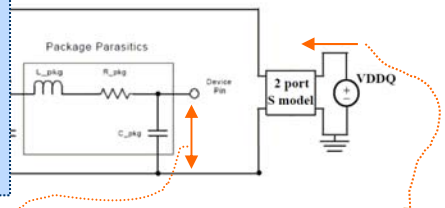
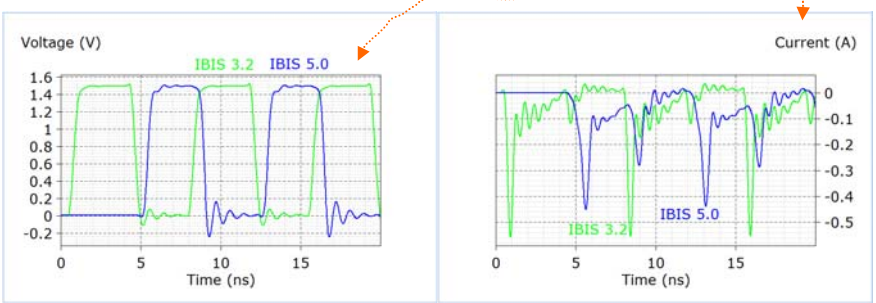
IBIS 5.0 vs IBIS 3.2

IBIS 3.2
→No Composite Current

IBIS 5.0
→ with Composite Current





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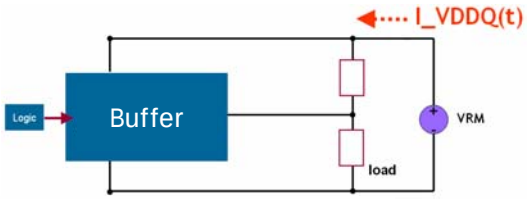
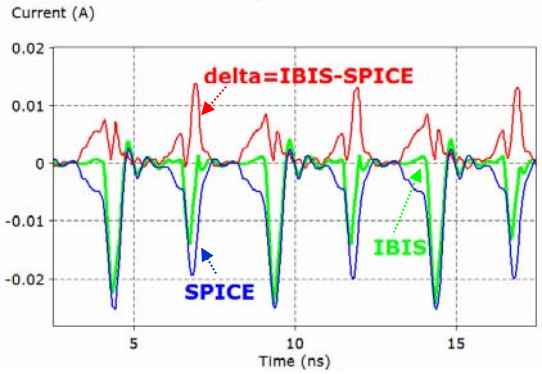
Power Current Difference

Test Circuit
Simulation : HSPICE
Buffer : DDR2-400 DQ
Load : Open





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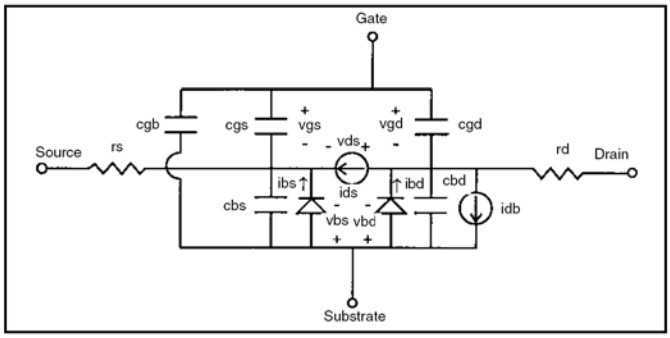
SIGRITY

What is the model missing?



- **Parasitic capacitance exists between all MOSFET terminals**
- **For the I/O pin, this is modeled in IBIS by C_comp**
- **A new compensation capacitor is needed for the power and ground parasitics to maximize SSO correlation with realistic PDS models**

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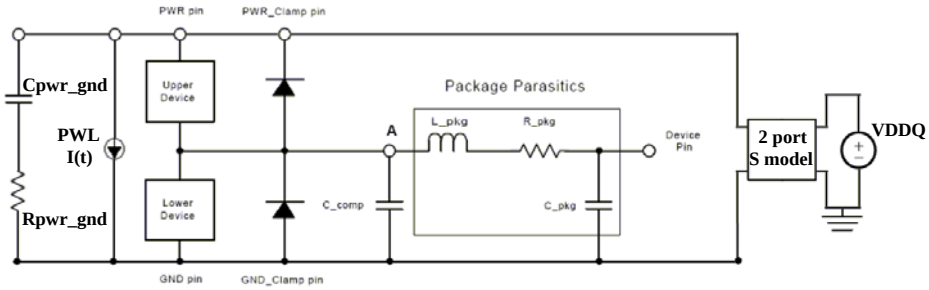
Suggested schematic to maximize correlation



- A frequency domain analysis was performed to determine the impedance between power and ground for the transistor level model
- The impedance was curve fit to a series RC circuit for time domain analysis
- This circuit was added in parallel to the PWL current and IBIS driver

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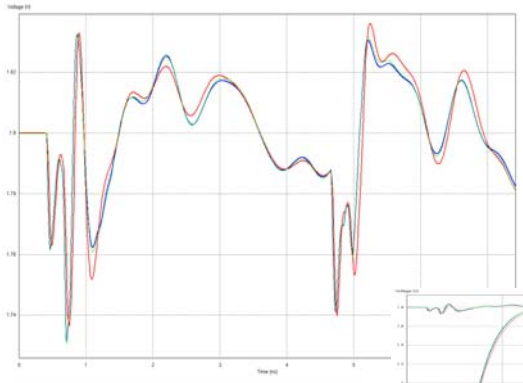
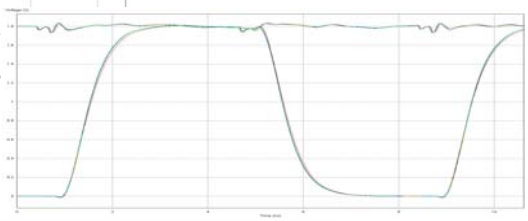
Voltage waveforms for the suggested improvement



The IBIS simulations now show excellent correlation with the SPICE results over the full simulation. With the addition of the RC circuit, the oscillations occur at the proper frequencies and the SSO magnitude is correct.

As before, waveforms from both IBIS simulations were similar and no artifacts were observed.



SSO waveforms with realistic PDS, 10 pF driver load, PWL I(t) and RC circuit in parallel with IBIS device

HSPICE transistor – Red HSPICE IBIS – Green EDA IBIS Tool – Blue

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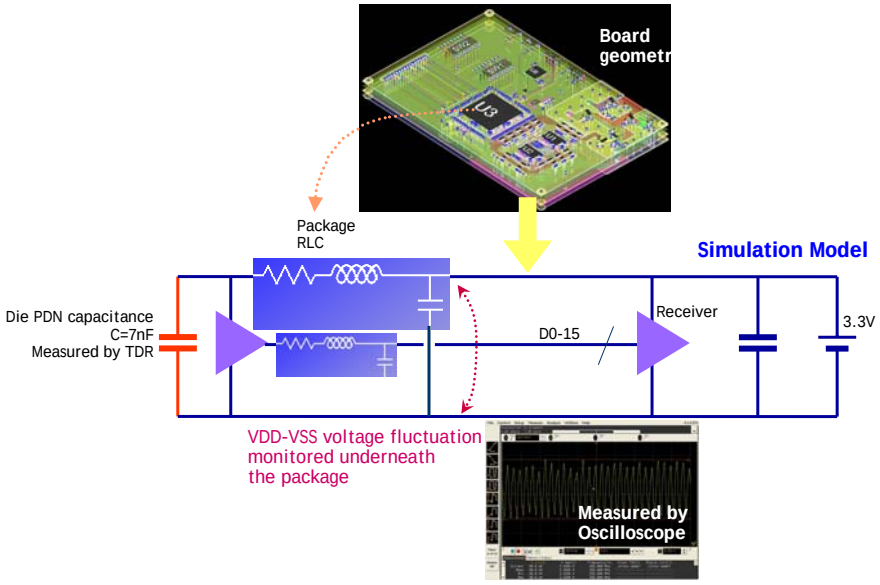
SSO Simulation with IBIS Model



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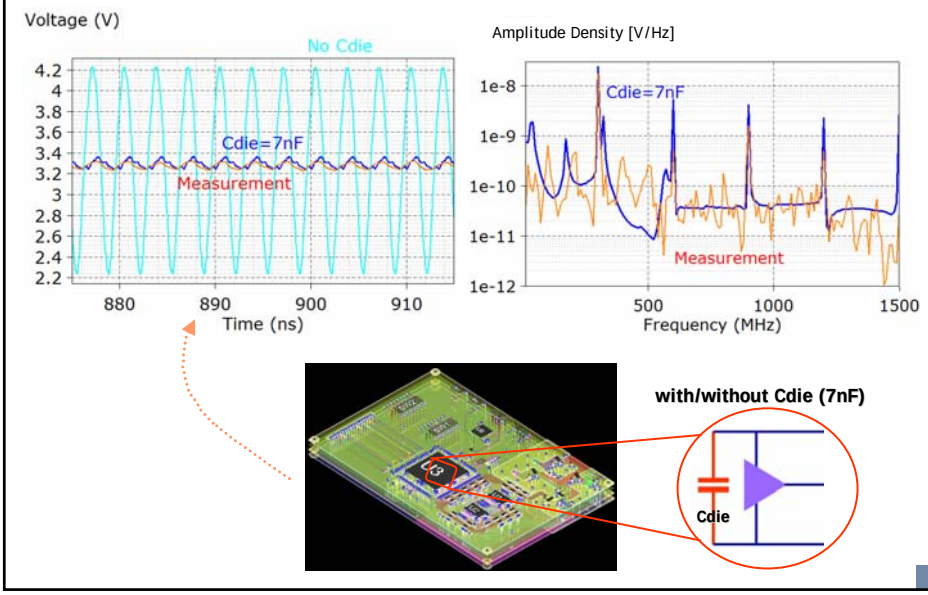
Comparison : w/wo Die PDN Capacitance



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SIGRITY

Contents

- Traditional I/O SSO Analysis
- Buffer Model in SSO Simulation
- BIRD95 Introduction
- Summary

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SIGRITY

Summary

- C_die value show a great impact on accuracy
- IBIS 5.0 improves accuracy in SSO simulation
  - $I_{Composite}$ extractions are relatively easy to generate
  - $I_{Pre\text{-}driver}$ can be calculated by $I_{Composite}$ and I_B
- IBIS model run with high efficiency and easy setup

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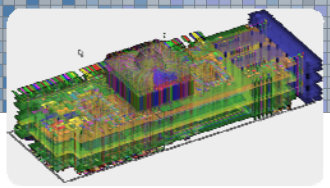
SIGRITY

Thank You!



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PDN design and analysis methodology in SI&PI co-design

www.huawei.com

Asian IBIS Summit, November 9, 2010, Shenzhen China

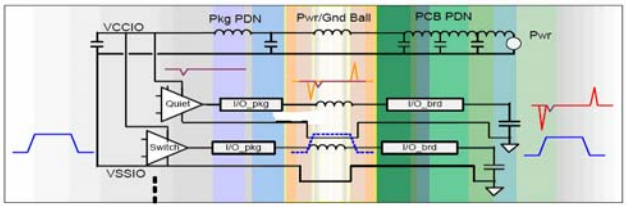
Luo Zipeng (luozipeng@huawei.com)
Liu Shuyao (liushuyao@huawei.com)

HUAWEI TECHNOLOGIES CO., LTD.

Agenda

- SI&PI co-design challenge
- Key parameters in PDN design
- Modeling the loop inductance of high frequency capacitor
- High frequency capacitor' global decouple effect
- Tight coupling Power-Gnd pair in board' PDN
- SSN analysis of PDN' SI&PI co-design via PDN' IBIS model

SI&PI co-design challenge

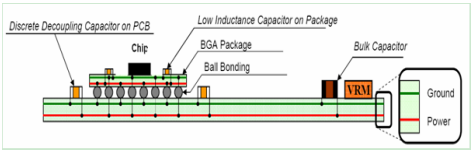


◆As signal IO voltage level decreasing and signal speed constantly increasing, the effect of SSN become serious,.

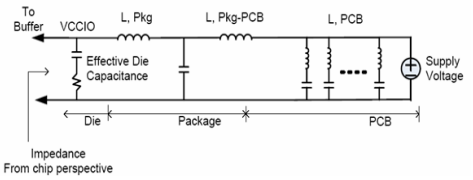
◆SSN noise directly affect noise margin of low voltage level and time margin of high speed signal.

◆Traditional independent SI and PI analysis bring the limitation.

Key parameters in PDN design



Board' PDN sketch map



Equivalent circuit of board' PDN

PDN of Board:

◆VRM

◆Bulk capacitor

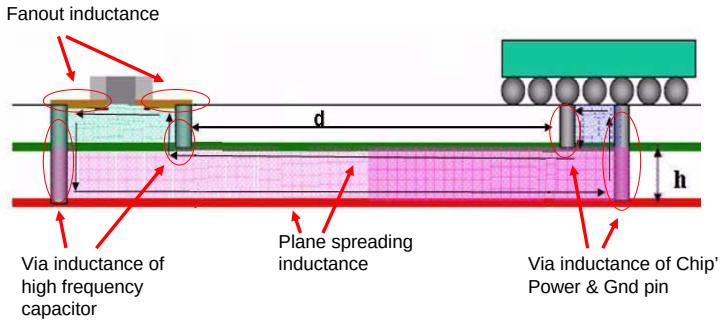
◆High frequency capacitor

◆Power-Gnd plane capacitor

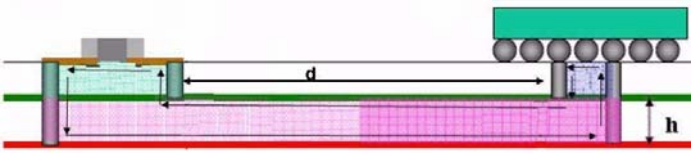
◆Chip' PDN

High frequency capacitor and Power-Gnd plane play an important role in PDN design;

Loop inductance of high frequency capacitor

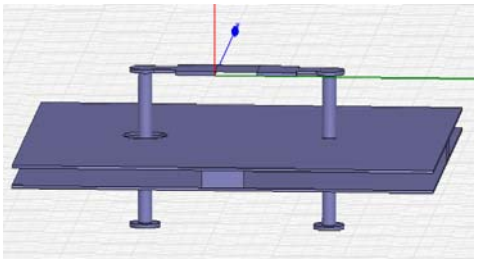


Via inductance effect in Loop inductance



- ◆Capacitor' ESL: 0.4~0.65nH;
- ◆Special fanout inductance: 0.25~0.3nH;
- ◆Plane spreading inductance: hundreds of pH;
- ◆Via inductance of Capacitor: 1nH~2.5nH,when in different stackup, The Value will be varied

Modeling the via inductance

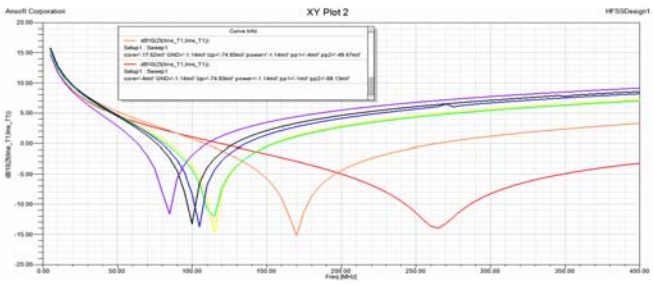


measurement	Simulation	precision
2.29nH	2.25nH	98%

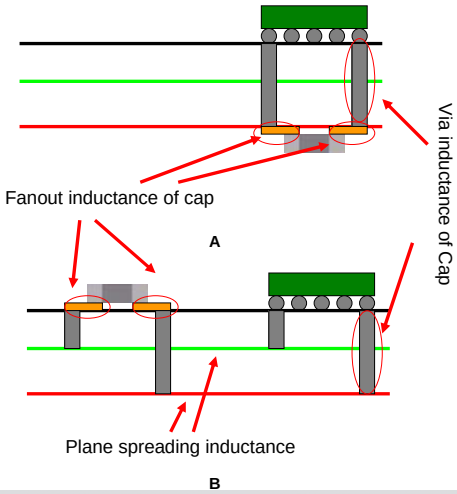
◆Via inductance is about 75%~80% of the total loop inductance;
◆As the the Power-Gnd pair space and location changed, the via inductance of capacitor may varies;
◆Optimizing the design of Power-Gnd pair will decrease the via inductance, increase the decouple effect of high frequency capacitor;
◆Evaluate the value of via inductance by simulation, comparison between simulation and measurement validate the precision of via inductance model.

Comparison of capacitor decouple effect with different via inductance

Power-Gnd plane space	Power-Gnd plane location	Via inductance of Caps	Corresponding line
S≤10mil	Above of the Stackup	0.3nH<L<0.55nH	Red line
10mil<S<30mil	Above of the Stackup	0.55nH<L<1.5nH	Orange line
S≤10mil	Center of the Stackup	L≈2.5nH	Green line
10mil<S<30mil	Center of the Stackup	2nH<L<2.5nH	Yellow line
30mil<S<65mil	Center of the Stackup	2.3nH<L<3nH	Blue line
10mil<S<30mil	Underside of the stackup	3nH≤L	Black line
S≤10mil	Underside of the stackup	3.2nH<L	Purple line

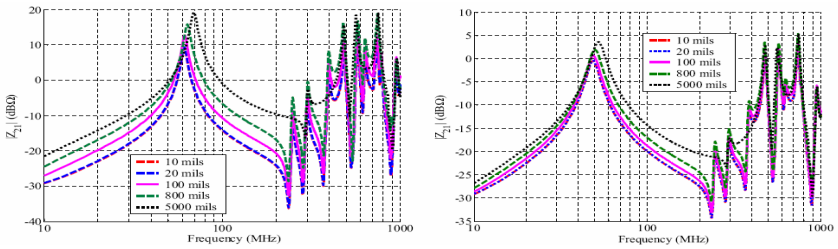


Plane spreading inductance affect high frequency cap decouple



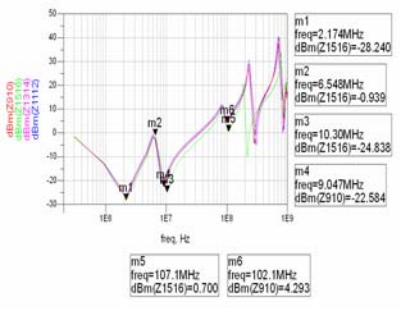
◆Designing the PDN of PCB, in order to decrease loop inductance of capacitor, high frequency decoupling capacitor will be located as close as possible to chips' power pin;
◆High frequency decaps usually locate under the chip, close to the power pin;
◆In actual design, Both chips and decaps need to be located on top side of PCB, for the limitation of chip's dimension, decaps only can be near to the chips, not close to power pin,
◆as seen as left fig B, plane spreading inductance increase while both chip and decap be located on top side of PCB;
◆ Compared with fig A, the total loop inductance in fig B will increase, and High frequency capacitor' decouple effect obviously decrease;

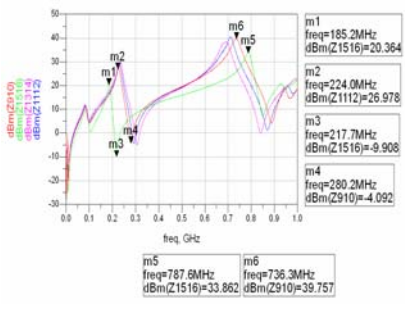
Global decouple effect of high frequency cap



◆ As decreasing the space between the Power Ground plane, the total loop inductance also decrease, and high frequency caps will show an global decouple effect.

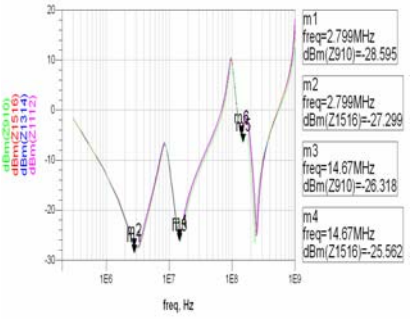
Power-Gnd pair space more than 30mils,high frequency capacitor show an local effect

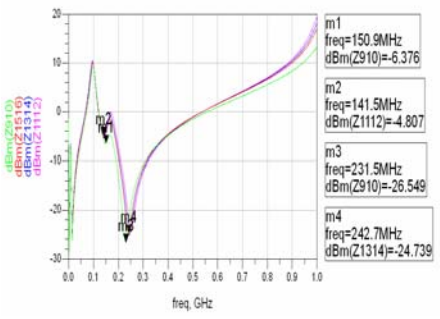




◆Power-Gnd pair space more than 30mils, distance between chip and capacitor varying from 500mils to 1000mils, the resonance frequency and anti-resonance frequency of high frequency capacitor will change.

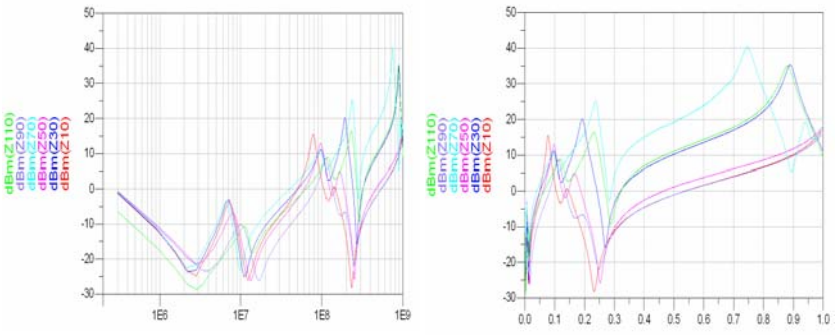
Power-Gnd pair space less than 10mils,high frequency capacitor show an global effect





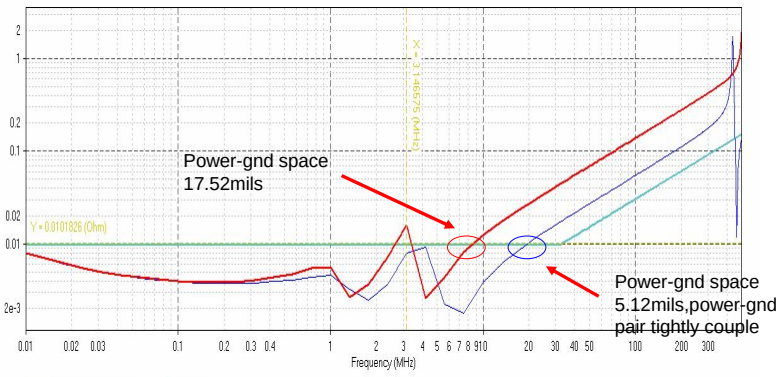
◆Power-Gnd pair space less than 10mils, distance between chip and capacitor varying from 500mils to 1000mils, the resonance frequency and anti-resonance frequency of high frequency capacitor almost keep same.

Power-Gnd pair space effect analysis of PDN design

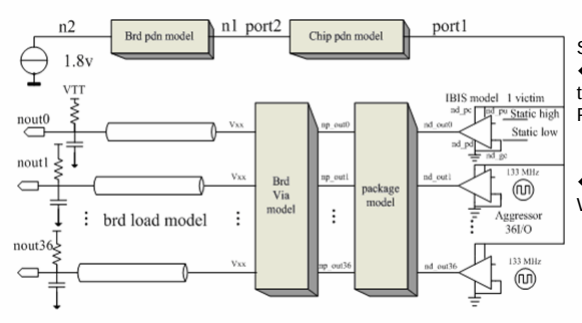


◆Distance between chip and capacitor keep constant, power-gnd pair space varying from 5.12mils to 56.2mils, the resonance frequency and anti-resonance frequency of high frequency capacitor change.

Tight coupling Power-Gnd pair in PDN



SSN Mechanism and SI/PI Co-Design Challenges



SSN Mechanisms:

◆Delta-I Noise and IR Drop from the System PDN (Including Die、Pkg and PCB)

$$V = L\frac{dI}{dT} + IR$$

◆Inductive Coupling from the Whole signal link

$$\Delta v' = \sum M_{iq}\, di/dt$$

SSN Influence :

◆Decrease the noise margin and timing margin

◆Increase Power noise and EMI problem

SSN Simulation challenges :

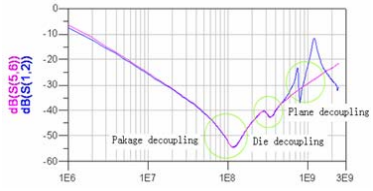
◆Multi signal and PDN co-design

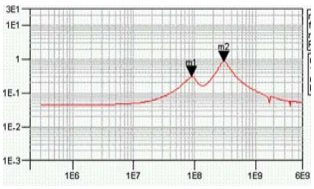
◆Whole PDN and Couping models

◆Source active models

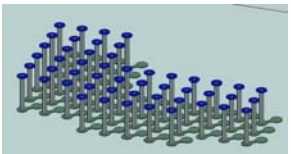
PDN Modeling and ibis active

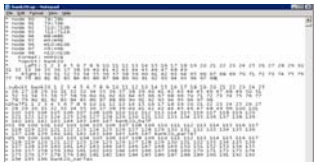
◆PDN Modeling：Die+Pkg PDN Model and System PDN Model



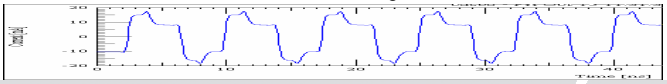


◆Coupling Modeling：Pkg Coupling Model and Via Coupling Model



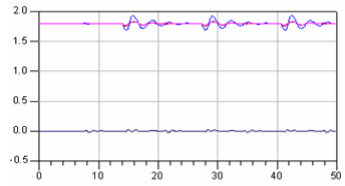


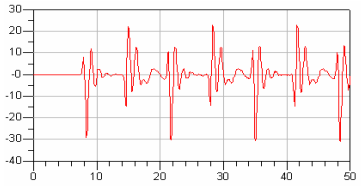
◆IBIS for the active model：IBIS buffer has some advantage and limitation for SSN simulation



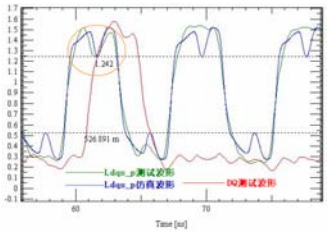
SSN Simulation using ibis models

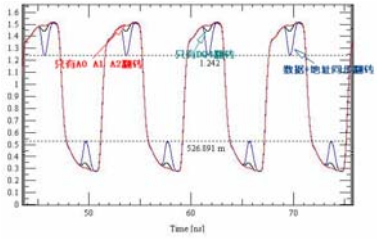
◆Delta-I Noise and Multi Crosstalk





◆SI+PI Co-simulation using ibis models





Conclusion

PDN directly determine the board' power delivery system design quality, and in board' PDN high frequency capacitor and Power-Gnd plane play an important role;

◆The loop inductance of high frequency capacitor decrease as smaller as possible in a well designed PDN ,and capacitor show an global decouple effect;

◆The tight coupling PDN adequately consider power-gnd plane capacitor, expanding the efficiency frequency band;

SSN analysis via PDN' IBIS model enhance simulation efficiency and speed. Implementing SI&PI co-design.

Thank you

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Correlating C_pin Capacitance with Measurements

Asian IBIS Summit
Shenzhen, China
November 9, 2010

Randy Wolff
Micron Technology
rrwolff@micron.com

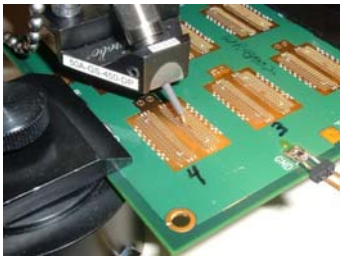
C_pin

- Package capacitance for a specific signal [Pin]
- Typically from diagonal elements of the capacitance matrix – extracted from 3D field solvers

```
|*****************************************************************************
| COMPONENT: MT41J256M8DA (78-Ball FBGA, x8, 8mm X 10.5mm)
|*****************************************************************************
|
[Component]     MT41J256M8DA
[Package Model] v89b_78ball_pkg
[Manufacturer]  Micron Technology,Inc.
[Package]
|               typ          min          max
R_pkg           257.47m      178.77m      383.81m
L_pkg           1.43nH       0.98nH       2.38nH
C_pkg           0.36pF       0.29pF       0.49pF
|
[Pin]           signal_name  model_name   R_pin        L_pin        C_pin
A1              VSS          GND
A2              VDD          POWER
A3              NC           NC
A7              NF_TDQS#     NF_TDQS      267.15m      1.36nH       0.41pF
A8              VSS          GND
A9              VDD          POWER
B1              VSS          GND
B2              VSSQ         GND
B3              DQ0          DQ           247.18m      1.08nH       0.39pF
B7              DM_TDQS      DM_TDQS      242.95m      1.47nH       0.37pF
```

Measured Capacitance

- Diagonal of matrix is total capacitance seen by each line with all other lines grounded
  - Fully-loaded capacitance is useful for single line simulations
- Measured capacitance is less than fully-loaded capacitance
  - Signal is referenced to power and ground (pwr/gnd decoupled)
  - All other signal lines are floating

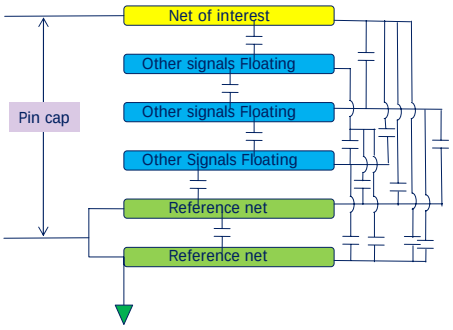


Why is this important?

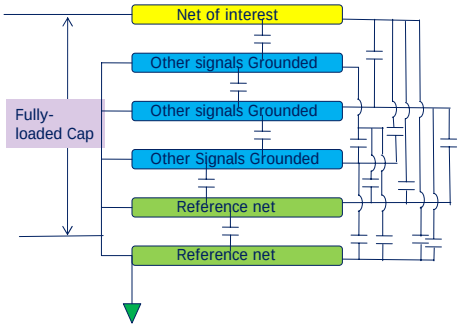
- C_comp calculation and Model correlation
  - C_comp = C_signal(measured) – C_pin(measured)
  - C_pin ≠ C_pin(measured)
- Datasheet comparisons
  - $C_{specification}$ is based on measured values, not total capacitance
  - Estimating measured values from package simulation data aids in optimizing package designs to meet capacitance specifications

Capacitance Parameters	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
CK and CK#	C_{CK}	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	0.8	1.3	pF
ΔC: CK to CK#	C_{DCK}	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	pF
Single-end I/O: DQ, DM	C_{IO}	1.5	3.0	1.5	3.0	1.5	2.5	1.5	2.3	1.4	2.2	pF
Differential I/O: DQS, DQS#, TDQS, TDQS#	C_{IO}	1.5	3.0	1.5	3.0	1.5	2.5	1.5	2.3	1.4	2.2	pF
ΔC: DQS to DQS#, TDQS, TDQS#	C_{DDQS}	0	0.2	0	0.2	0	0.15	0	0.15	0	0.15	pF
ΔC: DQ to DQS	C_{DIO}	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF

C_pin (measured) vs. Fully-loaded Cap

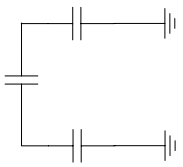


Measured Pin Cap Setup
(Extracted pin cap after matrix post-processing)



Fully-loaded Cap
(Diagonals of Maxwell's Matrix)

Calculating C_pin(measured)



- The matrix form of the capacitance equation is [Q] = [C] * [V]
- For a 2x2 system, the C matrix is :

  | Ct1 -C12 |

  | -C12 Ct2 |

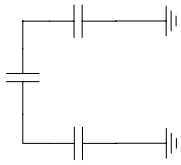
- Ct1 = C1 + C12 and Ct2 = C2 + C12

Calculating C_pin(measured)

- Deposit a charge of Q on Node 1

  | Ct1 -C12 | * | V1 | = | Q |

  | -C12 Ct2 | * | V2 | = | 0 |



- Ct1 * V1 – C12 * V2 = Q
- -C12 * V1 + Ct2 * V2 = 0, V2 = C12/Ct2 * V1
- (Ct1 - C12^2/Ct2) * V1 = Q
- Cnode1 = Q/V1 = (Ct1 - C12^2/Ct2)
- In matrix form, let Q = 1 coulomb

  | V1 | = Inv (| Ct1 -C12 |) * | 1 |

  | V2 | = Inv (| -C12 Ct2 |) * | 0 |

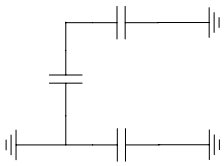
- This yields V1 and V2 and Cnode1 = 1/V1, since Q = 1

Calculating C_pin(measured)

- Let Node 2 be grounded - this forces V2 = 0 and allows a net negative charge on Node 2

  | Ct1 -C12 | * | V1 | = | 1 |

  | -C12 Ct2 | * | 0 | = | Q |



- 1: Ct1 * V1 – C12 * 0 = 1 , V1 = 1/Ct1
- 2: -C12 * V1 + Ct2 * 0 = Q, Q = - C12/Ct1
- The only value of interest is V1, only equation 1 is needed. This is the same as eliminating the 2nd row of the [C] matrix.
- V2 = 0, so all of the terms in the 2nd column will multiply to 0. This eliminates the 2nd column of [C].
- The matrix equation reduces to | Ct1 | * | V1 | = | 1 |

Calculating C_pin(measured)

- Generalized: Let [C] be an n+m x n+m matrix representing n floating nodes and m nodes clamped to power or ground.
- Step 1 – eliminate the rows and columns associated with clamped nodes.
  - [C] -> [C'], where [C'] is an n x n matrix.
  - |C'| = |Reduction Matrix2| * |C| * |Reduction Matrix1|
  - If net i is clamped then row i of Reduction Matrix1 is all 0s
  - If net i is floating then row i of Reduction Matrix1 is all 0s with a 1 in column x
    x = i - # of clamped nets between net 1 and net i
  - If net i is clamped then column i of Reduction Matrix2 is all 0s
  - If net i is floating then column i of Reduction Matrix2 is all 0s with a 1 in row x
    x = i - # of clamped nets between net 1 and net i

Calculating C_pin(measured)

- Step 2 – Generate Q matrix – n x n identity matrix
  - Represents a 1 coulomb charge deposited on each floating node, one at a time.
- Step 3 – solve for [V] matrix
  - [V] = inv([C']) * [Q], where [Q] is identity matrix
- Step 4 – Calculate floating node capacitances
  - Cnode(x) = 1/Vxx, where Vxx are the diagonal elements of [V]
- Overall effect is mutual capacitances are reduced due to shorting of the mutual terms to power and ground nets

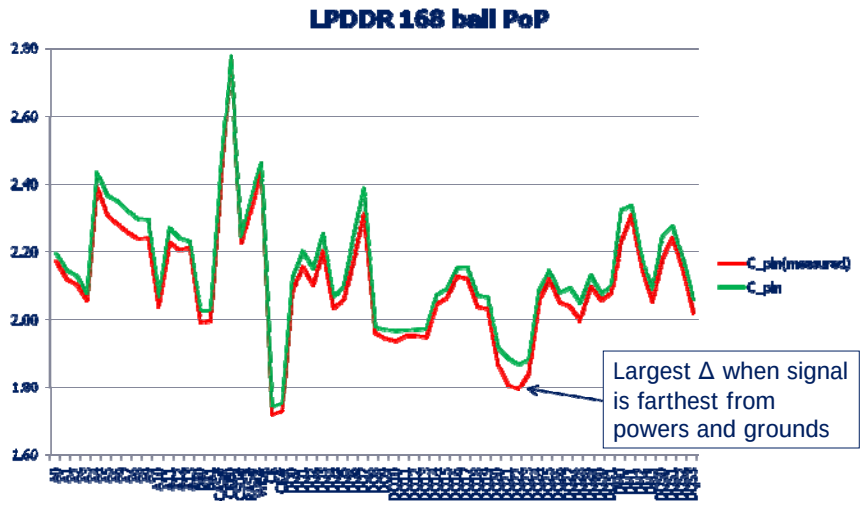
Micron's Capacitance Analyzer Tool

- Excel spreadsheet macro
- Reads in matrix data from several Field Solver tools
- Solves for 'measured' capacitance
- Nets are defined as either 'floating' or 'grounded'

Line number	Line Name	Signal_State
1	A0	Floating
2	A1	Floating
3	A2	Floating
59	VDD	Grounded
60	VDDQ	Grounded
61	VSS	Grounded
62	VSSQ	Grounded
63	WE#	Floating

Signal Names	Pin Capacitance	Maxwell Diagonal Capacitance
A0	9.48269E-13	1.22479E-12
A1	1.05993E-12	1.29176E-12
A2	1.06298E-12	1.20089E-12
A3	9.97877E-13	1.0904E-12
A4	7.88691E-13	8.36509E-13
A5	8.79004E-13	1.09757E-12

C_pin versus C_pin(measured)



Conclusions

- Capacitance matrix data must be manipulated when comparing it to measured capacitance
  - Maxwell capacitance is not what is typically measured
  - Important for datasheet comparisons and model to simulation correlation

Acknowledgements

- Thanks to Bruce Schober at Micron for development of the analyzer tool and figuring out the matrix math.


Micron

Automated AMI Model Generation & Validation

José Luis Pino
Amolak Badesha

Manuel Luschas
Antonis Orphanou
Halil Civit

Agilent EEsof EDA

NETLOGIC MICROSYSTEMS

Asian IBIS Summit, Shenzhen China November 9, 2010
(Presented previously at the IBIS Summit on June 15, 2010)

Agenda

- AMI Model Generation Barriers
- Automated AMI Model-generation flow
  - Example-1: 6.25 Gb/s
  - Example-2: 10.3125 Gb/s
- TX Model Correlation Study
  - -with Transistor Simulations
  - -with Measurements
- Benefits of Automated AMI flow

#1 AMI modeling barrier

Model Generation Time

AMI Modeling suppose to Speed-up System Design Cycle,
BUT, Model-generation takes Significant Time & Resources

….System Vendors have to wait a LONG time before accurate AMI models become available

Note: Vendors with NO experience in AMI modeling are spending 6-12+ months to come up with first-generation models

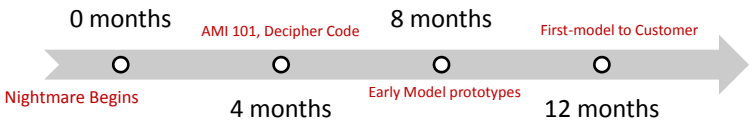
Models come very late in Design Cycle → used only for Validation, NOT Design

Why AMI-model generation takes so long?

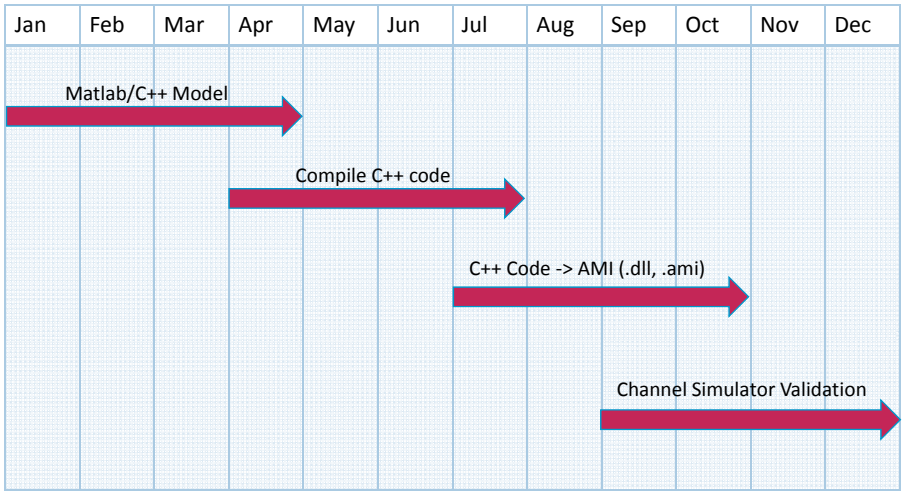
Typical Signal Integrity Engineers are NOT programmers

….they are having "Nightmares" in trying to develop AMI models

- Cryptic Matlab/C++ code passed from System-Architectures → AMI Modeler (if lucky)
- Challenge to Convert Algorithm design Code → AMI format



Typical AMI model generation flow…



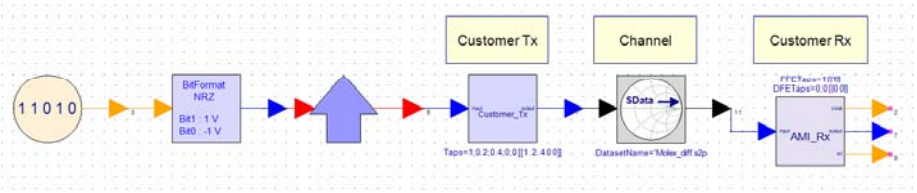
Automated AMI model generation flow…

ESL flow for Automated AMI Modeling

Electronic System Level (**ESL**) design and verification is an emerging electronic design methodology that focuses on the *higher abstraction* level concerns first and foremost.

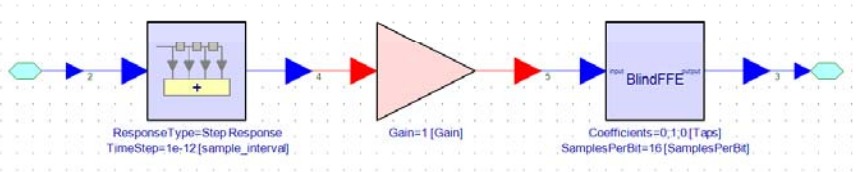
ESL flow facilitates utilization of appropriate abstractions in order to *increase comprehension about a system*, and to enhance the probability of a successful implementation of functionality in a *cost-effective* manner

Here is an Example of SerDes modeling using ESL flow-



ESL flow: TX Modeling Example (1)

Step-1: Starting Architecture Design with Generic Model



FIR/IIR filter

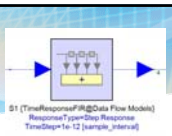
Gain

n-tap FFE

Different blocks represent high-level TX architecture

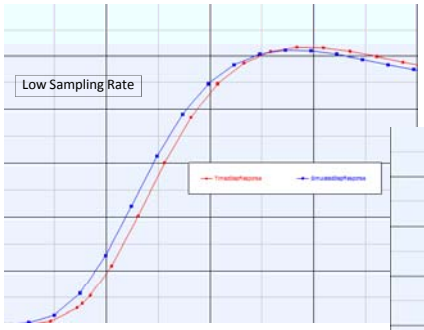
More on FIR Filter…

How to bring in Spice or Measured data?

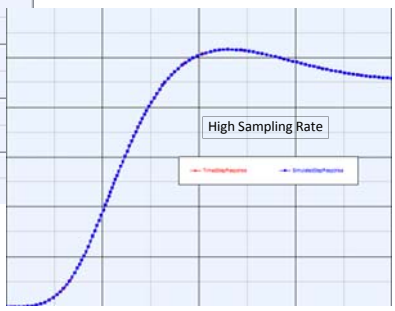


Challenges:

1. Typical Simulation and Measured Data is not equally time-stepped



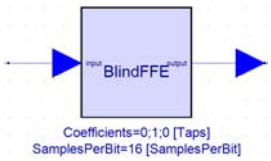
Sampling Rate determines Simulation Accuracy



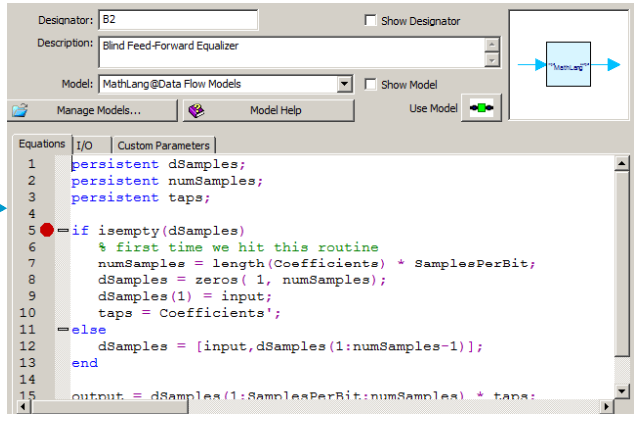
FIR model should support "Arbitrary" Sampling Rate

ESL flow: TX Modeling Example (2)

Step-2: Customize IP -> Bring in Math Lang or C++ Code

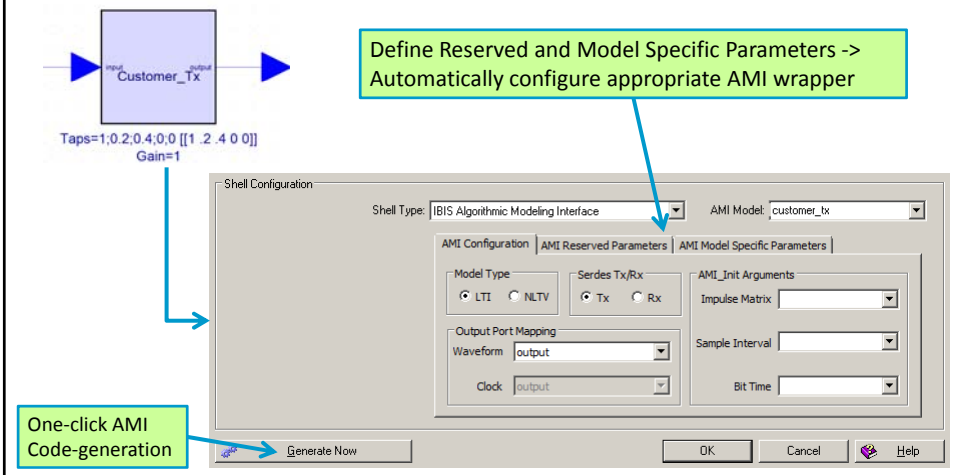


Fine-tune and Customize models with Math Lang and/or C++ code



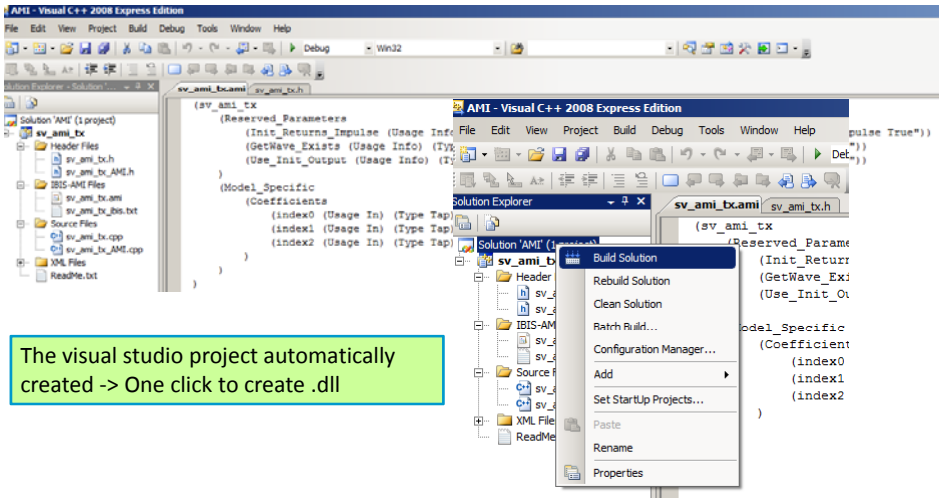
ESL flow: TX Modeling Example (3)

Step-3: One-click AMI Code-Generation

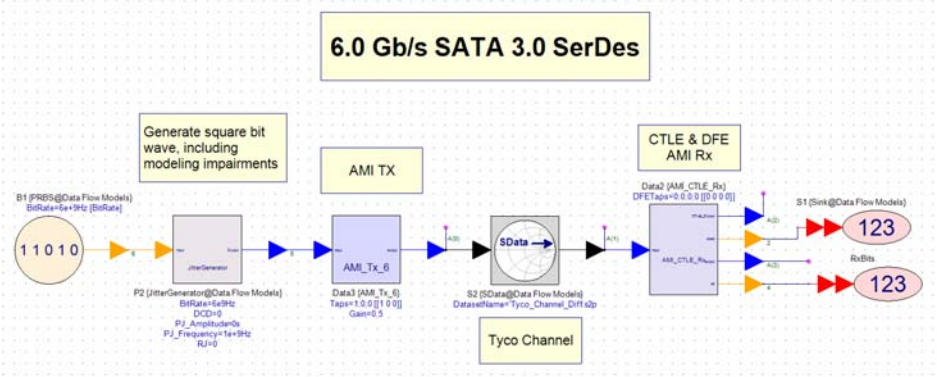


ESL flow: TX Modeling Example (4)

Step-4: Automatically Generated .ami and Visual-Studio project

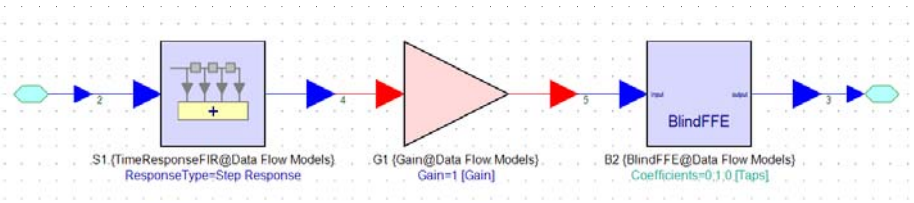


Example #1
6.0 Gb/s (SATA 3.0)



TX Modeling
6.0 Gb/s (SATA 3.0)

TX Architecture

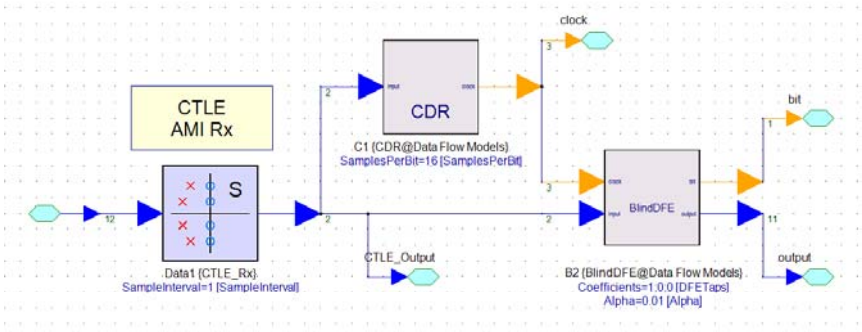


FIR filter

3-tap FFE

RX Modeling
6.0 Gb/s (SATA 3.0)

RX Architecture

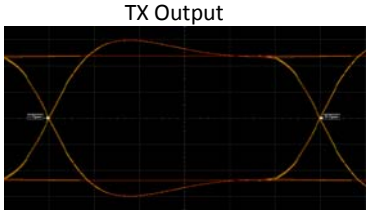


S-domain filter

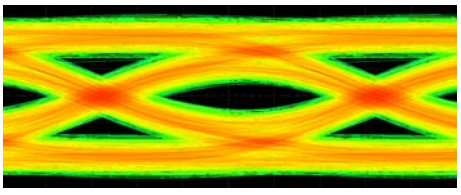
3-tap DFE

Results
6.0 Gb/s (SATA 3.0)

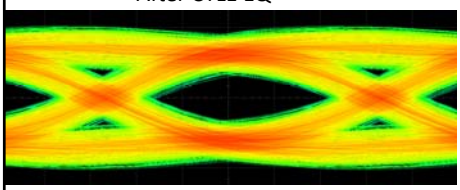
TX Output



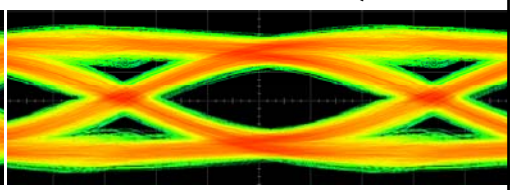
After Channel



After CTLE EQ

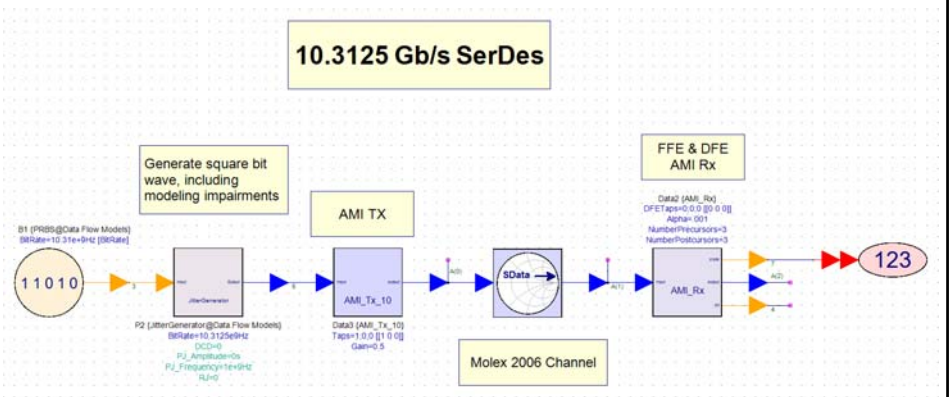


After CTLE+DFE EQ

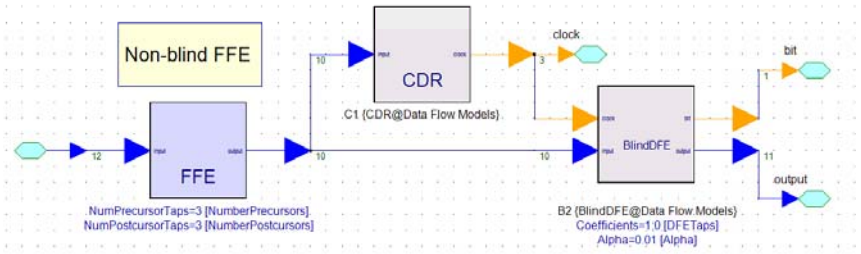


*Note: EQ taps not optimized for maximum eye

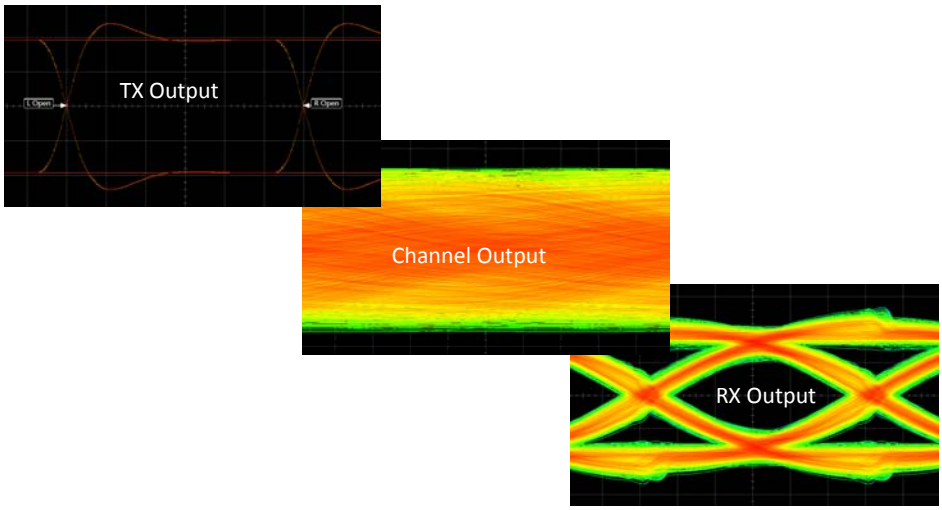
Example #2
10.3125 Gb/s (10-GB Ethernet)



RX Modeling
10.3125 Gb/s (10-GB Ethernet)



Example #2
10.3125 Gb/s (10-GB Ethernet)



TX 10.3125 Gb/s
AMI model correlation study

Strategy

1. Correlate Transistor Simulation vs. AMI model
2. Correlate Measured vs. AMI model

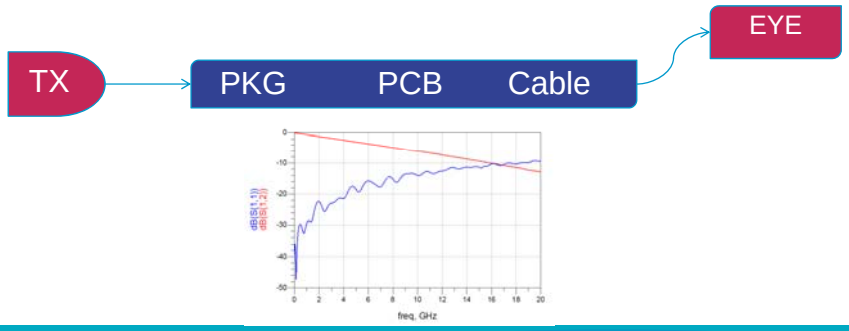
Transistor Simulation vs. AMI Model

Steps-

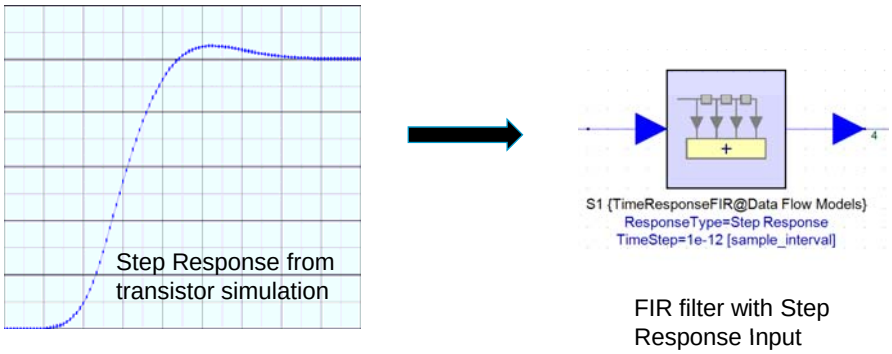
1.Generate Step Response from transistor simulation

2.Generate AMI model using EDA tool

3.Compare

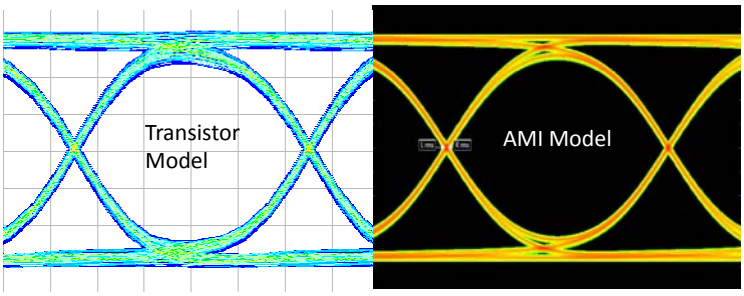


Step Response Model



FIR filter with Step Response Input

Correlation
transistor model vs. AMI model



Excellent match between transistor simulation and AMI model

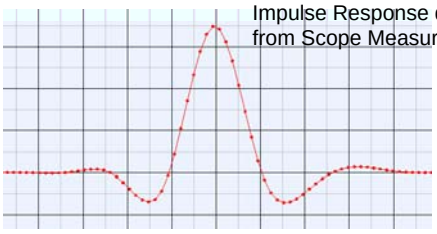
Good faith in model-generation methodology!

Measurement vs. AMI Model

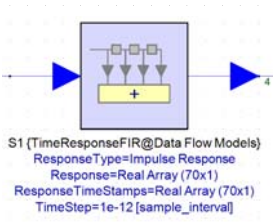
Steps-

1. Measure waveform
2. De-embed Channel
3. Output Impulse response

Impulse Response Model

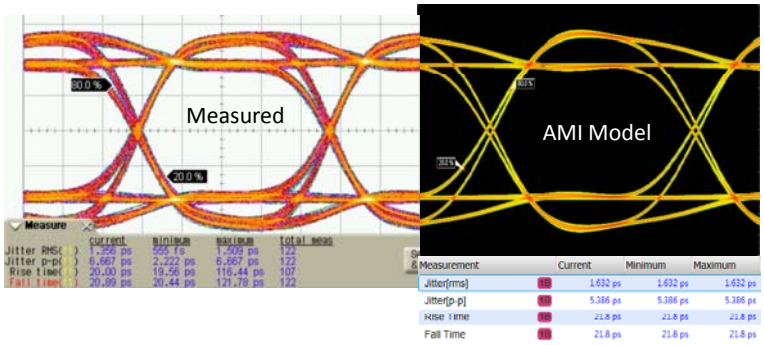


Impulse Response derived from Scope Measurement



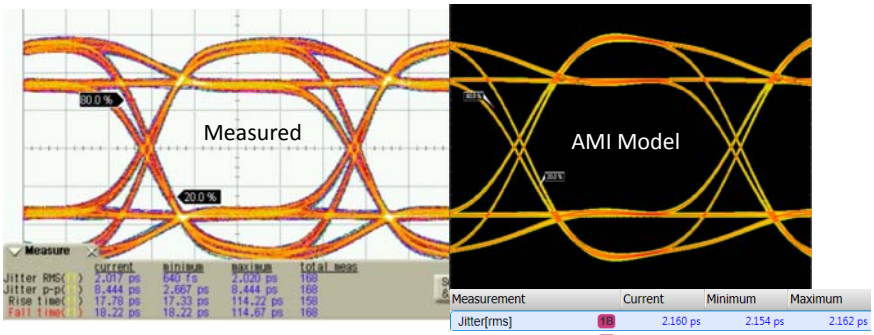
FIR filter with Impulse Response Input

TX Correlation Measured
emphasis #1: tap 0, 1, -0.2



TX Correlation Measured

emphasis #2: tap 0, 1, -0.25



Measurement	Current	Minimum	Maximum
Jitter[rms]	2.160 ps	2.154 ps	2.162 ps
Jitter[p-p]	6.464 ps	6.248 ps	6.464 ps
Rise Time	20.4 ps	20.4 ps	20.4 ps
Fall Time	20.4 ps	20.4 ps	20.4 ps

Benefits of ESL Design Flow

Automated AMI-Model Generation

1. Complete "Automation" of Code-generation and Model Compilation
   a task that routinely takes months because of its complexity
2. Basic building blocks that can used to start model development
   FIR/IIR filters, FFE, DFE, CDR etc.
3. Easily customize models to include custom IP
   Custom C++ and Math-Lang

Spice Subcircuit Support for Serial Link Channel Design Using IBIS [External Model]

www.huawei.com

Asian IBIS Summit, November 9, 2010

Xiaoqing Dong, Huawei Technologies

Zhangmin Zhong, Sigrity

Ken Willis, Sigrity

HUAWEI TECHNOLOGIES CO., LTD.

HUAWEI

SIGRITY

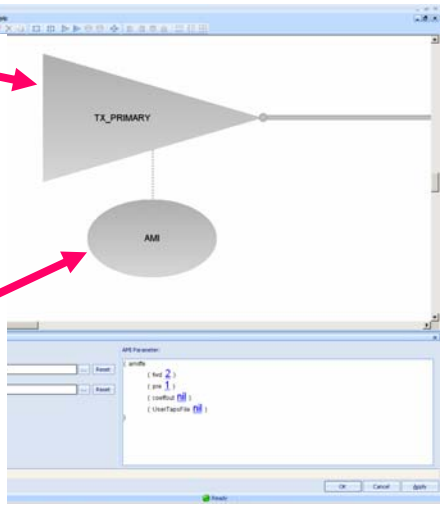
Agenda

- Review existing solutions for serial link IBIS models in channel design
- The advantages of using Spice-based IO models for serial links
- Support Spice-based models using IBIS [External Model] keyword

SIGRITY

IBIS-AMI Model Sub-Components

- Circuit part
  - IO buffer stage
  - Voltage swing
  - Parasitics
  - Spice or traditional IBIS format
- Algorithmic part
  - On-chip
  - Equalization functionality
  - DLL + AMI file



This presentation focuses on the "circuit" part

SIGRITY

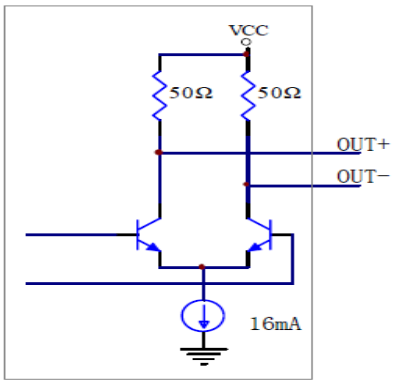
Existing Solutions for Serial Link IBIS Circuit Models

- Most of the models use Spice-based subcircuits
  - No standards for the description of the subcircuits
  - May need much manual work to edit the netlist for specific EDA tools
- Specified (not standard) keywords in IBIS models
  - Specifications are provided by specified EDA tool
  - Don't need manual work to edit the netlist, but only appropriate for specified EDA tool

SIGRITY

Spice-Based IO Circuit Model

- Can easily represent the actual IO structure (ex. pullup resistor with pulldown current source for CML)



SIGRITY

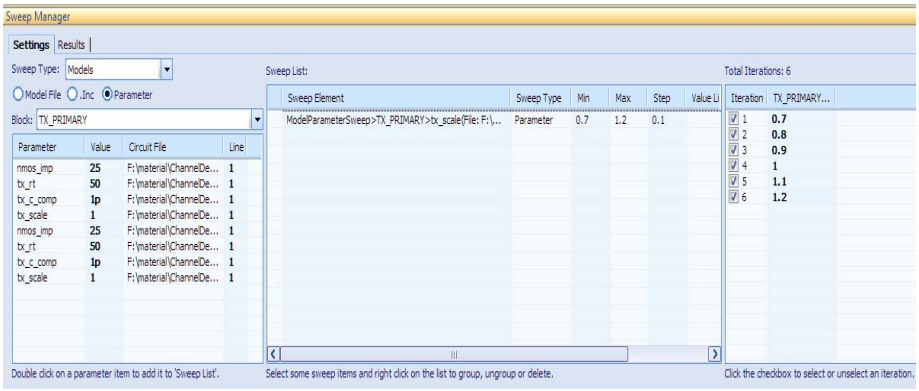
Spice-Based IO Circuit Model (Cont.)

- Incorporate hookups for non-ideal power connections
  - External power supply can be linked with the power node of the Spice subcircuit and used for non-ideal power analysis
- Incorporate on-chip parasitics easily, including PDS, S-params for RDL routing, etc.

SIGRITY

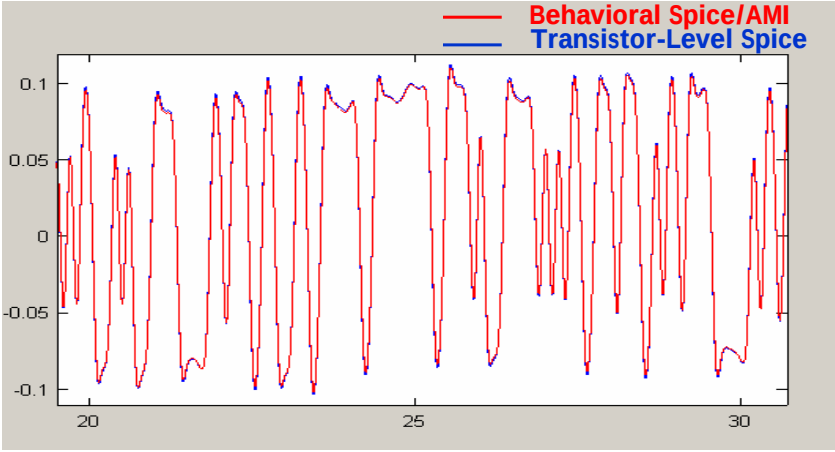
Spice-Based IO Circuit Model (Cont.)

- Usage of parameterized subcircuits, where these parameters can be swept in EDA tools



SIGRITY

Behavioral Spice/AMI vs. Transistor-Level Spice at 10 Gbps, EQ on (from telecomm chip company)



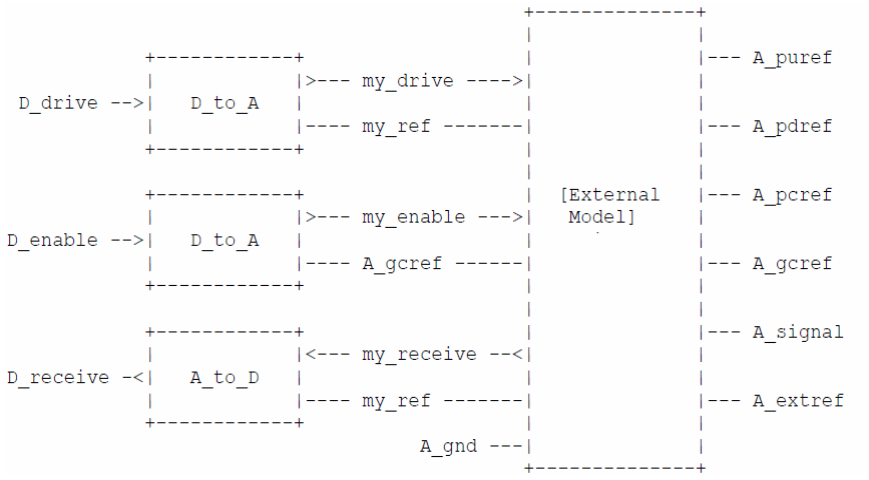
SIGRITY

IBIS [External Model]

- Used to reference an external file written in one of the supported languages containing an arbitrary circuit definition
- Can be used to support the Spice-based IO models
  - Standard IBIS keyword
  - Don't need manual work to edit the netlist
  - Suitable for all EDA tools if the tool can support standard IBIS [External Model] keyword

SIGRITY

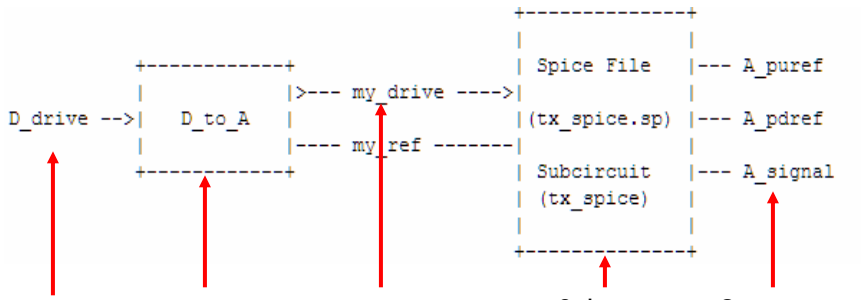
Ports Under [External Model]



Refer to IBIS Specification

SIGRITY

Example of an [External Model] Output Buffer Using Spice



Digital stimulus

Defines voltage levels, input ramp rise and fall times

Voltage stimulus for Spice subcircuit

Spice-based model

Output port, pull up and pull down reference ports

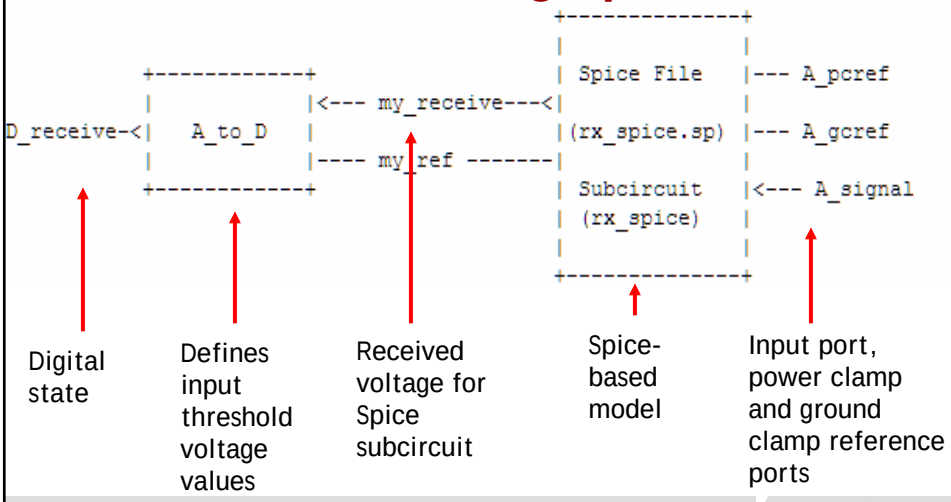
SIGRITY

[External Model] Description for Output

```
[External Model]
Language Spice
| Corner  corner_name  file_name     circuit_name (.subckt name)
Corner       Typ          tx_Spice.sp          tx_Spice
|
| Ports List of port names (in same order as in Spice)
Ports    A_puref    A_pdref   A_signal   my_drive
|
| D_to_A   d_port      port1         port2      vlow   vhigh   trise   tfall      corner_name
D_to_A    D_drive   my_drive   A_pdref     0.0     1.0    0.020n 0.020n     Typ
|
[End External Model]
```

SIGRITY

Example of an [External Model] Input Buffer Using Spice



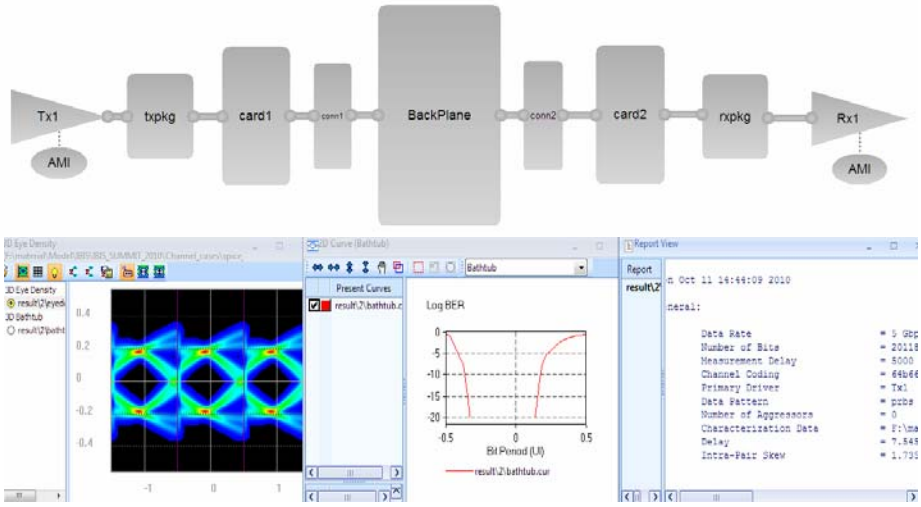
SIGRITY

[External Model] Description for Input

```
[External Model]
Language Spice
|
| Corner  corner_name    file_name      circuit_name (.subckt name)
Corner      Typ            rx_Spice.sp      rx_Spice
|
| Ports List of port names (in same order as in Spice)
Ports    A_pcref   A_gcref   A_signal   my_receive
|
| A_to_D   d_port        port1          port2          vlow   vhigh   corner_name
|A_to_D   D_receive  my_receive    A_gcref     -400m   400m     Typ
|
[End External Model]
```

SIGRITY

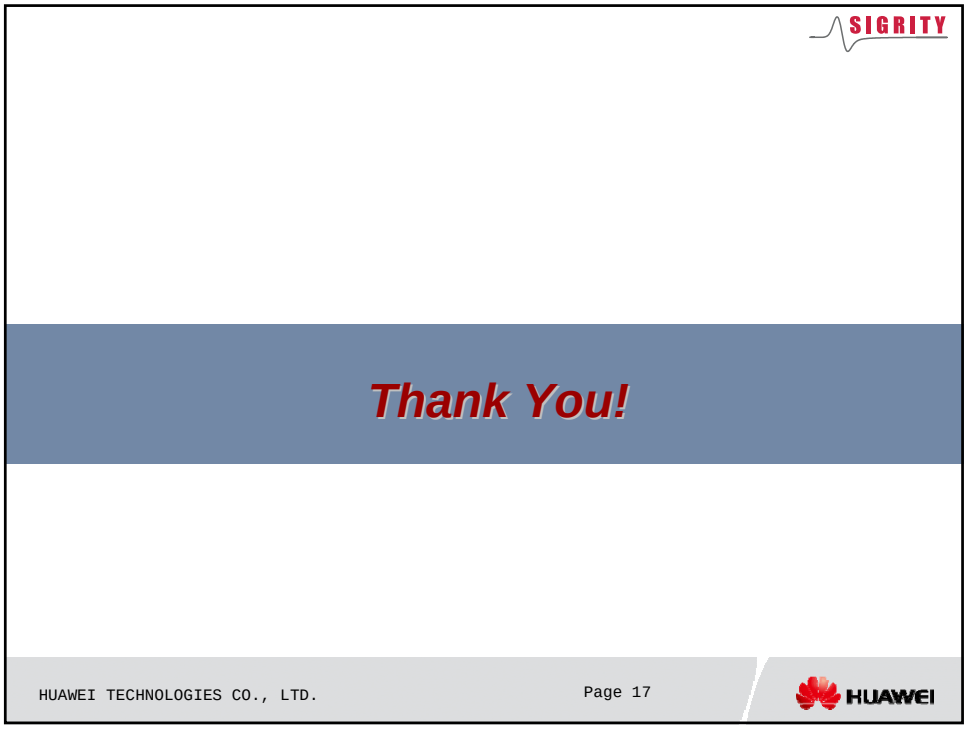
System Analysis



SIGRITY

Summary

- Spice-based subcircuits are convenient, fast, and accurate for serial link IO circuit modeling
- IBIS [External Model] keyword can be used to support Spice-based IO models, and don't require the [Pulldown], [Pullup], [POWER Clamp], [GND Clamp] data


SIGRITY
Thank You!
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Page 17
HUAWEI

Extending/Leveraging IBIS Constructs to Model High-Speed I/Os and Packages using AMI, Spice, and S-Parameters

John Lin
Flextronics, Inc

Taranjit Kukal, Feras Al-Hawari, Ambrish Varma
Cadence Design Systems, Inc.

Presented by: Dr. Wenliang Dai - Cadence

Asian IBIS Summit
Shenzhen China
November 9, 2010

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Agenda

- **IBIS Overview**
- **Why extend IBIS to SPICE models**
  - **Current Limitations**
- **Leveraging [External Model] to allow including Package S-Parameters for High Speed simulation**
  - **Example**
- **Extending [External Model] to:**
  - Simulate VI-VT model in conjunction with Spice sub-circuits that represent RDL elements, DSP Spice code, etc.
  - Dynamically switch sub-circuits to take care of corners and parametric variations.
  - Simulate AMI with [External Model] that represents analog IO modeled in Spice or S-parameters.
- **Summary**

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- **Summary**

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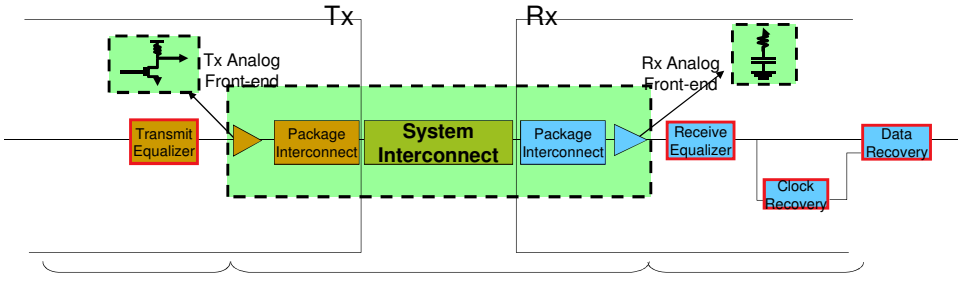
IBIS overview

- Analog IO model is modelled by IBIS VI and VT curves
- Equalization (DSP algorithmic) portion of IO model is modelled by AMI C-code (Algorithmic Model Interface) that is pointed by IBIS model
- RDL and or pin parasitics are lumped into pin R/L/C values



Partitioning – Algorithms and Circuit elements

cadence

Why extend IBIS to SPICE models

- **At high frequencies, IO buffers could have portions that need to be modeled using Spice files**:
  - On DIE Terminations (ODT) that vary with frequencies need to be expressed as s-parameters or RLGC Spice files
  - On DIE RDL parasitics become significant and vary with frequencies and hence have to be expressed as s-parameters or SPEF
  - Analog portion of IO-buffer is expressed as Spice as against VI-VT curve; s-parameters can also be used to describe transfer characteristics of IO-buffer amplifiers.
  - Some algorithmic portion may be modeled in Spice as against AMI code

cadence

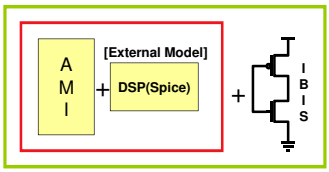
Why extend IBIS to SPICE models

- **Multiple Sub-circuits / Spice files**
  - Different Spice sub-circuits could be applicable for different process corners. On-DIE RDL could be expressed as different s-parameter files for typ/min/max conditions.
  - Different Spice sub-circuits could be applicable for different buffer configurations. For example, Pre-emphasis portion could have been modeled as Spice using different sub-circuits for different settings.
  - ODT could be a function of current being drawn out of IO-buffer (Dynamic ODT) and could have been expressed as behavioral Spice, Verilog-A

cadence

Current Approach and Limitations

- Package parasitics can be used as S-parameters by including them as part of interconnect network in a way similar to external interconnect parasitics.
  - Limitation
    - RDL parasitics that need to be part of IO-buffer characterization are treated as interconnects and assumed bi-directional.
- Spice IO-buffers can be included as part of IBIS using [External Model] Keyword.
  - Limitations
    - Cannot model DSP (in SPICE) in conjunction with AMI model
      - Use of [External Model] in conjunction with VI-VT (IBIS) is not recommended today
    - Does not directly support s-parameters (Touchstone)
      - For example, it is not easy to model RDL and other elements in conjunction with VI-VT curves cannot take care of process corners and parametric selection of subcircuits



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- Summary

cadence

Leveraging [External Model] to Support Package S-Parameters

- Long-term: IBIS model should have Keywords to support Touchstone S-parameters under Package section, with fields to
  - point to touchstone file from the Package section
  - provide port-mapping of IO-buffer pins to s-parameter ports
  - R/L/C values should be ignored by SI tools if s-parameter file is used
- Short-term: This can be achieved through use of [External Model] keyword
  - Set R/L/C values in package keyword as ZERO (to avoid double counting)
  - Point to the touchstone file of the package inside the Spice subcircuits

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Example : Support for S-parameters for package parasitics using [External Model]

- Use IBIS Device with 4 pins (1, 2, 3, and 4)
- Pins 1 and 2 are +ve and -ve diff pins respectively, with a “tx” diff model assigned to both of them
- Pins 3 and 4 are +ve and -ve diff pins respectively, with a “rx” tdiff model assigned to both of them
- Tx and Rx contain corresponding
  - [External Model] section

cadence

Example ….

```
[Component]     MyComp
[Manufacturer]  xyz

[Package]
| variable      typ           min           max
R_pkg           0.0m          0.0m          0.0m
L_pkg           0nH           0nH           0nH
C_pkg           0pF           0pF           0pF
|
|-----------------------------------------------------------------
[Pin]    signal_name      model_name       R_pin    L_pin    C_pin
|
  1      OUT1             tx               NA       NA       NA
  2      OUT2             tx               NA       NA       NA
  3      IN1              rx               NA       NA       NA
  4      IN2              rx               NA       NA       NA
|
[Diff Pin]  inv_pin  vdiff   tdelay_typ tdelay_min tdelay_max
|
 1          2        200mV    0ns        0ns        0ns
 3          4        200mV    0ns        0ns        0ns
|
```

Make values zero or NA

- Set the values of all package parasitics to 0 or NA because in this case we will model the package using an s-parameter that is referenced from the Rx/Tx subckts
- Assign the same model to each diff pin (e.g., tx is assigned to pins 1 and 2)
- Define the diff pins (e.g., 3 and 4) and specify vdiff

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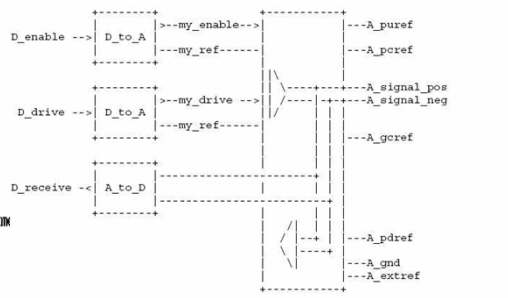
Example ….

```
|
[External Model]
Language SPICE
|
| Corner corner_name file_name   circuit_name (.subckt name)
Corner    Typ         tdiff_tx.spc  tdiff_tx_typ
Corner    Min         tdiff_tx.spc  tdiff_tx_min
Corner    Max         tdiff_tx.spc  tdiff_tx_max
|
| Ports List of port names (in same order as our 8-term macromodel)
Ports A_puref A_signal_pos A_pdref my_drive my_enable
Ports A_pcref A_gcref A_signal_neg my_ref
|
| D_to_A d_port   port1      port2    vlow vhigh trise tfall corner_name
D_to_A   D_drive  my_drive   my_ref   0.0  3.3   0.5n  0.3n  Typ
D_to_A   D_drive  my_drive   my_ref   0.0  3.0   0.6n  0.3n  Min
D_to_A   D_drive  my_drive   my_ref   0.0  3.6   0.4n  0.3n  Max
|
[End External Model]
|
```



Example SPICE, Verilog-A(MS) or VHDL-A(MS) implementation of a true differential buffer

- Specify language as SPICE
- Specify the SPICE files that contain the subckts for the typ/min/max corners i.e., tdiff_rx.spc in this case;
- tdiff_rx.spc should contains the following subckts tdiff_rx_typ, tdiff_rx_min, and tdiff_rx_max
- Ports can be split on separate lines, but each line is a continuation for the previous one (in this case each subckt has 9 ports)
- Add the D/A or A/D statements (no need for D_enable and D_Drive conversion for input models)

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Example ….

```
.subckt tdiff_tx_typ 1 2 3 my_drive my_enable 6 7 8 my_ref
* The terminals in an 8-terminal differential MacroModel are as follows:
*     power = 1
*     outp = 2
*     ground = 3
*     input = 4
*     enable = 5
*     power_clamp_reference = 6
*     ground_clamp_reference = 7
*     outn = 8

v1 my_ref 0 0
r1 my_enable 0 1e6
r2 my_drive my_ref 1e6

erx in 0 v='v(my_drive,my_ref)'
einv inv 0 v='v(1) - v(in)'

S1 in 2 inv 8 algorithm=default file= diff_pkg.s4p

.ends
```

- The SPICE subckt tdiff_tx_typ for the typical corner in tdiff_tx.spc is as shown on the left. Min and Max similar.
- We need to connect the extra IBIS nodes inside the subckt to make sure there are no disconnected nodes in the circuit
- This is a simple pass-through driver that applies the “in” stimulus and its inverted pattern to the package input nodes
- The s-parameter file (diff_pkg.dat) for the package is referenced internally in the subckt and connects the in and inv stimulus to the I/O output nodes i.e. 2 and 8

Similar for Rx

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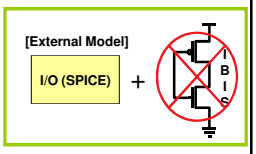
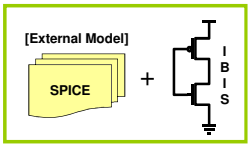
Simulate VI-VT model in conjunction with Spice

- Traditionally [External Model] keyword has been used for IO-buffer that needs to characterized as Spice IO in which case IBIS VI-VT data is not required.



- Extend use of [External Model] keyword to point to Spice sub-circuits that augment VI-VT data for complete characterization of IO-buffer.
  - Model On-DIE RDL parasitics using Spice or S-parameters that connect to Analog IO-buffer characterized as VI-VT data
  - Model DSP algorithm in Spice that works in conjunction with VI-VT data



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Simulate VI-VT model in conjunction with Spice

```
[External Model]
Language SPICE | SPARAM
Type Other
```

(VI-VT tables are required when Type is not I/O, Allowed Types are 'I/O' and 'Other', where 'Other' can be RDL, ODT, DSP, etc or any combination)

```
|corner       file_name                    circuit_name
 Typ          dsp.spc | dsp_typ.s4p        dsp_typ
 Min          dsp.spc | dsp_min.s4p        dsp_min
 Max          dsp.spc | dsp_max.s4p        dsp_max

| Ports List of port names (in same order as in SPICE | SPARAM)
Ports A_signal_pos A_signal_neg my_receive my_drive my_enable
Ports A_puref A_pdref A_pcref A_gcref A_extref my_ref A_gnd
```


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Agenda

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- Summary

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Dynamically switch sub-circuits to take care of corners and parametric variations.

[External Model]
Language SPICE

|corner	file_name	circuit_name	switch_param	switch_param_val
Typ	tdiff.spc	tdiff_txrx_typ	temp	50,100,150
Typ	tdiff.spc	tdiff_txrx_typ	freq	1,2,5
Min	tdiff.spc	tdiff_txrx_min	temp	-50,-100,-150
Max	tdiff.spc	tdiff_txrx_max	temp	70, 120, 200

Parameterized subcircuit selection

Allowed values with 1st as default

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- **Summary**

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Using AMI in conjunction with [External Model]

- Analog IO buffers in some cases could be modeled as s-parameters or as Spice sub-circuits. These models then work in conjunction with AMI code that represents DSP portion of IO-buffers. There could be even situations where IO-core itself becomes part of this AMI code.
- Hence we need to support AMI model simulation in absence of VI-VT data.
  - AMI model + Analog buffer represented as Spice-IO
  - AMI model + VI-VT Analog buffer + RDL (etc) in [External Model] (Case 1)
  - AMI model + Analog buffer represented as S-parameter-IO (Case 2)
  - AMI model (contains Analog-IO buffer coded as in AMI itself) + S-parameter/Spice RDL (Case 3)

```
[External Model]
Language SPARAM
Type I/O                    (VI-VT tables are not required as S-Params represent the analog I/O buffer or RDL etc + I/O buffer)

|corner              file_name
 Typ                 io_typ.s4p
 Min                 io_min.s4p
 Max                 io_max.s4p

| Ports List of port names (in same order as in SPICE | SPARAM)
Ports A_signal_pos A_signal_neg my_receive my_drive my_enable
Ports A_puref A_pdref A_pcref A_gcref A_extref my_ref A_gnd
```


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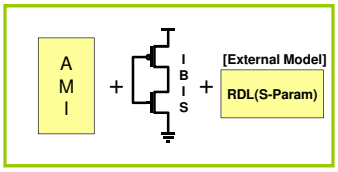
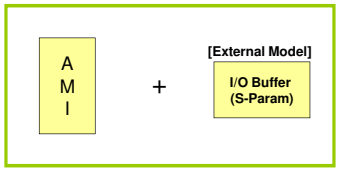
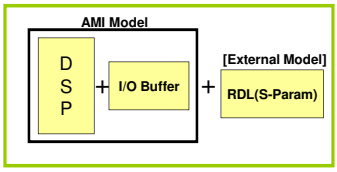
Using AMI in conjunction with [External Model]



Case 1



Case 2



Case 3

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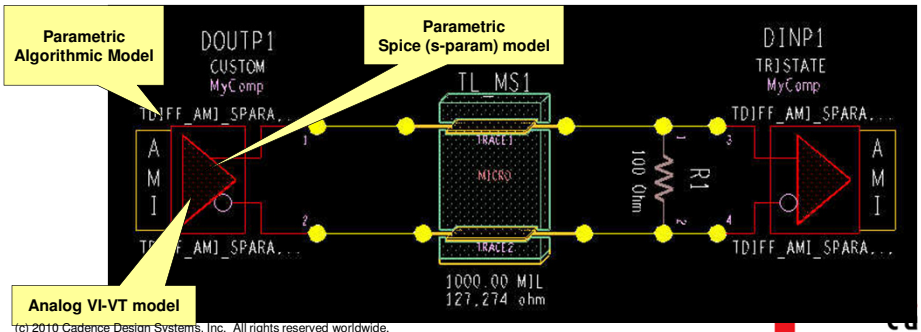
Summary

- Package parasitics can be modeled as SPICE using [External Model]; but we need to support S-parameters and it should be under proper keyword in Package-Section
- [External Model] has been traditionally used as alternate to VI-VT data; but we need to leverage it to use this model in conjunction with VI-VT
- [External Model] should support parameter switching to pick subcircuits dynamically
- AMI model today assumes analog-IO available as VI-VT; AMI model should work in conjunction with [External Model]



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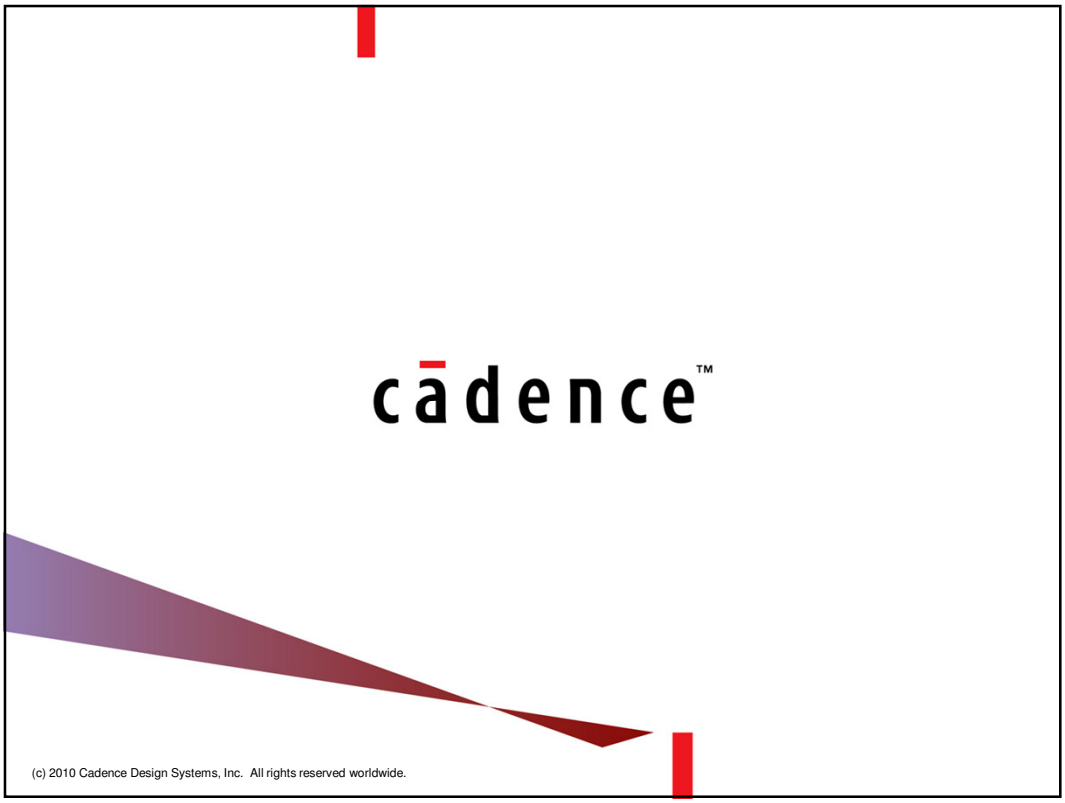
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IBIS-ISS: What It Is and What It Means to You

Michael Mirmak
Intel Corporation
Chair, IBIS Open Forum

马梦宽
英特尔公司
IBIS 委员会主席

IBIS Summit
Shenzhen, China
November 9, 2010

亚洲 IBIS 技术研讨会
中国深圳
2010 年 11 月 9 日

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2

Agenda

- The Problem of SPICE* Model Portability
- The Concept of IBIS-ISS
- What Is and Isn't Supported
- IBIS-ISS and Good SPICE Usage
- Status and Future Work
- Summary and Call for Action!

A Standard SPICE* Does Not Exist

- What does the following SPICE* statement do?

```
Bexample 1 2 I=sin(V(3,0))
```

- Results depend on the SPICE tool you use
  - IBIS or non-linear dependent source?
- Some elements are not supported or do not share a common meaning in all SPICE variants
  - Other non-universal elements include P, W, Y, Z

How do you ensure a model works in your tool or your customers' tools?

A Solution for SI/PI Interconnects

- SPICE* netlists include interconnects, devices and engine commands
  - e.g., .tran analysis for a driver and receiver on a PCB trace
- IBIS supports portable device models directly
- Engine commands are specific to EDA tools
- How to ensure interconnect models are portable?
  - Package, via, connector, PCB trace, on-die PDN…

IBIS-ISS: an industry baseline for interconnect modeling in SPICE

5

IBIS-ISS in Simple Terms

- IBIS-ISS: IBIS Interconnect SPICE* Subcircuits
- Defines a limited set of common, basic elements useful for SI interconnect modeling
- Based on documents and concepts donated by Synopsys as seen in Synopsys HSPICE*
- Developed with SI community through IBIS Interconnect Task Group
  - EDA vendors, IC vendors and system vendors

6

What Is (and Is Not) Supported

- Fundamental circuit elements
  - Resistors, Inductors, Capacitors: R, L, K, C
  - Dependent Sources: E, F, G, H
  - Transmission Lines: T, W (including tabular, Foster, etc.)
  - S-parameters: S
- Subcircuit definitions and instantiation
  - .subckt, .ends, X element
- Other basic commands
  - .include, .end, .param

… but no engine commands, no active device support, and no field solver

Usage Model

- IBIS-ISS consists entirely of subcircuits and subcircuit definitions
  - IBIS-ISS does not define netlists
  - Subcircuits may be nested or independent
- All parameters are local, and passed explicitly
- Multiple files are supported (.include)
- Compliant tools simply accept IBIS-ISS files
  - Meaning, properly apply IBIS-ISS assumptions within the scope of the top-level subcircuit

How Does It Work?

```
.subckt my_trace_group 1 2 3 4 5 6 7 8 ref length=5e-3
* Units are meters
* This is a top-level subcircuit
* The user/system designer will instantiate this circuit in a netlist

Xtrace_a 1 ref 2 ref single_trace local_length=length
Xtrace_b 3 ref 4 ref single_trace local_length=length
Xtrace_c 5 ref 6 ref single_trace local_length=length
Xtrace_d 7 ref 8 ref single_trace local_length=length

* This circuit assumes no crosstalk

  .subckt single_trace in local_ref out local_ref local_length=1

  Wsingle in local_ref out local_ref N=1 L='local_length'
  + TABLEMODEL='single_line_table'

  .include 'single_line_table.inc'
  * This file defines the tabular data using .MODEL
  * This file should also be written using ISS rules
  .ends

.ends
```


Using SPICE* Correctly

- Good SPICE* habits will make IBIS-ISS adoption and use easier
  - Pass parameters explicitly and sparingly
  - Do not rely on global parameter definitions
  - Avoid using global nodes
  - Use modular circuit design
  - Make node, parameter and element names clear and unique
  - Avoid setting engine options in subcircuits
  - Avoid ambiguous units and multipliers (e.g., amps vs. atto-)

Practice using IBIS-ISS rules in your circuits today

Status and Future Work

- Draft v0.7 now in review
- Once drafts are complete, the document will be provided to the IBIS Open Forum for approval
- A parser is under consideration
- Documents and background materials on-line:
  - http://www.eda.org/ibis/interconnect_wip/
- Mailing list available for updates and discussion:
  - http://www.freelists.org/list/ibis-interconn/

Questions and comments are welcome!

Summary

- If you model interconnects, IBIS-ISS can help ensure usability across SPICE* tools
- If you use SPICE of any kind, IBIS-ISS will be familiar to you
- Following principles of good SPICE circuit construction makes IBIS-ISS easy to use

Please study, learn, discuss and comment on the IBIS-ISS draft.

Your contributions are important!

Modeling Methods for Complex S-Parameters in Touchstone V2.0

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High-Speed System Lab , ZTE Corporation

Bringing you closer

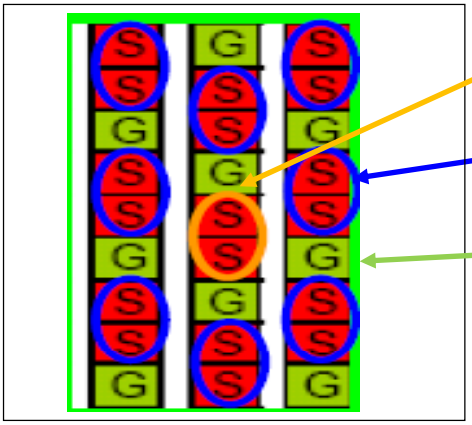
Asian IBIS Summit

Shenzhen,China
November 9, 2010

Agenda

- Requirement of Multi-port S-Parameters for Crosstalk Analysis
- Advantage of Touchstone V2.0
- Modeling Methods for Complex S-Parameters
- Lab Correlation for S28P Parameters
- Conclusions

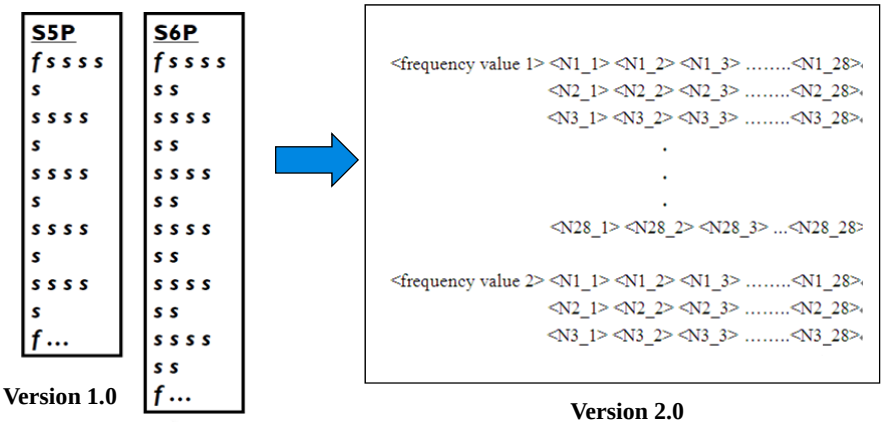
Requirement of Multi-port S-Parameters for Crosstalk Analysis



- Touchstone V2.0 file can include more crosstalk information of > 4 port case
- In this case，we need 28-port S-parameters for crosstalk analysis

Advantages of Touchstone V2.0

- No restriction exists on the number of data pairs on a line in Version 2.0 files.(Data format restrictions relaxed)

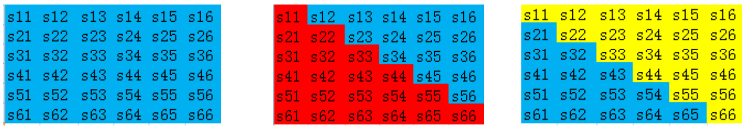


Version 1.0

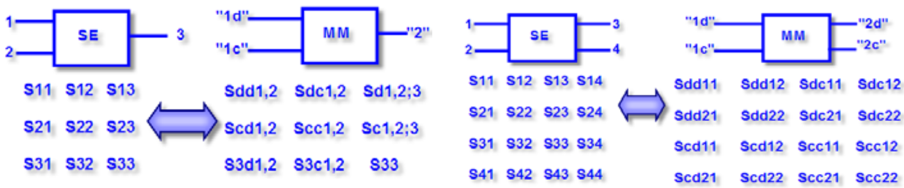
Version 2.0

Advantages of Touchstone V2.0

- The [Matrix Format] keyword: “Full”, “Lower”, or “Upper”.



- SE, MM & GMM data



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What can an N-port（n≥4）VNA do ?

- VNAs with less than 4 ports are very common.
- Even 16 ports VNA can’t get whole information directly in this sort of case.
- Some methods can be used for n-port （n≥4） S-parameters conversion based on 4-port S-parameters.

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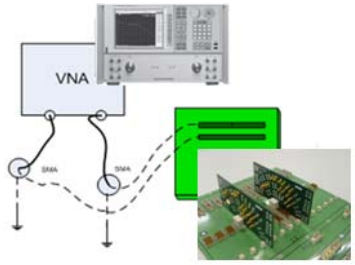
Modeling Methods for Complex S-Parameters

- How do we get s4p file if we have a 2 ports VNA only?

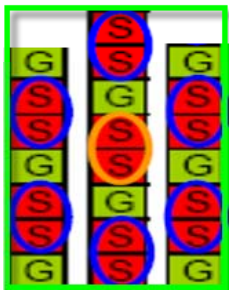


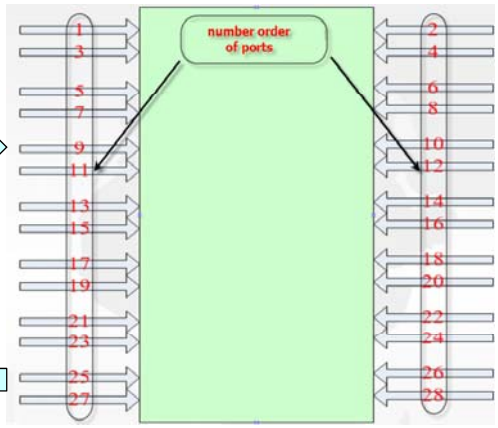
s11	s12	s13	s14
s21	s22	s23	s24
s31	s32	s33	s34
s41	s42	s43	s44

- Need 6 times measurement to get all data $C_4^2 = 6$

Modeling Methods for Complex S-Parameters

- This is a actual case

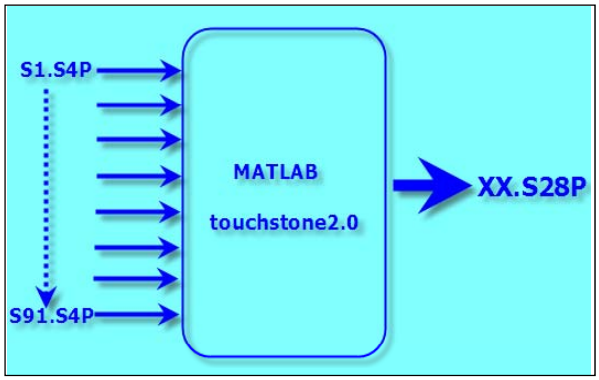




$C_{14}^2 = 91$

- Needs 91 times measurement with a 4 port VNA **Step1**

Modeling Methods for Complex S-Parameters



- Using Matlab to abstract proper data
- According to Touchstone V2.0 format

Step2

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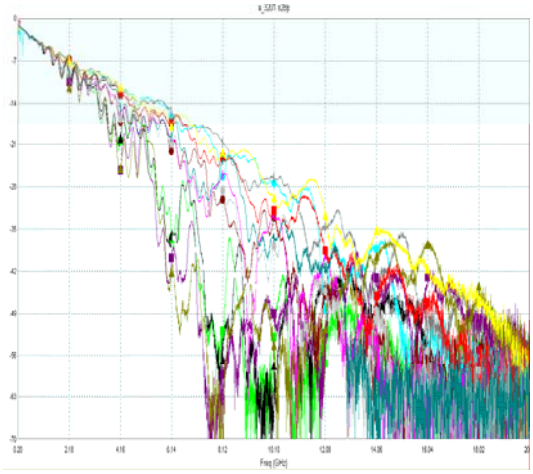
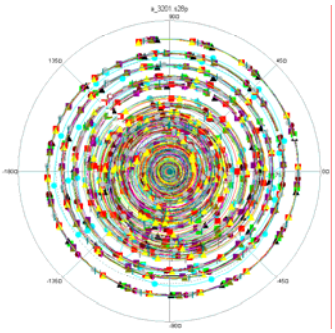
Modeling Methods for Complex S-Parameters





- Error check
- Passivity & Causality

Step3

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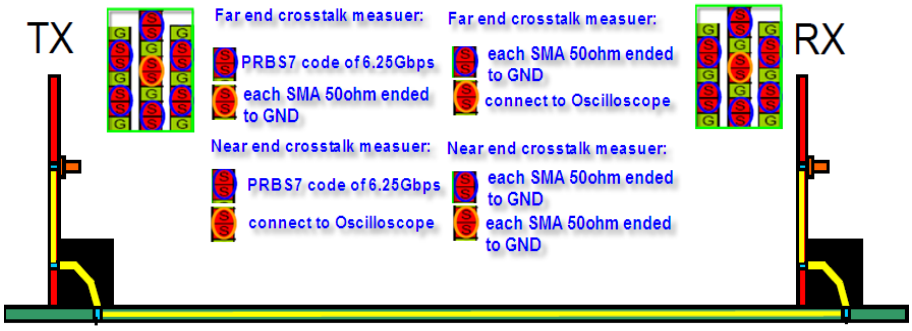
Lab Correlation for S28P Parameters

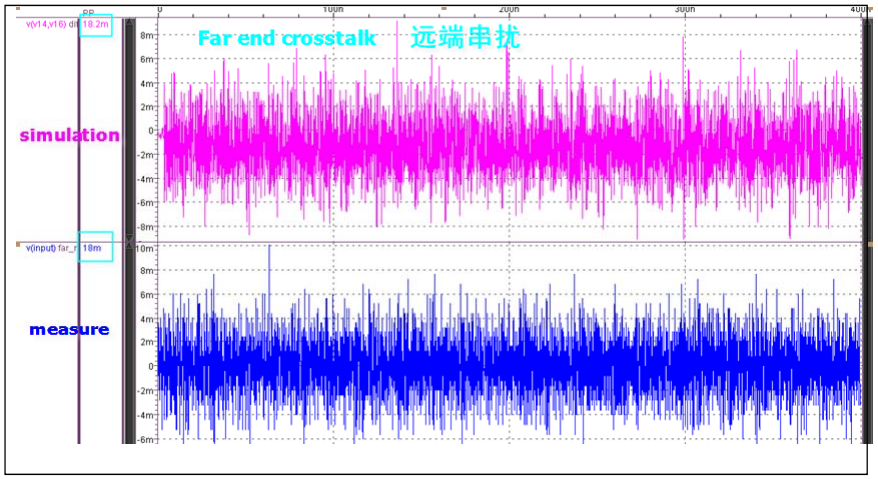
- Based on victim differential signal measurements



- Saving every channel waveform and recalling them as a PWL source in Hspice netlist
- Using S28P file to model whole channel

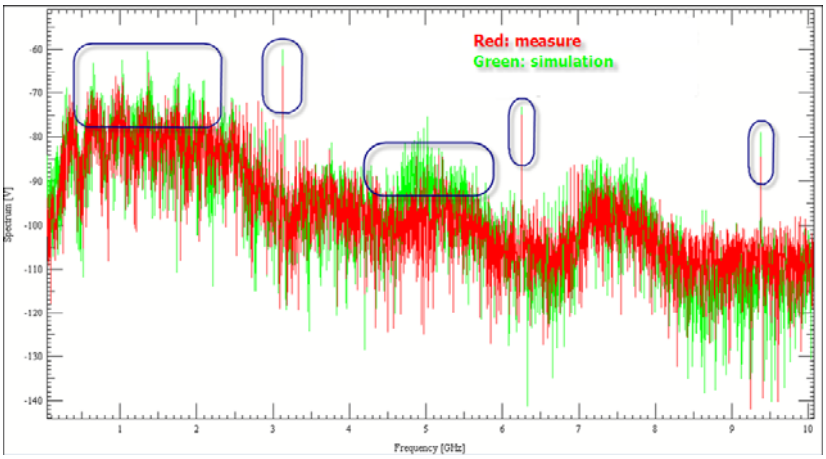
Lab Correlation for S28P Parameters

- Far end crosstalk in time-Domain



Lab Correlation for S28P Parameters

- Far end crosstalk in frequency-Domain



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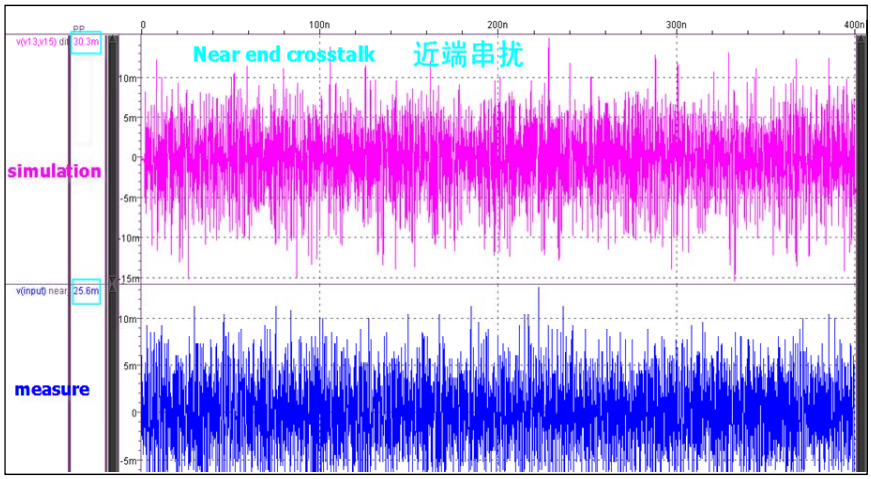
Lab Correlation for S28P Parameters

- Near end crosstalk in time-Domain



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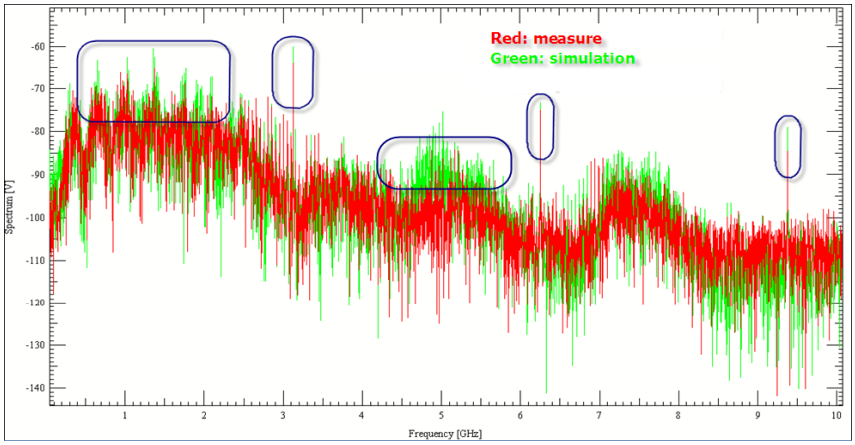
Lab Correlation for S28P Parameters

- Near end crosstalk in frequency-Domain



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Lab Correlation for S28P Parameters

- Contrast with measure data and result of FFT , this method is effective for modeling of multi-port S parameters.
- FFT analysis shows the S28P file can include detail information of frequency response very clearly.
- Matlab programming is useful to process individual cases . But the way we coding is not a general way.

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Lab Correlation for S28P Parameters

- A proposition for complex S-parameters modeling
  - Adding keywords to give information of S-parameters need to be combined
- Such as **[Combine information] Ninp Noutp Tsn Sorder**
  - **Ninp** means **(**number of input S file port) for example : 4
  - **Noutp** means (number of output S file port) for example : 28
  - **Tsn** means (total S parameter Number) for example : 91
  - **Sorder** means (input S file combination order) for example : 2 of 91

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Conclusions

- Multi-port S-parameter is widely used for crosstalk analysis in high-speed system design, Touchstone V2.0 provide favourable conditions to model multi-port interconnect networks.
- Based on certain times 4-port S-parameter measurement we can get SnP (n>4) file through programming process
- We expect a general S-parameter conversion method supported by EDA software.
- We may give keywords to combine S4P files , and software can abstract proper data from each S4P file in a general rules and orders.

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References

- **Touchstone Syntax for Versions 1.0 and 2.0**
  Bob Ross TERASPEED CONSULTING GROUP
- **Touchstone Version 2.0 Mixed-Mode Syntax –Updated**
  Bob Ross TERASPEED CONSULTING GROUP
- **S-Parameter Conversions**
  Tony Donisi Ansoft Corporation

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Thanks!

Bringing you closer

Model Connection Protocol extensions for Mixed Signal SiP

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Presented by: Dr. Wenliang Dai - Cadence

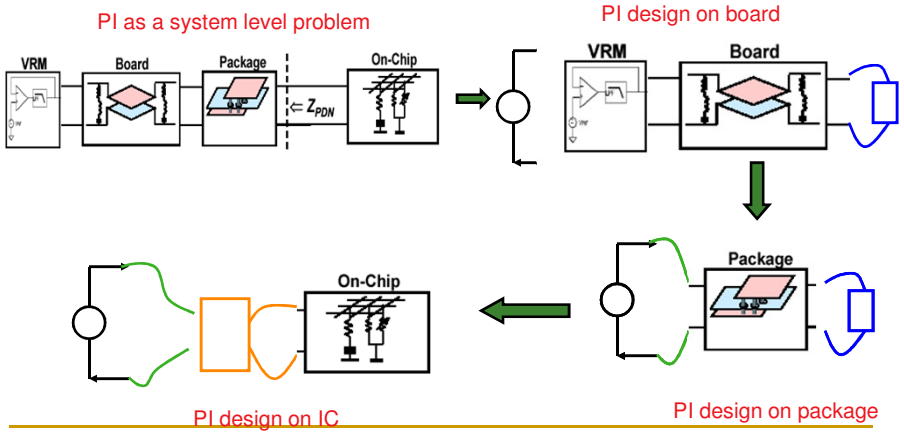
Asian IBIS Summit
Shenzhen China
November 9, 2010

Agenda

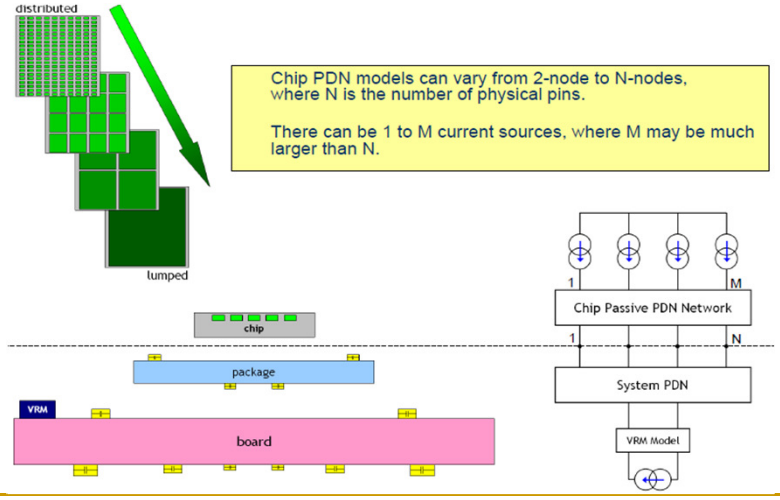
- Why Model Connection Protocol
- Model Connection Protocol overview
- Extensions required for Mixed Signal SiP
- MCP Applications
- Summary

Why Model Connection Protocol - IC/Pkg/Board PDN Co-design

- Design low impedance path: supply to chip



Why Model Connection Protocol - IC/Pkg/Board PDN Co-design

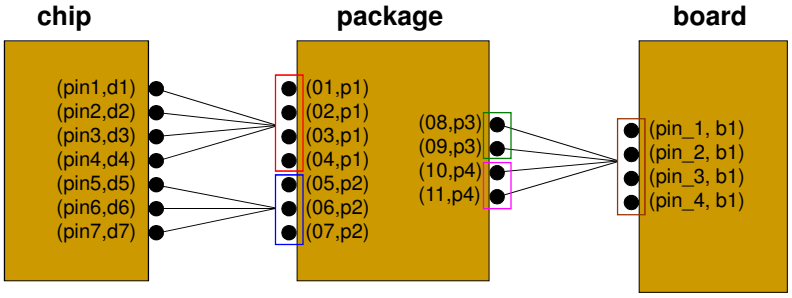


Why Model Connection Protocol - IC/Pkg/Board PDN Co-design

- Chip/Package/Board have many physical connections
  - Chip-Package Boundary:100-6000
  - Package-Board Boundary: 100-3000
- Not all electrical nodes can have per-pin resolution
  - Models may become too large for computation, simulation
- Need way to group pins and auto-connect models across IC/Pkg/Board

MCP Overview - Establish mapping

- Pin grouping and mapping
  - **physical pin (of layout) to electrical node (of model) per Net**
  - **Mapping to connecting structure using physical location**



Example of VDD net across chip-pkg-board

MCP Overview
- Establish mapping

Pins of net

Electrical node

Netname

X-Y loc of pin

```
.subckt chip  d1 d2 d3 d4 d5 d6 d7
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] DIE
* [MCP Source] chip extraction tool
* [Coordinate Unit] um
* [Connection] pkg1  pkg_bumps  7
*   [Connection Type] PKG
*     [Power Nets]
*       pin1  d1  VDD    0    0
*       pin2  d2  VDD    0  100
*       pin3  d3  VDD  100    0
*       pin4  d4  VDD  100  100
*       pin5  d5  VDD   50    0
*       pin6  d6  VDD   50   50
*       pin7  d7  VDD   50  100
* [MCP End]
 --- SPICE elements ---
.ends
```

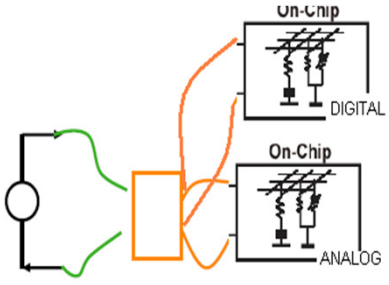
```
.subckt package  p1 p2 p3 p4
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] PKG
* [MCP Source] package extraction tool
* [Coordinate Unit] um
* [Connection] die1  myCPU  7
*   [Connection Type] DIE
*     [Power Nets]
*       01  p1  VDD    0    0
*       02  p1  VDD    0  100
*       03  p1  VDD  100    0
*       04  p1  VDD  100  100
*       05  p2  VDD   50    0
*       06  p2  VDD   50   50
*       07  p2  VDD   50  100
* [Connection] board1  my_board  4
*   [Connection Type] PCB
*     [Power Nets]
*       08  p3  VDD    0    0
*       09  p3  VDD    0  200
*       10  p4  VDD  200    0
*       11  p4  VDD  200  200
* [MCP End]
 --- SPICE elements ---
.ends
```

```
.subckt board  b1
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] PCB
* [MCP Source] board extraction tool
* [Coordinate Unit] mm
* [Connection] pkg1  pkg_balls  4
*   [Connection Type] PKG
*     [Power Nets]
*       pin_1  b1  VDD  0.0  0.0
*       pin_2  b1  VDD  0.0  0.2
*       pin_3  b1  VDD  0.2  0.0
*       pin_4  b1  VDD  0.2  0.2
* [MCP End]
 --- SPICE elements ---
.ends
```

Example of VDD net across chip-pkg-board

MCP Extensions for Mixed Signal SiP

- Analyze power-delivery to ICs when Package rails supply power to
  - different ICs that could be digital and/or analog
  - RF-modules and Passive/Active SMDs
- Need Schematic driven Mixed Signal Simulations to process IR-drop at power-rails



PDN supplying Analog and Digital multi-DIE system

MCP Extensions for Mixed Signal SiP
-Current MCP scope

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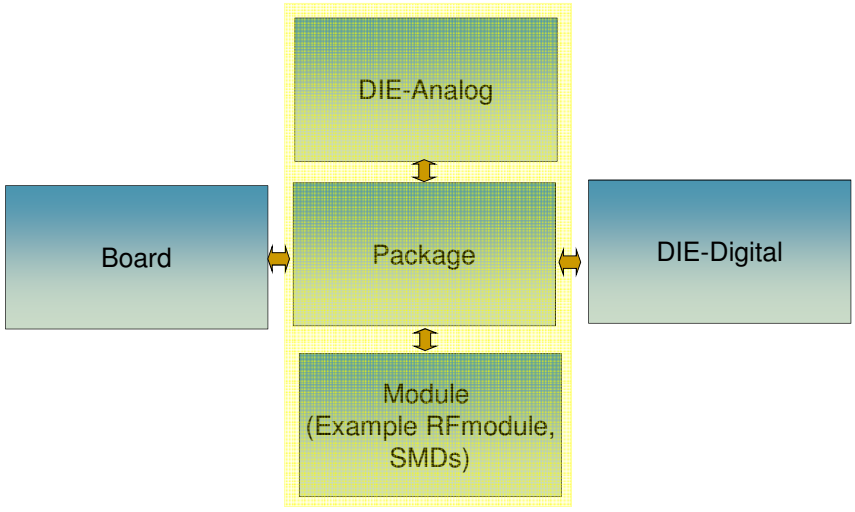
MCP Extensions for Mixed Signal SiP



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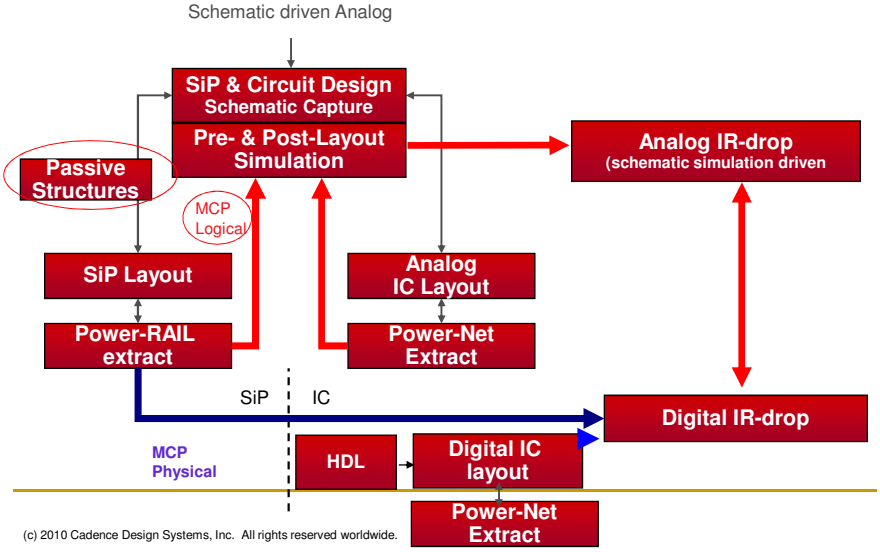
MCP Extensions for Mixed Signal SiP

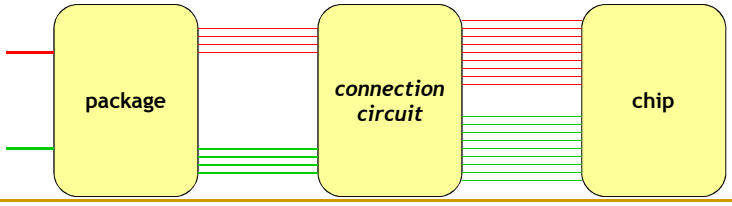
- Mixed Signal IR-drop Task Flow



MCP Extensions for Mixed Signal SiP

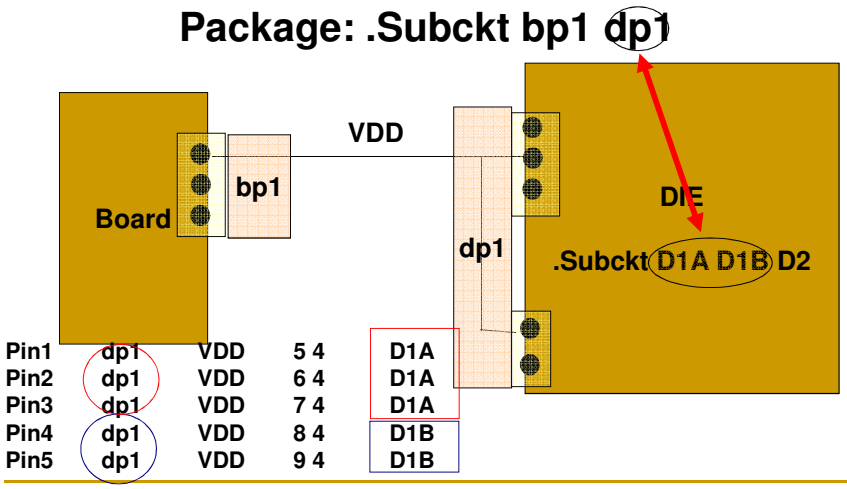
- Electrical connectivity of models with disparate pin grouping

- Support for mapping of different electrical port-groups across different structures
  - As an example
    - a package model with 2-by-2 grid-based pin grouping
    - a chip model with 3-by-3 grid-based pin grouping
  - desired is an electrical circuit to interface between an 8 node circuit and an 18 node circuit



MCP Extensions for Mixed Signal SiP

– Optional Column for mapping of electrical nodes across structures

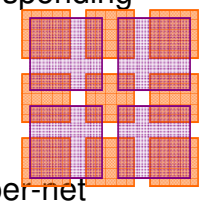


MCP Extensions for Mixed Signal SiP

- Caution: Electrical connectivity with disparate pin grouping

- Examine the nodes of the each net
  - for overlapping pin group domains, the corresponding nodes are shorted together
    - (1,1) node shorts together {(1,1), (1,2), (2,1), (2,2)} nodes
    - (1,2) node shorts together {(1,2), (1,3), (2,2), (2,3)} nodes
    - (2,1) node shorts together {(2,1), (2,2), (3,1), (3,2)} nodes
    - (2,2) node shorts together {(2,2), (2,3), (3,2), (3,3)} nodes

    alternately
    - (2,2) node shorts together {(1,1), (1,2), (2,1), (2,2)} nodes
  - all nodes are shorted together, reducing to per-net connectivity
    - instead of 8 or 18 node electrical connectivity it is actually 2 node connectivity



- Recommendation
  - Connecting two disparately pin-grouped models is possible by choosing to short together electrical nodes that have overlapping pin domains
    - ~~but it can reduce the effective resolution of the model at the chip/package interface~~
    - Useful in case of early debugging and quick connectivity

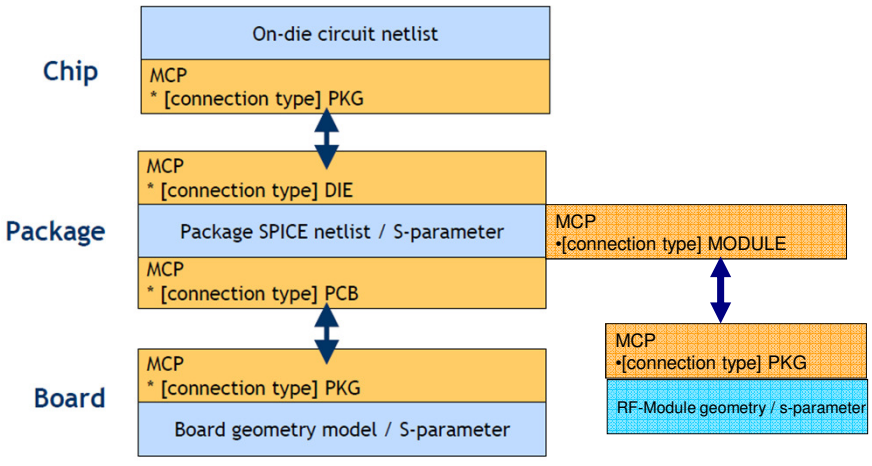
Extensions over existing MCP

- Support for Modules as connect type structures

- Mixed Signal SiPs would have elements other that ICs like
  - RFmodules
  - Metal Passive structures
  - SMD components
  - Silicon Interposers
- These structure draw power impacting PDN loading and hence we need to support [Module] category besides IC, Package and Board

Extensions over existing MCP

- Support for Modules as connect type structures



Extensions over existing MCP

- Connection by Refdes besides X-Y location

- In order to connect to structures that are SMD or metal-passive structures on SiP – usually a case for Mixed Signal SiP, it becomes difficult to connect by X-Y locations.
- Early analysis may require quick way of stitching the models across structures and minor placement or resolution changes can cause X-Y mapping to fail.
- Optional column showing connection by REFDES makes easy mapping for Mixed-Signal modules and early trials
  - Examples of connecting interfaces could be
    - IO-cellname (DIE IO)
    - R1:1 (pin 1 of R1)
    - CONN:1 (pin1 of PCB connector)
    - my_model_opamp:3 (port-3 of opamp subcircuit)

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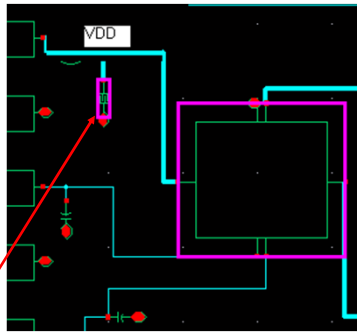
Extensions over existing MCP

- Connection by Refdes besides X-Y location

- Simulating Analog DIE in package schematics with loading from passive structures connected to DIE
- The simulation data is post-processed to obtain IR-drop at power-rails



[connection type MODULE]

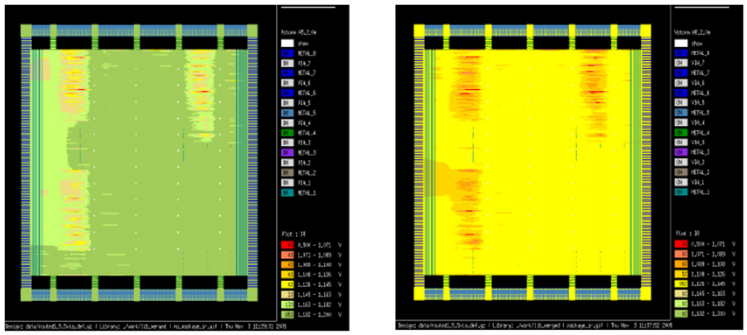
Pin1	**dp1**	**VDD**	**5**	**4**
Pin2	**dp1**	**VDD**	**6**	**4**
Pin3	**dp1**	**VDD**	**7**	**4**

varistor1:2 //Reference_design:pin//
varistor2:2

MCP applications: Digital DIE IR-drop

- Digital DIE in context of package model

Simulation results of Vdd rail: Dynamic IR-Drop



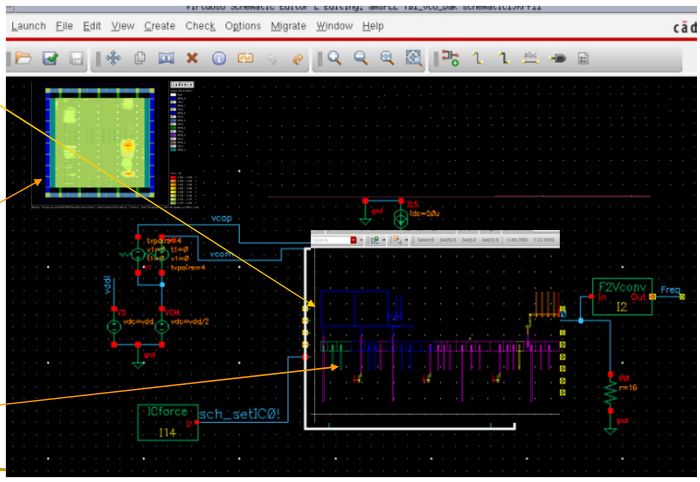
Without package effects
worst-case IR drop :
147.5mV

With package effects
worst-case IR drop :
179.3mV

MCP applications: Analog DIE IR-drop

-Analog DIE in context of package model & Digital DIE-models

- Analog DIE test-bench with power-rail model
- Digital DIE model connected to represent loading of power-rail
- Analog DIE IR-drop post simulations



Summary: MCP format updated in context of Mixed Signal contents

```
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] {DIE|PKG|PCB}        Device Info (self)
* [MCP Source] source text
* [Coordinate Unit] unit                Device Info (external)
* [Connection] connectionName partName numberPhysicalPins
*   [Connection Type] {DIE|PKG|PCB}     Module      Connection Info
*       [Power Nets]                                 I/F electrical node column   I/F part-ref column
*         pinName  modelNodeName  netName  x  y
*         …
*         pinName  modelNodeName  netName  x  y
*      [Ground Nets]
*         pinName  modelNodeName  netName  x  y      Pin Info
*         …
*         pinName  modelNodeName  netName  x  y
*       [Signal Nets]
*         pinName  modelNodeName  netName  x  y
*         …
*         pinName  modelNodeName  netName  x  y
* [MCP End]
```

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