IBIS Open Forum Minutes

Meeting Date: **November 6, 2009**
Meeting Location: **Tokyo, Japan**

VOTING MEMBERS AND 2009 PARTICIPANTS

Actel	(Prabhu Mohan)
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Apple Computer	(Matt Herndon)
Applied Simulation Technology	(Fred Balistreri)
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Cadence Design Systems	Terry Jernberg, Ambrish Varma, Aileen Chen, Lanbing Chen, Wenliang Dai, Fenghua Gao, Feng Li, Ping Liu, Yubao Meng, Jian (John) Peng, Qian (Candy) Shen, Muker Wang, Yifong Wen, Jun Wu, Zhi (Benny) Yan, Wayne Zhang, Wenjiang Zhang, Qi (Alex) Zhao, Yukio Masuko*, Morihiro Masuko*
Cisco Systems	Luis Boluna, Tram Bui, Bill Chen, Syed Huq, Mike LaBonte, Pedo Miran, Huyen Pham, [AbdulRahman (Abbey) Rafiq], Ashwin Vasudevan, Zhiping Yang, Guan (Greg) Fu, Jin (Leo) Hu, Chunhai Li, Weifeng Shu, Xinghai Tang
Ericsson	Anders Ekholm*
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IBM	Adge Hawes
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Myoung J. Choi, Michael Mirmak, Vishram Pandit, Jon Powell, Sirisha Prayaga, Lili Deng, Leo Fang, Haifeng (Bill) Gong, Fanghui Li, Jenny Li, Wenjie Mao, Yiunglei Ren, Yang Wu, Maoxin Yin, Xinjun Zhang
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Sigrity	Brad Brim, Sam Chitwood, Raymond Chen, Jiangsong Hu, Li Li, Xianfeng Li, Lily Lou, Zhangmin Zhong
Synopsys	Ted Mido, Xuefeng Chen, Wenyun Gu, Jinghua Huang, Bo Liu, Qin (Kitty) Zhang
Teraspeed Consulting Group	Bob Ross*
Toshiba	Yoshihiro Hamaji*
Xilinx	[David Banas]
ZTE	Xiaolin Chen, Yanbin Chen, Jinku Guan, Mai Hu, Nan Jiang, Fei Lu, Xiaorong Lu, Xianyu Meng, Junwei Zhang, Shunlin Zhu
Zuken	Michael Schaeder, Ralf Bruening, Motoyuki Matsuawa*, Hirohiko Matsuawa*

OTHER PARTICIPANTS IN 2009

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AET	Mikio Kiyono
Altera	Hui Fu
Apache	Yu Lin, Junyong Deng, Shulong Wu
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Celestica	Fajiang Liu, Cao Wang, David Wu, Baoshu Xu, Fei Xue, Van Zhu
Circuit Spectrum	Zaven Tashjian
CST	Antonio Ciccomancini, Martin Schauem
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Exar	Helen Nguyen
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Fujitsu VLSI	Tetsuya Inoue*
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Hua Symantec	Senliang Han
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IdemWorks	Michelangelo Bandinu
Japan Aviation Electronics Industry	Hiroaki Ikeda*
JEITA EC Center	Atsushi Ishikawa*
Juniper	Kevin Ko
Kineret Design	Ricardo Teliuteuesh
Kyocera Elco Corporation	Noniyuki Akai*
LeCroy Corporation	Weidong (Derek) Hu, Scott Zhang
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Mindspeed Technologies	Bobby Alkay
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NetLogic Microsystems	Eric Hsu
Politecnico di Torino	Igor Stievano
Sanmina SCI	Vladimir Drivanenko
Sedona International	Joe Socha
Shanghai ITG Information Technology	Rongsheng Yuan
Siemens	Manfred Maurer
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Texas Instruments	Pavani Jella
TDK	Yoshikazu Fujishiro*
THine Electronics	Yohei Izhizone*
Towa Electronics	Yoshikazu Suzuki*
Vendor Chain International	Jing Lou
Xsigo Systems	Robert Badel
Zuken Support and Service	Seikou Go*, Ryosuke Tokonami*, Tomotaka Unose*, Yin Yi*
Independent	Ian Dodd

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
November 20, 2009	208 910 728	IBIS

For teleconference dial-in information, use the password at the following website:
https://cisco.webex.com/cisco/j.php?J=208910728

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

WELCOME AND KEYNOTE COMMENTS

The IBIS Open Forum Summit was held in Tokyo, Japan at the Japanese Electronics and Information Technology Industries Association (JEITA) headquarters. About 39 people representing 25 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/pub/ibis/summits/nov09b/

Toshiro Honda of Sony and head of the JEITA EC Center provided a brief welcome when the meeting started at 2:00 PM. This was followed by welcoming remarks from Takeshi Watanabe who heads the EDA working group under the JEITA EC Center.

Bob Ross also welcomed everyone to the Asian IBIS Summit and noted that the meeting will cover several IBIS topics. The IBIS committee wants to learn the concerns of Japan and other regions of the world. Along with JEITA, he thanked the three co-sponsors for making the meeting possible: ATE Services Corporation (Sigrity), Cadence Design Systems, and Zuken.

Bob introduced the Lance Wang, IBIS Vice Chair, and Anders Ekholm, IBIS Model Librarian as visitors from abroad. He looked forward to a productive meeting.

RECENT IBIS ACTIVITIES

Bob Ross (Teraspeed Consulting Group, USA)

Bob Ross showed the new IBIS logo and the list of new IBIS officers, most who have been to the Asian IBIS summits. He thanked Michael Mirmak, past Chair for his six years of service. He showed the active task groups and noted that IBIS has been active since 1993 with regular

meetings.

IBIS Version 5.0 was released in 2008, and Bob illustrated the ibischk5 (available the previous week) new flags for the algorithmic modeling interface (-ami) and numbered errors and warnings (-numbered). Bob also noted that Touchstone Version 2.0 was approved and also that he just received an alpha release of the tschk2 parser. The Quality Specification Version 2.0 was approved the previous week. While advances on the Algorithmic Modeling Interface are continuing, the Interconnect Spice Subcircuit project is temporarily on hold.

Overall work is continuing on IBIS advances, and the IBIS committee remains very active, attracts top talent, and has active international participation.

JAPAN IBIS ACTIVITIES UPDATE 2009

Kazuyoshi Shoji (Hitachi ULSI Systems, Japan)

Kazuyoshi Shoji stated that the Japanese economic outlook is still weak, and the recovery is slow. But design opportunities are increasing in selected areas. The modeling outlook is positive. Sales, lower cost and advanced technology are enhanced by IBIS models of high quality and also new technology models.

IBIS support in Japan is led by Takeshi Watanbe of the JEITA EC Center/EDA WG. Within this group are Kazuyoshi Shoji for Promotion, Yoshihiro Hamaji for Quality, and Hiroaki Ikeda for New Technology including interconnect modeling.

Because of popular demand, an IBIS Guidebook in Japanese authored by Kazuyoshi will be published soon to provide IBIS information in Japanese. It introduces IBIS and shows a design example using IBIS. It will also contain a Japanese explanation of IBIS Version 5.0.

GUIDANCE OF PASSIVE EDA MODELS

Hiroaki Ikeda (Japan Aviation Electronics Industry, Japan)

Hiroaki Ikeda stated that S-parameter data is widely used as the simulation model for signal integrity. However, models from different vendors may have different bandwidths, upper or lower frequencies, and frequency steps. Some simulator calculations are sensitive to these choices.

Hiroaki showed a measurement setup and then showed how a set of transient simulation for S-parameter files with different limitations compared to measurements. Two different simulators were used, and simulator A showed a good match to measurement while simulator B had significant DC shift when 0 Hz data was not provided. Lower bandwidth models had problems (offset and ringing) with simulator A, and these models failed in simulator B.

Further work will be continued by this group to provide guidelines about 0 Hz and/or data extrapolation, upper frequency limits and number of frequency steps.

SPARSE MATRIX MAPPING IN FUTURE TOUCHSTONE 2.1

Bob Ross (Teraspeed Consulting Group, USA)

Bob Ross first gave a brief overview of the recently released Touchstone Version 2.0 history and 13 IBIS-like keywords and block arrangement. He also showed the more rigid Touchstone 1.0 fixed format structure that contains less direct information about its content.

Bob then introduced the sparse matrix mapping concept with a 2-row, 3-column physically symmetrical connector. First, he showed the existing .pkg and .ebd coupled package concept with unique coupling from pin 1 to global ground, to the other pins 2 to 6 and the thru path to the other side. This is the standard LRGC model structure, as used for [Define Package Model]. It documents only the upper triangle coupling relationships since for passive networks, the lower triangle are identical about the matrix diagonal.

He then used the same example to demonstrate the [Sparse Matrix Mapping] keyword under discussion for Touchstone Version 2.1. Because of the physical symmetry assumption, the amount of data can be reduced significantly in a Touchstone file. Many of the columns that are required under [Network Data] are identical. So, an indirect method mapping all the identical columns (designated by their row,column index-pairs) into a single column of complex data entries (data-pairs) under [Network Data] can be done using integer-labels, an integer that references the specific column storing the complex data information for each frequency.

The example of the 6-pin connector corresponds to a fully filled out 12-port file (the port numbers 1-6 were chosen for side 1, and port numbers 7-12 were chosen for side 2 so that the labeling would be identified with the port to which the coupling occurs. In general there is no restriction to the port labeling. The corresponding N-port would require 144 complex entries per frequency under [Network Data]. But by identifying the unique coupling on side 1 (including to global ground, and the thru path to side 2), only 7 unique entries are needed. An additional 5 entries are needed for the unique coupling from side 1 to the remaining 5 ports of side 2, but some users might need to include these entries. These effects are currently neglected in the standard .pkg and .ebd formats.

Bob used one coupling (port 1 to 5 on side 1) and identified the 16 identical coupling relationships if physical symmetry is assumed. Since the reciprocal relationships are included, this set can be reduced to 8 upper or 8 lower relationships by making use of the [Matrix Format] keyword and choices Upper or Lower.

With similar reductions for all the coupling relationships, Bob showed the syntax for a complete example (with only 7 integer-labels and only 7 columns of complex data-pairs. (If all the unique coupling relationships were included, 12 columns would be needed.) Only 7 (or 12) columns of complex data are needed for an N-port instead of up to 144 columns.

This set of unique coupling relationships can be used to document the coupling to the adjacent two physical columns on either side and then expanded to model larger connectors with many more physical columns. The relationships beyond two columns are assumed “0” and omitted. So Bob showed tables for 6-pin, 40-pin, and 200-pin connectors and the number of index-pairs needed for each integer-label. He also showed a bank of isolated 40 pin connector blocks that a manufacturer might design for expandable configurations. In all cases the number of data-pairs is 7 (or 12), and this amount of data is less than a traditional 3-port description.

The exact details are still being discussed. All other keywords are compatible with this approach including differential representations with [Mixed-Mode Order].

IBIS QUALITY REVIEW, A STATUS REVIEW OF THE IBIS QUALITY SPECIFICATION

Anders Ekholm* and Mike LaBonte** (*Ericsson, Sweden and **Cisco Systems, USA)

Anders Ekholm provided the basic meeting information for the Quality Task Group and how to subscribe to its reflector. He gave a brief history from its beginning in 2002, Version 1.0 release in 2004, and the recent release of Version 2.0 on the previous Friday, October 30, 2009.

Anders outlined the levels of the IBIS Quality Specification Version 1.0 from IQ0 through IQ3. He noted its issues, particularly with level 0 meaning that the IBIS model passed ibischk. The IBIS Quality Specification Version 2.0 adjusted the levels from IQ0 though IQ4 and also added some modifiers: S, M, X, and G. The new levels are:

IQ0 - not checked
IQ1 - passes ibischk
IQ2 - suitable for waveform simulations
IQ3 - suitable for timing analysis
IQ4 - suitable for power analysis (defined but no checks yet)

And modifiers:

S - simulation correlated
M - measurement correlated
X - exceptions
G - has golden waveforms

He showed some sample tests related to each level. The previous correlation section will be moved to refer to the IBIS Accuracy Handbook. The committee produced many drafts and will produce a few BUG reports related to some of the checks. Anders noted that the active members included systems companies, users and semiconductor company developers of IBIS models. He expects adoption by IC vendors and librarians in systems companies and quality checks to be included in modeling tools.

JEITA IBIS QUALITY WG UPDATE

Yoshiro Hamaji (Toshiba, Japan)

Yoshiro Hamaji presented the motivation for a quality framework. The model maker, chip vendor, and EDA vendor all question if the IBIS model is generated correctly and the simulator is used correctly. The JEITA IBIS Quality WG can provide a framework for getting better IBIS models and qualifying the EDA simulators.

Currently only low speed models are considered to evaluate/debug the framework. With a qualified IBIS model, a qualified simulator and a qualified user, good agreement is achieved between SPICE and IBIS simulations. Twelve test circuits were shown.

The quality framework is a web-based system to serve all parties. Yoshiro presented several pictures to show how various parties can supply and get information.

Yoshiro also showed the verification of IBIS framework where the chip vendor provides a golden IBIS model. The model maker provides simulation results. The quality framework also showed that a Version 2.1 IBIS model produced better results than a [Ramp] based Version 5.0 model.

With the IBIS Quality Framework, problems were resolved and all Version 2.1 level models passed all 12 tests.

Future work includes extending the framework for more advanced models with higher speeds and for differential IBIS models. Also this framework will be available on the JEITA web site in the future and promoted with seminars.

C_COMP EXTRACTION METHODS FOR HIGH-SPEED I/O BUFFERS

Lance Wang (IO Methodology, USA)

Lance Wang introduced several methods to extract C_comp. They were the time-domain ramp up/down approach, the resonant frequency approach, and a direct .AC extraction of the impedance. While the first two methods can show voltage dependencies, the .AC approach can also show a C_comp dependency on frequency. Lance used the last approach for the remainder of the study.

In a test setup, Lance extracted the individual C_comp values for both clamps and the pullup and pulldown transistors. He presented several plots showing voltage and frequency dependences for driving and non-driving modes.

The C_comp values for clamps showed minor variation, and a high frequency extraction would be reasonable. More variation existed for the C_comp values associated with the pullup and pulldown transistors.

Lance provided some guidance that the extraction frequency should be related to the [Ramp] information (Foutput = 1/(dt_r + dt_f). The voltage settings could be centered around actual operation. He also concluded that the IBIS specification could be improved with separate driving and non-driving C_comp values and with separate C_comps for different DC values depending on the application.

SUBCKT PACKAGE MODEL IN IBIS

Wenliang Dai (Cadence Design Systems, China)

[Presented by Yukio Masuko, Cadence Design Systems, Japan]

Yukio Masuko gave an overview of the existing IBIS package model options: (1) simplified RLC, (2) segmented/forked RLC, and (3) coupled RLC matrix values. Currently, field solvers can extract coupled package model SPICE subcircuits and Touchstone S-parameter models.

Because of current requirements and the need to consider decoupling capacitors for power and SSN analysis, the subckt and S-parameter models are needed along with pin-port mappings.

Yukio showed the existing [Define Package Model] structure and then proposed enhancing it with the following keywords: [Subckt Package Model], [Pin-Node Mapping]/[End Pin-Node

Mapping], [Subckt Model Data]/[End Subckt Model Data]. He presented more syntactical details and concluded that such a structure can support accurate Power/SSN analysis, bring in SPICE or S-parameter data, and work with IC-Package-Board co-design applications.

APPLICATON OF MODEL CONNECTION PROTOCOLS FOR POWER DELIVERY NETWORK ANALYSIS

Yutaka Honda* and Brad Brim** (ATE Service Corporation, Japan* and Sigrity, USA**)

Yutaka Honda noted that no standards exist for dealing with chip/package/board system designs consisting of hundreds or thousands of physical connections (such as pins). One issue is to connect a large number of pins from one model format to another. IBIS has pin connection methods, but does not provide return path power/ground information. Also IBIS does not provide die (chip) side information.

Yutaka outlined some requirements including arbitrarily pin-grouped models and automated connection among models in EDA tools. Several vendor-specific model protocols exist and are implemented by comment lines in "headers".

Yutaka introduced the Sigrity Model Connection Protocol (MCP). It includes pinName, modelNodeName, netName and x and y positions for physical pins. It can group [Power Nets], [Ground Nets] and [Signal Nets]. It has IBIS-like keywords and supports [Structure Type] and [Connecton Type] choices of {DIE | PKG | PCB}. The syntax is implemented as comment lines in the header. Yutaka showed several examples including one where the decoupling capacitors can be placed on the printed circuit board. He also illustrated PDN analysis setup and showed how models can be linked by the MCP.

Yutaka concluded that a standard model connection protocol is needed and that the authors will discuss this topic with IBIS.

HANDLING OF PASSIVE COMPONENT MODEL IN TRANSMISSION-LINE SIMULATION

Motoyuki Kobayashi (Zuken, Japan)

Motoyuki Kobayashi showed a flow involving motherboard and daughter boards where high-speed interconnects need to be modeled. Filter components (inductors) are also needed for noise. Passive models are needed, but they might come in a variety of forms that are not usable. A useful utility can produce an N-port circuit model from a variety of sources including equivalent circuits, SPICE data and S-parameter data.

The conversion of the N-port format needs to preserve passivity and causality. Otherwise the results could be wrong or diverge during simulation. Motoyuki showed some successful flows with an equivalent circuit, an N-port passive model, and failure with an N-port non-passive model.

CONCLUDING ITEMS

Bob Ross thanked the JEITA people for setting up the meeting, the presenters for excellent presentations, the sponsors, and everyone for attending. The meeting adjourned at approximately 5:50 PM.

NEXT MEETING

The next IBIS Open Forum teleconference will be held November 20, 2009 from 8:00 to 10:00 AM US Pacific Standard Time.

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NOTES

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In the body, for the IBIS Open Forum Reflector:
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subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda.org)
IBIS Users' Group Reflector (ibis-users@eda.org)
State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported

BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

IBIS CURRENT MEMBER VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	October 9, 2009	October 30, 2009	November 4, 2009	November 6, 2009
Actel	Producer	Inactive				
Advanced Micro Devices	Producer	Inactive				√
Agilent Technologies	User	Inactive			√	
Ansoft	User	Inactive			√	
Apple Computer	User	Inactive				
Applied Simulation Technology	User	Inactive				
ARM	Producer	Inactive				
Cadence Design Systems	User	Active	√	√	√	√
Cisco Systems	User	Active	√	√	√	
Ericsson	Producer	Active	√	√	√	√
Green Streak Programs	General Interest	Inactive				
Hitachi ULSI Systems	Producer	Inactive				√
Huawei Technologies	Producer	Inactive			√	
IBM	Producer	Inactive		√		
Infineon Technologies AG	Producer	Inactive				
Intel Corp.	Producer	Active	√		√	
IO Methodology	User	Active	√		√	√
LSI	Producer	Inactive	√	√		
Mentor Graphics	User	Inactive	√			
Micron Technology	Producer	Inactive	√	√		
Nokia Siemens Networks	Producer	Inactive	√	√		
Samtec	Producer	Inactive				
Signal Integrity Software	User	Inactive	√	√		
Sigrity	User	Inactive			√	
Synopsys	User	Inactive			√	
Teraspeed Consulting	General Interest	Active	√	√	√	√
Toshiba	Producer	Inactive				√
Xilinx	Producer	Inactive				
ZTE	User	Inactive			√	
Zuken	User	Inactive				√

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

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