Huawei's IBIS model quality specification and technology

Asian IBIS Summit, Shanghai China
November 4, 2009

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Overview

Huawei’s model quality process

- Golden model specification
- Model quality report

IBIS model Correction

- Correction methodology
- Correction case

Golden Model Specification

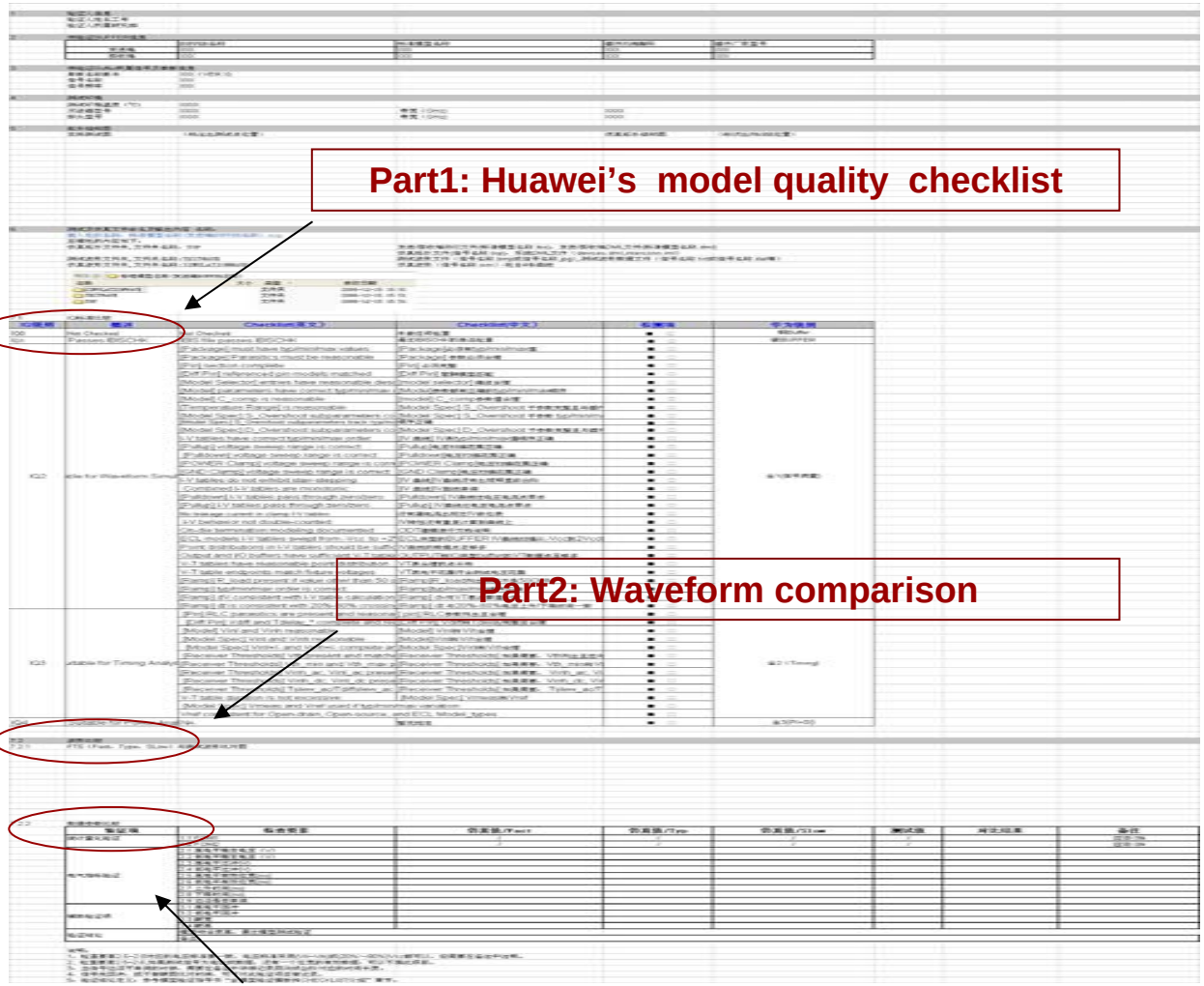
Background:

- IBIS model provided by many different chip vendors;
- System vendor's requirement should be considered in IQ spec

Huawei's specification:

- Huawei follows the IQ Spec, but more detailed;
- Actual PCB measurement based correlation;
- Model level: Copper model
  Silver model
  Golden1 model (for signal reflection)
  Golden2 model (for timing)
  Golden3 model (for SI+PI co-design)

Huawei IBIS Quality report



Part1: Huawei's model quality checklist

Part2: Waveform comparison

Part3: Electrical Specifications: simulation VS measurement

If passed , Huawei model level will be set as followed:

- Copper model
- Silver model
- Golden1 model (for signal reflect)
- Golden2 model (for timing)
- Golden3 model (for SI+PI co-design)

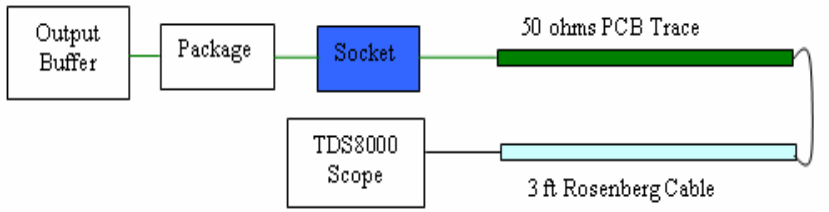
Golden Model Specification

Part1: Huawei's model quality checklist

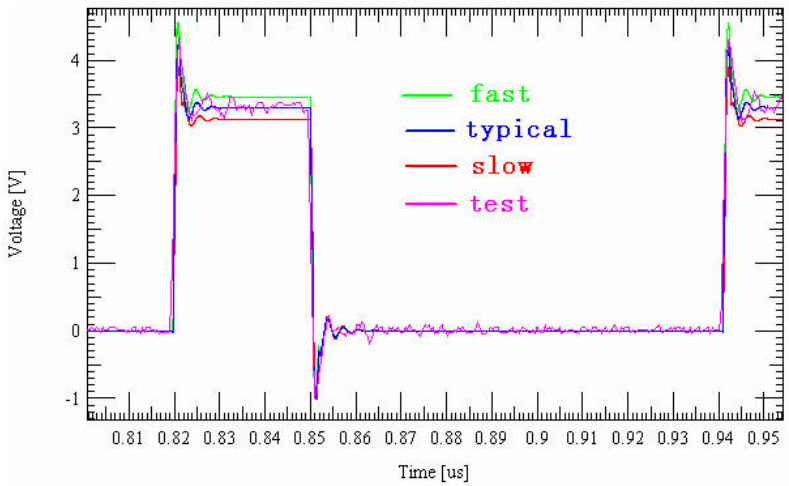
IQ级别	概述	Checklist(英文)	Checklist(中文)	检测项	华为级别
IQ0	Not Checked	Not Checked	未做任何检查	■ □	铜Buffer
IQ1	Passes IBISCHK	IBIS file passes IBISCHK	通过IBISCHK的语法检查	■ □	银BUFFER
IQ2	ible for Waveform Simul	[Package] must have typ/min/max values	[Package]必须有typ/min/max值	■ □	金1(信号质量)
		[Package] Parasitics must be reasonable	[Package] 参数必须合理	■ □	
		[Pin] section complete	[Pin] 必须完整	■ □	
		[Diff Pin] referenced pin models matched	[Diff Pin] 管脚模型匹配	■ □	
		[Model Selector] entries have reasonable desc	[model selector] 描述合理	■ □	
		[Model] parameters have correct typ/min/max	[Model]参数都有正确的typ/min/max顺序	■ □	
		[Model] C_comp is reasonable	[model] C_comp参数值合理	■ □	
		[Temperature Range] is reasonable	[Model Spec] S_Overshoot 干参数完整且与器件	■ □	
		[Model Spec] S_Overshoot subparameters cor	[Model Spec] S_Overshoot 干参数 typ/min/ma	■ □	
		[Model Spec] S_Overshoot subparameters track typ/	顺序正确	■ □	
		[Model Spec] D_Overshoot subparameters cor	[Model Spec] D_Overshoot 干参数完整且与器件	■ □	
		I-V tables have correct typ/min/max order	[IV 曲线] IV表typ/min/max值顺序正确	■ □	
		[Pullup] voltage sweep range is correct	[Pullup]电压扫描范围正确	■ □	
		[Pulldown] voltage sweep range is correct	[Pulldown]电压扫描范围正确	■ □	
		[POWER Clamp] voltage sweep range is corre	[POWER Clamp]电压扫描范围正确	■ □	
		[GND Clamp] voltage sweep range is correct	[GND Clamp]电压扫描范围正确	■ □	
		I-V tables do not exhibit stair-stepping	[IV 曲线]IV 曲线没有出现明显的台阶	■ □	
		Combined I-V tables are monotonic	[IV 曲线]IV 曲线单调	■ □	
		[Pulldown] I-V tables pass through zero/zero	[Pulldown] IV 曲线过电压电流点零点	■ □	
		[Pullup] I-V tables pass through zero/zero	[Pullup] IV 曲线过电压电流点零点	■ □	
		No leakage current in clamp I-V tables	没有漏电流出现在IV 嵌位表	■ □	
		I-V behavior not double-counted	IV特性没有重复计算到曲线上	■ □	
		On-die termination modeling documented	ODT建模进行文档说明	■ □	
		ECL models I-V tables swept from -Vcc to +2	ECL类型的BUFFER IV 曲线扫描从-Vcc到2Vcc范	■ □	
		Point distributions in I-V tables should be suffic	IV 曲线的数据点足够多	■ □	
		Output and I/O buffers have sufficient V-T tab	OUTPUT和IO类型buffer的VT数据点足够多	■ □	
		V-T tables have reasonable point distribution	VT表合理的点分布	■ □	
		V-T table endpoints match fixture voltages	VT表电平范围符合测试电压范围	■ □	
		[Ramp] R_load present if value other than 50 o	[Ramp]R_load列出如果不是50OHM	■ □	
		[Ramp] typ/min/max order is correct	[Ramp]typ/max/min顺序正确	■ □	
		[Ramp] dV consistent with I-V table calculation	[Ramp] dv 与VT表计算值一致	■ □	
		[Ramp] dt is consistent with 20%-80% crossin	[Ramp] dt 与20%-80%电压上升/下降时间一致	■ □	

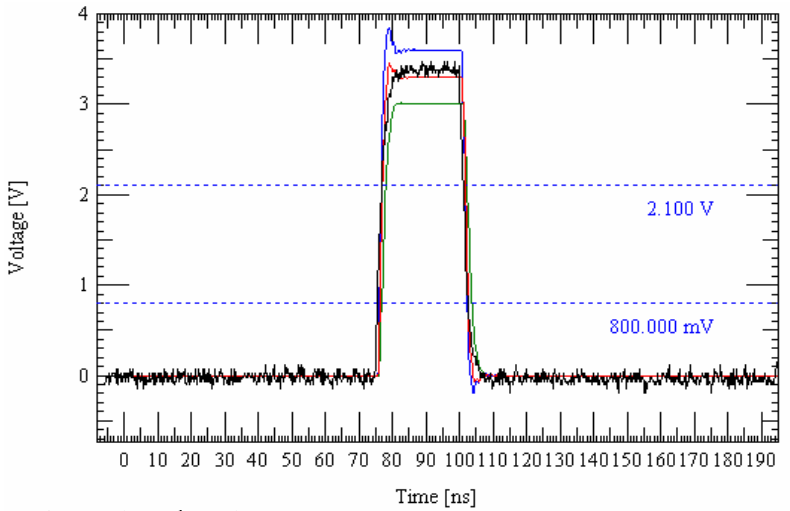
Golden Model Specification

Part2: Waveform comparison: FTS (Fast/typical/slow) simulation VS measurment



Channel S-parameter test



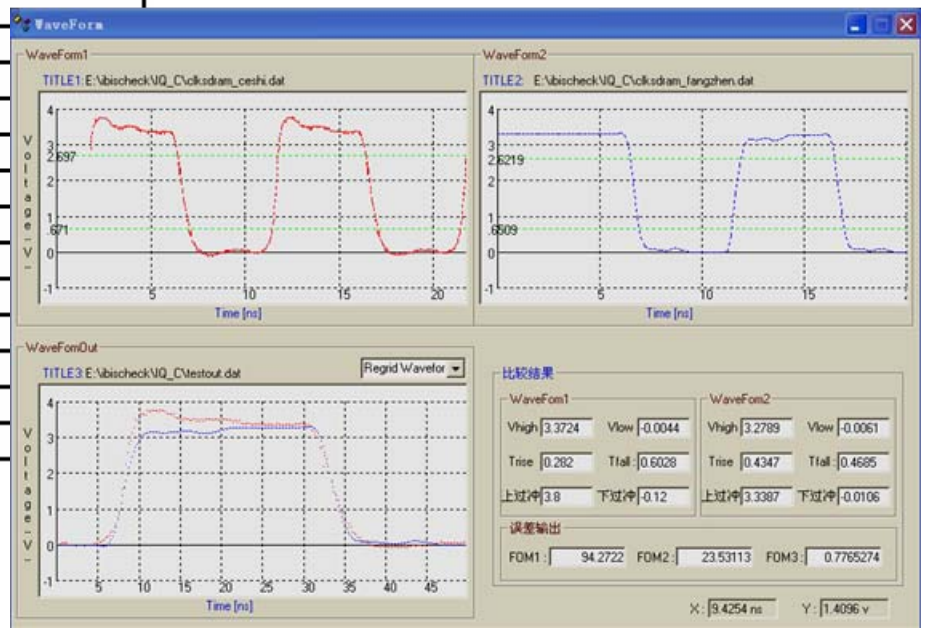


actual PCB measurement VS simulation

Model Quality report

Part3: Electrical Specifications: simulation VS measurement

验证项	检查要素
统计量化验证	1.1 FOM1
	1.2 FOM2
电气指标验证	2.1 高电平稳定电压（V）
	2.2 低电平稳定电压（V）
	2.3 高电平过冲(V)
	2.4 低电平过冲(V)
	2.5 高电平有效位宽(ns)
	2.6 低电平有效位宽(ns)
	2.7 上升时间(ns)
	2.8 下降时间(ns)
	2.9 边沿是否单调
辅助验证项	3.1 高电平回冲
	3.2 低电平回冲
	3.3 眼宽
	3.4 眼高



FOM:

$$FOM1 = 100 \cdot \left[1 - \frac{\sum_{i=1}^{N} |Y1_i - Y2_i|}{YW \cdot N}\right]$$

$$FOM2 = 100 \cdot \left[\frac{\max|Y1_i - Y2_i|}{YW}\right]$$

$$FOM3 = \max|Y1_i - Y2_i|$$

Overview

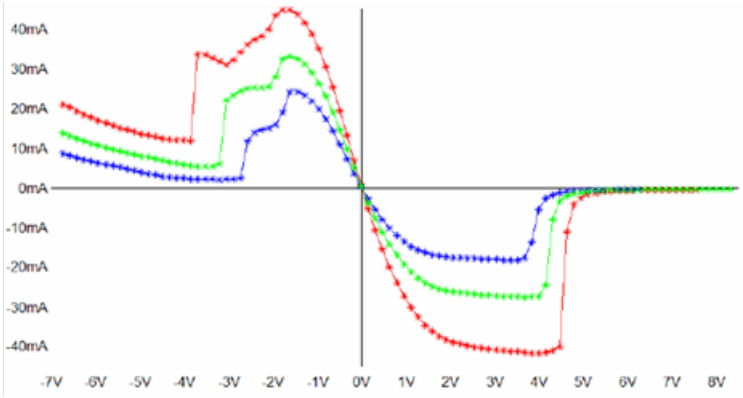
Huawei’s model quality process

- Golden model specification
- Model validation/quality report

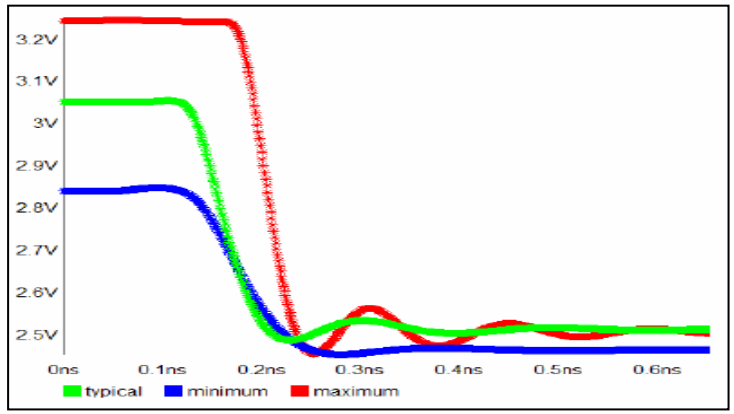
- **IBIS model Correction**
- Correction methodology
- Correction case

Background

- **Once there are some data issues in IBIS model：**



Non-monotonic VI table



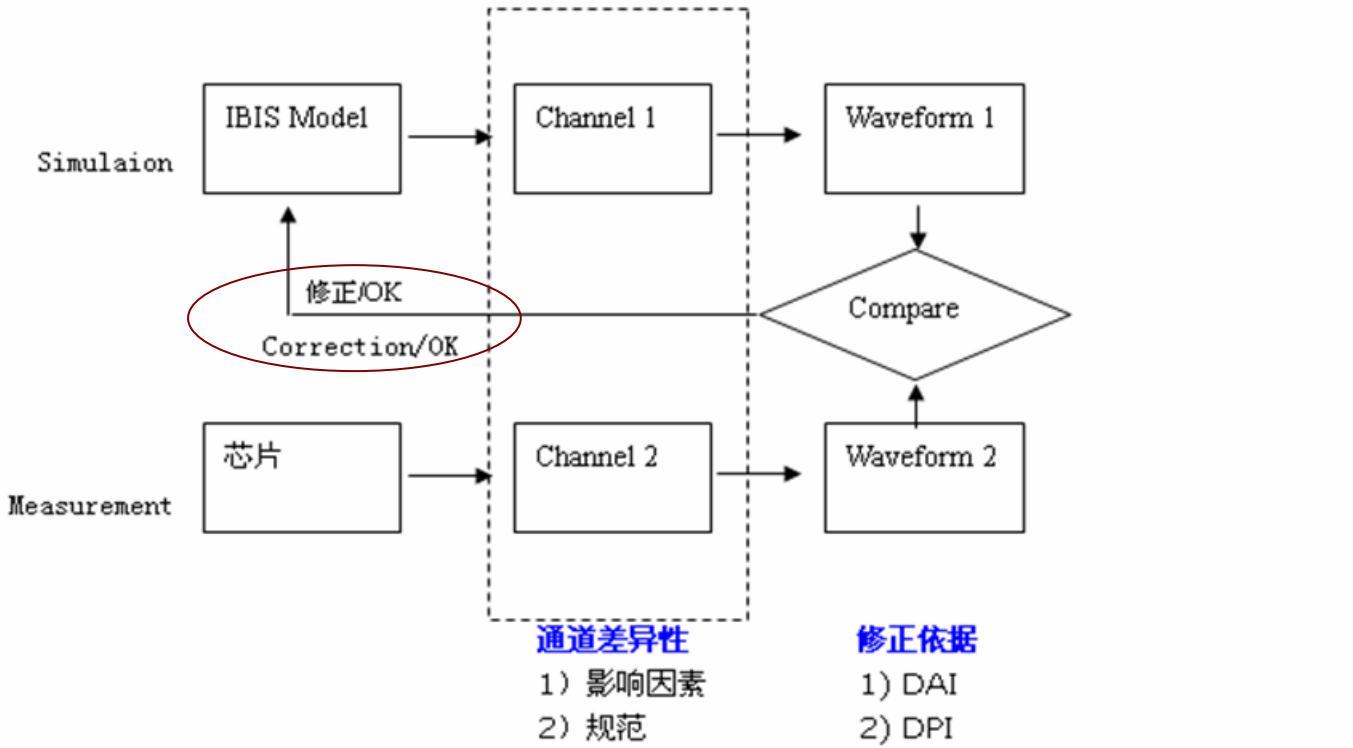
Non-monotonic Vt table

What can we do ?

Correction Methodology

Topology. :

Driver → Interconnect → Receiver



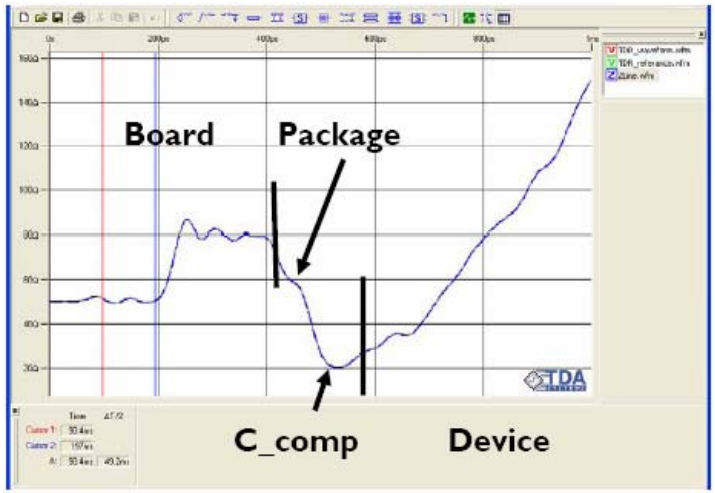
■ It’s important to keep consistent with the channel1 and channel2

Correction Methodology

（1） PKG correction

- ✓ PKG and C_comp parameters should match the datasheet
- ✓ PKG and C_comp model should match the TDR curves

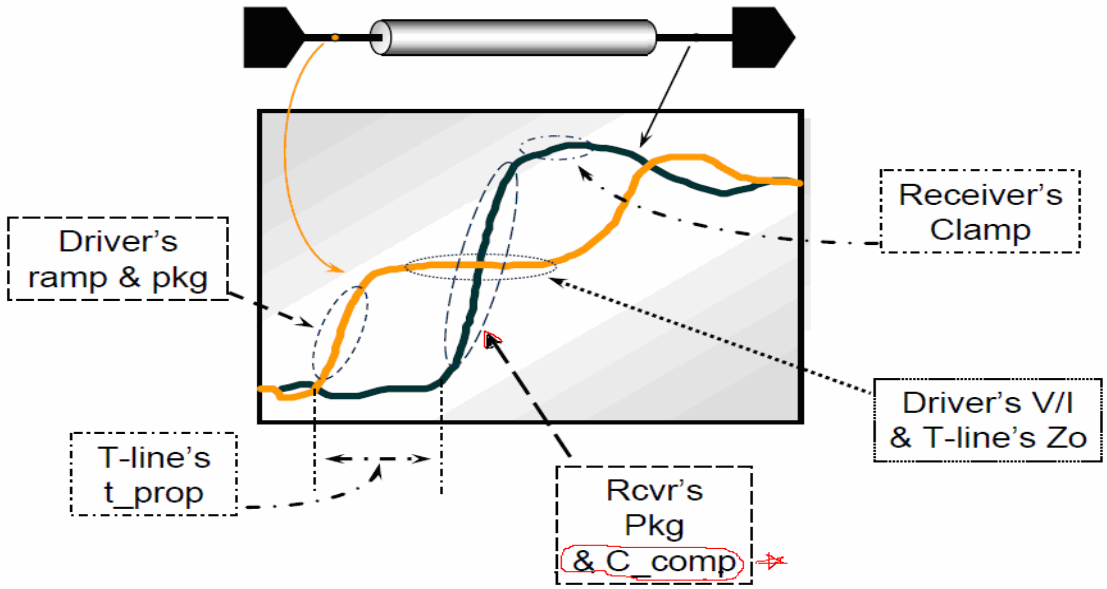
		IBIS		Datasheet (DDR3-1333)	
		Min	max	min	max
DQ	C_comp	1.66pF	1.95pF		
	C package	0.20pF	0.26pF		
	C_total	1.86pF	2.21pF	1.5pF	2.5pF
INPUT	C_comp	0.93pF	1.20pF		
	C package	0.17pF	0.36pF		
	C_total	1.10pF	1.56pF	0.75pF	1.3pF
CLK	C_comp	0.97pF	1.19pF		
	C package	0.20pF	0.21pF		
	C_total	1.17pF	1.40pF	0.8pF	1.4pF



Correction Methodology

（2）VI/VT data table correction

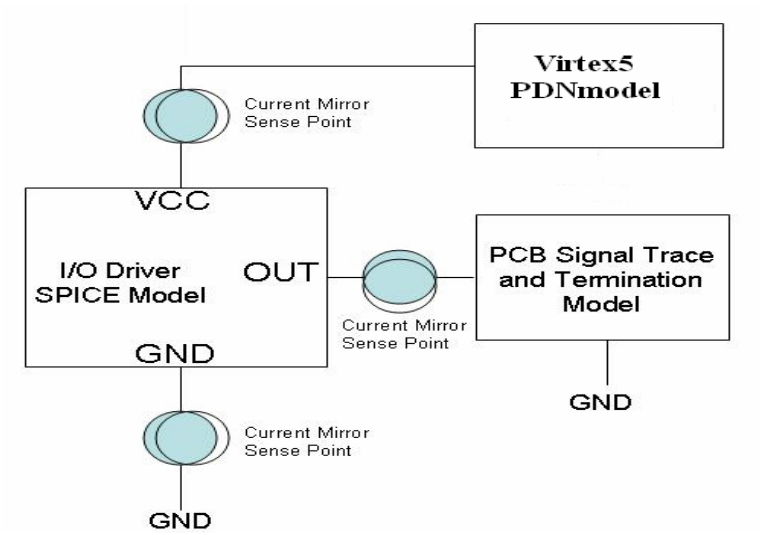
- ✓ VI/VT data is not really accuracy, should be adjusted sometimes;
- ✓ Rubbish VI/VT data in, rubbish waveform out.

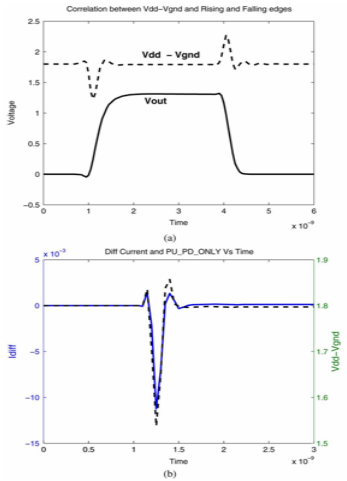


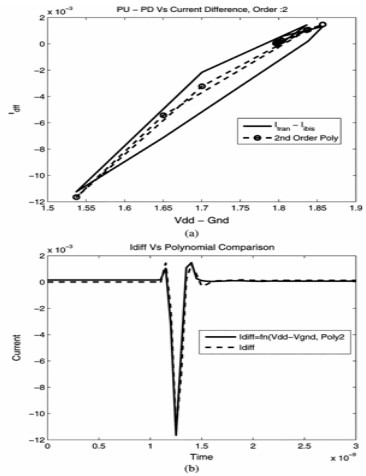
Correction Methodology

（3） Macro model Correction

- ✓ More faster rising edge, more SSN，
- ✓ Traditional IBIS could not support SSN modeling



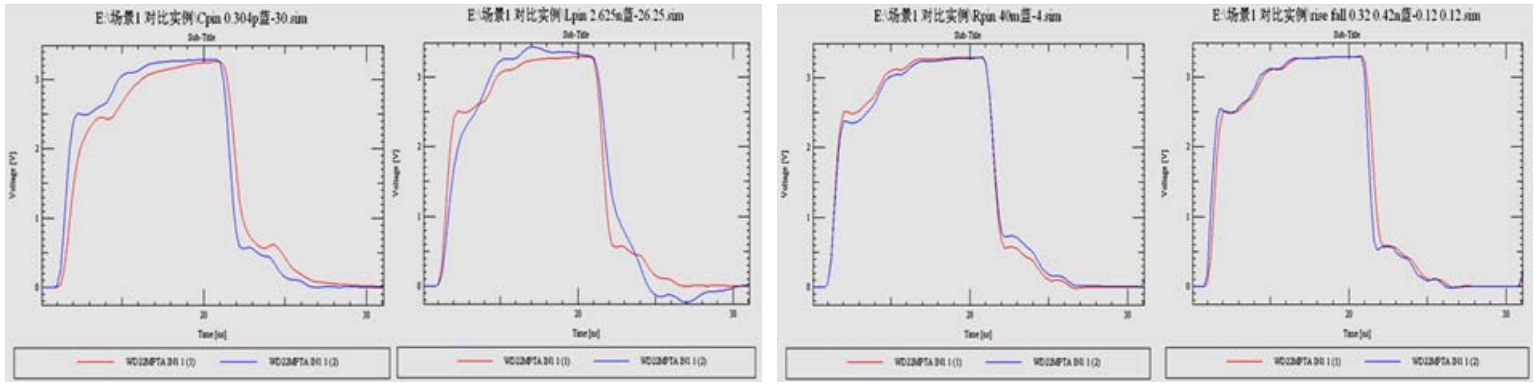




- **We add a behavioral current source in IBIS, modeling the SSN.**
- **Would Improve the simulation accuracy**

Correction case

Correction case：



吻合度参数： 35% → 15% → 10% → 5%

- The correction technology improved the model quality significantly

Conclusion

- Huawei follows the IQ Spec, but more detailed;
- Actual PCB measurement based correlation is significance;
- Model correction technology is a good way to improve model quality;
- Expect to release IBIS correction technology specification

References

● **Official IBIS Website, including tools, articles, specifications**
– http://www.eigroup.org/ibis/

● **iq_ver_2_0.pdf**
– http://www.eda.org/pub/ibis/quality_wip/iq_ver_2_0.pdf

● **IBIS Summit presentations 2007~2008**
– http://www.eda-stds.org/ibis/summits/index-bydate.htm

● **Micron model quality report**
– http://www.micron.com/products/partdetail?part=MT18JSF25672AY-1G1

● **Altera model quality**
– http://www.altera.com/literature/wp/signal-integrity_s2-v4.pdf

● **Mark Alexander Xilinx Corp. 《ssn master circuit》**
– http://www.xilinx.com/products/virtex4/pdfs/virtex-4_power_system_performance.pdf

Thank you

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